Device Overview

The 89HPES16NT2 is a member of the IDT PRECISE™ family of PCI Express® switching solutions offering the next-generation I/O interconnect standard. The PES16NT2 is a 16-lane, 2-port peripheral chip that provides high-performance switching and non-transparent bridging (NTB) functions between a PCIe® upstream port and an NTB downstream port. The PES16NT2 is a part of the IDT PCIe System Interconnect Products and is intended to be used with IDT PCIe System Interconnect Switches. Together, the chipset targets multi-host and intelligent I/O applications such as communications, storage, and blade servers where inter-domain communication is required.

Features

- **High Performance PCI Express Switch**
  - Sixteen PCI Express lanes (2.5Gbps), two switch ports
  - Delivers 64 Gbps (8 GBps) of aggregate switching capacity
  - Low latency cut-through switch architecture
  - Support for Max Payload size up to 2048 bytes
  - Supports one virtual channel and eight traffic classes
  - PCI Express Base specification Revision 1.0a compliant
- **Flexible Architecture with Numerous Configuration Options**
  - Supports automatic per port link width negotiation (x8, x4, x2, or x1)
  - Static lane reversal on all ports
  - Automatic polarity inversion on all lanes
  - Supports locked transactions, allowing use with legacy software
  - Ability to load device configuration from serial EEPROM
  - Ability to control device via SMBus
- **Non-Transparent Port**
  - Crosslink support on NTB port
  - Four mapping windows supported
    - Each may be configured as a 32-bit memory or I/O window
    - May be paired to form a 64-bit memory window
  - Interprocessor communication
    - Thirty-two inbound and outbound doorbells
    - Four inbound and outbound message registers
    - Two shared scratchpad registers
  - Allows up to sixteen masters to communicate through the non-transparent port
  - No limit on the number of supported outstanding transactions through the non-transparent bridge
  - Completely symmetric non-transparent bridge operation allows similar/same configuration software to be run
  - Supports direct connection to a transparent or non-transparent port of another switch
- **Highly Integrated Solution**
  - Requires no external components
  - Incorporates on-chip internal memory for packet buffering and queueing
  - Integrates sixteen 2.5 Gbps embedded full duplex SerDes, 8B/10B encoder/decoder (no separate transceivers needed)

Block Diagram

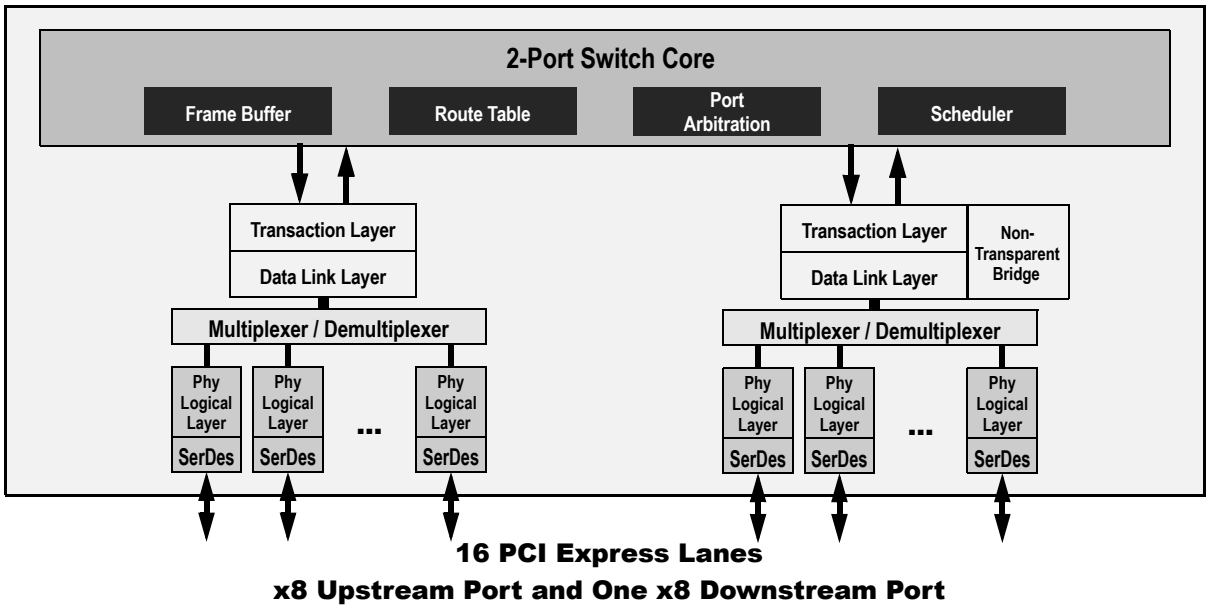


Figure 1 Internal Block Diagram

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- **Reliability, Availability, and Serviceability (RAS) Features**
  - Internal end-to-end parity protection on all TLPs ensures data integrity even in systems that do not implement end-to-end CRC (ECRC)
  - Supports ECRC pass-through
  - Supports Hot-Swap
- **Power Management**
  - Supports PCI Power Management Interface specification, Revision 1.1 (PCI-PM)
  - Unused SerDes are disabled
- **Testability and Debug Features**
  - Built in SerDes Pseudo-Random Bit Stream (PRBS) generator
  - Ability to read and write any internal register via the SMBus
  - Ability to bypass link training and force any link into any mode
  - Provides statistics and performance counters
- **Two SMBus Interfaces**
  - Slave interface provides full access to all software-visible registers by an external SMBus master
  - Master interface provides connection for an optional serial EEPROM used for initialization
  - Master and slave interfaces may be tied together so the switch can act as both master and slave
- **Eight General Purpose Input/Output pins**
- **Packaged in a 23mm x 23mm 484-ball BCG with 1mm ball spacing**

Product Description

Utilizing standard PCI Express interconnect, the PES16NT2 provides the most efficient high-performance I/O connectivity solution for applications requiring high throughput, low latency, and simple board layout with a minimum number of board layers. With support for non-transparent bridging, the PES16NT2 is part of the IDT PCIe System Interconnect Products that target multi-host and intelligent I/O applications requiring inter-domain communication. The PES16NT2 provides 64 Gbps (8 GBps) of aggregated, full-duplex switching capacity through 16 integrated serial lanes, using proven and robust IDT technology. Each lane provides 2.5 Gbps of bandwidth in both directions and is fully compliant with PCI Express Base specification 1.0a.

The PES16NT2 is based on a flexible and efficient layered architecture. The PCI Express layer consists of SerDes, Physical, Data Link, and Transaction layers in compliance with PCI Express Base specification Revision 1.0a. The PES16NT2 can operate either as a store and forward or cut-through switch depending on the packet size and is designed to switch memory and I/O transactions. It supports eight Traffic Classes (TCs) and one Virtual Channel (VC) with sophisticated resource management.

Switch Configuration

The PES16NT2 is a two port switch that contains sixteen PCI Express lanes. Each of the two ports is statically allocated eight lanes with ports labeled as A and C. Port A is the upstream port and port C is the non-transparent downstream port.

During link training, link width is automatically negotiated. Each PES16NT2 port is capable of independently negotiating to a x8, x4, x2, or x1 width. Thus, the PES16NT2 may be used in virtually any two port switch configuration (e.g., {x8, x8}, {x4, x4}, {x4, x2}, etc.). The PES16NT2 supports static lane reversal. For example, lane reversal for upstream port A may be configured by asserting the PCI Express Port A Lane Reverse (PEALREV) input signal or through serial EEPROM or SMBus initialization. Lane reversal for port C may be enabled via a configuration space register, serial EEPROM, or the SMBus.

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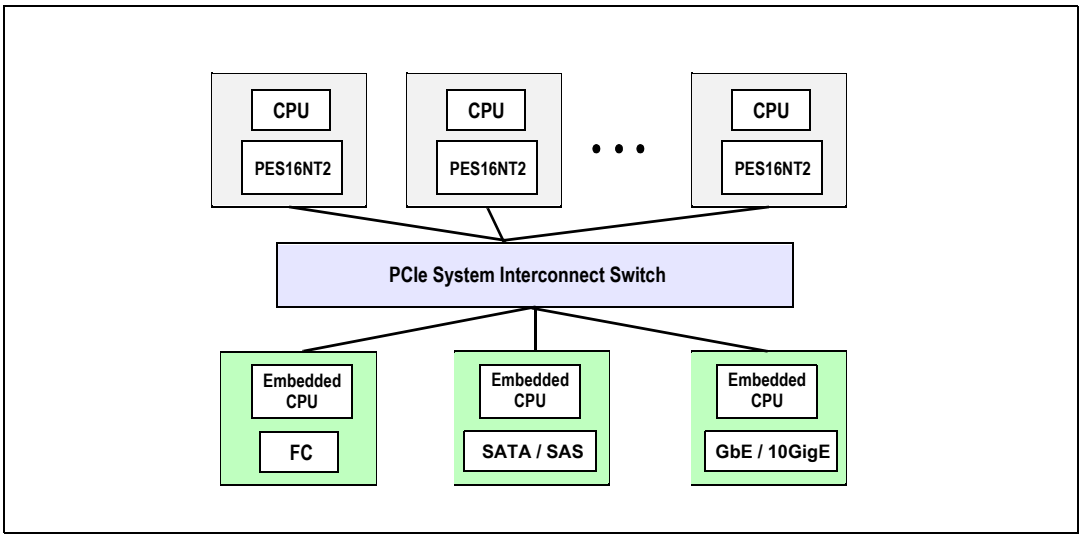


Figure 2 PCIe System Interconnect Architecture Block Diagram

Pin Description

The following tables list the functions of the pins provided on the PES16NT2. Some of the functions listed may be multiplexed onto the same pin. The active polarity of a signal is defined using a suffix. Signals ending with an "N" are defined as being active, or asserted, when at a logic zero (low) level. All other signals (including clocks, buses, and select lines) will be interpreted as being active, or asserted, when at a logic one (high) level.

Signal	Type	Name/Description
PEALREV	I	**PCI Express Port A Lane Reverse.** When this bit is asserted, the lanes of PCI Express Port A are reversed. This value may be overridden by modifying the value of the PALREV bit in the PA_SWCTL register.
PEARP[7:0] PEARN[7:0]	I	**PCI Express Port A Serial Data Receive.** Differential PCI Express receive pairs for port A.
PEATP[7:0] PEATN[7:0]	O	**PCI Express Port A Serial Data Transmit.** Differential PCI Express transmit pairs for port A
PECLREV	I	**PCI Express Port C Lane Reverse.** When this bit is asserted, the lanes of PCI Express Port C are reversed. This value may be overridden by modifying the value of the PCLREV bit in the PA_SWCTL register.
PECRP[7:0] PECRN[7:0]	I	**PCI Express Port C Serial Data Receive.** Differential PCI Express receive pairs for port C.
PECTP[7:0] PECTN[7:0]	O	**PCI Express Port C Serial Data Transmit.** Differential PCI Express transmit pairs for port C
PEREFCLKP[1:0] PEREFCLKN[1:0]	I	**PCI Express Reference Clock.** Differential reference clock pair input. This clock is used as the reference clock by on-chip PLLs to generate the clocks required for the system logic and on-chip SerDes. The frequency of the differential reference clock is determined by the REFCLKM signal.
REFCLKM	I	**PCI Express Reference Clock Mode Select.** These signals select the frequency of the reference clock input. 0x0 - 100 MHz 0x1 - 125 MHz

Table 1 PCI Express Interface Pins

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Signal	Type	Name/Description
MSMBADDR[4:1]	I	**Master SMBus Address.** These pins determine the SMBus address of the serial EEPROM from which configuration information is loaded.
MSMBCLK	I/O	**Master SMBus Clock.** This bidirectional signal is used to synchronize transfers on the master SMBus. It is active and generating the clock only when the EEPROM is being accessed.
MSMBDAT	I/O	**Master SMBus Data.** This bidirectional signal is used for data on the master SMBus.
SSMBADDR[5,3:1]	I	**Slave SMBus Address.** These pins determine the SMBus address to which the slave SMBus interface responds.
SSMBCLK	I/O	**Slave SMBus Clock.** This bidirectional signal is used to synchronize transfers on the slave SMBus.
SSMBDAT	I/O	**Slave SMBus Data.** This bidirectional signal is used for data on the slave SMBus.

Table 2 SMBus Interface Pins

Signal	Type	Name/Description
GPIO[0]	I/O	**General Purpose I/O.** This pin can be configured as a general purpose I/O pin.
GPIO[1]	I/O	**General Purpose I/O.** This pin can be configured as a general purpose I/O pin. Alternate function pin name: PECRSTN Alternate function pin type: Output Alternate function: Reset output for downstream port C
GPIO[2]	I/O	**General Purpose I/O.** This pin can be configured as a general purpose I/O pin. Alternate function pin name: PALINKUPN Alternate function pin type: Output Alternate function: Port A link up status output
GPIO[3]	I/O	**General Purpose I/O.** This pin can be configured as a general purpose I/O pin.
GPIO[4]	I/O	**General Purpose I/O.** This pin can be configured as a general purpose I/O pin. Alternate function pin name: PCLINKUPN Alternate function pin type: Output Alternate function: Port C link up status output
GPIO[5]	I/O	**General Purpose I/O.** This pin can be configured as a general purpose I/O pin. Alternate function pin name: FAILOVERP Alternate function pin type: Input Alternate function: NTB upstream port failover
GPIO[6]	I/O	**General Purpose I/O.** This pin can be configured as a general purpose I/O pin.
GPIO[7]	I/O	**General Purpose I/O.** This pin can be configured as a general purpose I/O pin.

Table 3 General Purpose I/O Pins

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Signal	Type	Name/Description
CCLKDS	I	**Common Clock Downstream.** When the CCLKDS pin is asserted, it indicates that a common clock is being used between the downstream device and the downstream port.
CCLKUS	I	**Common Clock Upstream.** When the CCLKUS pin is asserted, it indicates that a common clock is being used between the upstream device and the upstream port.
MSMBSMODE	I	**Master SMBus Slow Mode.** The assertion of this pin indicates that the master SMBus should operate at 100 KHz instead of 400 KHz. This value may not be overridden.
PENTBRSTN	I	**Non-Transparent Bridge Reset.** Assertion of this signal indicates a reset on the external side of the non-transparent bridge. This signal is only used when the switch mode selects a non-transparent mode and has no effect otherwise.
PERSTN	I	**Fundamental Reset.** Assertion of this signal resets all logic inside the PES16NT2 and initiates a PCI Express fundamental reset.
RSTHALT	I	**Reset Halt.** When this signal is asserted during a PCI Express fundamental reset, the PES16NT2 executes the reset procedure and remains in a reset state with the Master and Slave SMBuses active. This allows software to read and write registers internal to the device before normal device operation begins. The device exits the reset state when the RSTHALT bit is cleared in the PA_SWCTL register by an SMBus master.
SWMODE[3:0]	I	**Switch Mode.** These configuration pins determine the PES16NT2 switch operating mode. 0x0 - Transparent mode 0x1 -Transparent mode with serial EEPROM initialization 0x2 - Non-transparent mode 0x3 - Non-transparent mode with serial EEPROM initialization 0x4 - Non-transparent failover mode 0x5 - Non-transparent failover mode with serial EEPROM initialization 0x6 through 0xF - Reserved

Table 4 System Pins

Signal	Type	Name/Description
JTAG_TCK	I	**JTAG Clock**. This is an input test clock used to clock the shifting of data into or out of the boundary scan logic or JTAG Controller. JTAG_TCK is independent of the system clock with a nominal 50% duty cycle.
JTAG_TDI	I	**JTAG Data Input**. This is the serial data input to the boundary scan logic or JTAG Controller.

Table 5 Test Pins (Part 1 of 2)

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Signal	Type	Name/Description
JTAG_TDO	O	**JTAG Data Output**. This is the serial data shifted out from the boundary scan logic or JTAG Controller. When no data is being shifted out, this signal is tri-stated.
JTAG_TMS	I	**JTAG Mode**. The value on this signal controls the test mode select of the boundary scan logic or JTAG Controller.
JTAG_TRST_N	I	**JTAG Reset**. This active low signal asynchronously resets the boundary scan logic and JTAG TAP Controller. An external pull-up on the board is recommended to meet the JTAG specification in cases where the tester can access this signal. However, for systems running in functional mode, one of the following should occur: 1) actively drive this signal low with control logic 2) statically drive this signal low with an external pull-down on the board

Table 5 Test Pins (Part 2 of 2)

Signal	Type	Name/Description
V_{DD}CORE	I	**Core V_{DD}.** Power supply for core logic.
V_{DD}IO	I	**I/O V_{DD}.** LVTTL I/O buffer power supply.
V_{DD}PE	I	**PCI Express Digital Power.** PCI Express digital power used by the digital power of the SerDes.
V_{DD}APE	I	**PCI Express Analog Power.** PCI Express analog power used by the PLL and bias generator.
V_{TT}PE	I	**PCI Express Termination Power.**
V_{SS}	I	**Ground.**

Table 6 Power and Ground Pins

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Pin Characteristics

Note: Some input pads of the PES16NT2 do not contain internal pull-ups or pull-downs. Unused inputs should be tied off to appropriate levels. This is especially critical for unused control signal inputs which, if left floating, could adversely affect operation. Also, any input pin left floating can cause a slight increase in power consumption.

Function	Pin Name	Type	Buffer	I/O Type	Internal Resistor	Notes
PCI Express Interface	PEALREV	I	LVTTL	Input	pull-down	
	PEARN[7:0]	I	CML	Serial link		
	PEARP[7:0]	I				
	PEATN[7:0]	O				
	PEATP[7:0]	O				
	PECLREV	I	LVTTL	Input	pull-down	
	PECRN[7:0]	I	CML	Serial link		
	PECRP[7:0]	I				
	PECTN[7:0]	O				
	PECTP[7:0]	O				
	PEREFCLKN[1:0]	I	LVPECL/ CML	Diff. Clock Input		Refer to Table 8
	PEREFCLKP[1:0]	I				
	REFCLKM	I	LVTTL	Input	pull-down	
SMBus	MSMBADDR[4:1]	I	LVTTL	Input	pull-up	
	MSMBCLK	I/O		STI		
	MSMBDAT	I/O				
	SSMBADDR[5,3:1]	I		Input	pull-up	
	SSMBCLK	I/O		STI		
	SSMBDAT	I/O				
General Purpose I/O	GPIO[7:0]	I/O	LVTTL	Input, High Drive	pull-up	
System Pins	CCLKDS	I	LVTTL	Input	pull-up	
	CCLKUS	I			pull-up	
	MSMBSMODE	I			pull-down	
	PENTBRSTN	I				
	PERSTN	I				
	RSTHALT	I			pull-down	
	SWMODE[3:0]	I			pull-up	
JTAG	JTAG_TCK	I	LVTTL	STI	pull-up	
	JTAG_TDI	I			pull-up	
	JTAG_TDO	O		Low Drive		
	JTAG_TMS	I		STI	pull-up	
	JTAG_TRST_N	I			pull-up	External pull-down

Table 7 Pin Characteristics

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Logic Diagram — PES16NT2

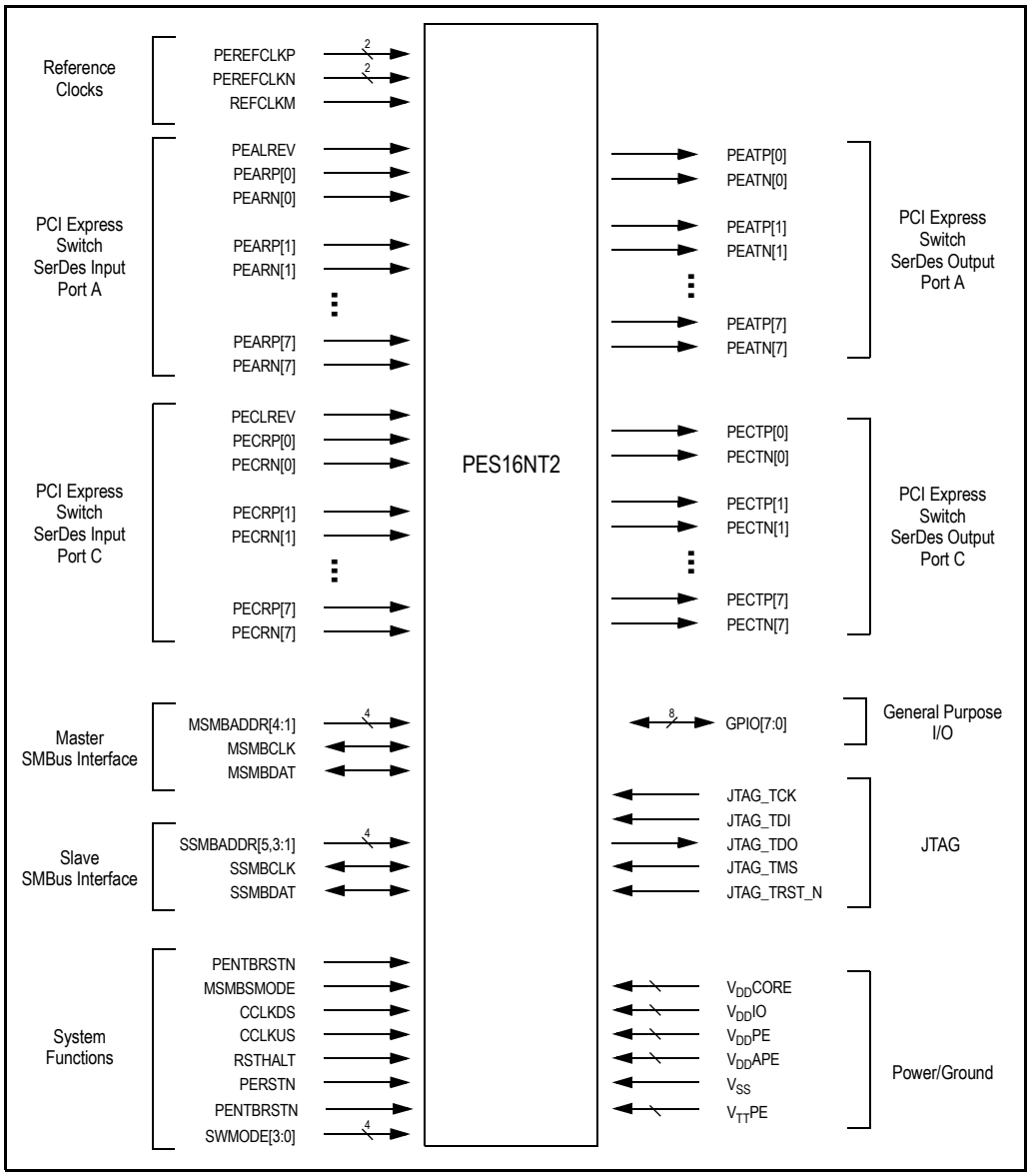


Figure 3 PES16NT2 Logic Diagram

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System Clock Parameters

Values based on systems running at recommended supply voltages and operating temperatures, as shown in Tables 12 and 13.

Parameter	Description	Min	Typical	Max	Unit
$Refclk_{FREQ}$	Input reference clock frequency range	100		125[1]	MHz
$Refclk_{DC}$[2]	Duty cycle of input clock	40	50	60	%
T_R, T_F	Rise/Fall time of input clocks			0.2*RCUI	RCUI[3]
V_{SW}	Differential input voltage swing[4]	0.6		1.6	V
T_{jitter}	Input clock jitter (cycle-to-cycle)			125	ps
R_T	Termination Resistor		110		Ohms

Table 8 Input Clock Requirements

1. The input clock frequency will be either 100 or 125 MHz depending on signal REFCLKM.
2. ClkIn must be AC coupled. Use 0.01 — 0.1 µF ceramic capacitors.
3. RCUI (Reference Clock Unit Interval) refers to the reference clock period.
4. AC coupling required.

AC Timing Characteristics

Parameter	Description	Min[1]	Typical[1]	Max[1]	Units
PCIe Transmit					
UI	Unit Interval	399.88	400	400.12	ps
T_{TX-EYE}	Minimum Tx Eye Width	0.7	.9		UI
$T_{TX-EYE-MEDIAN-to-MAX-JITTER}$	Maximum time between the jitter median and maximum deviation from the median			0.15	UI
$T_{TX-RISE}$, $T_{TX-FALL}$	D+ / D- Tx output rise/fall time	50	90		ps
$T_{TX- IDLE-MIN}$	Minimum time in idle	50			UI
$T_{TX-IDLE-SET-TO-IDLE}$	Maximum time to transition to a valid Idle after sending an Idle ordered set			20	UI
$T_{TX-IDLE-TO-DIFF-DATA}$	Maximum time to transition from valid idle to diff data			20	UI
$T_{TX-SKEW}$	Transmitter data skew between any 2 lanes		500	1300	ps
PCIe Receive					
UI	Unit Interval	399.88	400	400.12	ps
T_{RX-EYE} (with jitter)	Minimum Receiver Eye Width (jitter tolerance)	0.4			UI

Table 9 PCIe AC Timing Characteristics (Part 1 of 2)

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Parameter	Description	Min[1]	Typical[1]	Max[1]	Units
$T_{RX-EYE-MEDIUM\ TO\ MAX\ JITTER}$	Max time between jitter median & max deviation			0.3	UI
$T_{RX-IDLE-DET-DIFF-ENTER\ TIME}$	Unexpected Idle Enter Detect Threshold Integration Time			10	ms
$T_{RX-SKEW}$	Lane to lane input skew			20	ns

Table 9 PCIe AC Timing Characteristics (Part 2 of 2)

1. Minimum, Typical, and Maximum values meet the requirements under PCI Specification 1.1

Signal	Symbol	Reference Edge	Min	Max	Unit	Timing Diagram Reference
GPIO						
GPIO[7:0][1]	Tpw_13b[2]	None	50	—	ns	

Table 10 GPIO AC Timing Characteristics

1. GPIO signals must meet the setup and hold times if they are synchronous or the minimum pulse width if they are asynchronous.
2. The values for this symbol were determined by calculation, not by testing.

Signal	Symbol	Reference Edge	Min	Max	Unit	Timing Diagram Reference
JTAG						
JTAG_TCK	Tper_16a	none	50.0	—	ns	See Figure 4.
	Thigh_16a, Tlow_16a		10.0	25.0	ns	
JTAG_TMS[1], JTAG_TDI	Tsu_16b	JTAG_TCK rising	2.4	—	ns	
	Thld_16b		1.0	—	ns	
JTAG_TDO	Tdo_16c	JTAG_TCK falling	—	20	ns	
	Tdz_16c[2]		—	20	ns	
JTAG_TRST_N	Tpw_16d[2]	none	25.0	—	ns	

Table 11 JTAG AC Timing Characteristics

1. The JTAG specification, IEEE 1149.1, recommends that JTAG_TMS should be held at 1 while the signal applied at JTAG_TRST_N changes from 0 to 1. Otherwise, a race may occur if JTAG_TRST_N is deasserted (going from low to high) on a rising edge of JTAG_TCK when JTAG_TMS is low, because the TAP controller might go to either the Run-Test/Idle state or stay in the Test-Logic-Reset state.
2. The values for this symbol were determined by calculation, not by testing.

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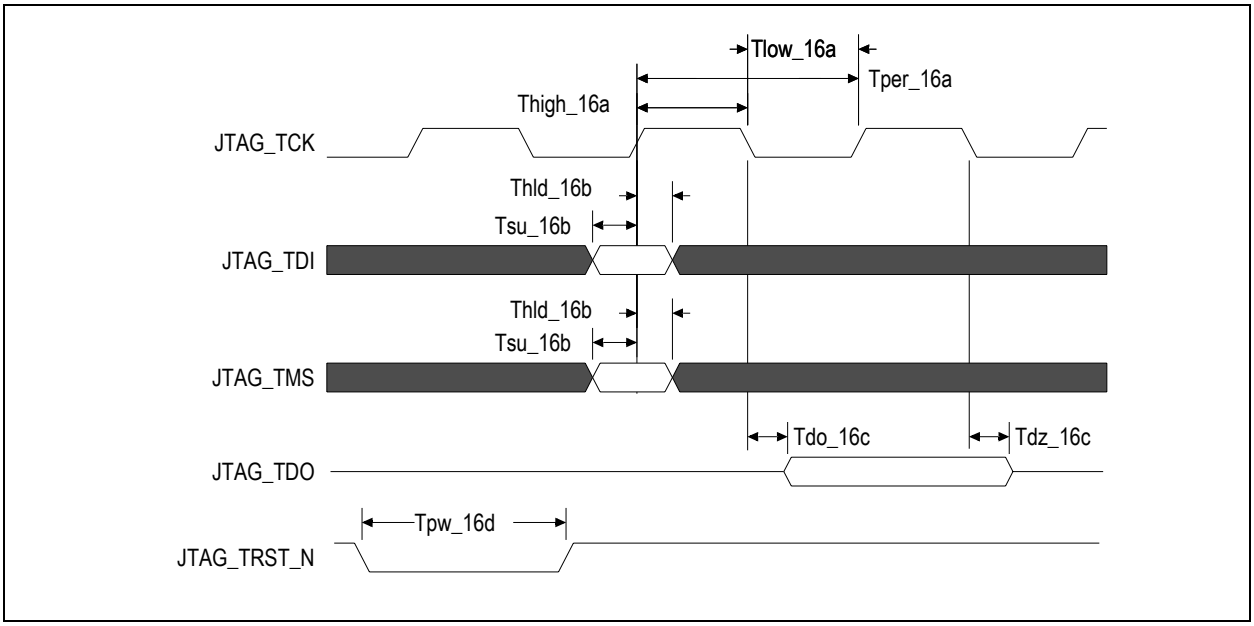


Figure 4 JTAG AC Timing Waveform

Recommended Operating Supply Voltages

Symbol	Parameter	Minimum	Typical	Maximum	Unit
V_{DD}CORE	Internal logic supply	0.9	1.0	1.1	V
V_{DD}I/O	I/O supply except for SerDes LVPECL/CML	3.0	3.3	3.6	V
V_{DD}PE	PCI Express Digital Power	0.9	1.0	1.1	V
V_{DD}APE	PCI Express Analog Power	0.9	1.0	1.1	V
V_{TT}PE	PCI Express Serial Data Transmit Termination Voltage	1.425	1.5	1.575	V
V_{SS}	Common ground	0	0	0	V

Table 12 PES16NT2 Operating Voltages

Power-Up Sequence

This section describes the sequence in which various voltages must be applied to the part during power-up to ensure proper functionality. For the PES16NT2, the power-up sequence must be as follows:

1. V_{DD}I/O — 3.3V
2. V_{DD}Core, V_{DD}PE, V_{DD}APE — 1.0V
3. V_{TT}PE — 1.5V

When powering up, each voltage level must ramp and stabilize prior to applying the next voltage in the sequence to ensure internal latch-up issues are avoided. There are no maximum time limitations in ramping to valid power levels. The power-down sequence must be in the reverse order of the power-up sequence.

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Recommended Operating Temperature

Grade	Temperature
Commercial	0°C to +70°C Ambient

Table 13 PES16NT2 Operating Temperatures

Power Consumption

Typical power is measured under the following conditions: 25°C Ambient, 35% total link usage on all ports, typical voltages defined in Table 14.

Maximum power is measured under the following conditions: 70°C Ambient, 85% total link usage on all ports, maximum voltages defined in Table 14.

All power measurements assume that the part is mounted on a 10 layer printed circuit board with 0 LFM airflow.

Number of Connected Lanes: Port-A/Port-C	Core (Watts) (1.0V supply)		PCIe Digital (Watts) (1.0V supply)		PCIe Analog (Watts) (1.0V supply)		PCIe Termination (Watts) (1.5V supply)		I/O (Watts) (3.3V supply)		Total (Watts)	
	Typ	Max	Typ	Max	Typ	Max	Typ	Max	Typ	Max	Typ	Max
8/8	472	546	697	905	266	345	354	440	1	3		
	0.47	0.60	0.70	1.00	0.27	0.38	0.53	0.69	0.003	0.01	1.97	2.68

Table 14 PES16NT2 Power Consumption

Thermal Considerations

This section describes thermal considerations for the PES16NT2 (23mm^2 BCG484 package). The data in Table 15 below contains information that is relevant to the thermal performance of the PES16NT2 switch.

Symbol	Parameter	Value	Units	Conditions
$T_{J(max)}$	Junction Temperature	125	°C	Maximum
$T_{A(max)}$	Ambient Temperature	70	°C	Maximum for commercial-rated products
$\theta_{JA(effective)}$	Effective Thermal Resistance, Junction-to-Ambient	11.5	°C/W	Zero air flow
		9.6	°C/W	1 m/S air flow
		9.0	°C/W	2 m/S air flow
θ_{JB}	Thermal Resistance, Junction-to-Board	10.9	°C/W	
θ_{JC}	Thermal Resistance, Junction-to-Case	5	°C/W	
P	Power Dissipation of the Device	2.68	Watts	Maximum

Table 15 Thermal Specifications for PES16NT2, 23x23mm BCG484 Package

Note: The parameter $\theta_{JA(eff)}$ is not the *absolute* thermal resistance for the package as defined by JEDEC (JESD-51). Because resistance can vary with the number of board layers, size of the board, and airflow, $\theta_{JA(eff)}$ is the *effective* thermal resistance. The values for effective θ_{JA} given above are based on a 10-layer, standard height, full length (4.3"x12.2") PCIe add-in card.

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DC Electrical Characteristics

Values based on systems running at recommended supply voltages, as shown in Table 12.

Note: See Table 7, Pin Characteristics, for a complete I/O listing.

I/O Type	Parameter	Description	Min[1]	Typ[1]	Max[1]	Unit	Conditions
Serial Link	**PCIe Transmit**						
	$V_{TX-DIFFp-p}$	Differential peak-to-peak output voltage	800		1200	mV	
	$V_{TX-DE-RATIO}$	De-emphasized differential output voltage	-3		-4	dB	
	$V_{TX-DC-CM}$	DC Common mode voltage	-0.1	1	3.7	V	
	$V_{TX-CM-ACP}$	RMS AC peak common mode output voltage			20	mV	
	$V_{TX-CM-DC-active-idle-delta}$	Abs delta of DC common mode voltage between L0 and idle			100	mV	
	$V_{TX-CM-DC-line-delta}$	Abs delta of DC common mode voltage between D+ and D-			25	mV	
	$V_{TX-Idle-DiffP}$	Electrical idle diff peak output			20	mV	
Serial Link (cont.)	$V_{TX-RCV-Detect}$	Voltage change during receiver detection			600	mV	
	$RL_{TX-DIFF}$	Transmitter Differential Return loss	12			dB	
	RL_{TX-CM}	Transmitter Common Mode Return loss	6			dB	
	$Z_{TX-DEFF-DC}$	DC Differential TX impedance	80	100	120	Ω	
	Z_{OSE}	Single ended TX Impedance	40	50	60	Ω	
	Transmitter Eye Diagram	TX Eye Height (De-emphasized bits)	505	650		mV	
	Transmitter Eye Diagram	TX Eye Height (Transition bits)	800	950		mV	
	PCIe Receive						
	$V_{RX-DIFFp-p}$	Differential input voltage (peak-to-peak)	175		1200	mV	
	$V_{RX-CM-AC}$	Receiver common-mode voltage for AC coupling			150	mV	
	$RL_{RX-DIFF}$	Receiver Differential Return Loss	15			dB	
	RL_{RX-CM}	Receiver Common Mode Return Loss	6			dB	
	$Z_{RX-DIFF-DC}$	Differential input impedance (DC)	80	100	120	Ω	
	$Z_{RX-COMM-DC}$	Single-ended input impedance	40	50	60	Ω	
	$Z_{RX-COMM-HIGH-Z-DC}$	Powered down input common mode impedance (DC)	200k	350k		Ω	
	$V_{RX-IDLE-DET-DIFFp-p}$	Electrical idle detect threshold	65		175	mV	
PCIe REFCLK							
	C_{IN}	Input Capacitance	1.5	—		pF	

Table 16 DC Electrical Characteristics (Part 1 of 2)

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I/O Type	Parameter	Description	Min[1]	Typ[1]	Max[1]	Unit	Conditions
Other I/Os							
LOW Drive Output	I_{OL}		—	2.5	—	mA	V_{OL} = 0.4v
	I_{OH}		—	-5.5	—	mA	V_{OH} = 1.5V
High Drive Output	I_{OL}		—	12.0	—	mA	V_{OL} = 0.4v
	I_{OH}		—	-20.0	—	mA	V_{OH} = 1.5V
Schmitt Trigger Input (STI)	V_{IL}		-0.3	—	0.8	V	—
	V_{IH}		2.0	—	$V_{DD}IO$ + 0.5	V	—
Input	V_{IL}		-0.3	—	0.8	V	—
	V_{IH}		2.0	—	$V_{DD}IO$ + 0.5	V	—
Capacitance	C_{IN}		—	—	8.5	pF	—
Leakage	Inputs		—	—	± 10	µA	$V_{DD}I/O$ (max)
	$I/O_{LEAK\ W/O}$ Pull-ups/downs		—	—	± 10	µA	$V_{DD}I/O$ (max)
	$I/O_{LEAK\ WITH}$ Pull-ups/downs		—	—	± 80	µA	$V_{DD}I/O$ (max)

Table 16 DC Electrical Characteristics (Part 2 of 2)

1. Minimum, Typical, and Maximum values meet the requirements under PCI Specification 1.0a.

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Package Pinout — 484-BGA Signal Pinout for PES16NT2

The following table lists the pin numbers and signal names for the PES16NT2 device.

Pin	Function	Alt	Pin	Function	Alt	Pin	Function	Alt	Pin	Function	Alt
A1	V_{SS}		B13	PEATN03		D3	V_{SS}		E15	V_{TT}PE	
A2	V_{SS}		B14	V_{SS}		D4	PEARN07		E16	V_{DD}PE	
A3	V_{DD}CORE		B15	PEATP02		D5	V_{SS}		E17	V_{SS}	
A4	V_{SS}		B16	V_{SS}		D6	PEARP06		E18	V_{SS}	
A5	PEATN07		B17	PEATN01		D7	V_{TT}PE		E19	PECRN07	
A6	V_{SS}		B18	V_{SS}		D8	PEARN05		E20	PECRP07	
A7	PEATN06		B19	PEATP00		D9	V_{TT}PE		E21	V_{SS}	
A8	V_{SS}		B20	V_{SS}		D10	PEARP04		E22	V_{SS}	
A9	PEATN05		B21	V_{SS}		D11	V_{DD}PE		F1	V_{SS}	
A10	V_{SS}		B22	V_{SS}		D12	PEARP03		F2	V_{SS}	
A11	PEATN04		C1	V_{DD}CORE		D13	V_{SS}		F3	V_{DD}CORE	
A12	V_{SS}		C2	V_{DD}CORE		D14	PEARN02		F4	V_{SS}	
A13	PEATP03		C3	V_{DD}CORE		D15	V_{SS}		F5	V_{SS}	
A14	V_{SS}		C4	PEARP07		D16	PEARP01		F6	V_{DD}IO	
A15	PEATN02		C5	V_{SS}		D17	V_{SS}		F7	V_{SS}	
A16	V_{SS}		C6	PEARN06		D18	PEARN00		F8	V_{DD}PE	
A17	PEATP01		C7	V_{SS}		D19	V_{SS}		F9	V_{DD}APE	
A18	V_{SS}		C8	PEARP05		D20	V_{SS}		F10	V_{DD}APE	
A19	PEATN00		C9	V_{SS}		D21	PECTP07		F11	V_{DD}PE	
A20	V_{SS}		C10	PEARN04		D22	PECTN07		F12	V_{DD}PE	
A21	V_{SS}		C11	V_{SS}		E1	V_{DD}CORE		F13	V_{DD}APE	
A22	V_{SS}		C12	PEARN03		E2	V_{DD}CORE		F14	V_{DD}APE	
B1	V_{SS}		C13	V_{TT}PE		E3	V_{SS}		F15	V_{DD}PE	
B2	V_{SS}		C14	PEARP02		E4	V_{DD}CORE		F16	V_{SS}	
B3	V_{DD}CORE		C15	V_{TT}PE		E5	V_{SS}		F17	V_{SS}	
B4	V_{SS}		C16	PEARN01		E6	V_{SS}		F18	V_{DD}PE	
B5	PEATP07		C17	V_{SS}		E7	V_{TT}PE		F19	V_{SS}	
B6	V_{SS}		C18	PEARP00		E8	V_{DD}PE		F20	V_{SS}	
B7	PEATP06		C19	V_{SS}		E9	V_{DD}APE		F21	PECTP06	
B8	V_{SS}		C20	V_{DD}CORE		E10	V_{TT}PE		F22	PECTN06	
B9	PEATP05		C21	V_{DD}CORE		E11	V_{SS}		G1	V_{DD}CORE	
B10	V_{SS}		C22	V_{DD}CORE		E12	V_{DD}PE		G2	V_{DD}CORE	
B11	PEATP04		D1	V_{SS}		E13	V_{TT}PE		G3	V_{SS}	
B12	V_{SS}		D2	V_{SS}		E14	V_{SS}		G4	V_{DD}CORE	

Table 17 PES16NT2 484-pin Signal Pin-Out (Part 1 of 4)

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Pin	Function	Alt	Pin	Function	Alt	Pin	Function	Alt	Pin	Function	Alt
G5	V_{SS}		H20	V_{SS}		K13	V_{DD}CORE		M6	V_{DD}CORE	
G6	V_{SS}		H21	PECTP05		K14	V_{SS}		M7	V_{SS}	
G7	V_{DD}IO		H22	PECTN05		K15	V_{DD}CORE		M8	V_{SS}	
G8	V_{SS}		J1	V_{SS}		K16	V_{SS}		M9	V_{DD}CORE	
G9	V_{SS}		J2	V_{DD}CORE		K17	V_{DD}APE		M10	V_{SS}	
G10	V_{SS}		J3	V_{SS}		K18	V_{SS}		M11	V_{DD}CORE	
G11	V_{DD}IO		J4	V_{DD}CORE		K19	V_{TT}PE		M12	V_{SS}	
G12	V_{SS}		J5	V_{SS}		K20	V_{TT}PE		M13	V_{DD}CORE	
G13	V_{SS}		J6	V_{DD}IO		K21	PECTN04		M14	V_{SS}	
G14	V_{DD}APE		J7	V_{SS}		K22	PECTP04		M15	V_{DD}CORE	
G15	V_{SS}		J8	V_{DD}CORE		L1	V_{SS}		M16	V_{SS}	
G16	V_{DD}IO		J9	V_{SS}		L2	V_{DD}CORE		M17	V_{DD}CORE	
G17	V_{DD}IO		J10	V_{DD}CORE		L3	V_{SS}		M18	V_{SS}	
G18	V_{SS}		J11	V_{SS}		L4	V_{DD}CORE		M19	V_{SS}	
G19	PECRP06		J12	V_{DD}CORE		L5	V_{SS}		M20	V_{SS}	
G20	PECRN06		J13	V_{SS}		L6	V_{DD}IO		M21	PECTP03	
G21	V_{SS}		J14	V_{DD}CORE		L7	V_{SS}		M22	PECTN03	
G22	V_{SS}		J15	V_{SS}		L8	V_{DD}CORE		N1	V_{SS}	
H1	V_{SS}		J16	V_{DD}APE		L9	V_{SS}		N2	V_{SS}	
H2	V_{SS}		J17	V_{SS}		L10	V_{DD}CORE		N3	V_{DD}CORE	
H3	V_{DD}CORE		J18	V_{DD}APE		L11	V_{SS}		N4	V_{DD}CORE	
H4	V_{SS}		J19	PECRN05		L12	V_{DD}CORE		N5	V_{DD}APE	
H5	V_{SS}		J20	PECRP05		L13	V_{SS}		N6	V_{DD}APE	
H6	V_{DD}CORE		J21	V_{SS}		L14	V_{DD}CORE		N7	V_{SS}	
H7	V_{SS}		J22	V_{SS}		L15	V_{SS}		N8	V_{DD}CORE	
H8	V_{DD}CORE		K1	V_{SS}		L16	V_{SS}		N9	V_{SS}	
H9	V_{SS}		K2	V_{SS}		L17	V_{DD}PE		N10	V_{DD}CORE	
H10	V_{DD}CORE		K3	V_{DD}CORE		L18	V_{DD}PE		N11	V_{SS}	
H11	V_{SS}		K4	V_{SS}		L19	PECRN04		N12	V_{DD}CORE	
H12	V_{SS}		K5	V_{SS}		L20	PECRP04		N13	V_{SS}	
H13	V_{DD}CORE		K6	V_{DD}CORE		L21	V_{SS}		N14	V_{DD}CORE	
H14	V_{SS}		K7	V_{SS}		L22	V_{SS}		N15	V_{SS}	
H15	V_{DD}CORE		K8	V_{SS}		M1	V_{SS}		N16	V_{SS}	
H16	V_{SS}		K9	V_{DD}CORE		M2	V_{SS}		N17	V_{DD}APE	
H17	V_{DD}PE		K10	V_{SS}		M3	V_{SS}		N18	V_{DD}APE	
H18	V_{TT}PE		K11	V_{DD}CORE		M4	V_{SS}		N19	PECRP03	
H19	V_{TT}PE		K12	V_{SS}		M5	V_{SS}		N20	PECRN03	

Table 17 PES16NT2 484-pin Signal Pin-Out (Part 2 of 4)

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Pin	Function	Alt	Pin	Function	Alt	Pin	Function	Alt	Pin	Function	Alt
N21	V_{TT}PE		R14	V_{SS}		U7	V_{SS}		V22	PECTN00	
N22	V_{TT}PE		R15	V_{SS}		U8	V_{SS}		W1	V_{SS}	
P1	PEREFCLKP0		R16	V_{SS}		U9	V_{SS}		W2	V_{DD}CORE	
P2	PEREFCLKN0		R17	V_{DD}APE		U10	V_{SS}		W3	V_{SS}	
P3	V_{SS}		R18	V_{DD}APE		U11	V_{SS}		W4	V_{DD}CORE	
P4	V_{SS}		R19	PECRN02		U12	V_{SS}		W5	V_{SS}	
P5	V_{SS}		R20	PECRP02		U13	V_{SS}		W6	V_{DD}IO	
P6	V_{DD}IO		R21	V_{SS}		U14	V_{SS}		W7	V_{SS}	
P7	V_{SS}		R22	V_{SS}		U15	V_{SS}		W8	V_{DD}IO	
P8	V_{SS}		T1	V_{SS}		U16	V_{DD}CORE		W9	V_{DD}CORE	
P9	V_{DD}CORE		T2	V_{SS}		U17	V_{DD}CORE		W10	V_{SS}	
P10	V_{SS}		T3	V_{SS}		U18	V_{DD}CORE		W11	V_{DD}IO	
P11	V_{DD}CORE		T4	V_{SS}		U19	PECRP01		W12	V_{SS}	
P12	V_{SS}		T5	V_{SS}		U20	PECRN01		W13	V_{SS}	
P13	V_{DD}CORE		T6	V_{DD}IO		U21	V_{DD}PE		W14	V_{DD}IO	
P14	V_{SS}		T7	V_{DD}IO		U22	V_{TT}PE		W15	V_{SS}	
P15	V_{DD}CORE		T8	V_{DD}IO		V1	V_{DD}CORE		W16	V_{DD}IO	
P16	V_{SS}		T9	V_{DD}CORE		V2	V_{SS}		W17	V_{SS}	
P17	V_{DD}PE		T10	V_{DD}IO		V3	V_{DD}CORE		W18	V_{SS}	
P18	V_{DD}PE		T11	V_{DD}CORE		V4	V_{SS}		W19	PECRN00	
P19	V_{SS}		T12	V_{DD}CORE		V5	V_{SS}		W20	PECRP00	
P20	V_{SS}		T13	V_{DD}IO		V6	V_{SS}		W21	V_{SS}	
P21	PECTP02		T14	V_{DD}IO		V7	V_{DD}CORE		W22	V_{SS}	
P22	PECTN02		T15	V_{DD}CORE		V8	V_{SS}		Y1	V_{DD}CORE	
R1	V_{SS}		T16	V_{DD}IO		V9	V_{SS}		Y2	V_{SS}	
R2	V_{SS}		T17	V_{DD}IO		V10	V_{DD}CORE		Y3	V_{DD}CORE	
R3	V_{DD}CORE		T18	V_{SS}		V11	V_{SS}		Y4	V_{DD}CORE	
R4	V_{DD}CORE		T19	V_{SS}		V12	V_{DD}CORE		Y5	JTAG_TDO	
R5	V_{SS}		T20	V_{DD}APE		V13	V_{SS}		Y6	MSMBADDR_1	
R6	V_{DD}CORE		T21	PECTP01		V14	V_{DD}CORE		Y7	MSMBADDR_4	
R7	V_{SS}		T22	PECTN01		V15	V_{SS}		Y8	SSMBADDR_1	
R8	V_{SS}		U1	V_{SS}		V16	V_{DD}CORE		Y9	SSMBADDR_5	
R9	V_{SS}		U2	V_{SS}		V17	V_{SS}		Y10	CCLKUS	
R10	V_{SS}		U3	V_{SS}		V18	V_{DD}CORE		Y11	CCLKDS	
R11	V_{SS}		U4	V_{DD}CORE		V19	V_{DD}PE		Y12	PEALREV	
R12	V_{SS}		U5	V_{SS}		V20	V_{TT}PE		Y13	SWMODE_1	
R13	V_{SS}		U6	V_{SS}		V21	PECTP00		Y14	PECLREV	

Table 17 PES16NT2 484-pin Signal Pin-Out (Part 3 of 4)

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Pin	Function	Alt	Pin	Function	Alt	Pin	Function	Alt	Pin	Function	Alt
Y15	RSTHALT		AA6	JTAG_TRST_N		AA19	REFCLKM		AB10	SSMBCLK	
Y16	GPIO_02	1	AA7	MSMBADDR_3		AA20	V_{DD}CORE		AB11	V_{SS}	
Y17	GPIO_05	1	AA8	MSMBDAT		AA21	V_{SS}		AB12	V_{SS}	
Y18	MSMBSMODE		AA9	SSMBADDR_3		AA22	V_{SS}		AB13	V_{SS}	
Y19	V_{SS}		AA10	SSMBDAT		AB1	V_{SS}		AB14	SWMODE_2	
Y20	V_{SS}		AA11	V_{SS}		AB2	V_{SS}		AB15	PERSTN	
Y21	PEREFCLKP1		AA12	V_{DD}CORE		AB3	V_{SS}		AB16	GPIO_00	
Y22	PEREFCLKN1		AA13	SWMODE_0		AB4	V_{SS}		AB17	GPIO_03	
AA1	V_{SS}		AA14	SWMODE_3		AB5	JTAG_TCK		AB18	GPIO_06	
AA2	V_{SS}		AA15	PENTBRSTN		AB6	JTAG_TMS		AB19	V_{SS}	
AA3	V_{DD}CORE		AA16	GPIO_01	1	AB7	MSMBADDR_2		AB20	V_{SS}	
AA4	V_{DD}CORE		AA17	GPIO_04	1	AB8	MSMBCLK		AB21	V_{SS}	
AA5	JTAG_TDI		AA18	GPIO_07		AB9	SSMBADDR_2		AB22	V_{SS}	

Table 17 PES16NT2 484-pin Signal Pin-Out (Part 4 of 4)

Alternate Signal Functions

Pin	GPIO	Alternate
AA16	GPIO_1	PECRSTN
Y16	GPIO_2	PALINKUPN
AA17	GPIO_4	PCLINKUPN
Y17	GPIO_5	FAILOVERP

Table 18 PES16NT2 Alternate Signal Functions

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Power Pins

V_{DD}Core	V_{DD}Core	V_{DD}Core	V_{DD}Core	V_{DD}IO	V_{DD}PE	V_{DD}APE	V_{TT}PE
A3	J2	M13	U16	F6	D11	E9	C13
B3	J4	M15	U17	G7	E8	F9	C15
C1	J8	M17	U18	G11	E12	F10	D7
C2	J10	N3	V1	G16	E16	F13	D9
C3	J12	N4	V3	G17	F8	F14	E7
C20	J14	N8	V7	J6	F11	G14	E10
C21	K3	N10	V10	L6	F12	J16	E13
C22	K6	N12	V12	P6	F15	J18	E15
E1	K9	N14	V14	T6	F18	K17	H18
E2	K11	P9	V16	T7	H17	N5	H19
E4	K13	P11	V18	T8	L17	N6	K19
F3	K15	P13	W2	T10	L18	N17	K20
G1	L2	P15	W4	T13	P17	N18	N21
G2	L4	R3	W9	T14	P18	R17	N22
G4	L8	R4	Y1	T16	U21	R18	U22
H3	L10	R6	Y3	T17	V19	T20	V20
H6	L12	T9	Y4	W6			
H8	L14	T11	AA3	W8			
H10	M6	T12	AA4	W11			
H13	M9	T15	AA12	W14			
H15	M11	U4	AA20	W16			

Table 19 PES16TN2 Power Pins

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Ground Pins

V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}
A1	D2	G13	K10	N9	T3	W10
A2	D3	G15	K12	N11	T4	W12
A4	D5	G18	K14	N13	T5	W13
A6	D13	G21	K16	N15	T18	W15
A8	D15	G22	K18	N16	T19	W17
A10	D17	H1	L1	P3	U1	W18
A12	D19	H2	L3	P4	U2	W21
A14	D20	H4	L5	P5	U3	W22
A16	E3	H5	L7	P7	U5	Y2
A18	E5	H7	L9	P8	U6	Y19
A20	E6	H9	L11	P10	U7	Y20
A21	E11	H11	L13	P12	U8	AA1
A22	E14	H12	L15	P14	U9	AA2
B1	E17	H14	L16	P16	U10	AA11
B2	E18	H16	L21	P19	U11	AA21
B4	E21	H20	L22	P20	U12	AA22
B6	E22	J1	M1	R1	U13	AB1
B8	F1	J3	M2	R2	U14	AB2
B10	F2	J5	M3	R5	U15	AB3
B12	F4	J7	M4	R7	V2	AB4
B14	F5	J9	M5	R8	V4	AB11
B16	F7	J11	M7	R9	V5	AB12
B18	F16	J13	M8	R10	V6	AB13
B20	F17	J15	M10	R11	V8	AB19
B21	F19	J17	M12	R12	V9	AB20
B22	F20	J21	M14	R13	V11	AB21
C5	G3	J22	M16	R14	V13	AB22
C7	G5	K1	M18	R15	V15	
C9	G6	K2	M19	R16	V17	
C11	G8	K4	M20	R21	W1	
C17	G9	K5	N1	R22	W3	
C19	G10	K7	N2	T1	W5	
D1	G12	K8	N7	T2	W7	

Table 20 PES16NT2 Ground Pins

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Signals Listed Alphabetically

Signal Name	I/O Type	Location	Signal Category
CCLKDS	I	Y11	System
CCLKUS	I	Y10	
GPIO_00	I/O	AB16	General Purpose Input/Output
GPIO_01	I/O	AA16	
GPIO_02	I/O	Y16	
GPIO_03	I/O	AB17	
GPIO_04	I/O	AA17	
GPIO_05	I/O	Y17	
GPIO_06	I/O	AB18	
GPIO_07	I/O	AA18	
JTAG_TCK	I	AB05	JTAG
JTAG_TDI	I	AA05	
JTAG_TDO	O	Y5	
JTAG_TMS	I	AB6	
JTAG_TRST_N	I	AA6	
MSMBADDR_1	I	Y6	SMBus
MSMBADDR_2	I	AB7	
MSMBADDR_3	I	AA7	
MSMBADDR_4	I	Y7	
MSMBCLK	I/O	AB8	
MSMBDAT	I/O	AA8	
MSMBSMODE	I	Y18	System
PEALREV	I	Y12	PCI Express
PEARN00	I	D18	
PEARN01	I	C16	
PEARN02	I	D14	
PEARN03	I	C12	
PEARN04	I	C10	
PEARN05	I	D8	
PEARN06	I	C6	
PEARN07	I	D4	
PEARP00	I	C18	
PEARP01	I	D16	
PEARP02	I	C14	

Table 21 89PES16NT2 Alphabetical Signal List (Part 1 of 4)

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Signal Name	I/O Type	Location	Signal Category
PEARP03	I	D12	PCI Express (cont.)
PEARP04	I	D10	
PEARP05	I	C8	
PEARP06	I	D6	
PEARP07	I	C4	
PEATN00	0	A19	
PEATN01	O	B17	
PEATN02	O	A15	
PEATN03	O	B13	
PEATN04	O	A11	
PEATN05	O	A9	
PEATN06	O	A7	
PEATN07	O	A5	
PEATP00	O	B19	
PEATP01	O	A17	
PEATP02	O	B15	
PEATP03	O	A13	
PEATP04	O	B11	
PEATP05	O	B9	
PEATP06	O	B7	
PEATP07	O	B5	
PECLREV	I	Y14	
PECRN00	I	W19	
PECRN01	I	U20	
PECRN02	I	R19	
PECRN03	I	N20	
PECRN04	I	L19	
PECRN05	I	J19	
PECRN06	I	G20	
PECRN07	I	E19	
PECRP00	I	W20	
PECRP01	I	U19	
PECRP02	I	R20	
PECRP03	I	N19	
PECRP04	I	L20	
PECRP05	I	J20	

Table 21 89PES16NT2 Alphabetical Signal List (Part 2 of 4)

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Signal Name	I/O Type	Location	Signal Category
PECRP06	I	G19	PCI Express (cont.
PECRP07	I	E20	
PECTN00	O	V22	
PECTN01	O	T22	
PECTN02	O	P22	
PECTN03	O	M22	
PECTN04	O	K21	
PECTN05	O	H22	
PECTN06	O	F22	
PECTN07	O	D22	
PECTP00	O	V21	
PECTP01	O	T21	
PECTP02	O	P21	
PECTP03	O	M21	
PECTP04	O	K22	
PECTP05	O	H21	
PECTP06	O	F21	
PECTP07	O	D21	
PENTBRSTN	I	AA15	System
PEREFCLKN0	I	P2	PCI Express
PEREFCLKN1	I	Y22	
PEREFCLKP0	I	P1	
PEREFCLKP1	I	Y21	
PERSTN	I	AB15	System
REFCLKM	I	AA19	PCI Express
RSTHALT	I	Y15	System
SSMBADDR_1	I	Y8	SMBus
SSMBADDR_2	I	AB9	
SSMBADDR_3	I	AA9	
SSMBADDR_5	I	Y9	
SSMBCLK	I/O	AB10	
SSMBDAT	I/O	AA10	

Table 21 89PES16NT2 Alphabetical Signal List (Part 3 of 4)

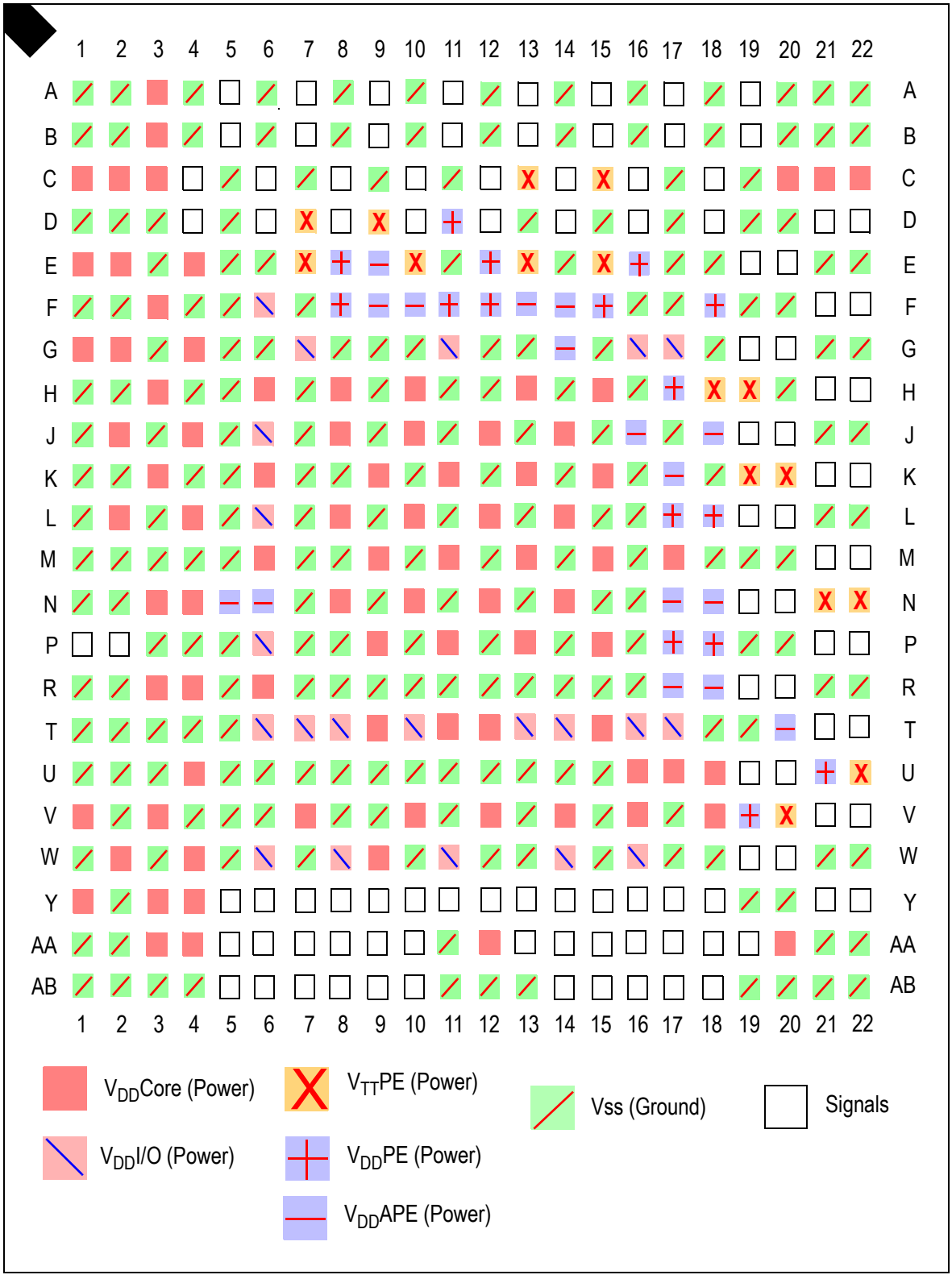
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Signal Name	I/O Type	Location	Signal Category
SWMODE_0	I	AA13	System
SWMODE_1	I	Y13	
SWMODE_2	I	AB14	
SWMODE_3	I	AA14	
V_{DD}CORE, V_{DD}APE, V_{DD}IO, V_{DD}PE, V_{TT}PE	See Table 19 for a listing of power pins.		
V_{SS}	See Table 20 for a listing of ground pins.		

Table 21 89PES16NT2 Alphabetical Signal List (Part 4 of 4)

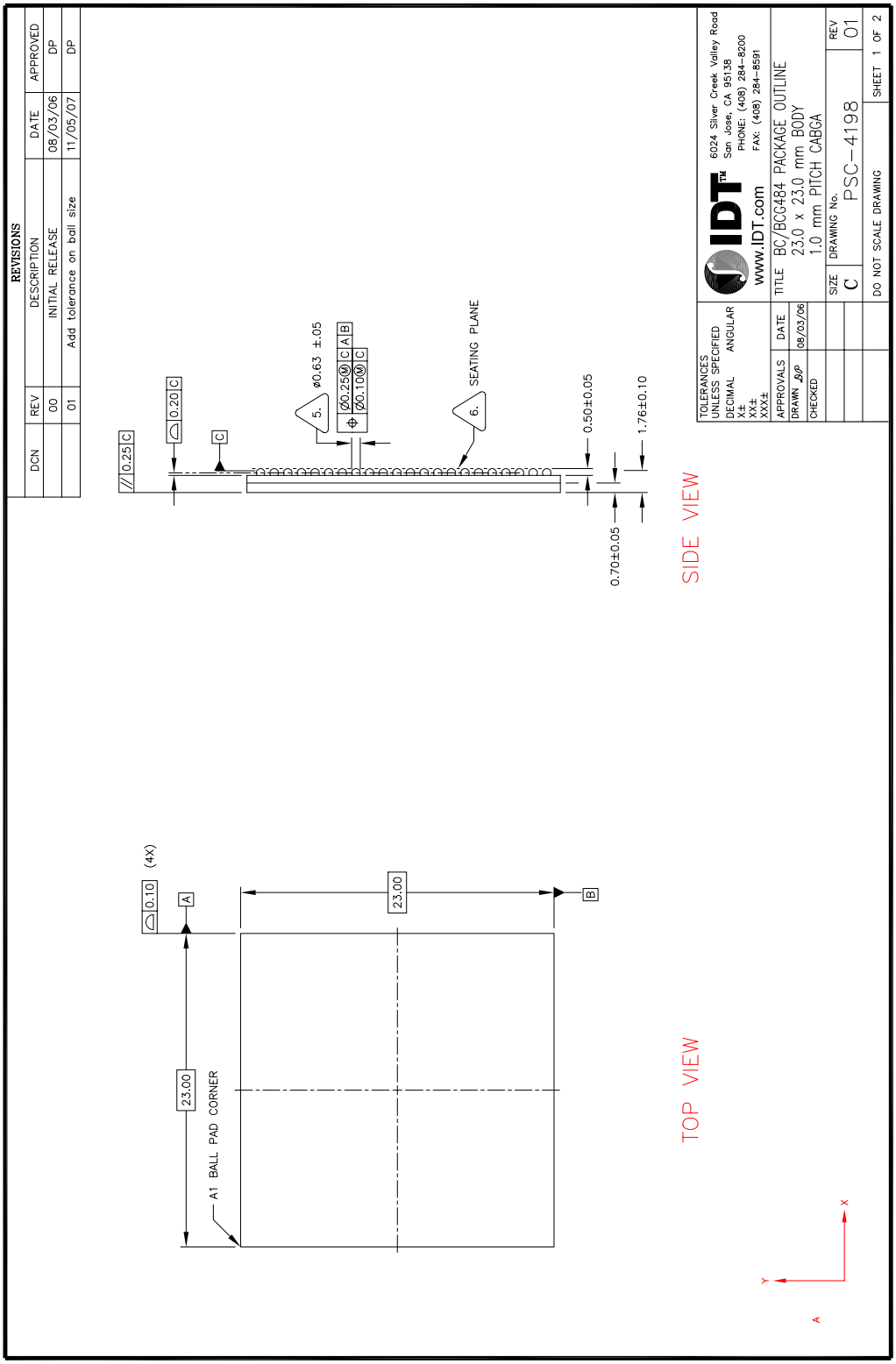
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PES16NT2 Pinout — Top View



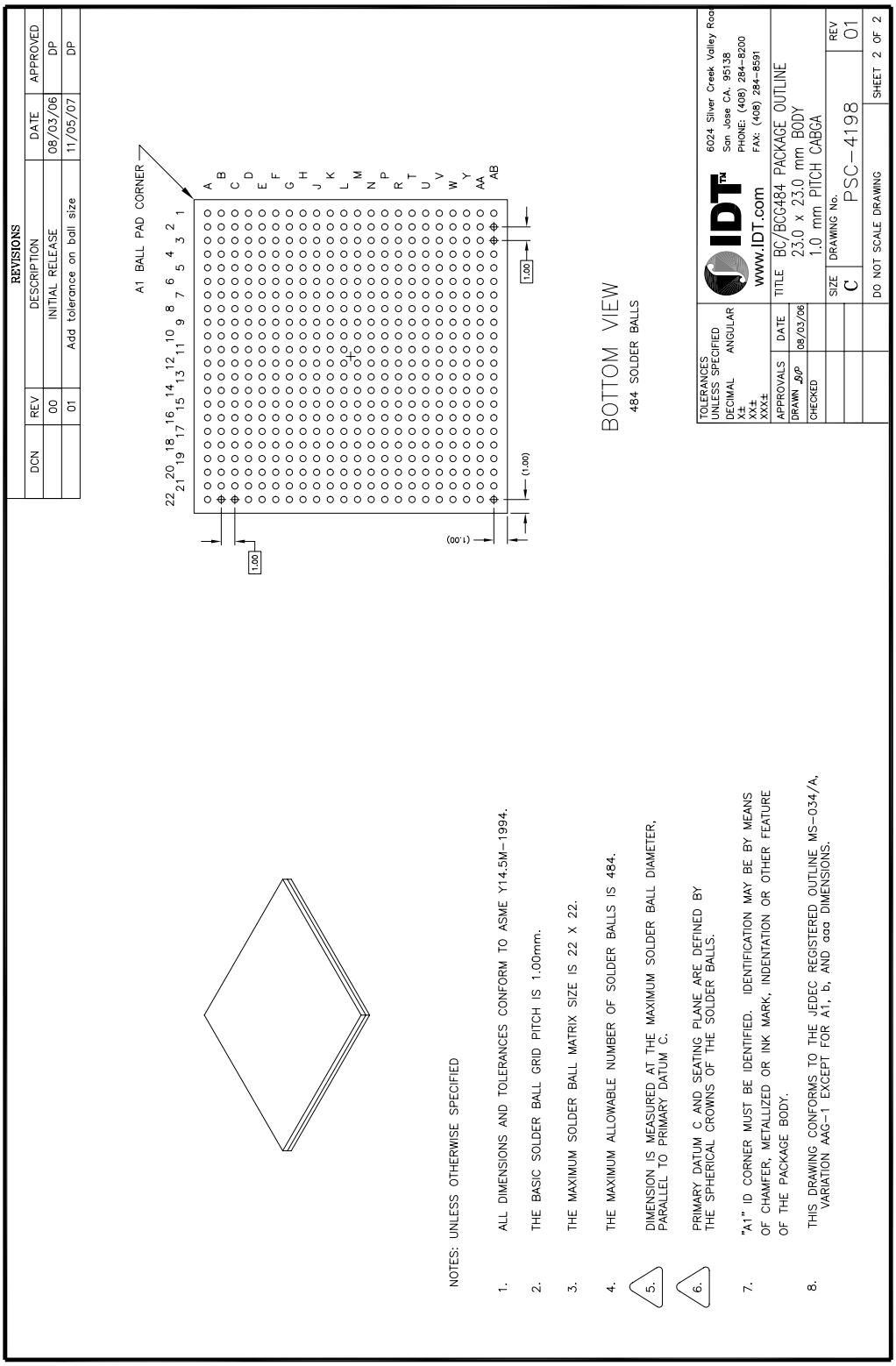
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PES16NT2 Package Drawing — 484-Pin BC484/BCG484



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PES16NT2 Package Drawing — Page Two



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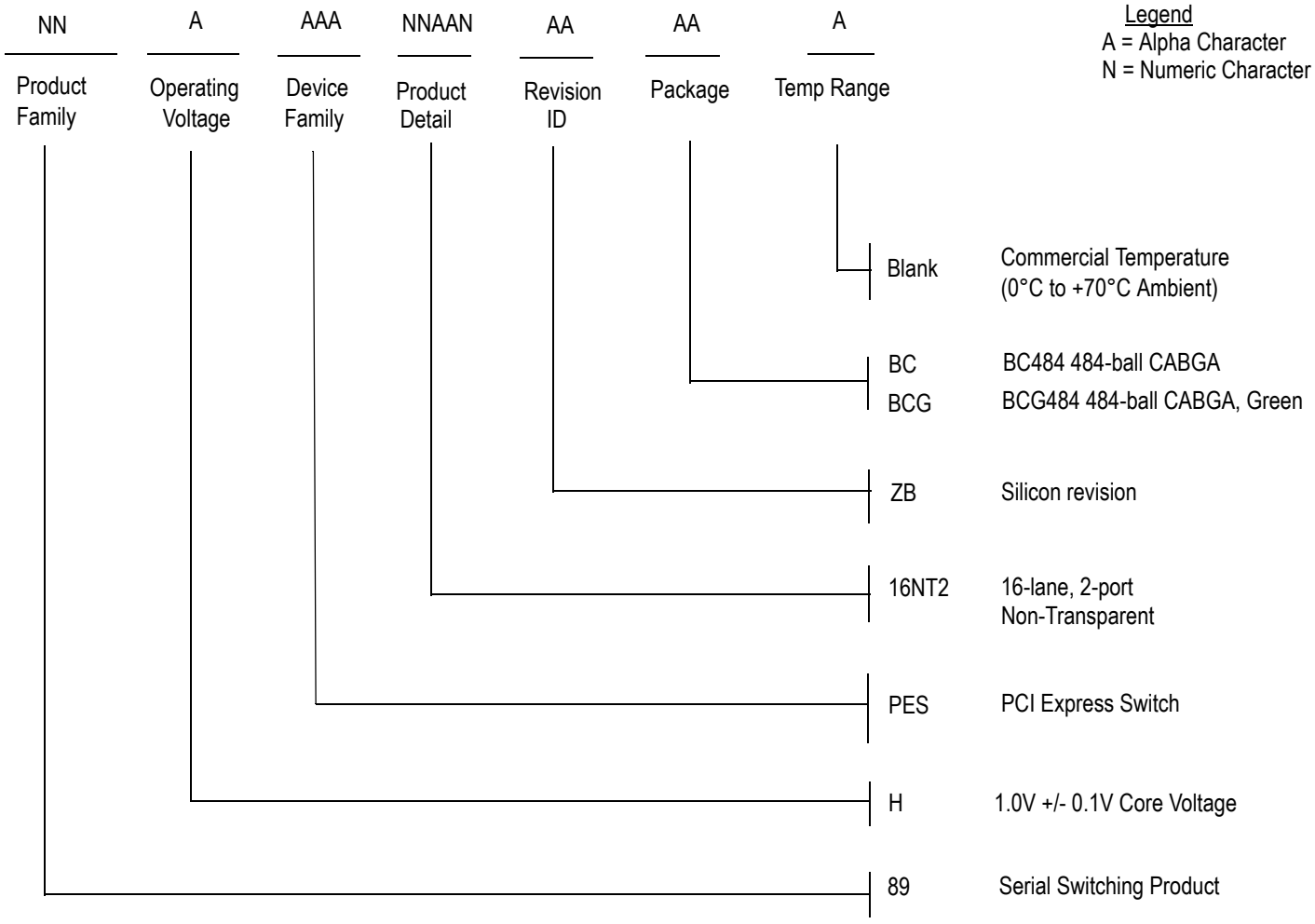
Revision History

April 15, 2008: Initial publication of data sheet.

January 5, 2009: On the Ordering Information page, changed silicon revision from ZA to ZB.

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Ordering Information



Valid Combinations

89HPES16NT2ZBBC	484-ball CABGA package, Commercial Temperature
89HPES16NT2ZBBCG	484-ball Green CABGA package, Commercial Temperature

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Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,
Koto-ku, Tokyo 135-0061, Japan
www.renesas.com

Contact Information

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