24-Lane 3-Port PCI Express® Switch

89HPES24N3A Data Sheet

Device Overview

The 89HPES24N3A is a member of the IDT PRECISE™ family of PCI Express® switching solutions. The PES24N3A is a 24-lane, 3-port peripheral chip that performs PCI Express packet switching with a feature set optimized for high performance applications such as servers, storage, and communications/networking. It provides connectivity and switching functions between a PCI Express upstream port and two downstream ports and supports switching between downstream ports.

Features

- High Performance PCI Express Switch
  - *Twenty-four 2.5 Gbps PCI Express lanes*
  - *Three switch ports*
  - *Upstream port configurable up to x8*
  - *Downstream ports configurable up to x8*
  - *Low-latency cut-through switch architecture*
  - *Support for Max Payload Size up to 2048 bytes*
  - *One virtual channel*
  - *Eight traffic classes*
  - *PCI Express Base Specification Revision 1.1 compliant*
- Flexible Architecture with Numerous Configuration Options
  - *Automatic per port link width negotiation to x8, x4, x2 or x1*
  - *Automatic lane reversal on all ports*
  - *Automatic polarity inversion on all lanes*
  - *Ability to load device configuration from serial EEPROM*
- Legacy Support
  - *PCI compatible INTx emulation*
  - *Bus locking*
- Highly Integrated Solution
  - *Requires no external components*
  - *Incorporates on-chip internal memory for packet buffering and queueing*
  - *Integrates twenty-four 2.5 Gbps embedded SerDes with 8B/10B encoder/decoder (no separate transceivers needed)*
- Reliability, Availability, and Serviceability (RAS) Features
  - *Supports ECRC and Advanced Error Reporting*
  - *Internal end-to-end parity protection on all TLPs ensures data integrity even in systems that do not implement end-to-end CRC (ECRC)*
  - *Supports PCI Express Native Hot-Plug, Hot-Swap capable I/O*
  - *Compatible with Hot-Plug I/O expanders used on PC and server motherboards*

Block Diagram

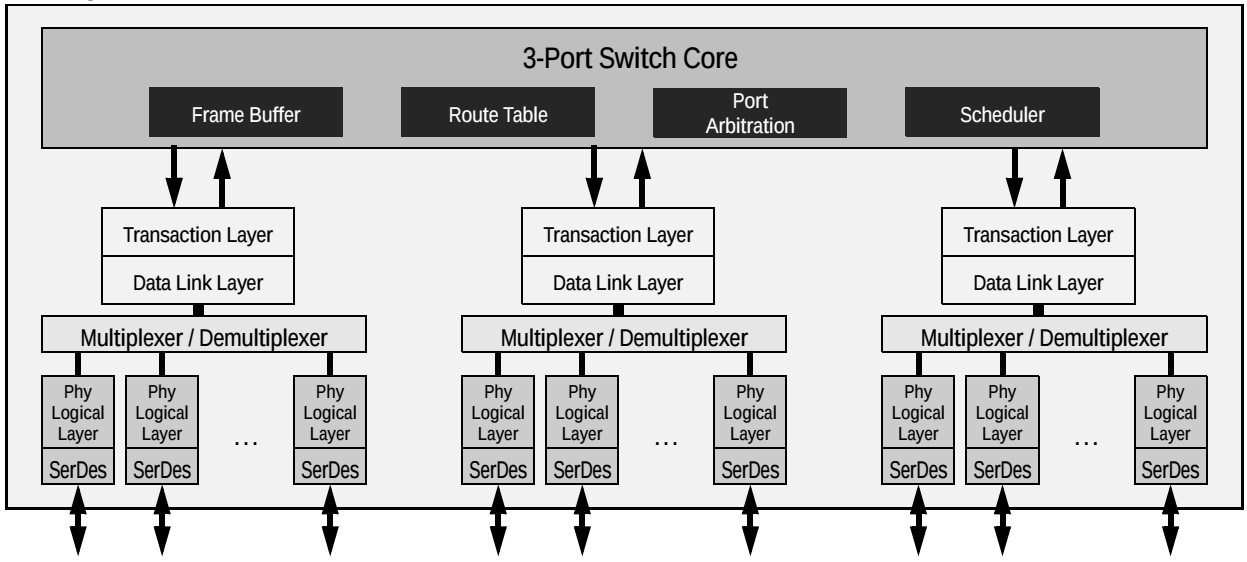


Figure 1 Internal Block Diagram

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- Power Management
  - *Utilizes advanced low-power design techniques to achieve low typical power consumption*
  - *Supports PCI Power Management Interface specification (PCI-PM 1.1)*
    - *Supports device power management states: D0, $D3_{hot}$ and $D3_{cold}$*
  - *Unused SerDes are disabled*
- Testability and Debug Features
  - *Ability to read and write any internal register via the SMBus*
- Eight General Purpose Input/Output Pins
  - *Each pin may be individually configured as an input or output*
  - *Each pin may be individually configured as an interrupt input*
  - *Some pins have selectable alternate functions*
- Packaged in 27x27mm 420 ball BGA with 1mm ball spacing

Product Description

Utilizing standard PCI Express interconnect, the PES24N3A provides the most efficient I/O connectivity solution for applications requiring high throughput, low latency, and simple board layout with a minimum number of board layers. It provides connectivity for up to 3 ports across 24 integrated serial lanes. Each lane provides 2.5 Gbps of bandwidth in both directions and is fully compliant with PCI Express Base specification revision 1.1.

SMBus Interface

The PES24N3A contains two SMBus interfaces. The slave interface provides full access to the configuration registers in the PES24N3A, allowing every configuration register in the device to be read or written by an external agent. The master interface allows the default configuration register values of the PES24N3A to be overridden following a reset with values programmed in an external serial EEPROM. The master interface is also used by an external Hot-Plug I/O expander.

Six pins make up each of the two SMBus interfaces. These pins consist of an SMBus clock pin, an SMBus data pin, and 4 SMBus address pins. In the slave interface, these address pins allow the SMBus address to which the device responds to be configured. In the master interface, these address pins allow the SMBus address of the serial configuration EEPROM from which data is loaded to be configured. The SMBus address is set up on negation of PERSTN by sampling the corresponding address pins. When the pins are sampled, the resulting address is assigned as shown in Table 1.

Bit	Slave SMBus Address	Master SMBus Address
1	SSMBADDR[1]	MSMBADDR[1]
2	SSMBADDR[2]	MSMBADDR[2]
3	SSMBADDR[3]	MSMBADDR[3]

Table 1 Master and Slave SMBus Address Assignment

Bit	Slave SMBus Address	Master SMBus Address
4	0	MSMBADDR[4]
5	SSMBADDR[5]	1
6	1	0
7	1	1

Table 1 Master and Slave SMBus Address Assignment

As shown in Figure 2, the master and slave SMBuses may be used in a unified or split configuration. In the unified configuration, shown in Figure 2(a), the master and slave SMBuses are tied together and the PES24N3A acts both as a SMBus master as well as a SMBus slave on this bus. This requires that the SMBus master or processor that has access to PES24N3A registers supports SMBus arbitration. In some systems, this SMBus master interface may be implemented using general purpose I/O pins on a processor or micro controller, and may not support SMBus arbitration. To support these systems, the PES24N3A may be configured to operate in a split configuration as shown in Figure 2(b).

In the split configuration, the master and slave SMBuses operate as two independent buses and thus multi-master arbitration is never required. The PES24N3A supports reading and writing of the serial EEPROM on the master SMBus via the slave SMBus, allowing in system programming of the serial EEPROM.

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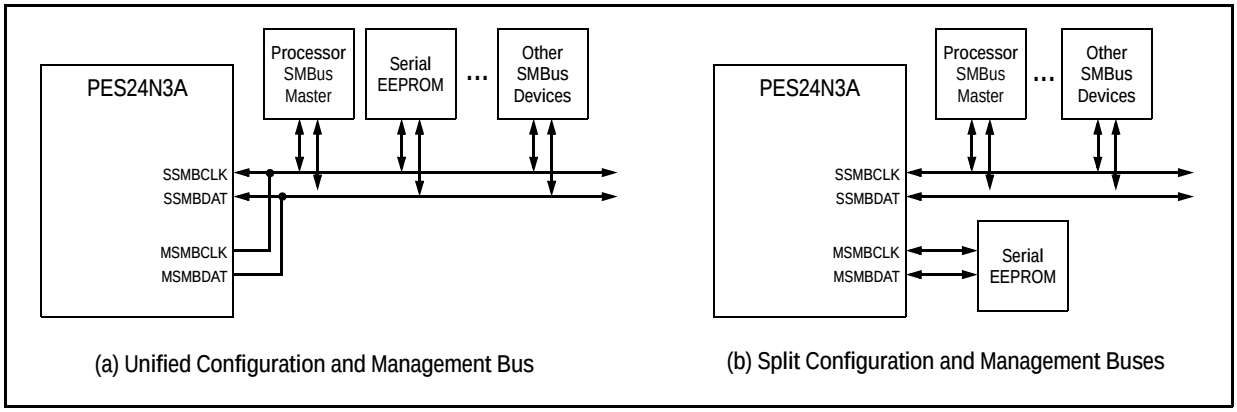


Figure 2 SMBus Interface Configuration Examples

Hot-Plug Interface

The PES24N3A supports PCI Express Hot-Plug on each downstream port. To reduce the number of pins required on the device, the PES24N3A utilizes an external I/O expander, such as that used on PC motherboards, connected to the SMBus master interface. Following reset and configuration, whenever the state of a Hot-Plug output needs to be modified, the PES24N3A generates an SMBus transaction to the I/O expander with the new value of all of the outputs. Whenever a Hot-Plug input changes, the I/O expander generates an interrupt which is received on the IOEXPINTN input pin (alternate function of GPIO) of the PES24N3A. In response to an I/O expander interrupt, the PES24N3A generates an SMBus transaction to read the state of all of the Hot-Plug inputs from the I/O expander.

General Purpose Input/Output

The PES24N3A provides eight General Purpose Input/Output (GPIO) pins that may be used by the system designer as bit I/O ports. Each GPIO pin may be configured independently as an input or output through software control. Some GPIO pins are shared with other on-chip functions. These alternate functions may be enabled via software, SMBus slave interface, or serial configuration EEPROM.

The PES24N3A is based on a flexible and efficient layered architecture. The PCI Express layer consists of SerDes, Physical, Data Link and Transaction layers in compliance with PCI Express Base specification Revision 1.1. The PES24N3A can operate either as a store and forward or cut-through switch and is designed to switch memory and I/O transactions. It supports eight Traffic Classes (TCs) and one Virtual Channel (VC) with sophisticated resource management to enable efficient switching and I/O connectivity for servers, storage, and embedded applications.

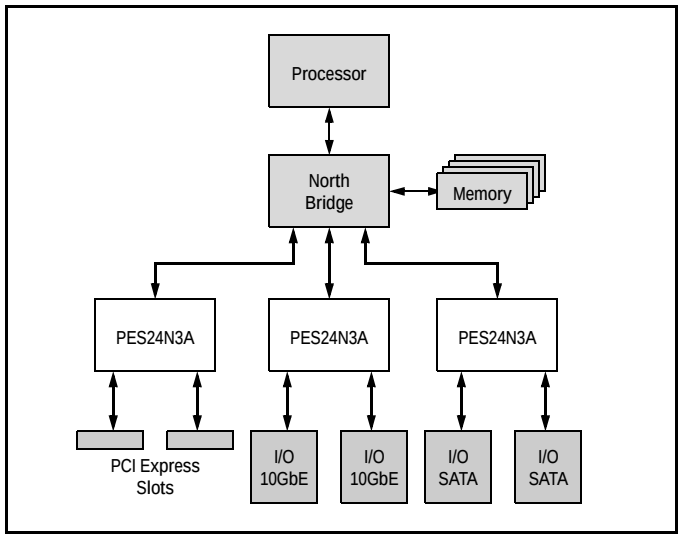


Figure 3 I/O Expansion Application

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Pin Description

The following tables list the functions of the pins provided on the PES24N3A. Some of the functions listed may be multiplexed onto the same pin. The active polarity of a signal is defined using a suffix. Signals ending with an "N" are defined as being active, or asserted, when at a logic zero (low) level. All other signals (including clocks, buses, and select lines) will be interpreted as being active, or asserted, when at a logic one (high) level.

Note: In the PES24N3A, the two downstream ports are labeled port 2 and port 4.

Signal	Type	Name/Description
PE0RP[7:0] PE0RN[7:0]	I	**PCI Express Port 0 Serial Data Receive.** Differential PCI Express receive pairs for port 0. Port 0 is the upstream port.
PE0TP[7:0] PE0TN[7:0]	O	**PCI Express Port 0 Serial Data Transmit.** Differential PCI Express transmit pairs for port 0. Port 0 is the upstream port.
PE2RP[7:0] PE2RN[7:0]	I	**PCI Express Port 2 Serial Data Receive.** Differential PCI Express receive pairs for port 2.
PE2TP[7:0] PE2TN[7:0]	O	**PCI Express Port 2 Serial Data Transmit.** Differential PCI Express transmit pairs for port 2.
PE4RP[7:0] PE4RN[7:0]	I	**PCI Express Port 4 Serial Data Receive.** Differential PCI Express receive pairs for port 4.
PE4TP[7:0] PE4TN[7:0]	O	**PCI Express Port 4 Serial Data Transmit.** Differential PCI Express transmit pairs for port 4.
PEREFCLKP[2:1] PEREFCLKN[2:1]	I	**PCI Express Reference Clock.** Differential reference clock pair input. This clock is used as the reference clock by on-chip PLLs to generate the clocks required for the system logic and on-chip SerDes. The frequency of the differential reference clock is determined by the REFCLKM signal.
REFCLKM	I	**PCI Express Reference Clock Mode Select.** This signal selects the frequency of the reference clock input. 0x0 - 100 MHz 0x1 - 125 MHz

Table 2 PCI Express Interface Pins

Signal	Type	Name/Description
MSMBADDR[4:1]	I	**Master SMBus Address.** These pins determine the SMBus address of the serial EEPROM from which configuration information is loaded.
MSMBCLK	I/O	**Master SMBus Clock.** This bidirectional signal is used to synchronize transfers on the master SMBus. It is active and generating the clock only when the EEPROM or I/O Expanders are being accessed.
MSMBDAT	I/O	**Master SMBus Data.** This bidirectional signal is used for data on the master SMBus.
SSMBADDR[5,3:1]	I	**Slave SMBus Address.** These pins determine the SMBus address to which the slave SMBus interface responds.
SSMBCLK	I/O	**Slave SMBus Clock.** This bidirectional signal is used to synchronize transfers on the slave SMBus.
SSMBDAT	I/O	**Slave SMBus Data.** This bidirectional signal is used for data on the slave SMBus.

Table 3 SMBus Interface Pins

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Signal	Type	Name/Description
GPIO[0]	I/O	General Purpose I/O. This pin can be configured as a general purpose I/O pin. Alternate function pin name: P2RSTN Alternate function pin type: Output Alternate function: Reset output for downstream port 2
GPIO[1]	I/O	General Purpose I/O. This pin can be configured as a general purpose I/O pin. Alternate function pin name: P4RSTN Alternate function pin type: Output Alternate function: Reset output for downstream port 4
GPIO[2]	I/O	General Purpose I/O. This pin can be configured as a general purpose I/O pin. Alternate function pin name: IOEXPINTN0 Alternate function pin type: Input Alternate function: I/O Expander interrupt 0 input
GPIO[3]	I/O	General Purpose I/O. This pin can be configured as a general purpose I/O pin.
GPIO[4]	I/O	General Purpose I/O. This pin can be configured as a general purpose I/O pin. Alternate function pin name: IOEXPINTN2 Alternate function pin type: Input Alternate function: I/O Expander interrupt 2 input
GPIO[5]	I/O	General Purpose I/O. This pin can be configured as a general purpose I/O pin.
GPIO[6]	I/O	General Purpose I/O. This pin can be configured as a general purpose I/O pin.
GPIO[7]	I/O	General Purpose I/O. This pin can be configured as a general purpose I/O pin. Alternate function pin name: GPEN Alternate function pin type: Output Alternate function: General Purpose Event (GPE) output

Table 4 General Purpose I/O Pins

Signal	Type	Name/Description
CCLKDS	I	Common Clock Downstream. When the CCLKDS pin is asserted, it indicates that a common clock is being used between the downstream device and the downstream port.
CCLKUS	I	Common Clock Upstream. When the CCLKUS pin is asserted, it indicates that a common clock is being used between the upstream device and the upstream port.
MSMBSMODE	I	Master SMBus Slow Mode. The assertion of this pin indicates that the master SMBus should operate at 100 KHz instead of 400 KHz. This value may not be overridden.

Table 5 System Pins (Part 1 of 2)

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Signal	Type	Name/Description
PERSTN	I	**Fundamental Reset.** Assertion of this signal resets all logic inside PES24N3A and initiates a PCI Express fundamental reset.
RSTHALT	I	**Reset Halt.** When this signal is asserted during a PCI Express fundamental reset, PES24N3A executes the reset procedure and remains in a reset state with the Master and Slave SMBuses active. This allows software to read and write registers internal to the device before normal device operation begins. The device exits the reset state when the RSTHALT bit is cleared in the SWCTL register by an SMBus master.
SWMODE[3:0]	I	**Switch Mode.** These configuration pins determine the PES24N3A switch operating mode. 0x0 - Normal switch mode 0x1 - Normal switch mode with Serial EEPROM initialization 0x2 - through 0xF Reserved

Table 5 System Pins (Part 2 of 2)

Signal	Type	Name/Description
JTAG_TCK	I	**JTAG Clock**. This is an input test clock used to clock the shifting of data into or out of the boundary scan logic or JTAG Controller. JTAG_TCK is independent of the system clock with a nominal 50% duty cycle.
JTAG_TDI	I	**JTAG Data Input**. This is the serial data input to the boundary scan logic or JTAG Controller.
JTAG_TDO	O	**JTAG Data Output**. This is the serial data shifted out from the boundary scan logic or JTAG Controller. When no data is being shifted out, this signal is tri-stated.
JTAG_TMS	I	**JTAG Mode**. The value on this signal controls the test mode select of the boundary scan logic or JTAG Controller.
JTAG_TRST_N	I	**JTAG Reset**. This active low signal asynchronously resets the boundary scan logic and JTAG TAP Controller. An external pull-up on the board is recommended to meet the JTAG specification in cases where the tester can access this signal. However, for systems running in functional mode, one of the following should occur: 1) actively drive this signal low with control logic 2) statically drive this signal low with an external pull-down on the board

Table 6 Test Pins

Signal	Type	Name/Description
V_{DD}CORE	I	**Core V_{DD}.** Power supply for core logic.
V_{DD}IO	I	**I/O V_{DD}.** LVTTL I/O buffer power supply.
V_{DD}PE	I	**PCI Express Digital Power.** PCI Express digital power used by the digital power of the SerDes.

Table 7 Power and Ground Pins

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Signal	Type	Name/Description
$V_{DD}APE$	I	PCI Express Analog Power. PCI Express analog power used by the PLL and bias generator.
$V_{TT}PE$	I	PCI Express Termination Power.
V_{SS}	I	Ground.

Table 7 Power and Ground Pins

Pin Characteristics

Note: Some input pads of the PES24N3A do not contain internal pull-ups or pull-downs. Unused inputs should be tied off to appropriate levels. This is especially critical for unused control signal inputs which, if left floating, could adversely affect operation. Also, any input pin left floating can cause a slight increase in power consumption.

Function	Pin Name	Type	Buffer	I/O Type	Internal Resistor[1]	Notes
PCI Express Interface	PE0RN[7:0]	I	CML	Serial link		
	PE0RP[7:0]	I				
	PE0TN[7:0]	O				
	PE0TP[7:0]	O				
	PE2RN[7:0]	I				
	PE2RP[7:0]	I				
	PE2TN[7:0]	O				
	PE2TP[7:0]	O				
	PE4RN[7:0]	I				
	PE4RP[7:0]	I				
	PE4TN[7:0]	O				
	PE4TP[7:0]	O				
	PEREFCLKN[2:1]	I	LVPECL/ CML	Diff. Clock Input		Refer to Table 9
	PEREFCLKP[2:1]	I				
	REFCLKM	I	LVTTL	Input	pull-down	
SMBus	MSMBADDR[4:1]	I	LVTTL	Input	pull-up	
	MSMBCLK	I/O		STI[2]		pull-up on board
	MSMBDAT	I/O		STI		pull-up on board
	SSMBADDR[5,3:1]	I		Input	pull-up	
	SSMBCLK	I/O		STI		pull-up on board
	SSMBDAT	I/O		STI		pull-up on board
General Purpose I/O	GPIO[7:0]	I/O	LVTTL	High Drive	pull-up	

Table 8 Pin Characteristics (Part 1 of 2)

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Function	Pin Name	Type	Buffer	I/O Type	Internal Resistor[1]	Notes
System Pins	CCLKDS	I	LVTTL	Input	pull-up	
	CCLKUS	I			pull-up	
	MSMBSMODE	I			pull-down	
	PERSTN	I				
	RSTHALT	I			pull-down	
	SWMODE[3:0]	I			pull-down	
EJTAG / JTAG	JTAG_TCK	I	LVTTL	STI	pull-up	
	JTAG_TDI	I		STI	pull-up	
	JTAG_TDO	O				
	JTAG_TMS	I		STI	pull-up	
	JTAG_TRST_N	I		STI	pull-up	External pull-down

Table 8 Pin Characteristics (Part 2 of 2)

1. Internal resistor values under typical operating conditions are 54K Ω for pull-up and 251K Ω for pull-down.

2. Schmitt Trigger Input (STI).

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Logic Diagram — PES24N3A

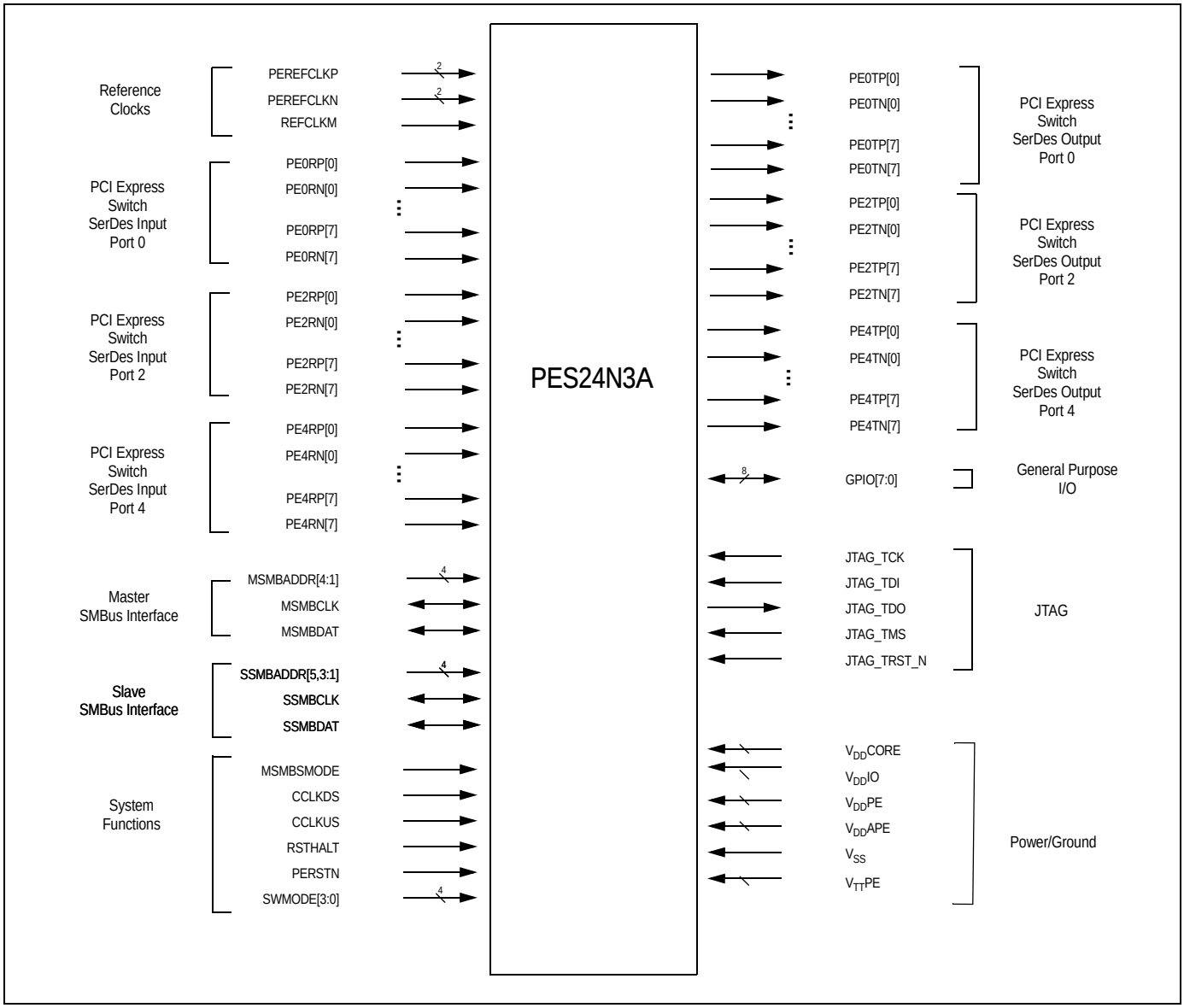


Figure 4 PES24N3A Logic Diagram

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System Clock Parameters

Values based on systems running at recommended supply voltages and operating temperatures, as shown in Tables 13 and 14.

Parameter	Description	Min	Typical	Max	Unit
$Refclk_{FREQ}$	Input reference clock frequency range	100		125[1]	MHz
$Refclk_{DC}$[2]	Duty cycle of input clock	40	50	60	%
T_R, T_F	Rise/Fall time of input clocks			0.2*RCUI	RCUI[3]
V_{SW}	Differential input voltage swing[4]	0.6		1.6	V
T_{jitter}	Input clock jitter (cycle-to-cycle)			125	ps
R_T	Termination Resistor		110		Ohms

Table 9 Input Clock Requirements

1. The input clock frequency will be either 100 or 125 MHz depending on signal REFCLKM.
2. ClkIn must be AC coupled. Use 0.01 — 0.1 µF ceramic capacitors.
3. RCUI (Reference Clock Unit Interval) refers to the reference clock period.
4. AC coupling required.

AC Timing Characteristics

Parameter	Description	Min[1]	Typical[1]	Max[1]	Units
PCIe Transmit					
UI	Unit Interval	399.88	400	400.12	ps
T_{TX-EYE}	Minimum Tx Eye Width	0.7	.9		UI
$T_{TX-EYE-MEDIAN-to-MAX-JITTER}$	Maximum time between the jitter median and maximum deviation from the median			0.15	UI
$T_{TX-RISE}$, $T_{TX-FALL}$	D+ / D- Tx output rise/fall time	50	90		ps
$T_{TX- IDLE-MIN}$	Minimum time in idle	50			UI
$T_{TX-IDLE-SET-TO-IDLE}$	Maximum time to transition to a valid Idle after sending an Idle ordered set			20	UI
$T_{TX-IDLE-TO-DIFF-DATA}$	Maximum time to transition from valid idle to diff data			20	UI
$T_{TX-SKEW}$	Transmitter data skew between any 2 lanes		500	1300	ps
PCIe Receive					
UI	Unit Interval	399.88	400	400.12	ps
$T_{RX-EYE (with jitter)}$	Minimum Receiver Eye Width (jitter tolerance)	0.4			UI

Table 10 PCIe AC Timing Characteristics (Part 1 of 2)

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Parameter	Description	Min[1]	Typical[1]	Max[1]	Units
$T_{RX-EYE-MEDIUM\ TO\ MAX\ JITTER}$	Max time between jitter median & max deviation			0.3	UI
$T_{RX-IDLE-DET-DIFF-ENTER\ TIME}$	Unexpected Idle Enter Detect Threshold Integration Time			10	ms
$T_{RX-SKEW}$	Lane to lane input skew			20	ns

Table 10 PCIe AC Timing Characteristics (Part 2 of 2)

1. Minimum, Typical, and Maximum values meet the requirements under PCI Specification 1.1

Signal	Symbol	Reference Edge	Min	Max	Unit	Timing Diagram Reference
GPIO						
GPIO[7:0][1]	Tpw[2]	None	50	—	ns	

Table 11 GPIO AC Timing Characteristics

1. GPIO signals must meet the setup and hold times if they are synchronous or the minimum pulse width if they are asynchronous.

2. The values for this symbol were determined by calculation, not by testing.

Signal	Symbol	Reference Edge	Min	Max	Unit	Timing Diagram Reference
JTAG						
JTAG_TCK	Tper_16a	none	50.0	—	ns	See Figure 5.
	Thigh_16a, Tlow_16a		10.0	25.0	ns	
JTAG_TMS[1], JTAG_TDI	Tsu_16b	JTAG_TCK rising	2.4	—	ns	
	Thld_16b		1.0	—	ns	
JTAG_TDO	Tdo_16c	JTAG_TCK falling	—	20	ns	
	Tdz_16c[2]		—	20	ns	
JTAG_TRST_N	Tpw_16d[2]	none	25.0	—	ns	

Table 12 JTAG AC Timing Characteristics

1. The JTAG specification, IEEE 1149.1, recommends that JTAG_TMS should be held at 1 while the signal applied at JTAG_TRST_N changes from 0 to 1. Otherwise, a race may occur if JTAG_TRST_N is deasserted (going from low to high) on a rising edge of JTAG_TCK when JTAG_TMS is low, because the TAP controller might go to either the Run-Test/Idle state or stay in the Test-Logic-Reset state.

2. The values for this symbol were determined by calculation, not by testing.

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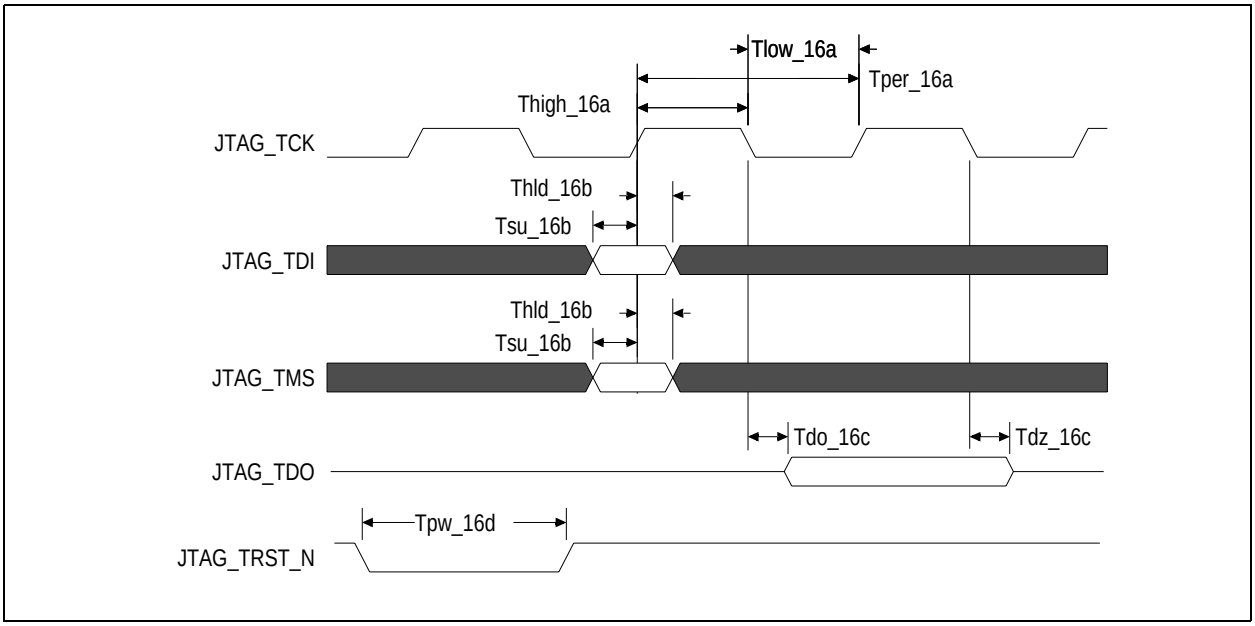


Figure 5 JTAG AC Timing Waveform

Recommended Operating Supply Voltages

Symbol	Parameter	Minimum	Typical	Maximum	Unit
V_{DD}CORE	Internal logic supply	0.9	1.0	1.1	V
V_{DD}I/O	I/O supply except for SerDes LVPECL/CML	3.0	3.3	3.6	V
V_{DD}PE	PCI Express Digital Power	0.9	1.0	1.1	V
V_{DD}APE	PCI Express Analog Power	0.9	1.0	1.1	V
V_{TT}PE	PCI Express Serial Data Transmit Termination Voltage	1.425	1.5	1.575	V
V_{SS}	Common ground	0	0	0	V

Table 13 PES24N3A Operating Voltages

Power-Up Sequence

This section describes the sequence in which various voltages must be applied to the part during power-up to ensure proper functionality. For the PES24N3A, the power-up sequence must be as follows:

1. V_{DD}I/O — 3.3V
2. V_{DD}Core, V_{DD}PE, V_{DD}APE — 1.0V
3. V_{TT}PE — 1.5V

When powering up, each voltage level must ramp and stabilize prior to applying the next voltage in the sequence to ensure internal latch-up issues are avoided. There are no maximum time limitations in ramping to valid power levels. The power-down sequence must be in the reverse order of the power-up sequence.

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Recommended Operating Temperature

Grade	Temperature
Commercial	0°C to +70°C Ambient

Table 14 PES24N3A Operating Temperatures

Power Consumption

Typical power is measured under the following conditions: 25°C Ambient, 35% total link usage on all ports, typical voltages defined in Table 13 (and also listed below).

Maximum power is measured under the following conditions: 70°C Ambient, 85% total link usage on all ports, maximum voltages defined in Table 13 (and also listed below).

Number of active Lanes per Port		Core Supply		PCIe Digital Supply		PCIe Analog Supply		PCIe Termination Supply		I/O Supply		Total	
		Typ 1.0V	Max 1.1V	Typ 1.0V	Max 1.1V	Typ 1.0V	Max 1.1V	Typ 1.5V	Max 1.575V	Typ 3.3V	Max 3.6V	Typ Power	Max Power
8/8/8	mA	705	928	1037	1247	415	455	520	617	1	1	2.9W	3.9W
	Watts	0.705	1.02	1.037	1.37	0.415	0.50	0.78	0.97	0.003	0.004		
8/4/4	mA	676	845	873	1004	409	434	360	408	1	1	2.5W	3.2W
	Watts	0.676	0.93	0.873	1.104	0.41	0.477	0.36	0.643	0.003	0.004		

Table 15 PES24N3A Power Consumption

Thermal Considerations

This section describes thermal considerations for the PES24N3A (27mm^2 BXG420 package). The data in Table 16 below contains information that is relevant to the thermal performance of the PES24N3A switch.

Symbol	Parameter	Value	Units	Conditions
$T_{J(max)}$	Junction Temperature	125	^{0}C	Maximum
$T_{A(max)}$	Ambient Temperature	70	^{0}C	Maximum for commercial-rated products
$\theta_{JA(effective)}$	Effective Thermal Resistance, Junction-to-Ambient	10.6	^{0}C/W	Zero air flow
		8.5	^{0}C/W	1 m/S air flow
		7.6	^{0}C/W	2 m/S air flow
θ_{JB}	Thermal Resistance, Junction-to-Board	6.8	^{0}C/W	
θ_{JC}	Thermal Resistance, Junction-to-Case	0.7	^{0}C/W	
P	Power Dissipation of the Device	3.9	Watts	Maximum

Table 16 Thermal Specifications for PES24N3A, 27x27 mm BXG420 Package

Note: The parameter $\theta_{JA(eff)}$ is not the *absolute* thermal resistance for the package as defined by JEDEC (JESD-51). Because resistance can vary with the number of board layers, size of the board, and airflow, $\theta_{JA(eff)}$ is the *effective* thermal resistance. The values for effective θ_{JA} given above are based on a 10-layer, standard height, full length (4.3"x12.2") PCIe add-in card.

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Heat Sink

Table 17 lists heat sink requirements for the PES24N3A under three common usage scenarios. As shown in this table, a heat sink is not required in most cases.

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Air Flow	Board Size	Board Layers	Heat Sink Requirement
Zero	3.9"x6.2" (ExpressModule form factor) or larger	10 or more	No heat sink required
Zero	Any	14 or more	No heat sink required
1 m/S or more	Any	Any	No heat sink required

Table 17 Heat Sink Requirements Based on Air Flow and Board Characteristics

Thermal Usage Examples

The junction-to-ambient thermal resistance is a measure of a device's ability to dissipate heat from the die to its surroundings in the absence of a heat sink. The general formula to determine θ_{JA} is:

$$\theta_{JA} = (T_J - T_A)/P$$

Thermal reliability of a device is generally assured when the actual value of T_J in the specific system environment being considered is less than the maximum T_J specified for the device. Using an ambient temperature of 70^oC and assuming a system with 1m/S airflow, the actual value of T_J is:

$$T_{J(actual)} = T_A + P * \theta_{JA(eff)} = 70^oC + 3.9W * 8.5W/^oC = 103^oC$$

The actual T_J of 103^oC is well below the maximum T_J of 125^oC specified for the device (shown in Table 16). Therefore, no heat sink is needed in this scenario. The formula is also useful from a system design perspective. It can be used to determine if a heat sink should be added to the device based on some desired value of T_J. For example, if for reliability purposes the desired T_J is 100^oC, then the maximum allowable T_A is:

$$T_{A(allowed)} = T_{J(desired)} - (P * \theta_{JA(effective)})$$
$$T_{A(allowed)} = 100^oC - (3.9W * 8.5W/^oC) = 100^oC - 33^oC = 67^oC$$

An appropriate level of increased air flow and/or a heat sink can be added to achieve this lower ambient temperature. Please contact ssdhelp@idt.com for further assistance.

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DC Electrical Characteristics

Values based on systems running at recommended supply voltages, as shown in Table 13.

Note: See Table 8, Pin Characteristics, for a complete I/O listing.

I/O Type	Parameter	Description	Min[1]	Typ[1]	Max[1]	Unit	Conditions
Serial Link	PCIe Transmit						
	$V_{TX-DIFFp-p}$	Differential peak-to-peak output voltage	800		1200	mV	
	$V_{TX-DE-RATIO}$	De-emphasized differential output voltage	-3		-4	dB	
	$V_{TX-DC-CM}$	DC Common mode voltage	-0.1	1	3.7	V	
	$V_{TX-CM-ACP}$	RMS AC peak common mode output voltage			20	mV	
	$V_{TX-CM-DC-active-idle-delta}$	Abs delta of DC common mode voltage between L0 and idle			100	mV	
	$V_{TX-CM-DC-line-delta}$	Abs delta of DC common mode voltage between D+ and D-			25	mV	
	$V_{TX-Idle-DiffP}$	Electrical idle diff peak output			20	mV	
Serial Link (cont.)	$V_{TX-RCV-Detect}$	Voltage change during receiver detection			600	mV	
	$RL_{TX-DIFF}$	Transmitter Differential Return loss	12			dB	
	RL_{TX-CM}	Transmitter Common Mode Return loss	6			dB	
	$Z_{TX-DEFF-DC}$	DC Differential TX impedance	80	100	120	Ω	
	Z_{OSE}	Single ended TX Impedance	40	50	60	Ω	
	Transmitter Eye Diagram	TX Eye Height (De-emphasized bits)	505	650		mV	
	Transmitter Eye Diagram	TX Eye Height (Transition bits)	800	950		mV	
	PCIe Receive						
	$V_{RX-DIFFp-p}$	Differential input voltage (peak-to-peak)	175		1200	mV	
	$V_{RX-CM-AC}$	Receiver common-mode voltage for AC coupling			150	mV	
	$RL_{RX-DIFF}$	Receiver Differential Return Loss	15			dB	
	RL_{RX-CM}	Receiver Common Mode Return Loss	6			dB	
	$Z_{RX-DIFF-DC}$	Differential input impedance (DC)	80	100	120	Ω	
	$Z_{RX-COMM-DC}$	Single-ended input impedance	40	50	60	Ω	
	$Z_{RX-COMM-HIGH-Z-DC}$	Powered down input common mode impedance (DC)	200k	350k		Ω	
	$V_{RX-IDLE-DET-DIFFp-p}$	Electrical idle detect threshold	65		175	mV	
PCIe REFCLK							
	C_{IN}	Input Capacitance	1.5	—		pF	

Table 18 DC Electrical Characteristics (Part 1 of 2)

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I/O Type	Parameter	Description	Min[1]	Typ[1]	Max[1]	Unit	Conditions
Other I/Os							
LOW Drive Output	I_{OL}		—	2.5	—	mA	V_{OL} = 0.4v
	I_{OH}		—	-5.5	—	mA	V_{OH} = 1.5V
High Drive Output	I_{OL}		—	12.0	—	mA	V_{OL} = 0.4v
	I_{OH}		—	-20.0	—	mA	V_{OH} = 1.5V
Schmitt Trigger Input (STI)	V_{IL}		-0.3	—	0.8	V	—
	V_{IH}		2.0	—	V_{DD}IO + 0.5	V	—
Input	V_{IL}		-0.3	—	0.8	V	—
	V_{IH}		2.0	—	V_{DD}IO + 0.5	V	—
Capacitance	C_{IN}		—	—	8.5	pF	—
Leakage	Inputs		—	—	± 10	µA	V_{DD}I/O (max)
	$I/O_{LEAK\ W/O}$ Pull-ups/downs		—	—	± 10	µA	V_{DD}I/O (max)
	$I/O_{LEAK\ WITH}$ Pull-ups/downs		—	—	± 80	µA	V_{DD}I/O (max)

Table 18 DC Electrical Characteristics (Part 2 of 2)

1. Minimum, Typical, and Maximum values meet the requirements under PCI Specification 1.1.

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Package Pinout — 420-BGA Signal Pinout for PES24N3A

The following table lists the pin numbers and signal names for the PES24N3A device.

Pin	Function	Alt	Pin	Function	Alt	Pin	Function	Alt	Pin	Function	Alt
A1	V_{SS}		B9	MSMBDAT		C17	$V_{DD}IO$		D25	V_{SS}	
A2	V_{SS}		B10	SSMBADDR_2		C18	V_{SS}		D26	PEREFCLKN2	
A3	V_{SS}		B11	SSMBADDR_5		C19	$V_{DD}IO$		E1	V_{SS}	
A4	JTAG_TDI		B12	SSMBDAT		C20	V_{SS}		E2	V_{SS}	
A5	JTAG_TMS		B13	NC		C21	$V_{DD}IO$		E3	V_{SS}	
A6	MSMBADDR_1		B14	SWMODE_0		C22	V_{SS}		E4	V_{SS}	
A7	MSMBADDR_3		B15	SWMODE_2		C23	$V_{DD}IO$		E5	V_{SS}	
A8	MSMBCLK		B16	NC		C24	V_{SS}		E6	$V_{DD}CORE$	
A9	SSMBADDR_1		B17	$V_{DD}IO$		C25	V_{SS}		E7	$V_{DD}CORE$	
A10	SSMBADDR_3		B18	GPIO_00	1	C26	PEREFCLKP2		E8	V_{SS}	
A11	SSMBCLK		B19	GPIO_02	1	D1	PEREFCLKP1		E9	$V_{DD}CORE$	
A12	CCLKUS		B20	GPIO_04	1	D2	V_{SS}		E10	V_{SS}	
A13	CCLKDS		B21	GPIO_06		D3	V_{SS}		E11	$V_{DD}CORE$	
A14	NC		B22	MSMBSMODE		D4	V_{SS}		E12	V_{SS}	
A15	SWMODE_1		B23	REFCLKM		D5	$V_{DD}CORE$		E13	$V_{DD}CORE$	
A16	SWMODE_3		B24	$V_{DD}IO$		D6	$V_{DD}CORE$		E14	V_{SS}	
A17	PERSTN		B25	V_{SS}		D7	V_{SS}		E15	$V_{DD}CORE$	
A18	RSTHALT		B26	V_{SS}		D8	$V_{DD}CORE$		E16	V_{SS}	
A19	GPIO_01	1	C1	PEREFCLKN1		D9	V_{SS}		E17	$V_{DD}CORE$	
A20	GPIO_03		C2	V_{SS}		D10	$V_{DD}CORE$		E18	V_{SS}	
A21	GPIO_05		C3	V_{SS}		D11	V_{SS}		E19	$V_{DD}CORE$	
A22	GPIO_07	1	C4	$V_{DD}CORE$		D12	$V_{DD}CORE$		E20	$V_{DD}CORE$	
A23	V_{SS}		C5	$V_{DD}IO$		D13	$V_{DD}CORE$		E21	$V_{DD}CORE$	
A24	V_{SS}		C6	V_{SS}		D14	V_{SS}		E22	V_{SS}	
A25	V_{SS}		C7	$V_{DD}IO$		D15	$V_{DD}CORE$		E23	V_{SS}	
A26	V_{SS}		C8	V_{SS}		D16	V_{SS}		E24	V_{SS}	
B1	V_{SS}		C9	$V_{DD}IO$		D17	$V_{DD}CORE$		E25	V_{SS}	
B2	V_{SS}		C10	V_{SS}		D18	$V_{DD}CORE$		E26	V_{SS}	
B3	$V_{DD}IO$		C11	$V_{DD}IO$		D19	$V_{DD}CORE$		F1	$V_{DD}CORE$	
B4	JTAG_TCK		C12	V_{SS}		D20	V_{SS}		F2	$V_{DD}CORE$	
B5	JTAG-TDO		C13	$V_{DD}IO$		D21	$V_{DD}CORE$		F3	$V_{DD}APE$	
B6	JTAG-TRST_N		C14	$V_{DD}CORE$		D22	$V_{DD}CORE$		F4	V_{SS}	
B7	MSMBADDR_2		C15	$V_{DD}IO$		D23	V_{SS}		F5	V_{SS}	
B8	MSMBADDR_4		C16	$V_{DD}CORE$		D24	V_{SS}		F22	V_{SS}	

Table 19 PES24N3A 420-pin Signal Pin-Out (Part 1 of 3)

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Pin	Function	Alt	Pin	Function	Alt	Pin	Function	Alt	Pin	Function	Alt
F23	V_{SS}		K4	V_{DD}APE		P1	V_{DD}CORE		U24	V_{DD}PE	
F24	V_{DD}APE		K5	V_{DD}APE		P2	V_{SS}		U25	PE4TP05	
F25	V_{DD}CORE		K22	V_{DD}APE		P3	V_{TT}PE		U26	PE4TN05	
F26	V_{DD}CORE		K23	V_{DD}APE		P4	V_{TT}PE		V1	V_{DD}CORE	
G1	PE2TN07		K24	V_{DD}APE		P5	V_{SS}		V2	V_{SS}	
G2	PE2TP07		K25	V_{SS}		P22	V_{SS}		V3	V_{DD}APE	
G3	V_{DD}PE		K26	V_{SS}		P23	V_{TT}PE		V4	V_{DD}APE	
G4	PE2RN07		L1	PE2TN05		P24	V_{TT}PE		V5	V_{DD}APE	
G5	PE2RP07		L2	PE2TP05		P25	V_{SS}		V22	V_{DD}APE	
G22	PE4RP00		L3	V_{DD}PE		P26	V_{DD}CORE		V23	V_{DD}APE	
G23	PE4RN00		L4	PE2RN05		R1	PE2TN03		V24	V_{DD}APE	
G24	V_{DD}PE		L5	PE2RP05		R2	PE2TP03		V25	V_{SS}	
G25	PE4TP00		L22	PE4RP02		R3	V_{DD}PE		V26	V_{DD}CORE	
G26	PE4TN00		L23	PE4RN02		R4	PE2RN03		W1	PE2TN01	
H1	V_{SS}		L24	V_{DD}PE		R5	PE2RP03		W2	PE2TP01	
H2	V_{SS}		L25	PE4TP02		R22	PE4RP04		W3	V_{DD}PE	
H3	V_{TT}PE		L26	PE4TN02		R23	PE4RN04		W4	PE2RN01	
H4	V_{TT}PE		M1	V_{DD}CORE		R24	V_{DD}PE		W5	PE2RP01	
H5	V_{SS}		M2	V_{SS}		R25	PE4TP04		W22	PE4RP06	
H22	V_{SS}		M3	V_{TT}PE		R26	PE4TN04		W23	PE4RN06	
H23	V_{TT}PE		M4	V_{TT}PE		T1	V_{DD}CORE		W24	V_{DD}PE	
H24	V_{TT}PE		M5	V_{SS}		T2	V_{SS}		W25	PE4TP06	
H25	V_{SS}		M22	V_{SS}		T3	V_{DD}APE		W26	PE4TN06	
H26	V_{SS}		M23	V_{TT}PE		T4	V_{DD}APE		Y1	V_{SS}	
J1	PE2TN06		M24	V_{TT}PE		T5	V_{SS}		Y2	V_{SS}	
J2	PE2TP06		M25	V_{SS}		T22	V_{SS}		Y3	V_{TT}PE	
J3	V_{DD}PE		M26	V_{DD}CORE		T23	V_{DD}APE		Y4	V_{TT}PE	
J4	PE2RN06		N1	PE2TN04		T24	V_{DD}APE		Y5	V_{SS}	
J5	PE2RP06		N2	PE2TP04		T25	V_{SS}		Y22	V_{SS}	
J22	PE4RP01		N3	V_{DD}PE		T26	V_{DD}CORE		Y23	V_{TT}PE	
J23	PE4RN01		N4	PE2RN04		U1	PE2TN02		Y24	V_{TT}PE	
J24	V_{DD}PE		N5	PE2RP04		U2	PE2TP02		Y25	V_{SS}	
J25	PE4TP01		N22	PE4RP03		U3	V_{DD}PE		Y26	V_{SS}	
J26	PE4TN01		N23	PE4RN03		U4	PE2RN02		AA1	PE2TN00	
K1	V_{SS}		N24	V_{DD}PE		U5	PE2RP02		AA2	PE2TP00	
K2	V_{SS}		N25	PE4TP03		U22	PE4RP05		AA3	V_{DD}PE	
K3	V_{DD}APE		N26	PE4TN03		U23	PE4RN05		AA4	PE2RN00	

Table 19 PES24N3A 420-pin Signal Pin-Out (Part 2 of 3)

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Pin	Function	Alt	Pin	Function	Alt	Pin	Function	Alt	Pin	Function	Alt
AA5	PE2RP00		AC3	V_{DD}CORE		AD11	V_{DD}PE		AE19	PE0TP01	
AA22	PE4RP07		AC4	V_{DD}CORE		AD12	V_{TT}PE		AE20	V_{SS}	
AA23	PE4RN07		AC5	V_{DD}CORE		AD13	V_{DD}PE		AE21	PE0TP00	
AA24	V_{DD}PE		AC6	V_{TT}PE		AD14	V_{TT}PE		AE22	V_{SS}	
AA25	PE4TP07		AC7	PE0RN07		AD15	V_{DD}PE		AE23	V_{DD}CORE	
AA26	PE4TN07		AC8	V_{DD}APE		AD16	V_{DD}APE		AE24	V_{DD}CORE	
AB1	V_{SS}		AC9	PE0RN06		AD17	V_{SS}		AE25	V_{SS}	
AB2	V_{SS}		AC10	V_{DD}APE		AD18	V_{DD}PE		AE26	V_{SS}	
AB3	V_{DD}CORE		AC11	PE0RN05		AD19	V_{DD}PE		AF1	V_{SS}	
AB4	V_{DD}CORE		AC12	V_{TT}PE		AD20	V_{TT}PE		AF2	V_{SS}	
AB5	V_{DD}CORE		AC13	PE0RN04		AD21	V_{DD}PE		AF3	V_{DD}CORE	
AB6	V_{SS}		AC14	V_{TT}PE		AD22	V_{SS}		AF4	V_{DD}CORE	
AB7	PE0RP07		AC15	PE0RN03		AD23	V_{DD}CORE		AF5	V_{DD}CORE	
AB8	V_{SS}		AC16	V_{DD}APE		AD24	V_{DD}CORE		AF6	V_{SS}	
AB9	PE0RP06		AC17	PE0RN02		AD25	V_{SS}		AF7	PE0TN07	
AB10	V_{DD}APE		AC18	V_{DD}APE		AD26	V_{SS}		AF8	V_{SS}	
AB11	PE0RP05		AC19	PE0RN01		AE1	V_{SS}		AF9	PE0TN06	
AB12	V_{SS}		AC20	V_{TT}PE		AE2	V_{SS}		AF10	V_{DD}CORE	
AB13	PE0RP04		AC21	PE0RN00		AE3	V_{DD}CORE		AF11	PE0TN05	
AB14	V_{DD}APE		AC22	V_{SS}		AE4	V_{DD}CORE		AF12	V_{DD}CORE	
AB15	PE0RP03		AC23	V_{DD}CORE		AE5	V_{SS}		AF13	PE0TN04	
AB16	V_{SS}		AC24	V_{DD}CORE		AE6	V_{SS}		AF14	V_{DD}CORE	
AB17	PE0RP02		AC25	V_{SS}		AE7	PE0TP07		AF15	PE0TN03	
AB18	V_{DD}APE		AC26	V_{SS}		AE8	V_{SS}		AF16	V_{DD}CORE	
AB19	PE0RP01		AD1	V_{SS}		AE9	PE0TP06		AF17	PE0TN02	
AB20	V_{SS}		AD2	V_{SS}		AE10	V_{SS}		AF18	V_{SS}	
AB21	PE0RP00		AD3	V_{DD}CORE		AE11	PE0TP05		AF19	PE0TN01	
AB22	V_{SS}		AD4	V_{DD}CORE		AE12	V_{SS}		AF20	V_{SS}	
AB23	V_{DD}CORE		AD5	V_{DD}CORE		AE13	PE0TP04		AF21	PE0TN00	
AB24	V_{DD}CORE		AD6	V_{TT}PE		AE14	V_{SS}		AF22	V_{SS}	
AB25	V_{SS}		AD7	V_{SS}		AE15	PE0TP03		AF23	V_{DD}CORE	
AB26	V_{SS}		AD8	V_{DD}PE		AE16	V_{SS}		AF24	V_{DD}CORE	
AC1	V_{SS}		AD9	V_{SS}		AE17	PE0TP02		AF25	V_{SS}	
AC2	V_{SS}		AD10	V_{DD}PE		AE18	V_{SS}		AF26	V_{SS}	

Table 19 PES24N3A 420-pin Signal Pin-Out (Part 3 of 3)

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Power Pins

V_{DD}Core	V_{DD}Core	V_{DD}Core	V_{DD}IO	V_{DD}PE	V_{DD}APE	V_{TT}PE
C4	F2	AE3	B3	G3	F3	H3
C14	F25	AE4	B17	G24	F24	H4
C16	F26	AE23	B24	J3	K3	H23
D5	M1	AE24	C5	J24	K4	H24
D6	M26	AF3	C7	L3	K5	M3
D8	P1	AF4	C9	L24	K22	M4
D10	P26	AF5	C11	N3	K23	M23
D12	T1	AF10	C13	N24	K24	M24
D13	T26	AF12	C15	R3	T3	P3
D15	V1	AF14	C17	R24	T4	P4
D17	V26	AF16	C19	U3	T23	P23
D18	AB3	AF23	C21	U24	T24	P24
D19	AB4	AF24	C23	W3	V3	Y3
D21	AB5			W24	V4	Y4
D22	AB23			AA3	V5	Y23
E6	AB24			AA24	V22	Y24
E7	AC3			AD8	V23	AC6
E9	AC4			AD10	V24	AC12
E11	AC5			AD11	AB10	AC14
E13	AC23			AD13	AB14	AC20
E15	AC24			AD15	AB18	AD6
E17	AD3			AD18	AC8	AD12
E19	AD4			AD19	AC10	AD14
E20	AD5			AD21	AC16	AD20
E21	AD23				AC18	
F1	AD24				AD16	

Table 20 PES24N3A Power Pins

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Ground Pins

V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}
A1	D9	F22	Y1	AD22
A2	D11	F23	Y2	AD25
A3	D14	H1	Y5	AD26
A23	D16	H2	Y22	AE1
A24	D20	H5	Y25	AE2
A25	D23	H22	Y26	AE5
A26	D24	H25	AB1	AE6
B1	D25	H26	AB2	AE8
B2	E1	K1	AB6	AE10
B25	E2	K2	AB8	AE12
B26	E3	K25	AB12	AE14
C2	E4	K26	AB16	AE16
C3	E5	M2	AB20	AE18
C6	E8	M5	AB22	AE20
C8	E10	M22	AB25	AE22
C10	E12	M25	AB26	AE25
C12	E14	P2	AC1	AE26
C18	E16	P5	AC2	AF1
C20	E18	P22	AC22	AF2
C22	E22	P25	AC25	AF6
C24	E23	T2	AC26	AF8
C25	E24	T5	AD1	AF18
D2	E25	T22	AD2	AF20
D3	E26	T25	AD7	AF22
D4	F4	V2	AD9	AF25
D7	F5	V25	AD17	AF26

Table 21 PES24N3A Ground Pins

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Alternate Signal Functions

Pin	GPIO	Alternate
B18	GPIO_00	P2RSTN
A19	GPIO_01	P4RSTN
B19	GPIO_02	IOEXPINTN0
B20	GPIO_04	IOEXPINTN2
A22	GPIO_07	GPEN

Table 22 PES24N3A Alternate Signal Functions

Signals Listed Alphabetically

Signal Name	I/O Type	Location	Signal Category
CCLKDS	I	A13	System
CCLKUS	I	A12	
GPIO_00	I/O	B18	General Purpose Input/Output
GPIO_01	I/O	A19	
GPIO_02	I/O	B19	
GPIO_03	I/O	A20	
GPIO_04	I/O	B20	
GPIO_05	I/O	A21	
GPIO_06	I/O	B21	
GPIO_07	I/O	A22	
JTAG_TCK	I	B4	JTAG
JTAG_TDI	I	A4	
JTAG_TMS	I	A5	
JTAG-TDO	O	B5	
JTAG-TRST_N	I	B6	
MSMBADDR_1	I	A6	SMBus
MSMBADDR_2	I	B7	
MSMBADDR_3	I	A7	
MSMBADDR_4	I	B8	
MSMBCLK	I/O	A8	
MSMBDAT	I/O	B9	
MSMBSMODE	I	B22	System

Table 23 89PES24N3A Alphabetical Signal List (Part 1 of 5)

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Signal Name	I/O Type	Location	Signal Category
NC		A14	PCI Express
NC		B13	
NC		B16	
PE0RN00	I	AC21	
PE0RN01	I	AC19	
PE0RN02	I	AC17	
PE0RN03	I	AC15	
PE0RN04	I	AC13	
PE0RN05	I	AC11	
PE0RN06	I	AC9	
PE0RN07	I	AC7	
PE0RP00	I	AB21	
PE0RP01	I	AB19	
PE0RP02	I	AB17	
PE0RP03	I	AB15	
PE0RP04	I	AB13	
PE0RP05	I	AB11	
PE0RP06	I	AB9	
PE0RP07	I	AB7	
PE0TN00	O	AF21	
PE0TN01	O	AF19	
PE0TN02	O	AF17	
PE0TN03	O	AF15	
PE0TN04	O	AF13	
PE0TN05	O	AF11	
PE0TN06	O	AF9	
PE0TN07	O	AF7	
PE0TP00	O	AE21	
PE0TP01	O	AE19	
PE0TP02	O	AE17	
PE0TP03	O	AE15	
PE0TP04	O	AE13	
PE0TP05	O	AE11	
PE0TP06	O	AE9	
PE0TP07	O	AE7	

Table 23 89PES24N3A Alphabetical Signal List (Part 2 of 5)

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Signal Name	I/O Type	Location	Signal Category
PE2RN00	I	AA4	PCI Express (Cont.)
PE2RN01	I	W4	
PE2RN02	I	U4	
PE2RN03	I	R4	
PE2RN04	I	N4	
PE2RN05	I	L4	
PE2RN06	I	J4	
PE2RN07	I	G4	
PE2RP00	I	AA5	
PE2RP01	I	W5	
PE2RP02	I	U5	
PE2RP03	I	R5	
PE2RP04	I	N5	
PE2RP05	I	L5	
PE2RP06	I	J5	
PE2RP07	I	G5	
PE2TN00	O	AA1	
PE2TN01	O	W1	
PE2TN02	O	U1	
PE2TN03	O	R1	
PE2TN04	O	N1	
PE2TN05	O	L1	
PE2TN06	O	J1	
PE2TN07	O	G1	
PE2TP00	O	AA2	
PE2TP01	O	W2	
PE2TP02	O	U2	
PE2TP03	O	R2	
PE2TP04	O	N2	
PE2TP05	O	L2	
PE2TP06	O	J2	
PE2TP07	O	G2	
PE4RN00	I	G23	
PE4RN01	I	J23	
PE4RN02	I	L23	
PE4RN03	I	N23	

Table 23 89PES24N3A Alphabetical Signal List (Part 3 of 5)

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Signal Name	I/O Type	Location	Signal Category
PE4RN04	I	R23	PCI Express (Cont.)
PE4RN05	I	U23	
PE4RN06	I	W23	
PE4RN07	I	AA23	
PE4RP00	I	G22	
PE4RP01	I	J22	
PE4RP02	I	L22	
PE4RP03	I	N22	
PE4RP04	I	R22	
PE4RP05	I	U22	
PE4RP06	I	W22	
PE4RP07	I	AA22	
PE4TN00	O	G26	
PE4TN01	O	J26	
PE4TN02	O	L26	
PE4TN03	O	N26	
PE4TN04	O	R26	
PE4TN05	O	U26	
PE4TN06	O	W26	
PE4TN07	O	AA26	
PE4TP00	O	G25	
PE4TP01	O	J25	
PE4TP02	O	L25	
PE4TP03	O	N25	
PE4TP04	O	R25	
PE4TP05	O	U25	
PE4TP06	O	W25	
PE4TP07	O	AA25	
PEREFCLKN1	I	C1	
PEREFCLKN2	I	D26	
PEREFCLKP1	I	D1	
PEREFCLKP2	I	C26	
PERSTN	I	A17	System
REFCLKM	I	B23	PCI Express
RSTHALT	I	A18	System

Table 23 89PES24N3A Alphabetical Signal List (Part 4 of 5)

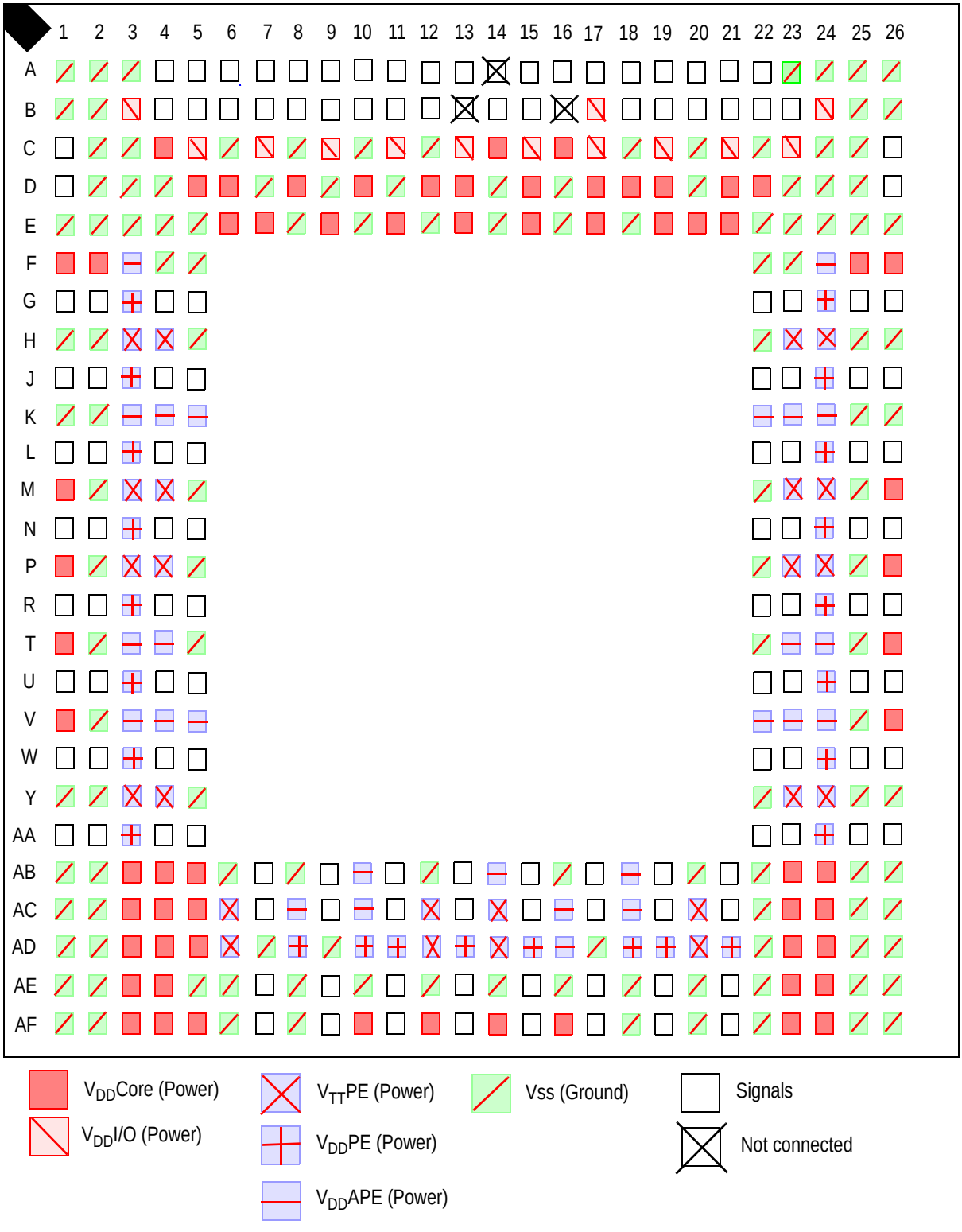
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Signal Name	I/O Type	Location	Signal Category
SSMBADDR_1	I	A9	SMBus
SSMBADDR_2	I	B10	
SSMBADDR_3	I	A10	
SSMBADDR_5	I	B11	
SSMBCLK	I/O	A11	SMBus
SSMBDAT	I/O	B12	
SWMODE_0	I	B14	System
SWMODE_1	I	A15	
SWMODE_2	I	B15	
SWMODE_3	I	A16	
V_{DD}CORE, V_{DD}APE, V_{DD}IO, V_{DD}PE, V_{TT}PE	See Table 20 for a listing of power pins.		
V_{SS}	See Table 21 for a listing of ground pins.		

Table 23 89PES24N3A Alphabetical Signal List (Part 5 of 5)

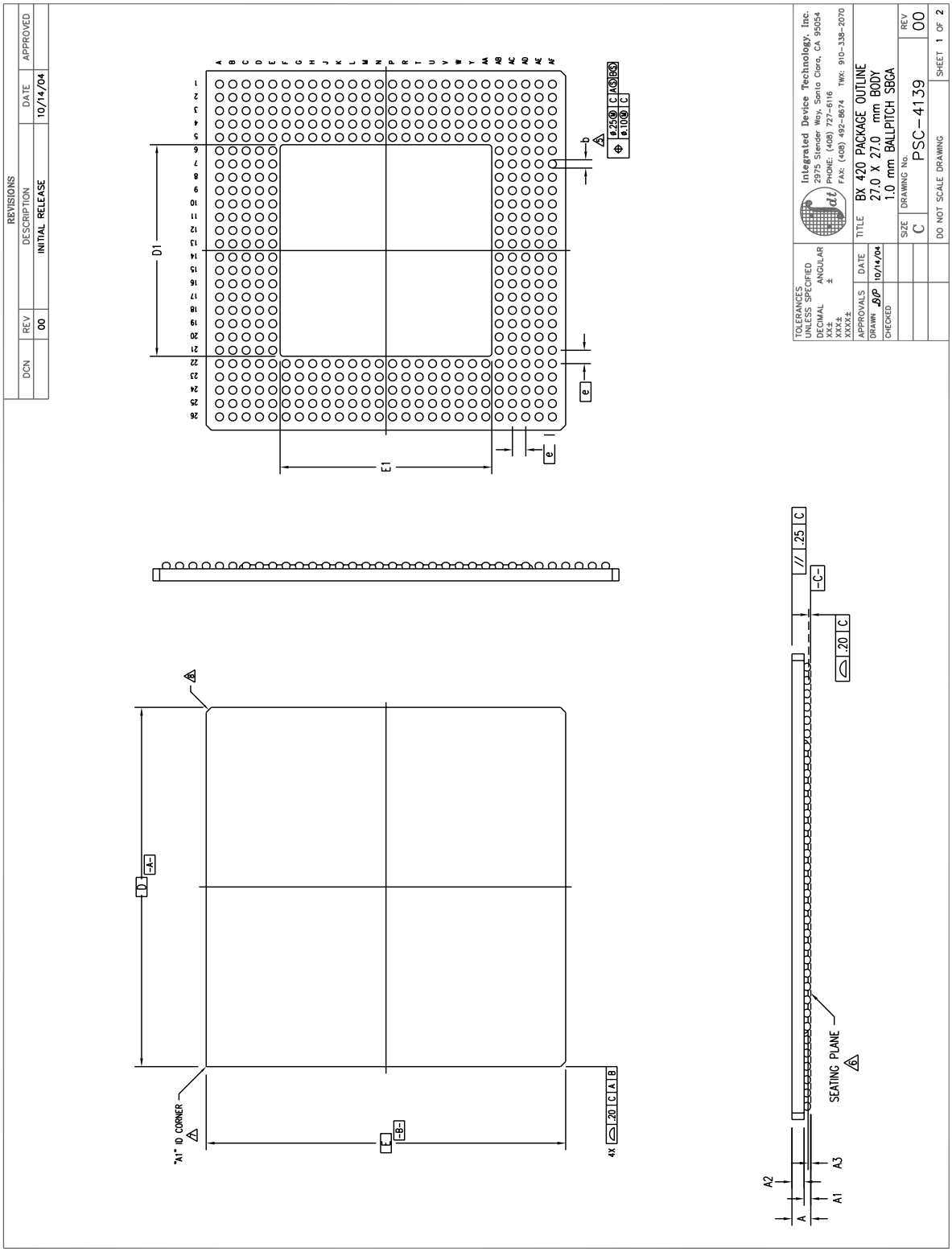
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PES24N3A Pinout — Top View



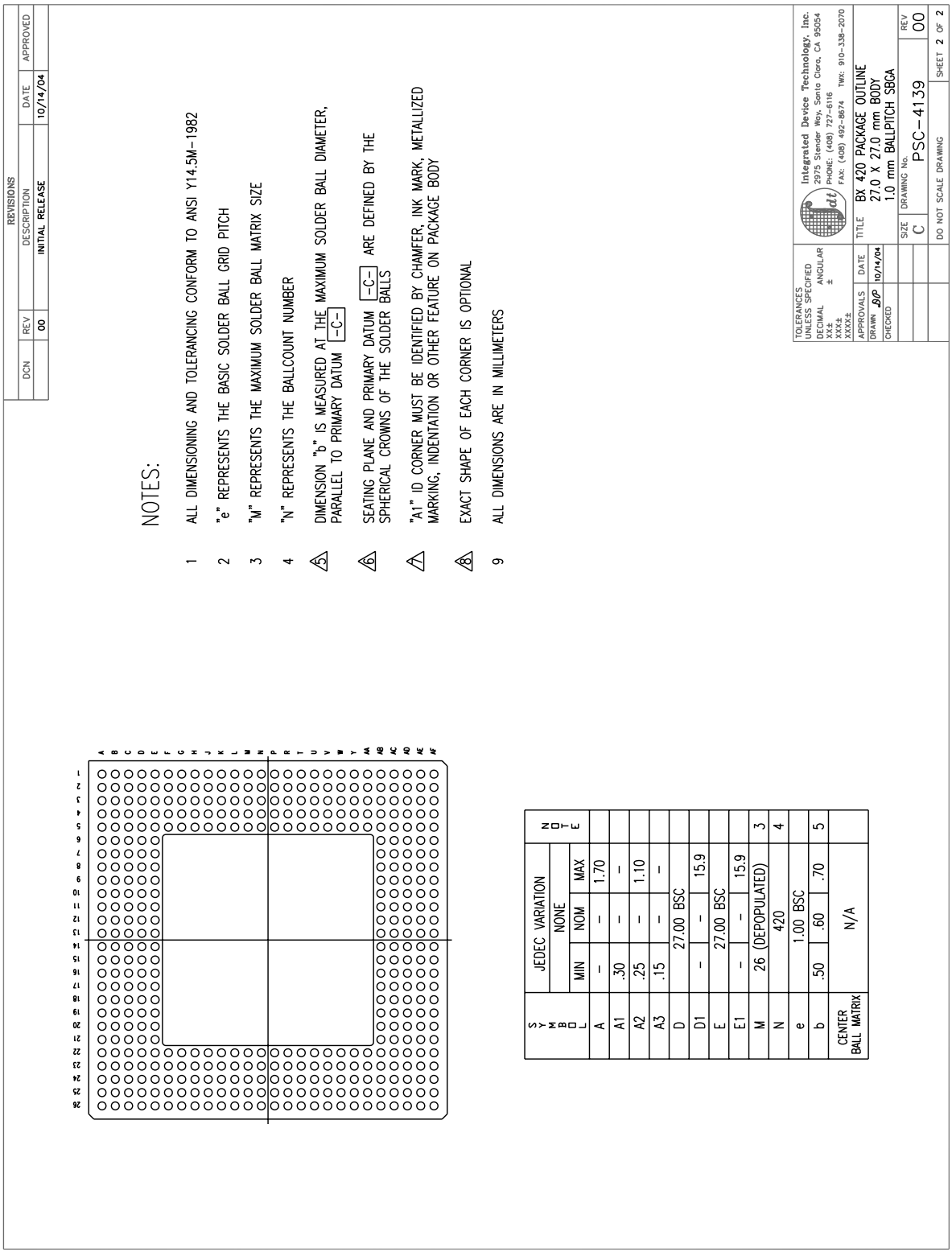
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PES24N3A Package Drawing — 420-Pin BX420/BXG420



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PES24N3A Package Drawing — Page Two



REVISIONS

DCN	REV	DESCRIPTION	DATE	APPROVED
	00	INITIAL RELEASE	10/14/04	

NOTES:

1. ALL DIMENSIONING AND TOLERANCING CONFORM TO ANSI Y14.5M-1982
2. "e" REPRESENTS THE BASIC SOLDER BALL GRID PITCH
3. "M" REPRESENTS THE MAXIMUM SOLDER BALL MATRIX SIZE
4. "N" REPRESENTS THE BALLCOUNT NUMBER
5. DIMENSION "b" IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER, PARALLEL TO PRIMARY DATUM -C-
6. SEATING PLANE AND PRIMARY DATUM -C- ARE DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS
7. "A1" ID CORNER MUST BE IDENTIFIED BY CHAMFER, INK MARK, METALLIZED MARKING, INDENTATION OR OTHER FEATURE ON PACKAGE BODY
8. EXACT SHAPE OF EACH CORNER IS OPTIONAL
9. ALL DIMENSIONS ARE IN MILLIMETERS

SYMBOL	JEDEC VARIATION NONE			NOTE
	MIN	NOM	MAX	
A	–	–	1.70	
A1	.30	–	–	
A2	.25	–	1.10	
A3	.15	–	–	
D	27.00 BSC			
D1	–	–	15.9	
E	27.00 BSC			
E1	–	–	15.9	
M	26 (DEPOPULATED)			3
N	420			4
e	1.00 BSC			
b	.50	.60	.70	5
CENTER BALL MATRIX	N/A			

TOLERANCES UNLESS SPECIFIED
DECIMAL ANGULAR
XX± ±
XXX±
XXXX±
APPROVALS DATE
DRAWN BJP 10/14/04
CHECKED

Integrated Device Technology, Inc.
2975 Stender Way, Santa Clara, CA 95054
PHONE: (408) 727-6116
FAX: (408) 492-8674 TWX: 910-338-2070

TITLE BX 420 PACKAGE OUTLINE
27.0 X 27.0 mm BODY
1.0 mm BALLPITCH SBGA

SIZE C DRAWING No. PSC-4139 REV 00

DO NOT SCALE DRAWING SHEET 2 OF 2

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Revision History

February 8, 2007: Initial publication.

April 4, 2007: In Table 3, revised description for MSMBCLK signal.

May 30, 2007: Added ZG device revision to Ordering Information.

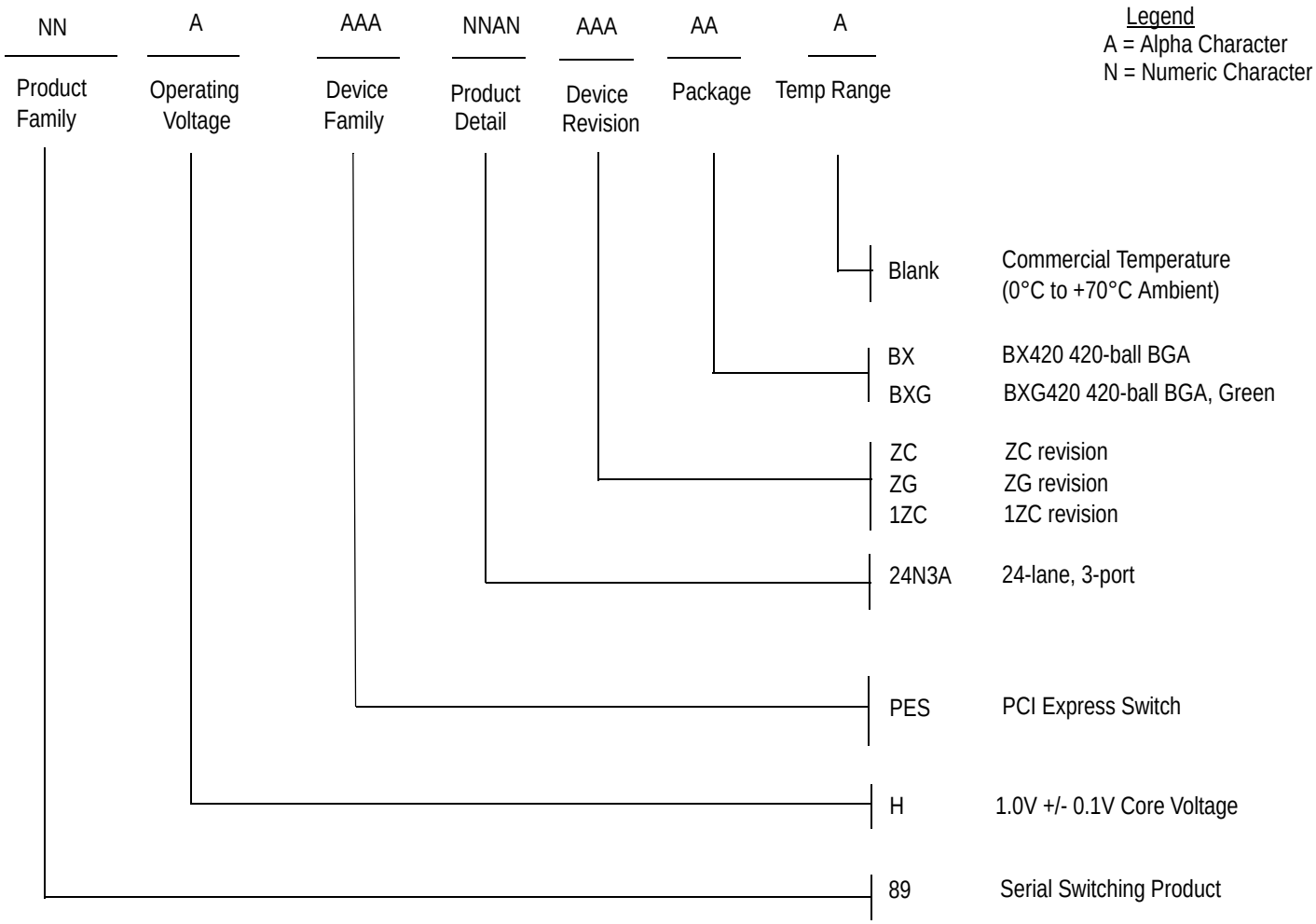
November 14, 2007: Added new parameter, Termination Resistor, to Table 9, Input Clock Requirements.

March 25, 2008: Added θ_{JB} and θ_{JC} parameters to Table 16, Thermal Specifications.

April 23, 2008: Added 1ZC device revision to Ordering Information.

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Ordering Information



Valid Combinations

89HPES24N3AZCBX	420-pin BX420 package, Commercial Temperature
89HPES24N3AZGBX	420-pin BX420 package, Commercial Temperature
89HPES24N3A1ZCBX	420-pin BX420 package, Commercial Temperature
89HPES24N3AZCBXG	420-pin Green BX420 package, Commercial Temperature
89HPES24N3AZGBXG	420-pin Green BX420 package, Commercial Temperature
89HPES24N3A1ZCBXG	420-pin Green BX420 package, Commercial Temperature

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(Rev.1.0 Mar 2020)

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