General Description

The 8N3PG10MBKI-161 is a very versatile programmable LVPECL synthesizer that can be used for OTN/SONET to Ethernet or 10GB Ethernet to OTN/SONET rate conversions. The conversion rate is pin-selectable and one of the four rates is supported at a time. In the default configuration, an input clock of 156.25MHz is converted to 161.1328125MHz output (dithering off).

The device uses IDT's fourth generation FemtoClock® NG technology to deliver low phase noise clocks combined with low power consumption. The RMS phase jitter at 161.1328125MHz output frequency is 0.567ps (12kHz - 20MHz integration range).

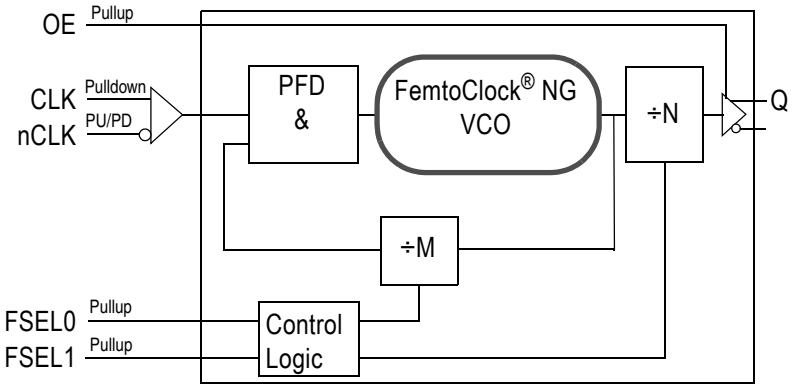
Features

- Fourth Generation FemtoClock® Next Generation (NG) technology
- Footprint compatible with 5mm x 7mm differential oscillators
- One differential LVPECL output pair
- CLK, nCLK input pair can accept the following levels: HCSL, LVDS, LVPECL, LVHSTL
- Output frequency: 161.1328125MHz
- RMS phase jitter, 12kHz – 20MHz = 0.567ps (typical)
- Full 3.3V or 2.5V operating supply
- -40°C to 85°C ambient operating temperature
- Lead-free (RoHS 6) packaging

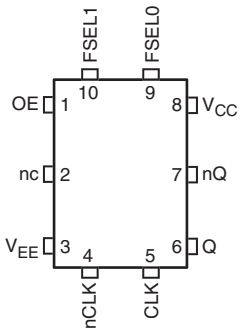
Frequency Select Table

FSEL[1:0]	Input (MHz)	Output Frequency (MHz)
00	156.25	161.1328125
01	156.25	161.1328125
10	156.25	161.1328125
11	156.25	161.1328125 (default)

Block Diagram



Pin Assignment



8N3PG10MBKI-161

10-Lead VFQFN
5mm x 7mm x 1mm package body
K Package
Top View

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Pin Descriptions and Characteristics

Table 1. Pin Descriptions

Number	Name	Type		Description
1	OE		Pullup	Output enable. External pullup required for normal operation. LVCMOS/LVTTL interface levels.
2	Reserved	Reserve		Reserved pin.
3	V_{EE}	Power		Negative supply pin.
4	nCLK	Input	Pullup/ Pulldown	Inverting differential clock input. $V_{CC}/2$ default when left floating
5	CLK	Input	Pulldown	Non-inverting differential clock input.
6, 7	Q, nQ	Output		Differential output pair. LVPECL interface levels.
8	V_{CC}	Power		Power supply pin.
9	FSEL0	Input	Pullup	Feedback control input. Sets the output divider value to one of four values. LVCMOS/LVTTL interface levels. See *Frequency Select Table* on page 1.
10	FSEL1	Input	Pullup	Feedback control input. Sets the output divider value to one of four values. LVCMOS/LVTTL interface levels. See *Frequency Select Table* on page 1.

NOTE: *Pullup* and *Pulldown* refer to internal input resistors. See Table 2, *Pin Characteristics,* for typical values.

Table 2. Pin Characteristics

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
C_{IN}	Input Capacitance			3.5		pF
R_{PULLUP}	Input Pullup Resistor			51		kΩ
$R_{PULLDOWN}$	Input Pulldown Resistor			51		kΩ

Function Table

Table 3. P, M, N Divider Function Table

FSEL[1:0]	P	M	N	Input Frequency (MHz)	Output Frequency (MHz)
0 0	÷2	÷28.87500	÷14	156.25	161.1328125
0 1	÷2	÷28.87500	÷14	156.25	161.1328125
1 0	÷2	÷28.87500	÷14	156.25	161.1328125
1 1 (default)	÷2	÷28.87500	÷14	156.25	161.1328125

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Absolute Maximum Ratings

NOTE: Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics or AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Item	Rating
Supply Voltage, V_{CC}	3.63V
Inputs, V_I	-0.5V to V_{CC} + 0.5V
Outputs, I_O Continuous Current Surge Current	 50mA 100mA
Package Thermal Impedance, θ_{JA}	39.2°C/W (0 mps)
Storage Temperature, T_{STG}	-65°C to 150°C

DC Electrical Characteristics

Table 4A. Power Supply DC Characteristics, V_{CC} = 3.3V ± 5%, V_{EE} = 0V, T_A = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{CC}	Power Supply Voltage		3.135	3.3	3.465	V
I_{EE}	Power Supply Current			151	189	mA

Table 4B. Power Supply DC Characteristics, V_{CC} = 2.5V ± 5%, V_{EE} = 0V, T_A = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{CC}	Power Supply Voltage		2.375	2.5	2.625	V
I_{EE}	Power Supply Current			146	182	mA

Table 4C. LVCMOS/LVTTL DC Characteristics, V_{CC} = 3.3V ± 5% or 2.5V ± 5%, V_{EE} = 0V, T_A = -40°C to 85°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
V_{IH}	Input High Voltage		V_{CC} = 3.465V	2		V_{CC} + 0.3	V
			V_{CC} = 2.625V	1.7		V_{CC} + 0.3	V
V_{IL}	Input Low Voltage		V_{CC} = 3.465V	-0.3		0.8	V
			V_{CC} = 2.625V	-0.3		0.7	V
I_{IH}	Input High Current	OE, FSEL[1:0]	V_{CC} = V_{IN} = 3.465V or 2.625V			5	µA
I_{IL}	Input Low Current	OE, FSEL[1:0]	V_{CC} = 3.465V or 2.625V, V_{IN} = 0V	-150			µA

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Table 4D. Differential DC Characteristics, V_{CC} = 3.3V ± 5% or 2.5V ± 5%, V_{EE} = 0V, T_A = -40°C to 85°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
I_{IH}	Input High Current	CLK, nCLK	$V_{CC} = V_{IN}$ = 3.465V or 2.625V			150	µA
I_{IL}	Input Low Current	CLK	V_{IN} = 0V, V_{CC} = 3.465V or 2.625V	-5			µA
		nCLK	V_{IN} = 0V, V_{CC} = 3.465V or 2.625V	-150			µA
V_{PP}	Peak-to-Peak Voltage; NOTE 1			0.15		1.3	V
V_{CMR}	Common Mode Input Voltage; NOTE 1, 2			V_{EE}		V_{CC} – 0.85	V

NOTE 1: V_{IL} should not be less than -0.3V.
NOTE 2: Common mode input voltage is defined as the crossing point.

Table 4E. LVPECL DC Characteristics, V_{CC} = 3.3V ± 5% or 2.5V ± 5%, V_{EE} = 0V, T_A = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{OH}	Output High Voltage; NOTE 1		V_{CC} – 1.4		V_{CC} – 0.8	V
V_{OL}	Output Low Voltage; NOTE 1		V_{CC} – 2.0		V_{CC} – 1.6	V
V_{SWING}	Peak-to-Peak Output Voltage Swing		0.6		1.0	V

NOTE 1: Outputs termination with 50Ω to V_{CC} – 2V.

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AC Electrical Characteristics

Table 5A. AC Characteristics, V_{CC} = 3.3V ± 5%, V_{EE} = 0V, T_A = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
f_{OUT}	Output Frequency			161.1328125		MHz
t_{jit}(cc)	Cycle-to-Cycle Jitter; NOTE 1			18	30	ps
t_{jit}(Ø)	RMS Phase Jitter (Random); NOTE 2, 3	f_{OUT} = 161.1328125MHz, Integration Range: 12kHz – 20MHz		0.567		ps
t_R / t_F	Output Rise/Fall Time	20% to 80%	150		450	ps
odc	Output Duty Cycle		49		51	%

NOTE: Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfpm. The device will meet specifications after thermal equilibrium has been reached under these conditions.
NOTE 1: This parameter is defined in accordance with JEDEC Standard 65.
NOTE 2: Refer to the Phase Noise plots.
NOTE 3: Characterized using Rhode Schwartz SMA100A for input clocks.

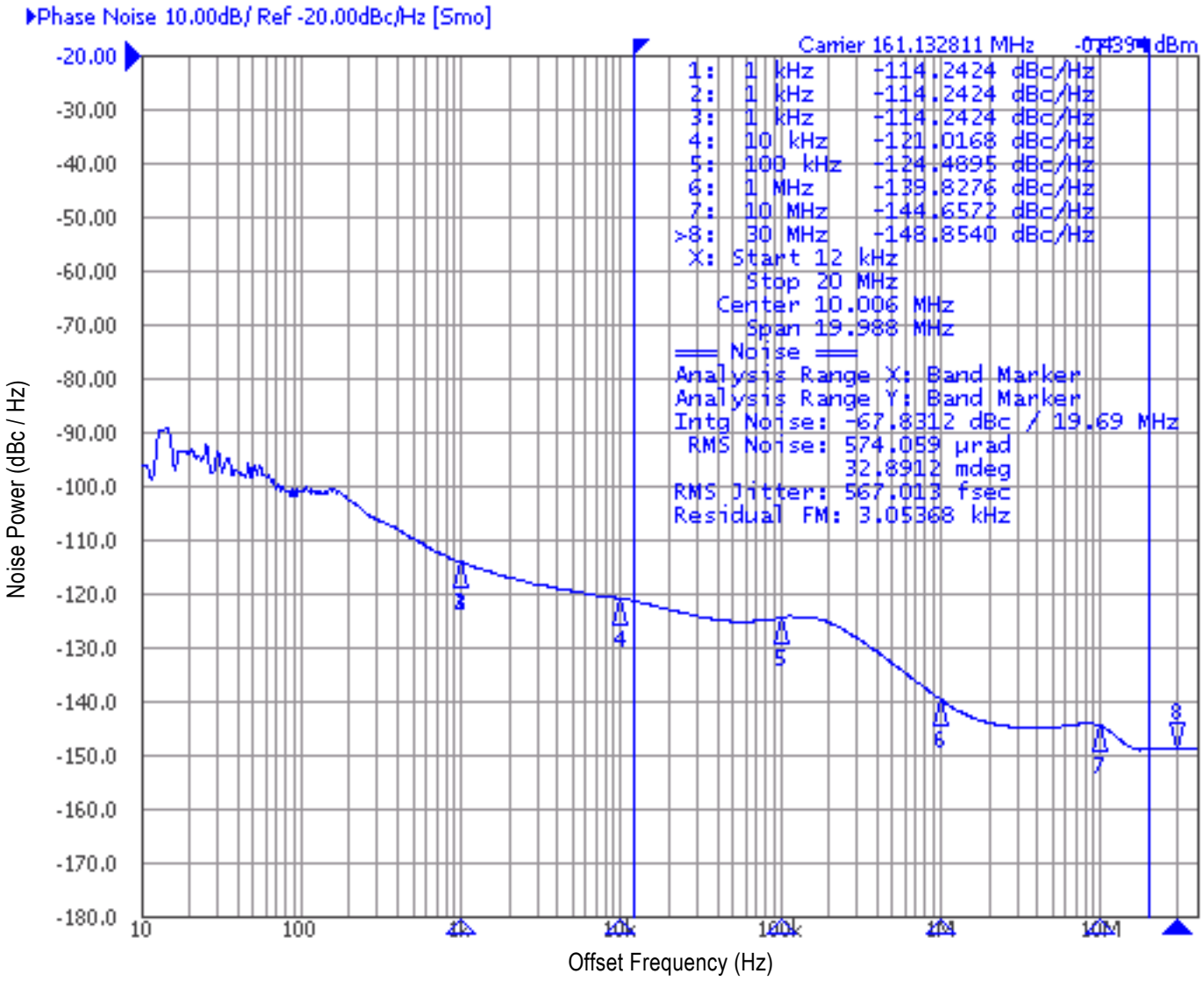
Table 5B. AC Characteristics, V_{CC} = 2.5V ± 5%, V_{EE} = 0V, T_A = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
f_{MAX}	Output Frequency			161.1328125		MHz
t_{jit}(cc)	Cycle-to-Cycle Jitter; NOTE 1			18	30	ps
t_{jit}(Ø)	RMS Phase Jitter (Random); NOTE 2, 3	f_{OUT} = 161.1328125MHz, Integration Range: 12kHz – 20MHz		0.567		ps
t_R / t_F	Output Rise/Fall Time	20% to 80%	100		500	ps
odc	Output Duty Cycle		49		51	%

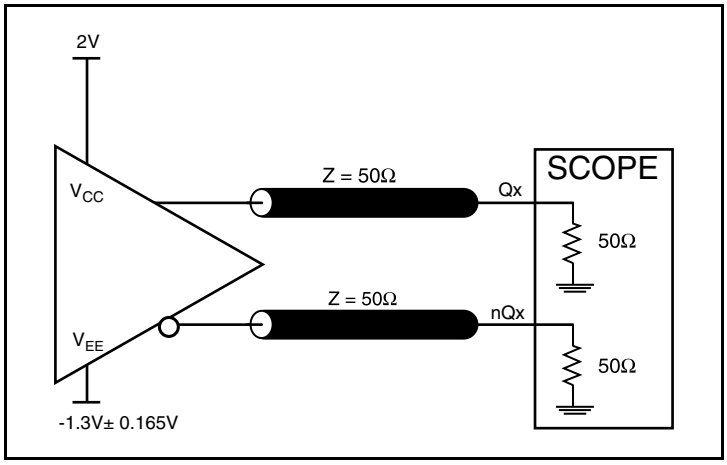
NOTE: Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfpm. The device will meet specifications after thermal equilibrium has been reached under these conditions.
NOTE 1: This parameter is defined in accordance with JEDEC Standard 65.
NOTE 2: Refer to the Phase Noise plots.
NOTE 3: Characterized using Rhode Schwartz SMA100A for input clocks.

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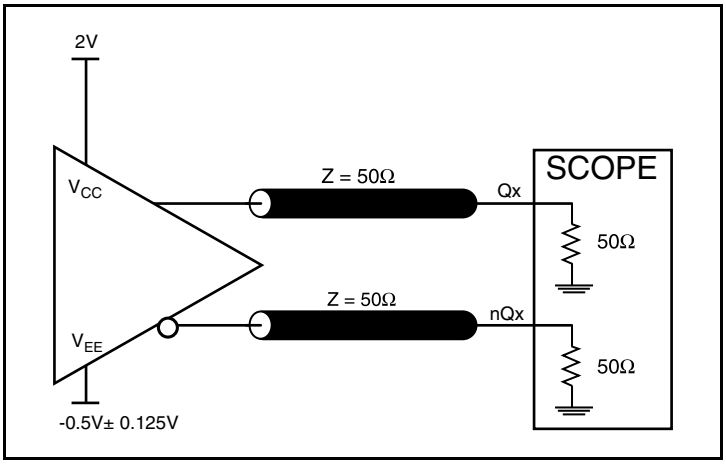
Typical Phase Noise at 161.1328125MHz



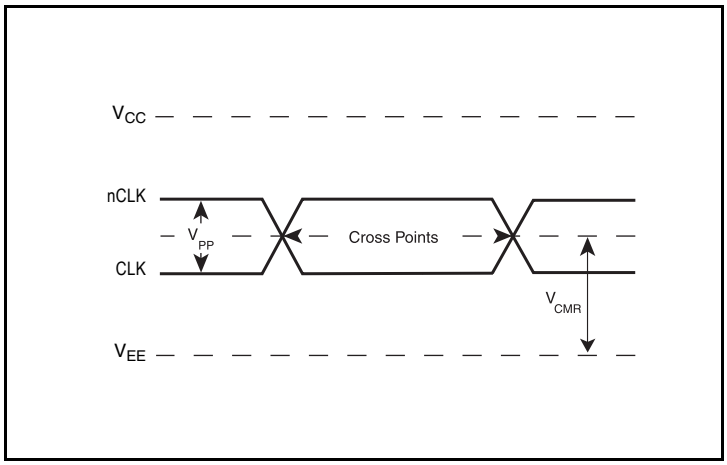
Parameter Measurement Information



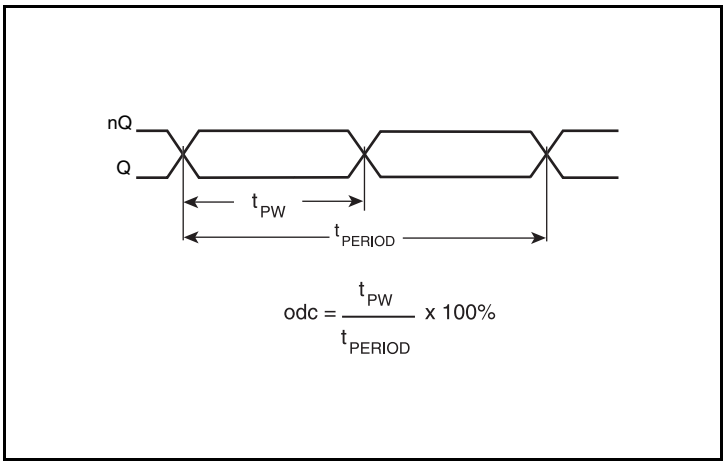
3.3V LVPECL Output Load Test Circuit



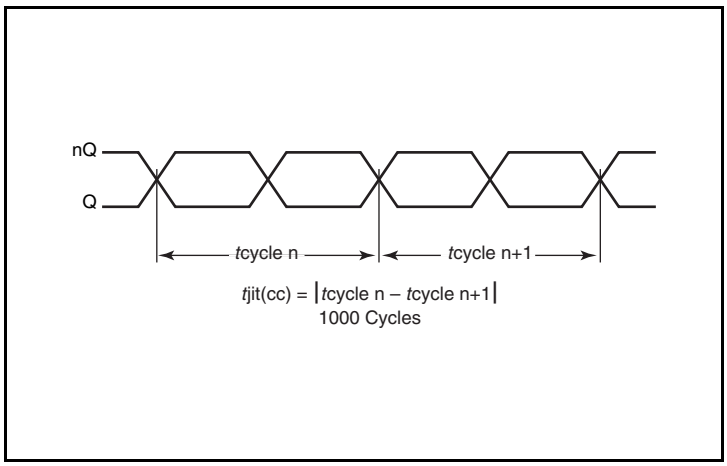
2.5V LVPECL Output Load Test Circuit



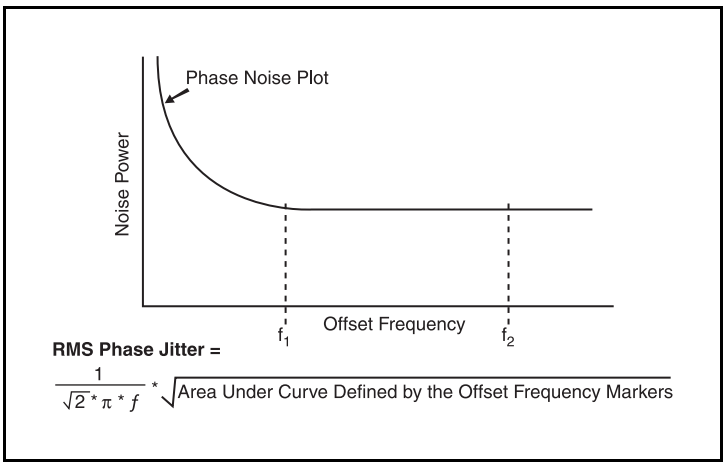
Differential Input Level



Output Duty Cycle/Pulse Width/Period

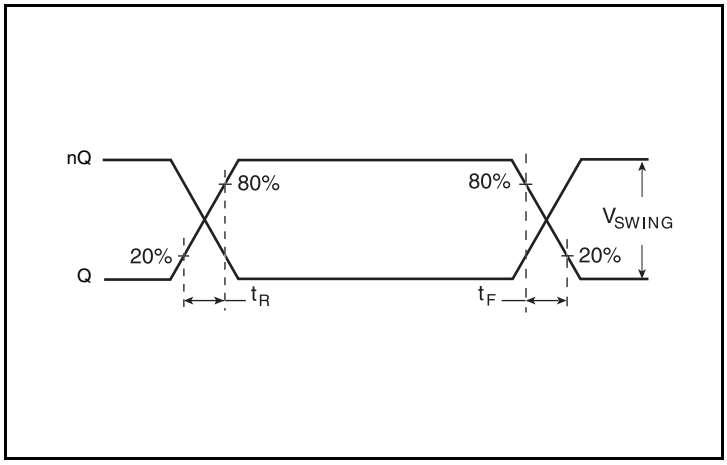


Cycle-to-Cycle Jitter



RMS Phase Jitter

Parameter Measurement Information, continued



Output Rise/Fall Time

Applications Information

Wiring the Differential Input to Accept Single-Ended Levels

Figure 1 shows how a differential input can be wired to accept single ended levels. The reference voltage $V_1 = V_{CC}/2$ is generated by the bias resistors R1 and R2. The bypass capacitor (C1) is used to help filter noise on the DC bias. This bias circuit should be located as close to the input pin as possible. The ratio of R1 and R2 might need to be adjusted to position the V_1 in the center of the input voltage swing. For example, if the input clock swing is 2.5V and V_{CC} = 3.3V, R1 and R2 value should be adjusted to set V_1 at 1.25V. The values below are for when both the single ended swing and V_{CC} are at the same voltage. This configuration requires that the sum of the output impedance of the driver (Ro) and the series resistance (Rs) equals the transmission line impedance. In addition, matched termination at the input will attenuate the signal in half. This can be done in one of two ways. First, R3 and R4 in parallel should equal the transmission line impedance. For most 50Ω applications, R3 and R4 can be 100Ω. The values of the resistors can be increased to reduce the loading for slower and weaker LVCMOS driver. When using single-ended signaling, the noise rejection benefits of differential signaling are reduced. Even though the differential input can handle full rail LVCMOS signaling, it is recommended that the amplitude be reduced. The datasheet specifies a lower differential amplitude, however this only applies to differential signals. For single-ended applications, the swing can be larger, however V_{IL} cannot be less than -0.3V and V_{IH} cannot be more than V_{CC} + 0.3V. Though some of the recommended components might not be used, the pads should be placed in the layout. They can be utilized for debugging purposes. The datasheet specifications are characterized and guaranteed by using a differential signal.

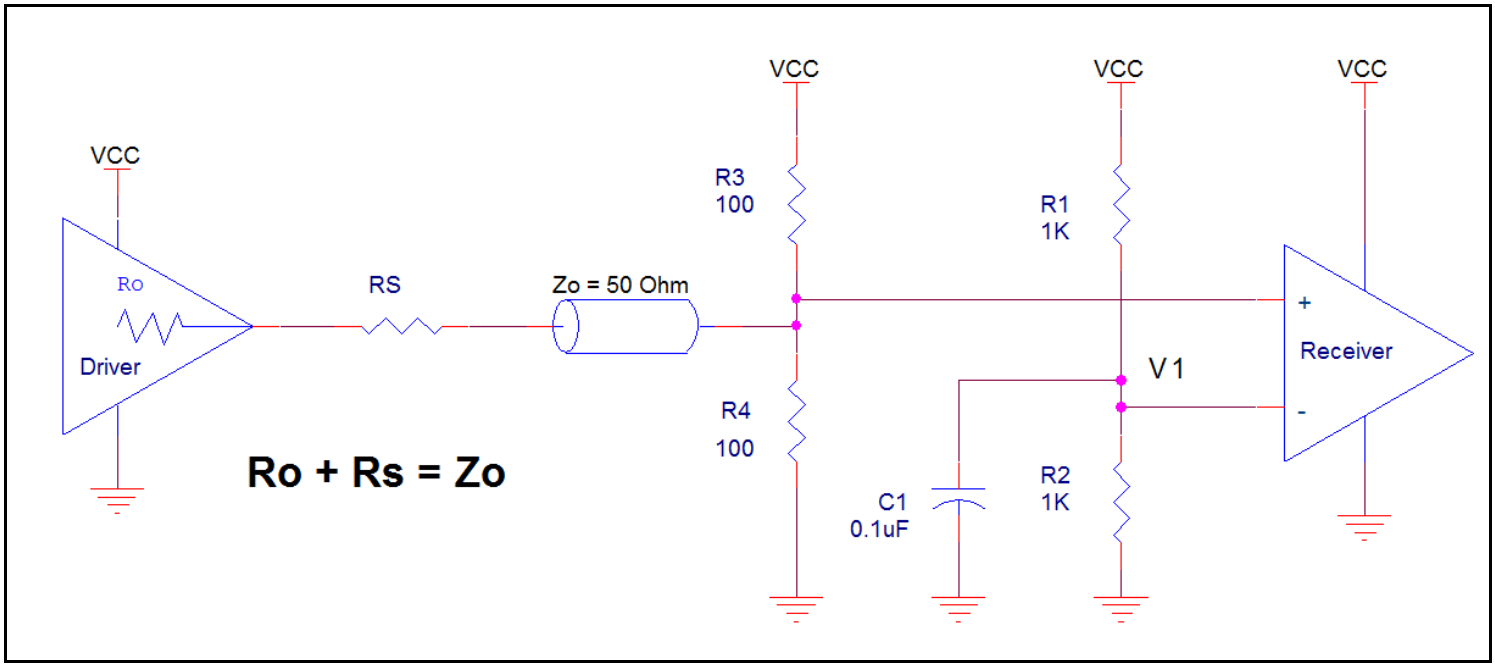


Figure 1. Recommended Schematic for Wiring a Differential Input to Accept Single-ended Levels

Recommendations for Unused Input Pins

Inputs:

LVCMOS Control Pins

For the control pins that have internal pullup resistors; additional resistance is not required but can be added for additional protection. A 1kΩ resistor can be used.

3.3V Differential Clock Input Interface

The CLK /nCLK accepts LVDS, LVPECL, LVHSTL, HCSL and other differential signals. Both V_{SWING} and V_{OH} must meet the V_{PP} and V_{CMR} input requirements. *Figures 2A to 2E* show interface examples for the CLK/nCLK input driven by the most common driver types. The input interfaces suggested here are examples only. Please consult with the vendor of the driver component to confirm the driver termination requirements. For example, in Figure 2A, the input termination applies for IDT open emitter LVHSTL drivers. If you are using an LVHSTL driver from another vendor, use their termination recommendation.

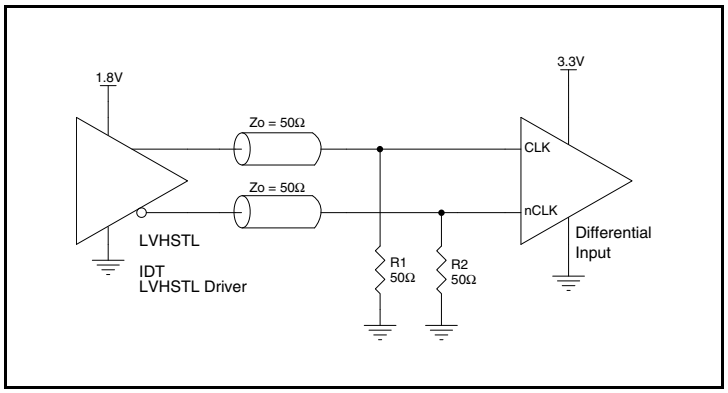


Figure 2A. CLK/nCLK Input Driven by an IDT Open Emitter LVHSTL Driver

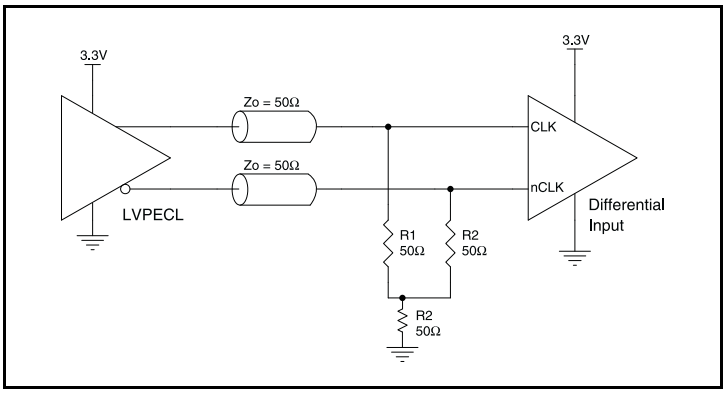


Figure 2B. CLK/nCLK Input Driven by a 3.3V LVPECL Driver

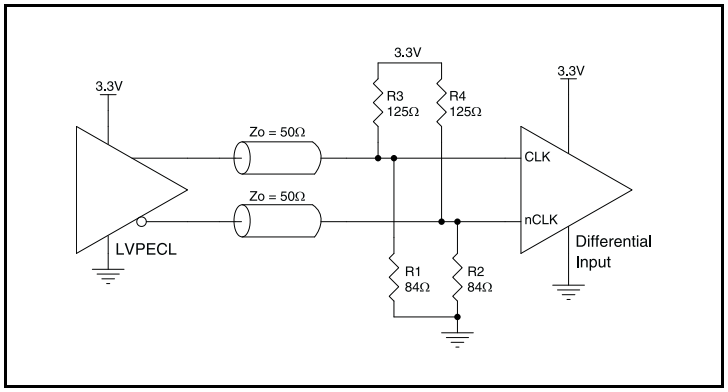


Figure 2C. CLK/nCLK Input Driven by a 3.3V LVPECL Driver

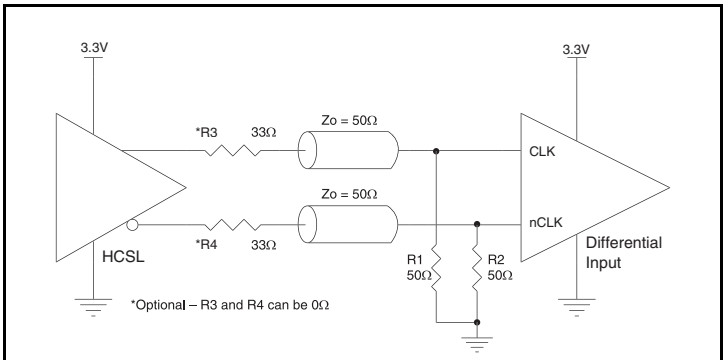


Figure 2D. CLK/nCLK Input Driven by a 3.3V HCSL Driver

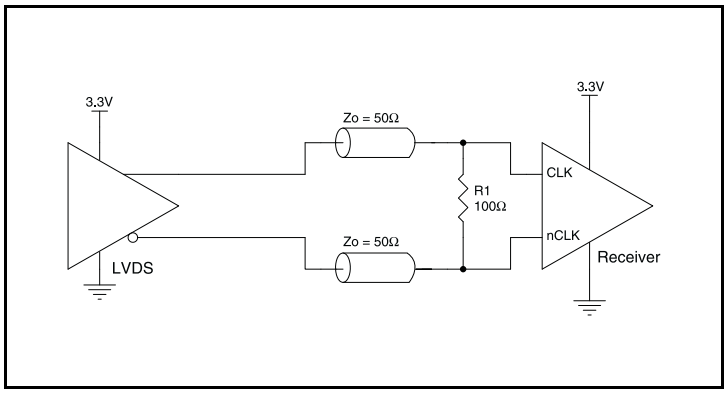


Figure 2E. CLK/nCLK Input Driven by a 3.3V LVDS Driver

2.5V Differential Clock Input Interface

The CLK /nCLK accepts LVDS, LVPECL, LVHSTL, HCSL and other differential signals. Both V_{SWING} and V_{OH} must meet the V_{PP} and V_{CMR} input requirements. *Figures 3A to 3E* show interface examples for the CLK/nCLK input driven by the most common driver types. The input interfaces suggested here are examples only. Please consult with the vendor of the driver component to confirm the driver termination requirements. For example, in Figure 3A, the input termination applies for IDT open emitter LVHSTL drivers. If you are using an LVHSTL driver from another vendor, use their termination recommendation.

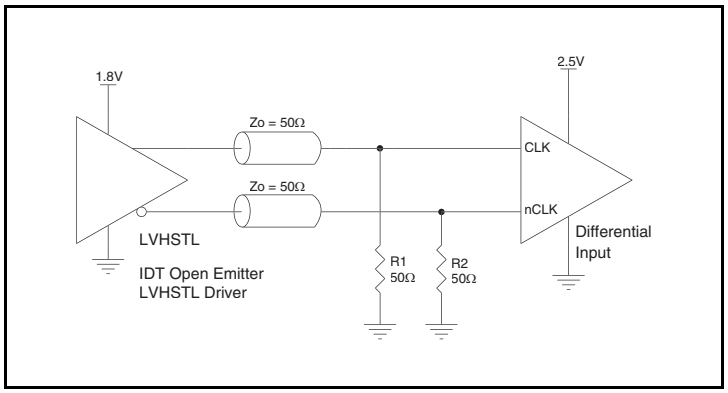


Figure 3A. CLK/nCLK Input Driven by an IDT Open Emitter LVHSTL Driver

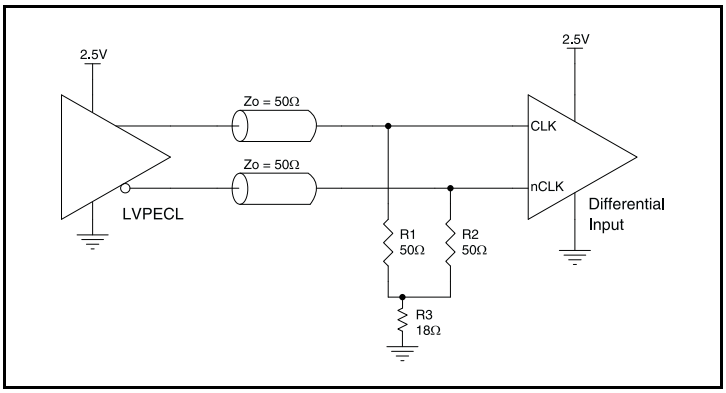


Figure 3B. CLK/nCLK Input Driven by a 2.5V LVPECL Driver

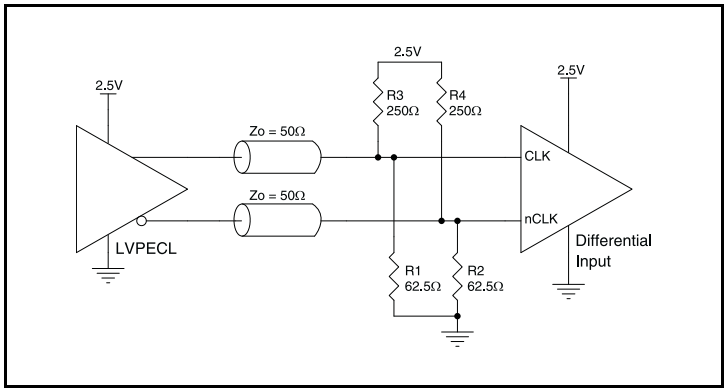


Figure 3C. CLK/nCLK Input Driven by a 2.5V LVPECL Driver

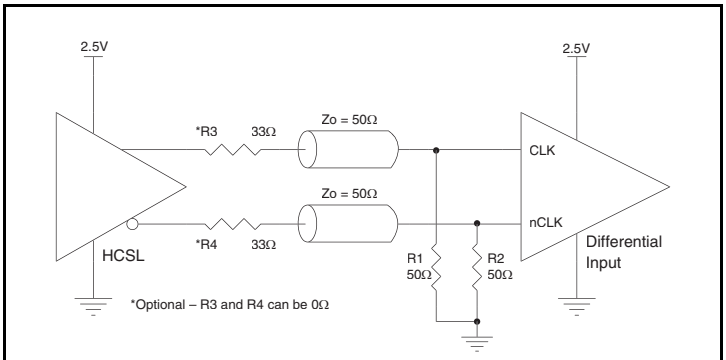


Figure 3D. CLK/nCLK Input Driven by a 2.5V HCSL Driver

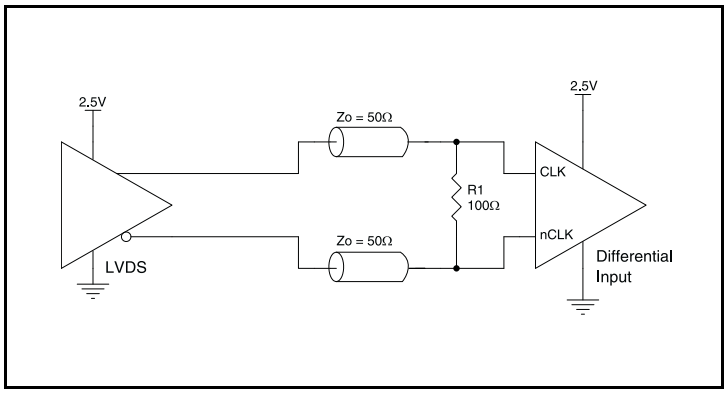


Figure 3E. CLK/nCLK Input Driven by a 2.5V LVDS Driver

VFQFN EPAD Thermal Release Path

In order to maximize both the removal of heat from the package and the electrical performance, a land pattern must be incorporated on the Printed Circuit Board (PCB) within the footprint of the package corresponding to the exposed metal pad or exposed heat slug on the package, as shown in *Figure 4.* The solderable area on the PCB, as defined by the solder mask, should be at least the same size/shape as the exposed pad/slug area on the package to maximize the thermal/electrical performance. Sufficient clearance should be designed on the PCB between the outer edges of the land pattern and the inner edges of pad pattern for the leads to avoid any shorts.

While the land pattern on the PCB provides a means of heat transfer and electrical grounding from the package to the board through a solder joint, thermal vias are necessary to effectively conduct from the surface of the PCB to the ground plane(s). The land pattern must be connected to ground through these vias. The vias act as “heat pipes”. The number of vias (i.e. “heat pipes”) are application specific and dependent upon the package power dissipation as well as electrical conductivity requirements. Thus, thermal and electrical analysis and/or testing are recommended to determine the minimum number needed. Maximum thermal and electrical performance is achieved when an array of vias is incorporated in the land pattern. It is recommended to use as many vias connected to ground as possible. It is also recommended that the via diameter should be 12 to 13mils (0.30 to 0.33mm) with 1oz copper via barrel plating. This is desirable to avoid any solder wicking inside the via during the soldering process which may result in voids in solder between the exposed pad/slug and the thermal land. Precautions should be taken to eliminate any solder voids between the exposed heat slug and the land pattern. Note: These recommendations are to be used as a guideline only. For further information, please refer to the Application Note on the Surface Mount Assembly of Amkor’s Thermally/ Electrically Enhance Leadframe Base Package, Amkor Technology.

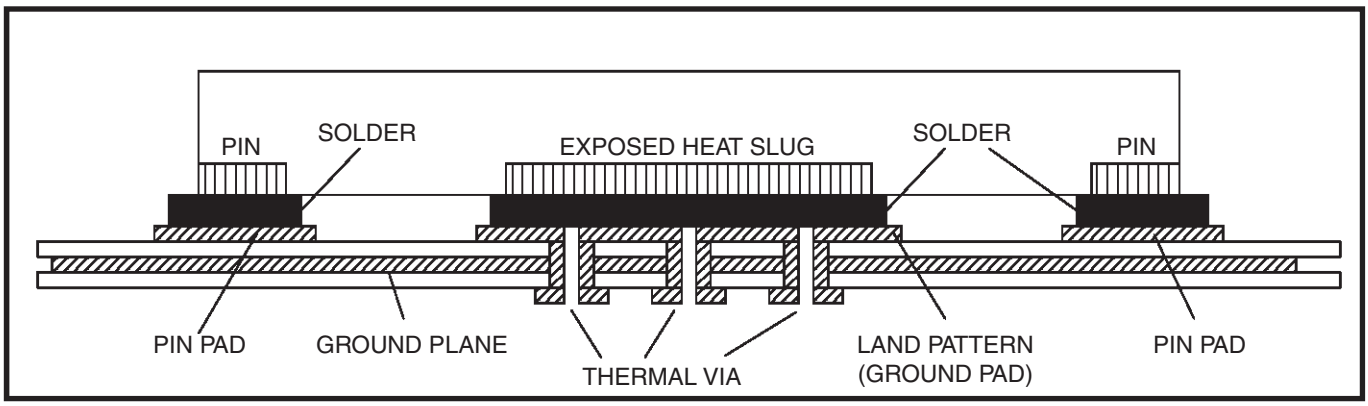


Figure 4. P.C. Assembly for Exposed Pad Thermal Release Path – Side View (drawing not to scale

Termination for 3.3V LVPECL Outputs

The clock layout topology shown below is a typical termination for LVPECL outputs. The two different layouts mentioned are recommended only as guidelines.

The differential outputs are low impedance follower outputs that generate ECL/LVPECL compatible signals. Therefore, terminating resistors (DC current path to ground) or current sources must be used for functionality. These outputs are designed to drive 50Ω transmission lines. Matched impedance techniques should be used to maximize operating frequency and minimize signal distortion. *Figures 5A and 5B* show two different layouts which are recommended only as guidelines. Other suitable clock layouts may exist and it would be recommended that the board designers simulate to guarantee compatibility across all printed circuit and clock component process variations.

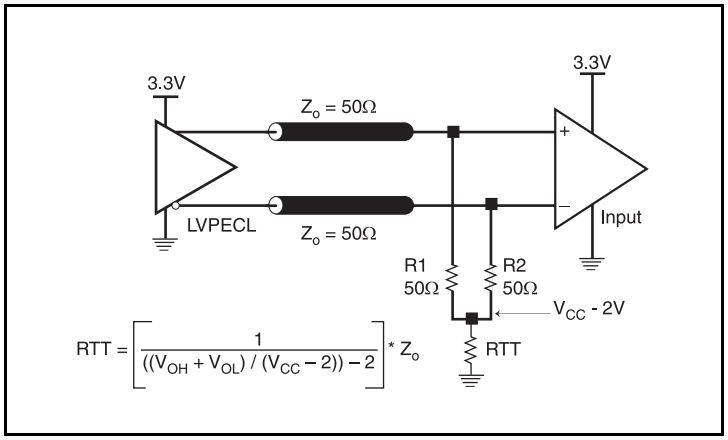


Figure 5A. 3.3V LVPECL Output Termination

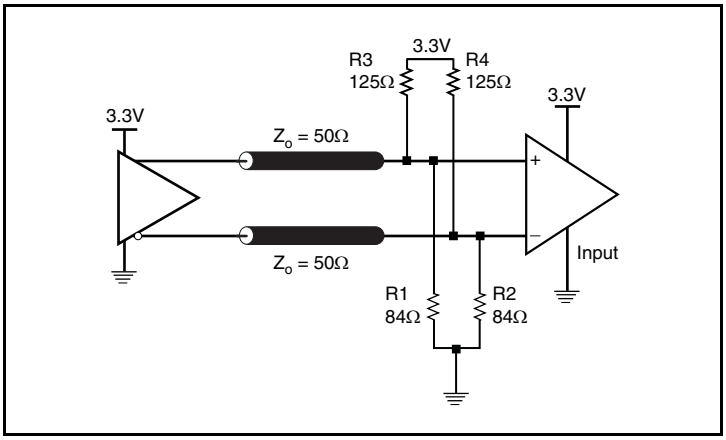


Figure 5B. 3.3V LVPECL Output Termination

Termination for 2.5V LVPECL Outputs

Figure 6A and *Figure 6C* show examples of termination for 2.5V LVPECL driver. These terminations are equivalent to terminating 50Ω to V_{CC} – 2V. For V_{CC} = 2.5V, the V_{CC} – 2V is very close to ground level. The R3 in *Figure 6B* can be eliminated and the termination is shown in *Figure 6C.*

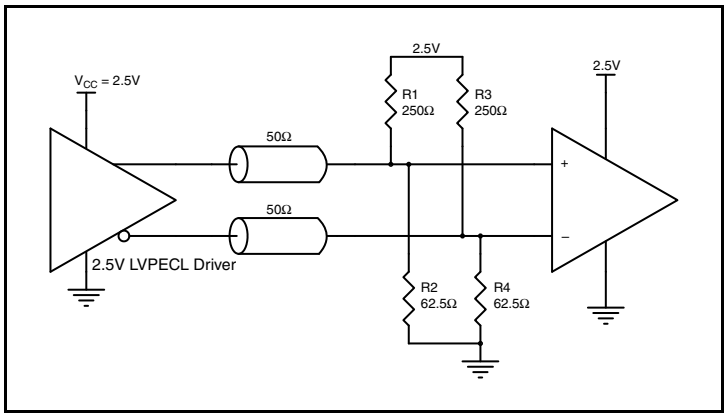


Figure 6A. 2.5V LVPECL Driver Termination Example

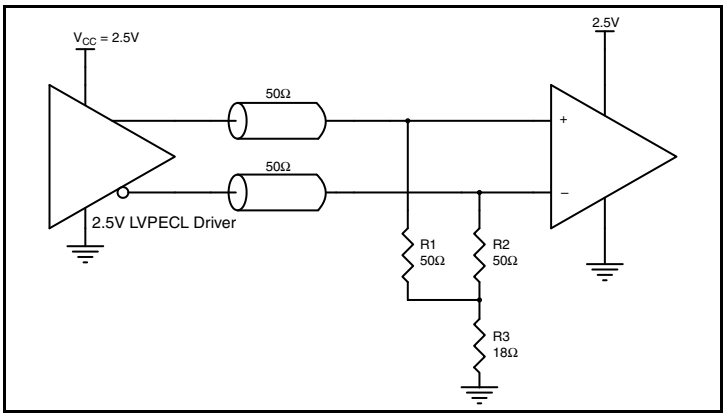


Figure 6B. 2.5V LVPECL Driver Termination Example

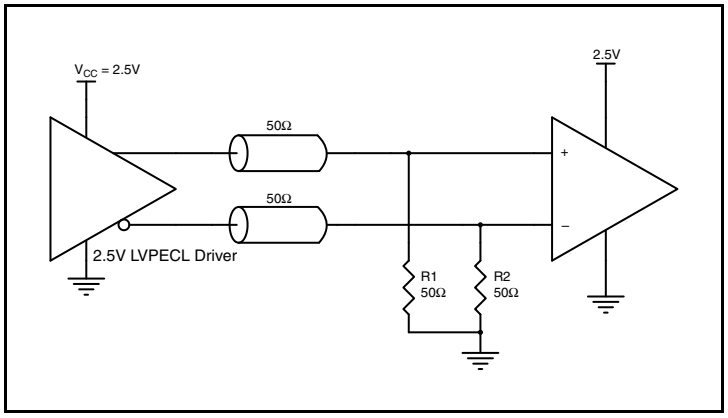


Figure 6C. 2.5V LVPECL Driver Termination Example

Schematic Example

Figure 7 shows an example IDT8N3PG10MBKI-161 application schematic in which the device is operated at V_{CC} = +3.3V. The schematic example focuses on functional connections and is intended as an example only and may not represent the exact user configuration. Refer to the pin description and functional tables in the datasheet to ensure the logic control inputs are properly set. For example OE, FSEL0 and FSEL1 can be configured from an FPGA instead of pull up and pull down resistors as shown.

The input is driven by a DC coupled LVDS driver, though HCSL and LVPECL are also compatible with the IDT CLK, nCLK differential inputs. There are two LVPECL termination options shown; the simple three resistor termination of R5, R6 and R7 and an AC termination, used when coupling the IDT8N3PG10MBKI-161 LVPECL output stage to a different logic family receiver. Note that the pull down resistors R8 and R9 that bias the LVPECL output stage are to be placed on the IDT8N3PG10MBKI-161 side of the PCB directly adjacent to pins 6 and 7 for best signal integrity. Most often each output of a 3.3V LVPECL driver will be DC terminated with a 130Ω pull up and an 82Ω pull down resistor at the 3.3V LVPECL receiver. This is also a valid option with the IDT8N3PG10MBKI-161, though the three resistor termination is simpler in regard to component count and layout as well as lower in power dissipation.

NOTE: This device package has an ePAD that is connected to ground internally. The ePAD should be connected to GND on the PCB through vias in order to improve heat dissipation.

As with any high speed analog circuitry, the power supply pins are vulnerable to random noise, so to achieve optimum jitter performance isolation of the V_{CC} pin from power supply is required. In order to achieve the best possible filtering, it is recommended that the placement of the filter components be on the device side of the PCB as close to the power pins as possible. If space is limited, the 0.1µF capacitor on the V_{CC} pin must be placed on the device side with direct return to the ground plane though vias. The remaining filter components can be on the opposite side of the PCB.

Power supply filter component recommendations are a general guideline to be used for reducing external noise from coupling into the devices. The filter performance is designed for a wide range of noise frequencies. This low-pass filter starts to attenuate noise at approximately 10kHz. If a specific frequency noise component is known, such as switching power supplies frequencies, it is recommended that component values be adjusted and if required, additional filtering be added. Additionally, good general design practices for power plane voltage stability suggests adding bulk capacitance in the local area of all devices.

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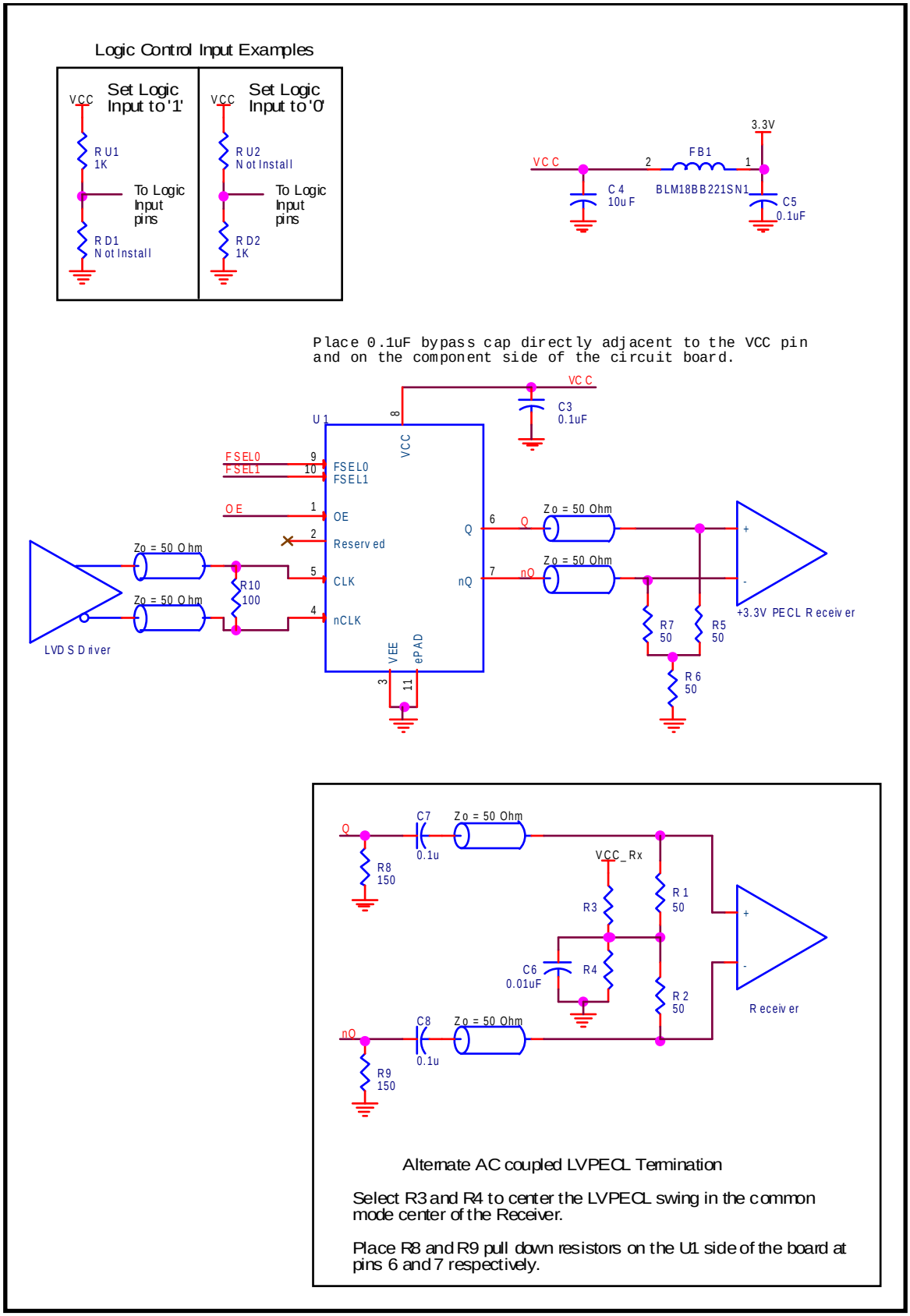


Figure 7. 8N3PG10MBKI-161 Schematic Layout Example

Power Considerations

This section provides information on power dissipation and junction temperature for the 8N3PG10MBKI-161.
Equations and example calculations are also provided.

1. Power Dissipation.

The total power dissipation for the 8N3PG10MBKI-161 is the sum of the core power plus the power dissipation due to loading.
The following is the power dissipation for V_{CC} = 3.3V + 5% = 3.465V, which gives worst case results.

NOTE: Please refer to Section 3 for details on calculating power dissipation due to loading.

- Power $(core)_{MAX} = V_{CC_MAX} * I_{EE_MAX}$ = 3.465V * 189mA = **654.885mW**
- Power $(outputs)_{MAX}$ = **32mW/Loaded Output pair**

Total Power$_{_MAX}$ (3.465V, with all outputs switching) = 654.885mW + 32mW = **686.885mW**

2. Junction Temperature.

Junction temperature, Tj, is the temperature at the junction of the bond wire and bond pad, and directly affects the reliability of the device. The maximum recommended junction temperature is 125°C. Limiting the internal transistor junction temperature, Tj, to 125°C ensures that the bond wire and bond pad temperature remains below 125°C.

The equation for Tj is as follows: $Tj = \theta_{JA} * Pd_total + T_A$

Tj = Junction Temperature

θ_{JA} = Junction-to-Ambient Thermal Resistance

Pd_total = Total Device Power Dissipation (example calculation is in section 1 above)

T_A = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance θ_{JA} must be used. Assuming no air flow and a multi-layer board, the appropriate value is 39.2°C/W per Table 6 below.

Therefore, Tj for an ambient temperature of 85°C with all outputs switching is:

85°C + 0.687W * 39.2°C/W = 111.9°C. This is well below the limit of 125°C.

This calculation is only an example. Tj will obviously vary depending on the number of loaded outputs, supply voltage, air flow and the type of board (multi-layer).

Table 6. Thermal Resistance θ_{JA} for 10 Lead VFQFN, Forced Convection

θ_{JA} **by Velocity**	
Meters per Second	**0**
Multi-Layer PCB, JEDEC Standard Test Boards	39.2°C/W

3. Calculations and Equations.

The purpose of this section is to calculate the power dissipation for the LVPECL output pair.

The LVPECL output driver circuit and termination are shown in *Figure 8.*

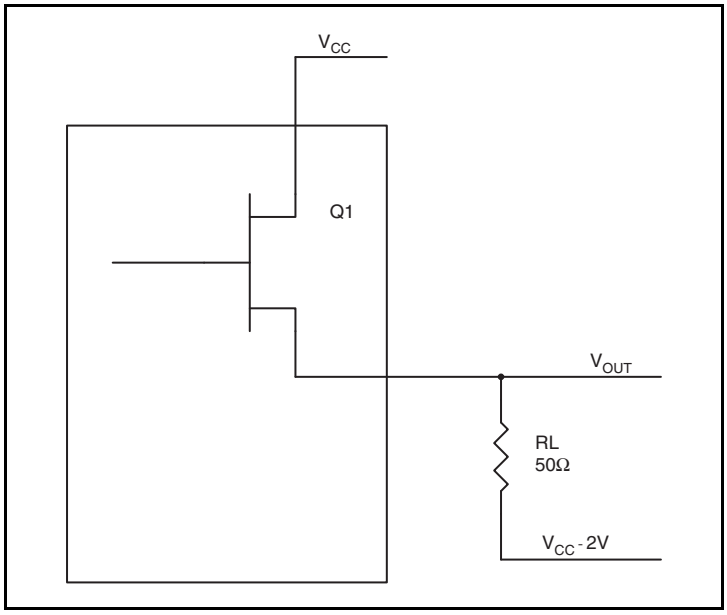


Figure 8. LVPECL Driver Circuit and Termination

To calculate power dissipation due to loading, use the following equations which assume a 50Ω load, and a termination voltage of V_{CC} – 2V.

- For logic high, $V_{OUT} = V_{OH_MAX} = \mathbf{V_{CC_MAX} - 0.8V}$
  $(V_{CC_MAX} - V_{OH_MAX}) = \mathbf{0.8V}$
- For logic low, $V_{OUT} = V_{OL_MAX} = \mathbf{V_{CC_MAX} - 1.6V}$
  $(V_{CC_MAX} - V_{OL_MAX}) = \mathbf{1.6V}$

Pd_H is power dissipation when the output drives high.

Pd_L is the power dissipation when the output drives low.

$Pd_H = [(V_{OH_MAX} – (V_{CC_MAX} – 2V))/R_L] * (V_{CC_MAX} – V_{OH_MAX}) = [(2V – (V_{CC_MAX} – V_{OH_MAX}))/R_L] * (V_{CC_MAX} – V_{OH_MAX}) =$
$[(2V – 0.8V)/50\Omega] * 0.8V =$ **19.2mW**

$Pd_L = [(V_{OL_MAX} – (V_{CC_MAX} – 2V))/R_L] * (V_{CC_MAX} – V_{OL_MAX}) = [(2V – (V_{CC_MAX} – V_{OL_MAX}))/R_L] * (V_{CC_MAX} – V_{OL_MAX}) =$
$[(2V – 1.6V)/50\Omega] * 1.6V =$ **12.8mW**

Total Power Dissipation per output pair = Pd_H + Pd_L = **32mW**

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Reliability Information

Table 7. θ_{JA} vs. Air Flow Table for a 10 Lead VFQFN

θ_{JA} vs. Air Flow	
Meters per Second	**0**
Multi-Layer PCB, JEDEC Standard Test Boards	39.2°C/W

Transistor Count

The transistor count for 8N3PG10MBKI-161 is: 42,520

Package Dimensions

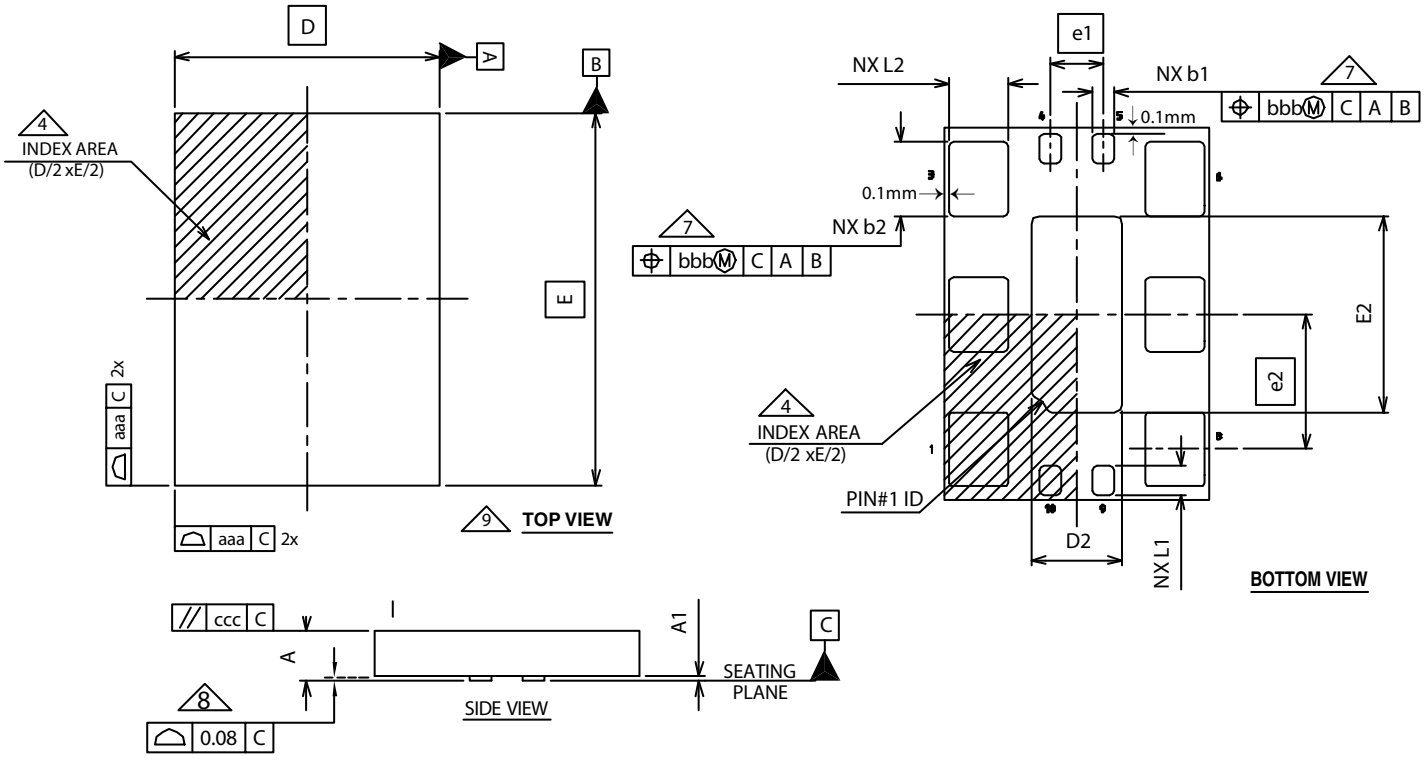
Table 8. Package Dimensions for 10-Lead VFQFN

VNJR-1 All Dimensions in Millimeters			
Symbol	**Minimum**	**Nominal**	**Maximum**
N		10	
A	0.80	0.90	1.00
A1	0	0.02	0.05
b1	0.35	0.40	0.45
b2	1.35	1.40	1.45
D		5.00 Basic	
D2	1.55	1.70	1.80
E		7.00 Basic	
E2	3.55	3.70	3.80
e1		1.0	
e2		2.54	
L1	0.45	0.55	0.65
L2	1.0	1.10	1.20
N	10		
N_D	2		
N_E	3		
aaa	0.15		
bbb	0.10		
ccc	0.10		

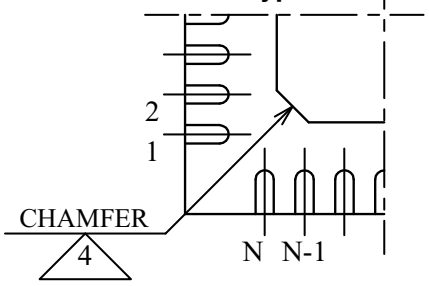
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Package Outline

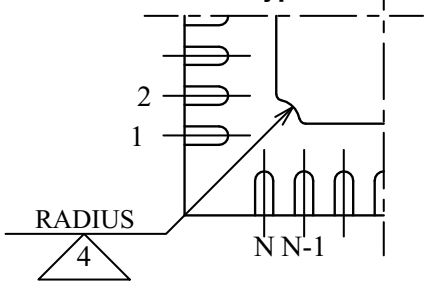
Package Outline - K Suffix for 10-Lead VFQFN



Bottom View w/Type A ID



Bottom View w/Type C ID



There are 2 methods of indicating pin 1 corner at the back of the VFQFN package:

1. Type A: Chamfer on the paddle (near pin 1)
2. Type C: Mouse bite on the paddle (near pin 1)

NOTE: The following package mechanical drawing is a generic drawing that applies to any pin count VFQFN package. This drawing is not intended to convey the actual pin count or pin layout of this device. The pin count and pinout are shown on the front page. The package dimensions are in Table 8.

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Ordering Information

Table 9. Ordering Information

Part/Order Number	Marking	Package	Shipping Packaging	Temperature
8N3PG10MBKI-161LF	ICS10MBI161L	“Lead-Free” 10 Lead VFQFN	Tray	-40°C to 85°C
8N3PG10MBKI-161LFT	ICS10MBI161L	“Lead-Free” 10 Lead VFQFN	Tape & Reel	-40°C to 85°C

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Revision History

Revision Date	Description of Change
January 28, 2016	▪ Removed ICS in the part number where needed. ▪ Updated header and footer.

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(Rev.1.0 Mar 2020)

Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,
Koto-ku, Tokyo 135-0061, Japan
www.renesas.com

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