Description

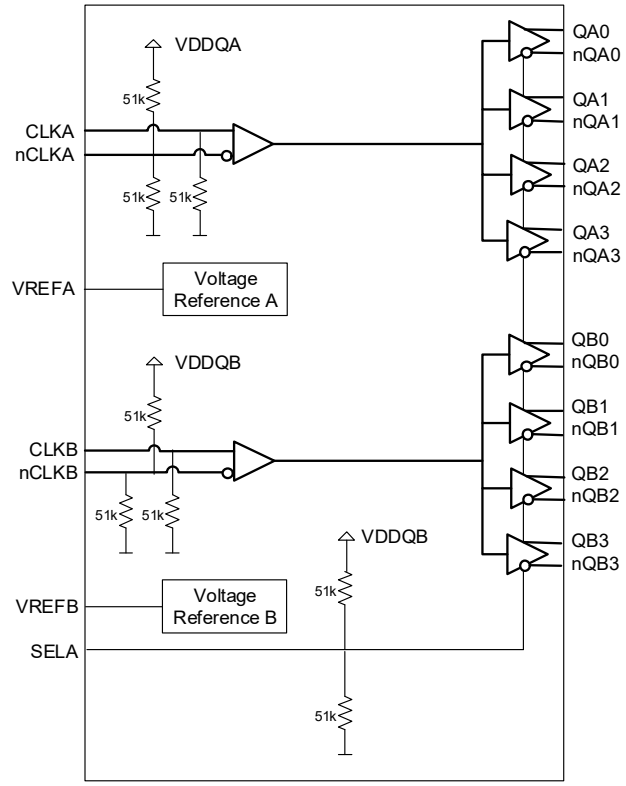
The 8P34S2104 is a high-performance, low-power, differential dual 1:4 LVDS Output 1.8V/2.5V fanout buffer. The device supports fail-safe operation and is designed for the fanout of high-frequency, very low additive phase-noise clock and data signals. Two independent buffer channels are available. Each channel has four low-skew outputs. High isolation between channels minimizes noise coupling. AC characteristics such as propagation delay are matched between channels.

Guaranteed output-to-output and part-to-part skew characteristics make the 8P34S2104 ideal for those clock distribution applications demanding well-defined performance and repeatability. The device is characterized to operate from a 1.8Vor a 2.5V power supply. The integrated bias voltage references enable easy interfacing of AC-coupled signals to the device inputs.

Features

- Dual 1:4 low skew, low additive jitter LVDS fanout buffers
- Matched AC characteristics across both channels
- High isolation between channels
- Both differential CLKA, nCLKA and CLKB, nCLKB inputs accept LVDS, LVPECL and single-ended LVCMOS levels
- Maximum input clock frequency: 2GHz
- Output amplitudes: 350mV, 500mV (selectable)
- Output bank skew: 8ps typical
- Output skew: 10ps typical
- Low additive phase jitter, RMS: 45fs typical (f_{REF} = 156.25MHz, 12kHz – 20MHz)
- Full 1.8V and 2.5V supply voltage mode
- Low device current consumption (I_{DD}):
  - 135mA typical: 1.8V
  - 145mA typical: 2.5V
- Lead-free (RoHS 6), 28-VFQFPN packaging
- -40°C to +85°C ambient operating temperature
- Supports case temperature up to +105°C

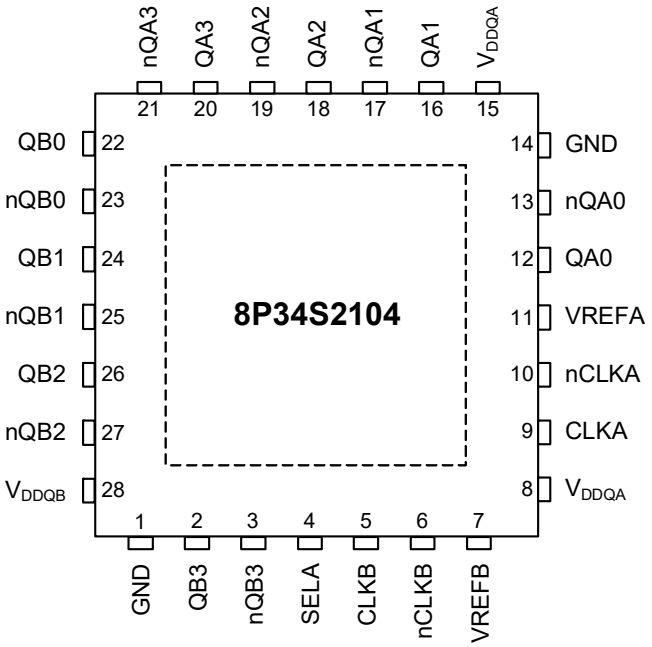
Block Diagram



8P34S2104 transistor count:

Pin Assignments

Figure 1. Pin Assignments for 5 × 5 mm 28-VFQFPN Package – Top View



Pin Descriptions

Table 1. Pin Descriptions

Number	Name	Type[a]	Description
1	GND	Power	Power supply ground.
2	QB3	Output	Differential output B3. LVDS interface levels.
3	nQB3	Output	Differential output B3. LVDS interface levels.
4	SELA	Input (PD/PU)	Control input. Output amplitude select.
5	CLKB	Input (PD)	Non-inverting differential clock/data input for channel B.
6	nCLKB	Input (PD/PU)	Inverting differential clock/data input for channel B.
7	VREFB	Output	Bias voltage reference for CLKB, nCLKB input pairs.
8	V_{DDQA}	Power	Power supply pin for the channel A core input and QA[0:3] outputs.
9	CLKA	Input (PD)	Non-inverting differential clock/data input for channel A.
10	nCLKA	Input (PD/PU)	Inverting differential clock/data input for channel A.
11	VREFA	Output	Bias voltage reference for CLKA, nCLKA input pairs.
12	QA0	Output	Differential output pair A0. LVDS interface levels.
13	nQA0	Output	Differential output pair A0. LVDS interface levels.
14	GND	Power	Power supply ground.
15	V_{DDQA}	Power	Power supply pin for the channel A core input and QA[0:3] outputs.
16	QA1	Output	Differential output pair A1. LVDS interface levels.
17	nQA1	Output	Differential output pair A1. LVDS interface levels.

Table 1. Pin Descriptions (Cont.)

Number	Name	Type[a]	Description
18	QA2	Output	Differential output pair A2. LVDS interface levels.
19	nQA2	Output	Differential output pair A2. LVDS interface levels.
20	QA3	Output	Differential output pair A3. LVDS interface levels.
21	nQA3	Output	Differential output pair A3. LVDS interface levels.
22	QB0	Output	Differential output pair B0. LVDS interface levels.
23	nQB0	Output	Differential output pair B0. LVDS interface levels.
24	QB1	Output	Differential output pair B1. LVDS interface levels.
25	nQB1	Output	Differential output pair B1. LVDS interface levels.
26	QB2	Output	Differential output pair B2. LVDS interface levels.
27	nQB2	Output	Differential output pair B2. LVDS interface levels.
28	V_{DDQB}	Power	Power supply pin for the channel B core input and QB[0:3] outputs.
ePad	GND_EPAD	Power	Exposed pad of package. Connect to ground.

[a] Pull-up (PU) and pull-down (PD) resistors are indicated in parentheses. Pull-up and pull-down refers to internal input resistors. See Table 4, DC Input Characteristics, for typical values.

Function Tables

Table 2. SELA Output Amplitude Selection Table

SELA	QA, QB Output Amplitude (mV)
0	350
Float (default)	500
1	Disable (power-down)

Absolute Maximum Ratings

NOTE: The absolute maximum ratings are stress ratings only. Stresses greater than those listed below can cause permanent damage to the device. Functional operation of the 8P34S2104 at absolute maximum ratings is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

Table 3. Absolute Maximum Ratings

Item	Rating
Supply Voltage, V_{DD}[a]	4.6V
Inputs, V_I	-0.5V to 4.6V
Inputs, I_I	20mA
Outputs, I_O Continuous Current Surge Current	 10mA 15mA
Input Sink/Source, I_{REF}	±2mA
Maximum Junction Temperature, $T_{J,MAX}$	125°C
Storage Temperature, T_{STG}	-65°C to 150°C
ESD - Human Body Model[b]	2000V
ESD - Charged Device Model[b]	1500V

[a] V_{DD} denotes V_{DDA}, V_{DDB}.

[b] According to JEDEC JS-001-2012/JESD22-C101E.

DC Electrical Characteristics

Table 4. DC Input Characteristics

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
C_{IN}	Input Capacitance			2		pF
$R_{PULLDOWN}$	Input Pull-down Resistor			51		kΩ
R_{PULLUP}	Input Pull-up Resistor			51		kΩ

Table 5. Power Supply DC Characteristics, V_{DDQA} = V_{DDQB} = 1.8V ± 5%, T_A = -40°C to +85°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
V_{DDQA}, V_{DDQB}	Power Supply Voltage			1.71	1.8	1.89	V
I_{DDQA} + I_{DDQB}	Power Supply Current	QA[0:3], QB[0:3] Outputs Terminated 100Ω between nQx, Qx	500mV amplitude		175	210	mA
			350mV amplitude		135	165	mA
I_{DDQA} + I_{DDQB}	Power Supply Current	QA[0:3], QB[0:3] Outputs disabled, SELA = 1			31	38	mA

Table 6. Power Supply DC Characteristics, V_{DDQA} = V_{DDQB} = 2.1V – 2.7V, T_A = -40°C to +85°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
V_{DDQA}, V_{DDQB}	Power Supply Voltage			2.1	2.5	2.7	V
I_{DDQA} + I_{DDQB}	Power Supply Current	QA[0:3], QB[0:3] Outputs Terminated 100Ω between nQx, Qx	500mV amplitude		188	225	mA
			350mV amplitude		145	175	mA
I_{DDQA} + I_{DDQB}	Power Supply Current	QA[0:3], QB[0:3] Outputs disabled, SELA = 1			31	38	mA

Table 7. LVCMOS Inputs DC Characteristics, V_{DDQA} = V_{DDQB} = 1.8V ±5%, 2.1V – 2.7V, T_A = -40°C to +85°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
V_{IH}	Input High Voltage	SELA		0.65 · V_{DD}[a]		V_{DD}[a] + 0.3	V
V_{IL}	Input Low Voltage	SELA		-0.3		0.35 · V_{DD}[a]	V
I_{IH}	Input High Current	SELA	V_{IN} = V_{DD}[a] = 1.89V, 2.7V			10	µA
I_{IL}	Input Low Current	SELA	V_{IN} = 0V, V_{DD}[a] = 1.89V, 2.7V	-150			µA
I_{LEAK}	Input Leakage Current	SELA	V_{IN} = 2.7V, V_{DD}[a] = 0V			250	µA

[a] V_{DD} denotes V_{DDA}, V_{DDB}.

Table 8. Differential Inputs Characteristics, V_{DDQA} = V_{DDQB} = 1.8V ±5%, 2.1V – 2.7V, T_A = -40°C to +85°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
I_{IH}	Input High Current	CLKA, nCLKA CLKB, nCLKB	V_{IN} = V_{DD}[a] = 1.89V, 2.7V			150	µA
I_{IL}	Input Low Current	CLKA, CLKB	V_{IN} = 0V, V_{DD}[a] = 1.89V, 2.7V	-10			µA
		nCLKA, nCLKB	V_{IN} = 0V, V_{DD}[a] = 1.89V, 2.7V	-150			µA
I_{LEAK}	Input Leakage Current	CLKA, nCLKA CLKB, nCLKB	V_{IN} = 2.7V, V_{DD}[a] = 0V			250	µA
V_{REF}	Reference Voltage[b]		I_{REF} = -100µA, V_{DD} = 1.8V, 2.5V	0.7 * V_{DD}		0.85 * V_{DD}	V

[a] V_{DD} denotes V_{DDA}, V_{DDB}.

[b] V_{REF} specification is applicable to the AC-coupled input interfaces shown in Figure 5 *and* Figure 6.

Table 9. LVDS DC Characteristics, V_{DDQA} = V_{DDQB} = 1.8V ±5%, 2.1V – 2.7V, T_A = -40°C to +85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
ΔV_{OD}	V_{OD} Magnitude Change				50	mV
ΔV_{OS}	V_{OS} Magnitude Change				50	mV

AC Electrical Characteristics

Table 10. AC Electrical Characteristics, V_{DD} = 1.8V ±5%, 2.1V – 2.7V, T_A = -40°C to +85°C [a]

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
f_{REF}	Input Frequency				2	GHz
$\Delta V/\Delta t$	Input Edge Rate		1.5			V/ns
t_{PD}	Propagation Delay[b], [c]	CLKA to any QAx, CLKB to any nQBx	100	225	400	ps
*t*sk(o)	Output Skew[d], [e]			10	30	ps
*t*sk(b)	Output Bank Skew[e], [f]			8	25	ps
*t*sk(p)	Pulse Skew[g]	f_{REF} = 100MHz		5	20	ps
*t*sk(pp)	Part-to-part Skew[e], [h]				200	ps
t_{JIT}	Buffer Additive Phase Jitter, RMSAdditive Phase Jitter	f_{REF} = 156.25MHz; square wave, V_{DD} = 1.8V ± 5%, V_{PP} = 0.5V; Integration range: 1kHz – 40MHz		60	75	fs
		f_{REF} = 156.25MHz square wave, V_{DD} = 1.8V ± 5%, V_{PP} = 1V; Integration range: 12kHz – 20MHz		45	55	fs
		f_{REF} = 156.25MHz; square wave, V_{DD} = 2.1V - 2.7V, V_{PP} = 0.5V; Integration range: 1kHz – 40MHz		56	60	fs
		f_{REF} = 156.25MHz square wave, V_{DD} = 2.1V - 2.7V, V_{PP} = 1V; Integration range: 12kHz – 20MHz		35	42	fs
Φ_N(≥30M)	Clock Single-side Band Phase Noise	≥30MHz offset from carrier and noise floor, V_{DD} = 1.8V		< -160		dBc/Hz
		≥30MHz offset from carrier and noise floor, V_{DD} = 2.5V		< -165		dBc/Hz
$t_{JIT, SP}$	Spurious Suppression, Coupling between Channels	f_{QA} = 491.52MHz, f_{QB} = 61.44MHz; V_{DD} = 1.8V, measured between neighboring outputs		-71		dB
		f_{QA} = 491.52MHz, f_{QB} = 15.36MHz; V_{DD} = 1.8V, measured between neighboring outputs		-82		dB
		f_{QA} = 491.52MHz, f_{QB} = 61.44MHz; V_{DD} = 2.5V, measured between neighboring outputs		-68		dB
		f_{QA} = 491.52MHz, f_{QB} = 15.36MHz; V_{DD} = 2.5V, measured between neighboring outputs		-79		dB

Table 10. AC Electrical Characteristics, V_{DD} = 1.8V ±5%, 2.1V – 2.7V, T_A = -40°C to +85°C [a]

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
t_R / t_F	Output Rise/ Fall Time		10% to 90%, outputs loaded with 100Ω, V_{DD} = 1.8V ±5%		220	400	ps
			20% to 80%, outputs loaded with 100Ω, V_{DD} = 1.8V ±5%		110	250	ps
			10% to 90%, outputs loaded with 100Ω, V_{DD} = 2.1V – 2.7V		350	400	ps
			20% to 80%, outputs loaded with 100Ω, V_{DD} = 2.1V – 2.7V		160	250	ps
V_{PP}	Input Voltage Amplitude	CLKA, CLKB		0.15		1.2	V
V_{PP_DIFF}	Differential Input Voltage Amplitude	CLKA, CLKB		0.3		2.4	V
V_{CMR}	Common Mode Input Voltage[i]			1.1		V_{DD} – ($V_{PP/2}$)	V
V_{OD}	Differential Output Voltage		SELA = 0, R_{OUT} = 100Ω, f_{REF} < 2GHz	247	350	454	mV
			SELA = float, R_{OUT} = 100Ω, f_{REF} < 2GHz	300	500	650	mV
			SELA = float, R_{OUT} = 100Ω, f_{REF} < 500MHz	450	550	650	mV
V_{OS}	Offset Voltage		SELA = 0, V_{DD} = 1.8V ±5%	0.61	0.77	0.91	V
			SELA = float, V_{DD} = 1.8V ±5%	0.53	0.68	0.82	V
			SELA = 0, V_{DD} = 2.1V	0.80	1.01	1.20	V
			SELA = float, V_{DD} = 2.1V	0.74	0.95	1.15	V
			SELA = 0, V_{DD} = 2.3V	1.00	1.21	1.42	V
			SELA = float, V_{DD} = 2.3V	0.95	1.15	1.36	V
			SELA = 0, V_{DD} = 2.5V	1.30	1.45	1.62	V
			SELA = float, V_{DD} = 2.5V	1.20	1.35	1.55	V
			SELA = 0, V_{DD} = 2.7V	1.40	1.61	1.82	V
			SELA = float, V_{DD} = 2.7V	1.34	1.55	1.75	V

[a] Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfpm. The device will meet specifications after thermal equilibrium has been reached under these conditions.

[b] Measured from the differential input crossing point to the differential output crossing point.

[c] Input V_{PP} = 400mV.

[d] Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at the differential cross points.

[e] This parameter is defined in accordance with JEDEC Standard 65.

[f] Defined as skew within a bank of outputs at the same voltage and with equal load conditions.

[g] Output pulse skew is the absolute value of the difference of the propagation delay times: $| t_{PLH} - t_{PHL} |$.

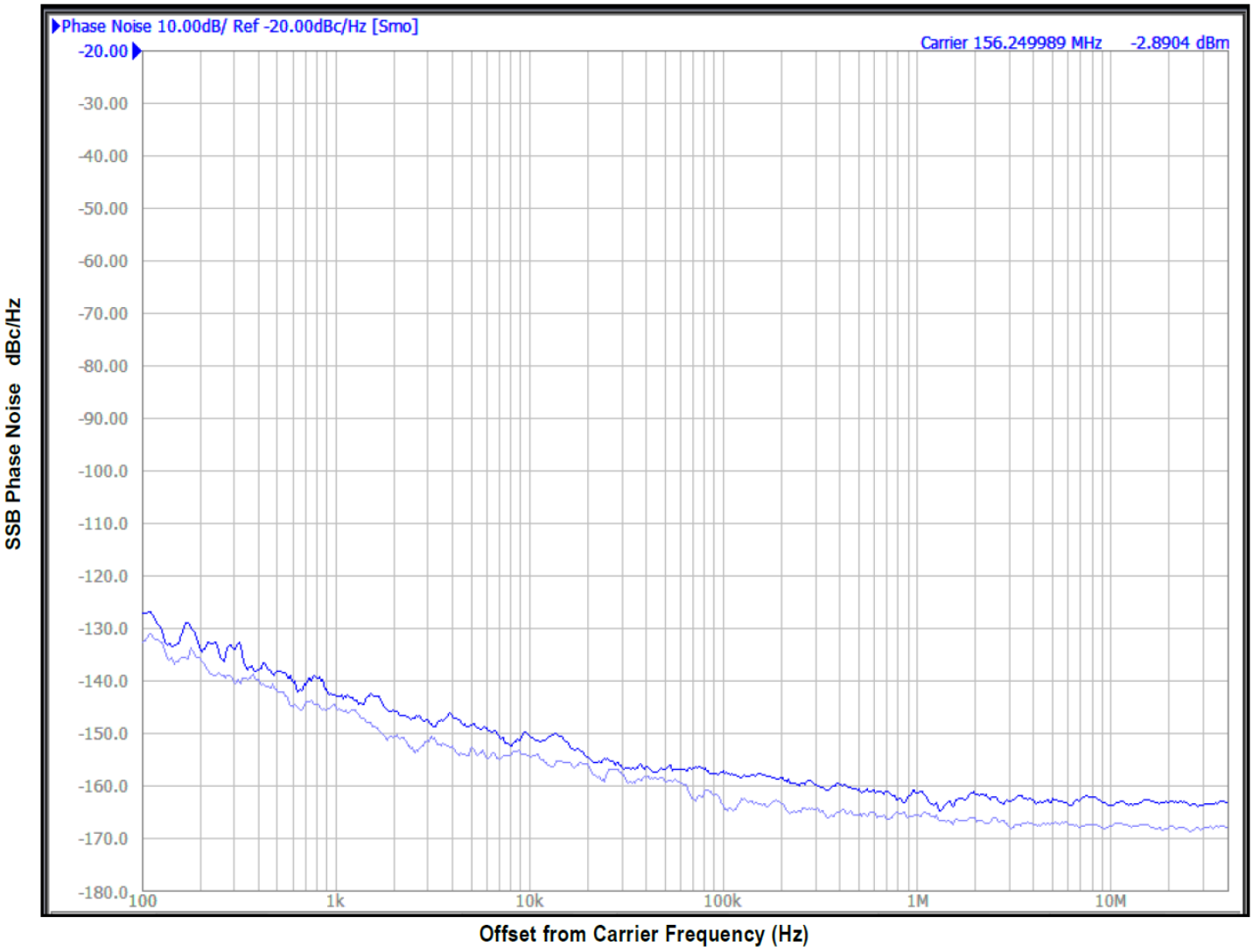
[h] Defined as skew between outputs on different devices operating at the same supply voltage, same frequency, same temperature and with equal load conditions. Using the same type of inputs on each device, the outputs are measured at the differential cross points.

[i] Common Mode Input Voltage is defined as the cross-point voltage.

Additive Phase Jitter

The spectral purity in a band at a specific offset from the fundamental compared to the power of the fundamental is called the **dBc Phase Noise.** This value is normally expressed using a Phase noise plot and is most often the specified plot in many applications. Phase noise is defined as the ratio of the noise power present in a 1Hz band at a specified offset from the fundamental frequency to the power value of the fundamental. This ratio is expressed in decibels (dBm) or a ratio of the power in the 1Hz band to the power in the fundamental. When the required offset is specified, the phase noise is called a **dBc** value, which simply means dBm at a specified offset from the fundamental. By investigating jitter in the frequency domain, we get a better understanding of its effects on the desired application over the entire time record of the signal. It is mathematically possible to calculate an expected bit error rate given a phase noise plot.

Figure 2. Additive Phase Jitter. Frequency: 156.25MHz, Integration Range: 12kHz to 20MHz = 45fs typical



As with most timing specifications, phase noise measurements have issues relating to the limitations of the measurement equipment. The noise floor of the equipment can be higher or lower than the noise floor of the device. Additive phase noise is dependent on both the noise floor of the input source and measurement equipment. Measured using a Wenzel 156.25MHz Oscillator as the input source.

Applications Information

Recommendations for Unused Input and Output Pins

Inputs

CLK/nCLK Inputs

For applications not requiring the use of the differential input, both CLK and nCLK can be left floating. Though not required, but for additional protection, a 1kΩ resistor can be tied from CLK to ground.

Outputs

LVDS Outputs

All unused LVDS output pairs can be either left floating or terminated with 100Ω across. If they are left floating there should be no trace attached.

VREF

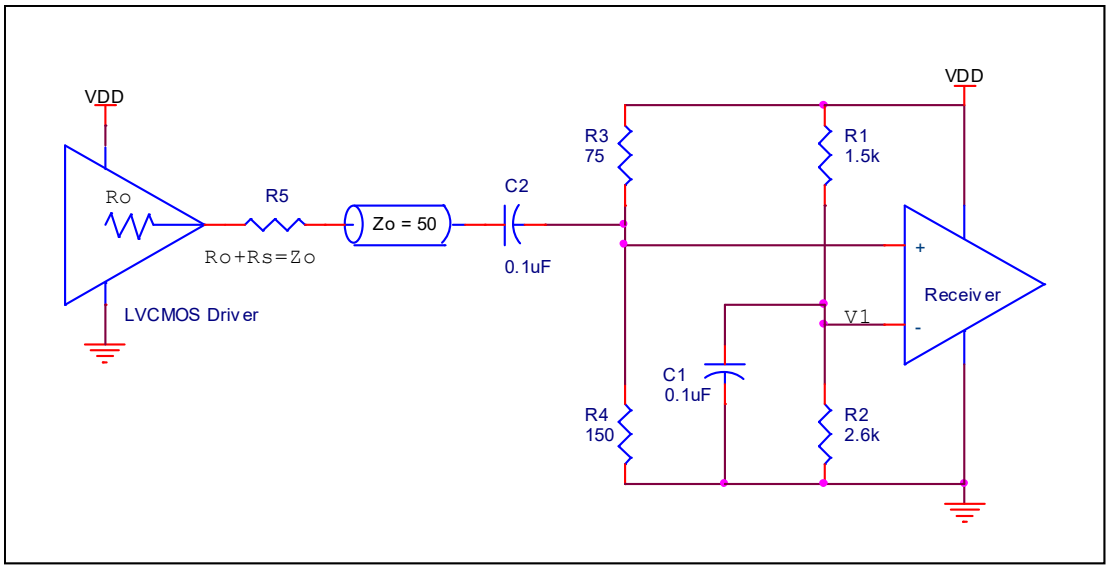
The unused VREF pin can be left floating. We recommend that there is no trace attached.

Wiring the Differential Input to Accept Single-Ended Levels

Figure 3 shows an example of how a differential input can be wired to accept single-ended levels. To satisfy the VCMR requirement, the reference voltage V1 is set to 1.2V which is generated by the bias resistors R1 and R2. The bypass capacitor (C1) is used to help filter noise on the DC bias. This bias circuit should be located as close to the input pin as possible. The ratio of R1 and R2 might need to be adjusted to position the V1 to meet the VCRM requirement. For example, if the input clock swing is 1.8V and VDD = 1.8V, R1 and R2 value should be adjusted to set V1 at 1.2V in this example. The values below are for when both the single-ended swing and VDD are at the same voltage. This configuration requires that the sum of the output impedance of the driver (Ro) and the series resistance (Rs) equals the transmission line impedance. In addition, matched termination at the input will attenuate the signal in half. This can be done in one of two ways.

First, R3 and R4 in parallel should equal the transmission line impedance and the signal DC offset after AC coupling should be equal to V1, i.e. 1.2V in this example. For most Zo = 50Ω applications, R3 = 75Ω and R4 can be 130Ω. By keeping the same R3/R4 ratio, the values of the resistors can be increased to reduce the loading for slower and weaker LVCMOS driver. When using single-ended signaling, the noise rejection benefits of differential signaling are reduced. Even though the input can handle larger amplitude signaling, it is recommended that the amplitude be reduced. For single-ended applications, the swing can be larger. Make sure the single-ended logic high and logic low signal operates within specification limit. Though some of the recommended components might not be used, the pads should be placed in the layout. They can be utilized for debugging purposes. The datasheet specifications are characterized and guaranteed by using a differential signal.

Figure 3. Example Schematic for Wiring a Differential Input to Accept Single-ended Levels



1.8V Differential Clock Input Interface

The CLK /nCLK accepts LVDS, LVPECL and other differential signals. The differential input signal must meet both the V_{PP} and V_{CMR} input requirements. Figure 4 to Figure 6 show interface examples for the CLK /nCLK input driven by the most common driver types. The input interfaces suggested here are examples only. If the driver is from another vendor, use their termination recommendation. Please consult with the vendor of the driver component to confirm the driver termination requirements.

Figure 4. Differential Input Driven by an LVDS Driver–DC Coupling

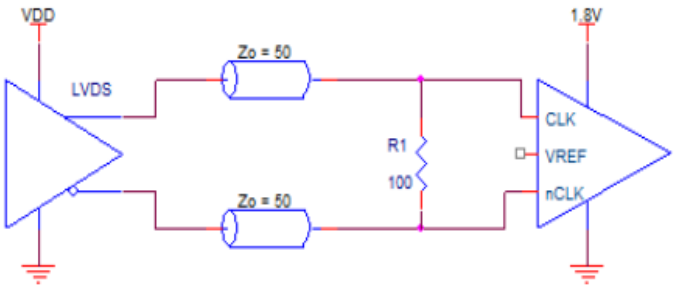


Figure 5. Differential Input Driven by an LVDS Driver–AC Coupling

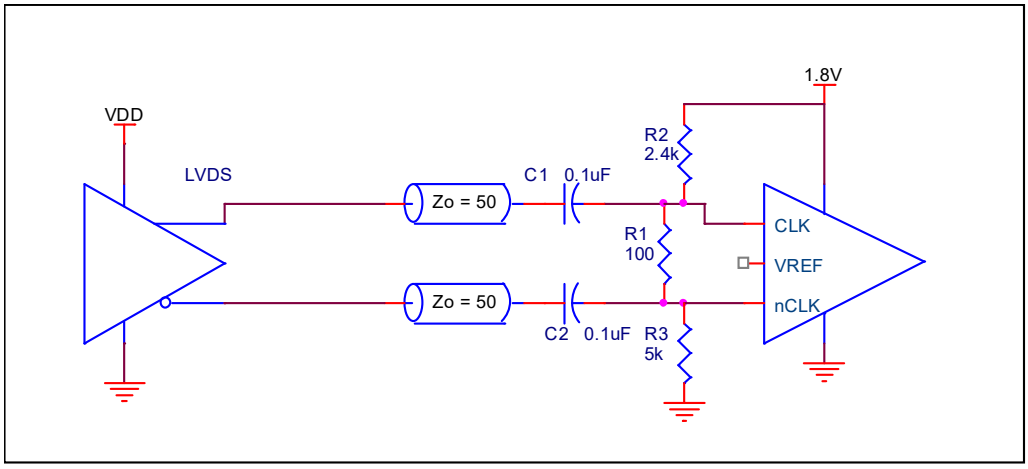
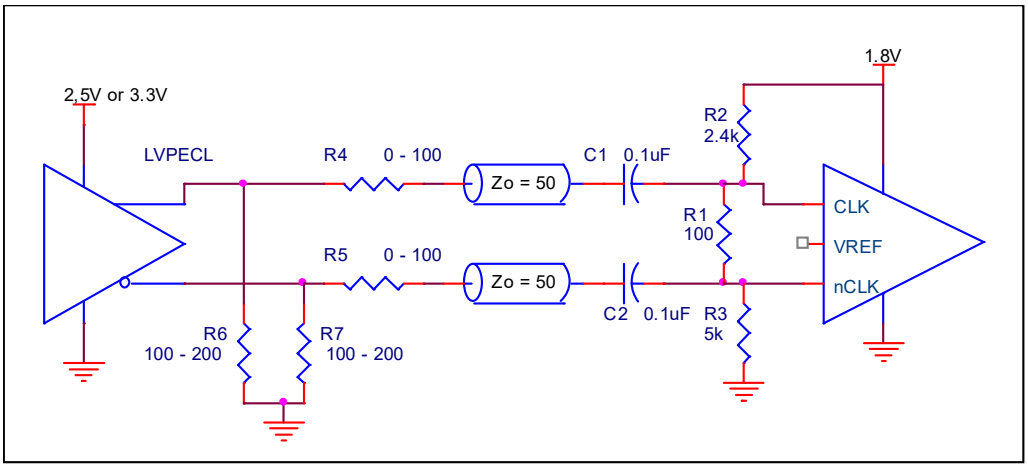


Figure 6. Differential Input Driven by an LVPECL Driver–AC Coupling



LVDS Driver Termination

For a general LVDS interface, the recommended value for the termination impedance (Z_T) is between 90Ω and 132Ω. The actual value should be selected to match the differential impedance (Z_0) of your transmission line. A typical point-to-point LVDS design uses a 100Ω parallel resistor at the receiver and a 100Ω differential transmission-line environment. In order to avoid any transmission-line reflection issues, the components should be surface mounted and must be placed as close to the receiver as possible. IDT offers a full line of LVDS compliant devices with two types of output structures: current source and voltage source. The standard termination schematic as shown in Figure 7 can be used with either type of output structure. Figure 8, which can also be used with both output types, is an optional termination with center tap capacitance to help filter common mode noise. The capacitor value should be approximately 50pF. If using a non-standard termination, it is recommended to contact IDT and confirm if the output structure is current source or voltage source type. In addition, since these outputs are LVDS compatible, the input receiver's amplitude and common-mode input range should be verified for compatibility with the output.

Figure 7. Standard LVDS Termination

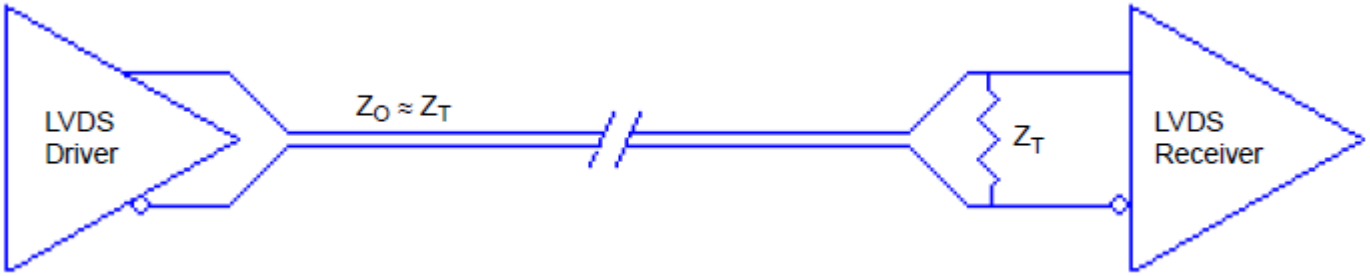
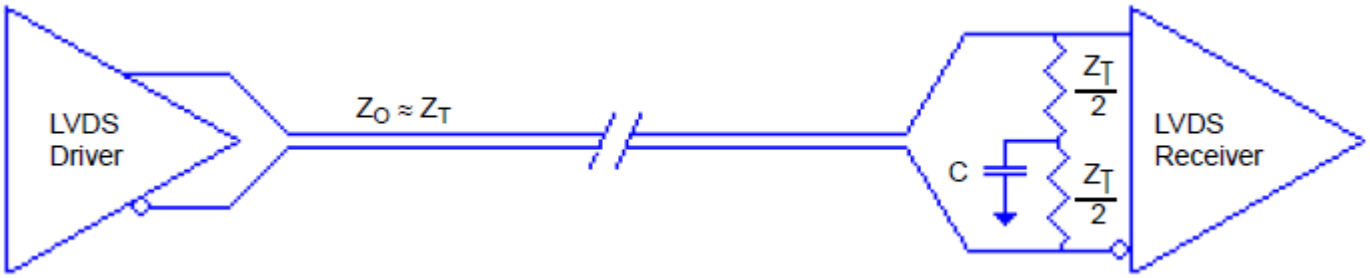


Figure 8. Optional LVDS Termination

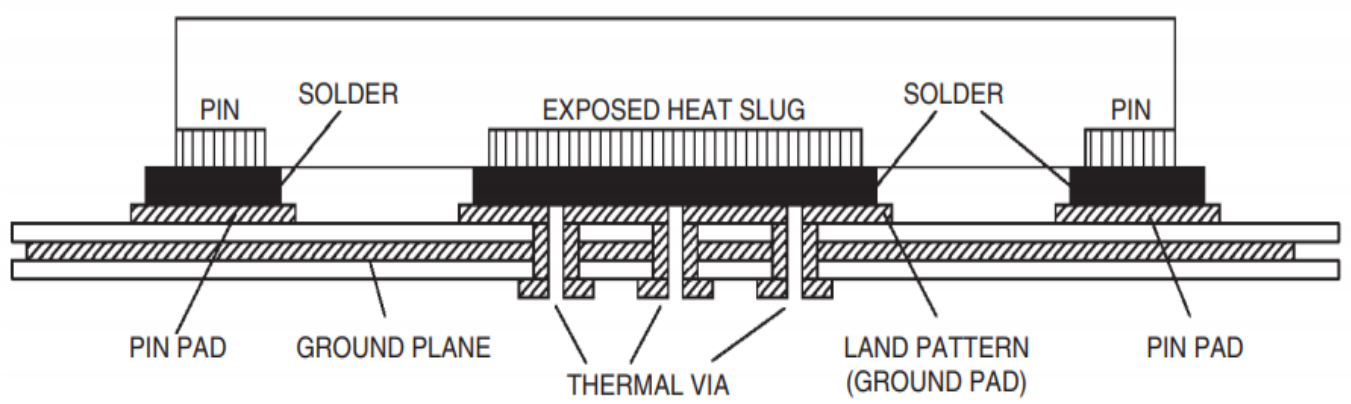


VFQFN EPAD Thermal Release Path

In order to maximize both the removal of heat from the package and the electrical performance, a land pattern must be incorporated on the Printed Circuit Board (PCB) within the footprint of the package corresponding to the exposed metal pad or exposed heat slug on the package, as shown in Figure 9. The solderable area on the PCB, as defined by the solder mask, should be at least the same size/shape as the exposed pad/slug area on the package to maximize the thermal/electrical performance. Sufficient clearance should be designed on the PCB between the outer edges of the land pattern and the inner edges of pad pattern for the leads to avoid any shorts.

While the land pattern on the PCB provides a means of heat transfer and electrical grounding from the package to the board through a solder joint, thermal vias are necessary to effectively conduct from the surface of the PCB to the ground plane(s). The land pattern must be connected to ground through these vias. The vias act as “heat pipes”. The number of vias (i.e. “heat pipes”) are application specific and dependent upon the package power dissipation as well as electrical conductivity requirements. Thus, thermal and electrical analysis and/or testing are recommended to determine the minimum number needed. Maximum thermal and electrical performance is achieved when an array of vias is incorporated in the land pattern. It is recommended to use as many vias connected to ground as possible. It is also recommended that the via diameter should be 12 to 13mils (0.30 to 0.33mm) with 1oz copper via barrel plating. This is desirable to avoid any solder wicking inside the via during the soldering process which may result in voids in solder between the exposed pad/slug and the thermal land. Precautions should be taken to eliminate any solder voids between the exposed heat slug and the land pattern. Note: These recommendations are to be used as a guideline only. For further information, please refer to the application note on the *Surface Mount Assembly of Amkor’s Thermally/ Electrically Enhance Leadframe Base Package, Amkor Technology.*

Figure 9. P.C. Assembly for Exposed Pad Thermal Release Path – Side View (drawing not to scale)



Case Temperature Considerations

This device supports applications in a natural convection environment which does not have any thermal conductivity through ambient air. The printed circuit board (PCB) is typically in a sealed enclosure without any natural or forced air flow and is kept at or below a specific temperature. The device package design incorporates an exposed pad (ePad) with enhanced thermal parameters which is soldered to the PCB where most of the heat escapes from the bottom exposed pad. For this type of application, it is recommended to use the junction-to-board thermal characterization parameter Ψ_{JB} (Psi-JB) to calculate the junction temperature (T_J) and ensure it does not exceed the maximum allowed junction temperature in the Absolute Maximum Rating table.

The junction-to-board thermal characterization parameter, $\Psi_{JB,}$ is calculated using the following equation:

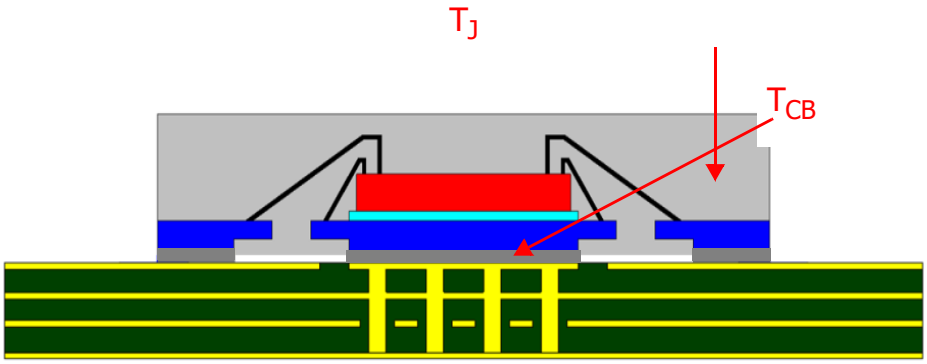
$T_J = T_{CB} + \Psi_{JB} \times P_{D,}$ where

T_J = Junction temperature at steady state condition in (°C).

T_{CB} = Case temperature (Bottom) at steady state condition in (°C).

Ψ_{JB} = Thermal characterization parameter to report the difference between junction temperature and the temperature of the board measured at the top surface of the board.

P_D = power dissipation (W) in desired operating configuration.



The ePad provides a low thermal resistance path for heat transfer to the PCB and represents the key pathway to transfer heat away from the IC to the PCB. It's critical that the connection of the exposed pad to the PCB is properly constructed to maintain the desired IC case temperature (T_{CB}). A good connection ensures that temperature at the exposed pad (T_{CB}) and the board temperature (T_B) are relatively the same. An improper connection can lead to increased junction temperature, increased power consumption and decreased electrical performance. In addition, there could be long-term reliability issues and increased failure rate.

Example Calculation for Junction Temperature (T_J): $T_J = T_{CB} + \Psi_{JB} \times P_D$

Package type	28 VFQFN
Body size (mm)	5 x 5 x 0.75
ePad size (mm)	3.25 x 3.25
Thermal Via	4 x 4 Matrix
Ψ_{JB}	2.4°C/W
T_{CB}	105°C
P_D	0.38W

For the variables above, the junction temperature is equal to 105.9°C. Since this is below the maximum junction temperature of 125°C, there are no long term reliability concerns. In addition, since the junction temperature at which the device was characterized using forced convection is 120.3°C, this device can function without the degradation of the specified AC or DC parameters.

Fail-Safe Operation

All clock inputs support fail-safe operation. That is, when the device is powered down, the clock inputs can be held at a DC voltage of up to 4.6V without damaging the device or the input pins.

Power Considerations

This section provides information on power dissipation and junction temperature for the 8P34S2104.
Equations and example calculations are also provided.

1. Power Dissipation

The following is the power dissipation for V_{DD} = 2.7V, which gives worst case results.

Maximum current at 85°C: V_{DD_MAX} = 225mA.

- Power$_{_MAX}$ = V_{DD_MAX} * I_{DD_MAX} = 2.7V * 225mA = **607.5mW**

2. Junction Temperature

Junction temperature, Tj, is the temperature at the junction of the bond wire and bond pad directly affects the reliability of the device. The maximum recommended junction temperature is 125°C. Limiting the internal transistor junction temperature, Tj, to 125°C ensures that the bond wire and bond pad temperature remains below 125°C.

The equation for Tj is as follows: Tj = θ_{JA} * Pd_total + T_A

Tj = Junction Temperature

θ_{JA} = Junction-to-Ambient Thermal Resistance

Pd_total = Total Device Power Dissipation (example calculation is in Power Dissipation section above)

T_A = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance θ_{JA} must be used. Assuming no air flow and a multi-layer board, the appropriate value is 46.2°C/W per Table 11 below.

Therefore, Tj for an ambient temperature of 85°C with all outputs switching is:

85°C + 0.6075W * 46.2°C/W = 113.07°C. This is below the limit of 125°C.

This calculation is only an example. Tj will obviously vary depending on the number of loaded outputs, supply voltage, air flow and the type of board (multi-layer).

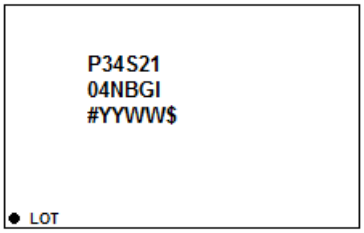
Table 11. Thermal Resistance θ_{JA} for 28-lead VFQFN, Forced Convection

θ_{JA} (°C/W) vs. Air Flow (m/s)			
Meters per Second	**0**	**1**	**2**
28-lead VFQFN Multi-Layer PCB, JEDEC Standard Test Boards	46.2	39.4	37.1

Package Outline Drawings

The package outline drawings are located at the end of this document and are accessible from the Renesas website (see Ordering Information for POD links). The package information is the most current data available and is subject to change without revision of this document.

Marking Diagram



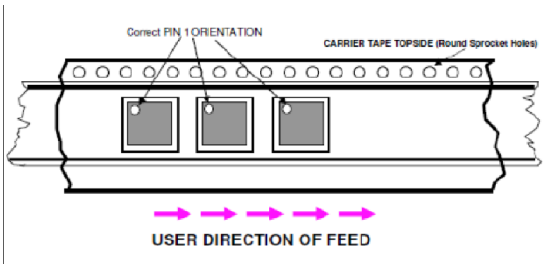
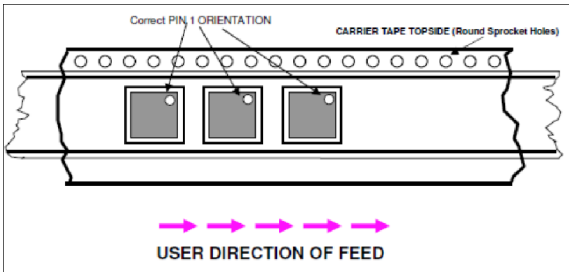
- Line 1 and line 2 indicates the truncated part number.
- Line 3:
  - "#" indicates stepping.
  - "YYWW" indicates the date code ("YY" are the last two digits of the year, and "WW" is a work week number that the part was assembled.
  - "$" indicates the mark code.

Ordering Information

Table 12. Ordering Information

Part Number	Marking	Package	Carrier Type	Temperature Range
8P34S2104NBGI	P34S2104NBGI	28-lead VFQFN, Lead-Free	Tray	-40°C to +85°C
8P34S2104NBGI8	P34S2104NBGI		Tape & Reel, Pin 1 Orientation: EIA-481-C	
8P34S2104NBGI/W	P34S2104NBGI		Tape & Reel, Pin 1 Orientation: EIA-481-D/E	

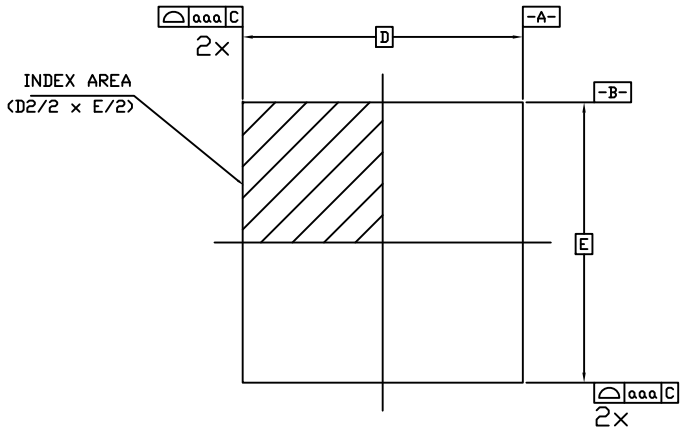
Table 13. Pin 1 Orientation in Tape and Reel Packaging

Part Number Suffix	Pin 1 Orientation	Illustration
8	Quadrant 1 (EIA-481-C)	
/W	Quadrant 2 (EIA-481-D/E)	

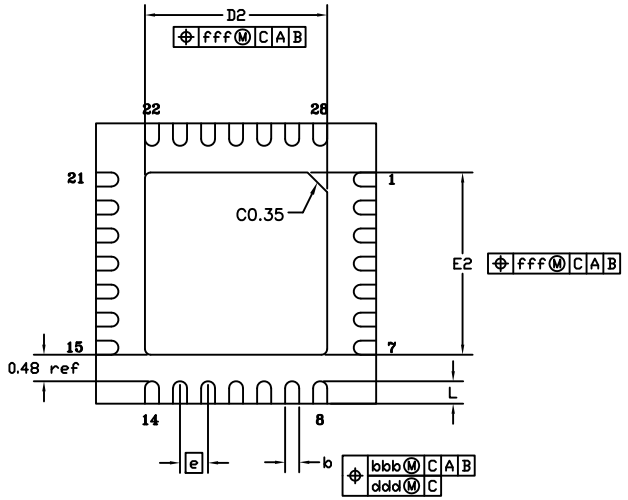
Revision History

Revision Date	Description of Change
June 6, 2022	▪ Updated the test condition and values for V_{REF} in Table 8
May 26, 2022	▪ Updated the Power Supply Current values in Table 5 and Table 6 ▪ Updated the maximum value for the Input Leakage Current in Table 7 and Table 8 ▪ Updated the test conditions for Differential Output Voltage and Offset Voltage in Table 10
May 17, 2022	▪ Added device support for Fail-Safe Operation. ▪ Updated SELA pin function. ▪ Added leakage current spec in Table 7 and Table 8.
November 9, 2021	Updated Table 10.
April 12, 2021	▪ Added electrical tables for 2.5V support (table 6 is new, tables 7, 8, 9, 10 are modified). ▪ Updated Package Outline Drawings section; added package link to Ordering Information table.
September 8, 2020	▪ Updated the section Wiring the Differential Input to Accept Single-Ended Levels. ▪ Updated Figures 3, 5 and 6. ▪ Reformatted document template.
September 4, 2018	▪ Updated Ordering Information part numbers (removed “L”). ▪ Updated Package Outline Drawings section and document disclaimer.
October 20, 2016	Initial Final datasheet.

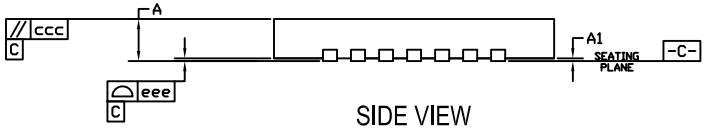
REVISIONS			
REV	DESCRIPTION	DATE	APPROVED
00	INITIAL RELEASE	06/04/10	KS
01	CORRECTION ON L	09/22/10	DP
02	COMBINE POD & LAND PATTERN	1/22/14	J.H



TOP VIEW



BOTTOM VIEW



SIDE VIEW

SYMBOL	DIMENSION		
	MIN	NOM	MAX
D2	3.15	3.25	3.35
E2	3.15	3.25	3.35
L	0.30	0.40	0.50
D		5.00 BSC	
E		5.00 BSC	
e		0.50 BSC	
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
b	.20	.25	.30
aaa		0.15	
bbb		0.10	
ccc		0.10	
ddd		0.05	
eee		0.08	
fff		0.10	

NOTES:

1. ALL DIMENSIONING AND TOLERANCING CONFORM TO ANSI Y14.5M–1982
2. ALL DIMENSIONS ARE IN MILLIMETERS.

TOLERANCES UNLESS SPECIFIED
DECIMAL ANGULAR
X± .1 ±1°
XX± .05
XXX± .030

APPROVALS	DATE
DRAWN YCS	06/02/10
CHECKED	

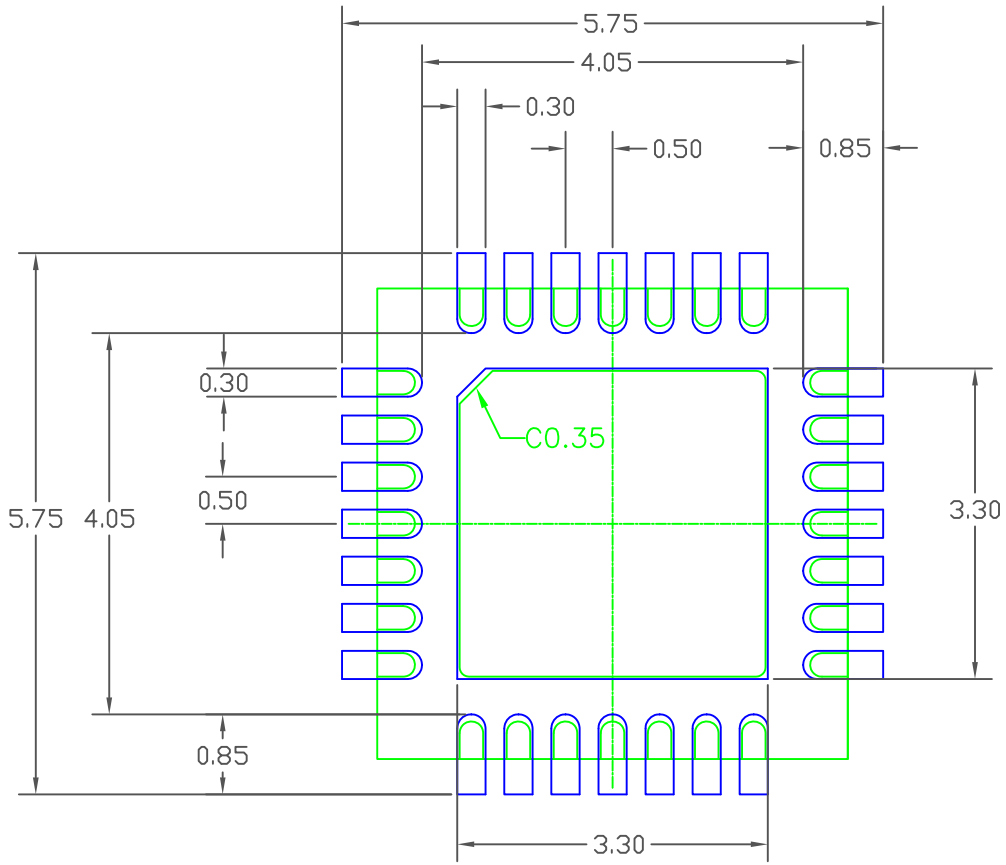
IDT™
www.IDT.com
6024 SILVER CREEK VALLEY ROAD. SAN JOSE, CA 95138
PHONE: (408) 284–8200
FAX: (408) 284–3572

TITLE NB/NBG28 PACKAGE OUTLINE
5.0 x 5.0 mm BODY
0.50 mm PITCH QFN

SIZE	DRAWING No.	REV
C	PSC–4312	02

DO NOT SCALE DRAWING

REVISIONS			
REV	DESCRIPTION	DATE	APPROVED
00	INITIAL RELEASE	06/04/10	KS
01	CORRECTION ON L	09/22/10	DP
02	COMBINE POD & LAND PATTERN	1/22/14	J.H



NOTES:

1. ALL DIMENSION ARE IN mm. ANGLES IN DEGREES.
2. TOP DOWN VIEW. AS VIEWED ON PCB.
3. COMPONENT OUTLINE SHOW FOR REFERENCE IN GREEN.
4. LAND PATTERN IN BLUE. NSMD PATTERN ASSUMED.
5. LAND PATTERN RECOMMENDATION PER IPC-7351B GENERIC REQUIREMENT FOR SURFACE MOUNT DESIGN AND LAND PATTERN.

TOLERANCES UNLESS SPECIFIED DECIMAL ANGULAR X± .1 ±1° XX± .05 XXX± .030		IDT™ www.IDT.com	6024 SILVER CREEK VALLEY ROAD. SAN JOSE, CA 95138 PHONE: (408) 284-8200 FAX: (408) 284-3572
APPROVALS	DATE	TITLE	NB/NBG28 PACKAGE OUTLINE 5.0 x 5.0 mm BODY 0.50 mm PITCH QFN
DRAWN XS	06/02/10		
CHECKED			
		SIZE C	DRAWING No. PSC-4312 REV 02
		DO NOT SCALE DRAWING	SHEET 2 OF 2

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(Rev.1.0 Mar 2020)

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