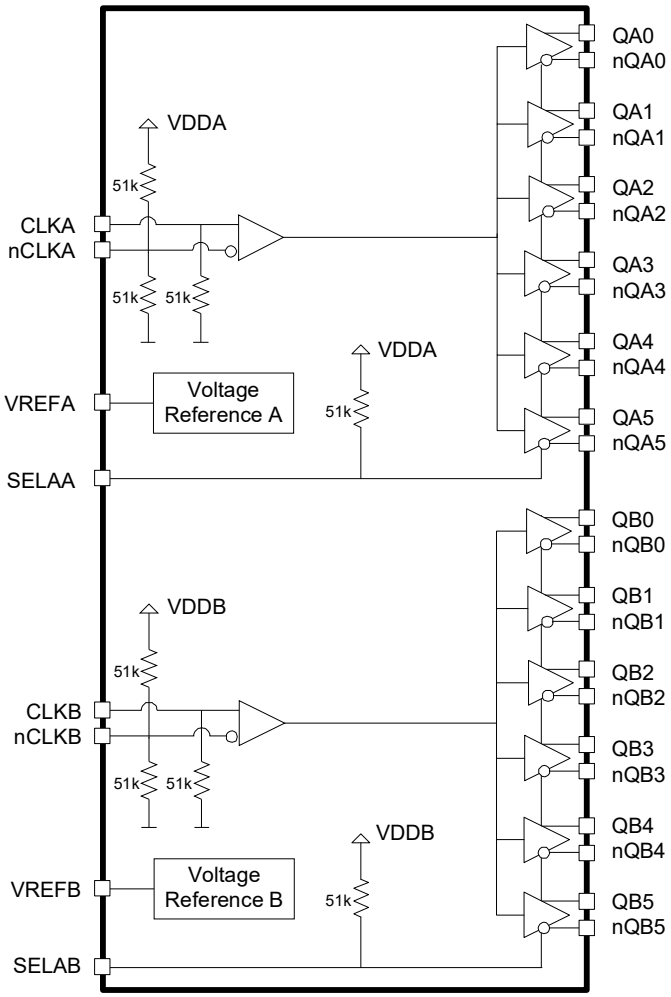
Description

The 8P34S2106 is a high-performance, low-power, differential dual 1:6 LVDS output 1.8V/2.5V fanout buffer. The device is designed for the fanout of high-frequency, very low additive phase-noise clock and data signals. Two independent buffer channels are available, each channel has six low skew outputs. High isolation between channels minimizes noise coupling. AC characteristics such as propagation delay are matched between channels.

Guaranteed output-to-output and part-to-part skew characteristics make the 8P34S2106 ideal for those clock distribution applications demanding well-defined performance and repeatability. The device is characterized to operate from a 1.8V/2.5V power supply. The integrated bias voltage references enable easy interfacing of AC-coupled signals to the device inputs.

Block Diagram



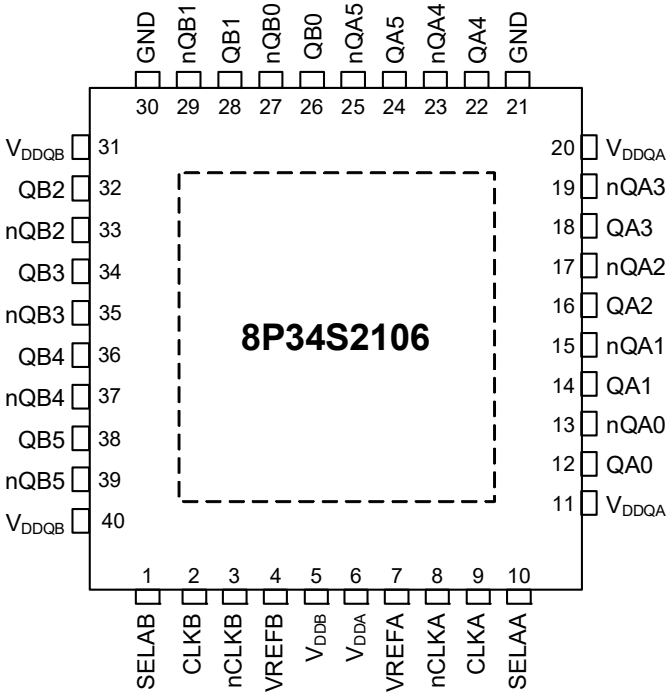
Features

- Dual 1:6 low skew, low additive jitter LVDS fanout buffers
- Matched AC characteristics across both channels
- High isolation between channels
- Low power consumption
- Both differential CLKA, nCLKA and CLKB, nCLKB inputs accept LVDS, LVPECL and single-ended LVCMOS levels
- Maximum input clock frequency: 2GHz
- Output amplitudes: 350mV, 500mV (selectable)
- Output bank skew: 10ps typical
- Output skew: 20ps typical
- Low additive phase jitter, RMS: 45fs typical (f_{REF} = 156.25MHz, 12kHz – 20MHz)
- Full 1.8V and 2.5V supply voltage mode
- Device current consumption (I_{DD}):
  - 210mA typical: 1.8V
  - 230mA typical: 2.5V
- Lead-free (RoHS 6) packaging:
  - 40-VFQFPN, 6 x 6 x 0.9 mm
  - 48-WL-CSP, 3.59 x 3.04 x 0.6 mm
- -40°C to 85°C ambient operating temperature
- Supports case temperature up to 105°C

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Pin Assignments for 40-VFQFPN Package

Figure 1. Pin Assignments for 40-VFQFPN, 6 x 6 mm Package – Top View



Pin Descriptions for 40-VFQFPN Package

Table 1. 40-VFQFPN Pin Descriptions[a]

Number	Name	Type	Description
1	SELAB	Input [PU]	Control input. Output amplitude select for channel B.
2	CLKB	Input [PD]	Non-inverting differential clock/data input for channel B.
3	nCLKB	Input [PD/PU]	Inverting differential clock/data input for channel B.
4	VREFB	Output	Bias voltage reference for the CLKB, nCLKB input pairs.
5	V_{DDB}	Power	Power supply pin for the core and inputs of channel B.
6	V_{DDA}	Power	Power supply pin for the core and inputs of channel A.
7	VREFA	Output	Bias voltage reference for the CLKA, nCLKA input pairs.
8	nCLKA	Input [PD/PU]	Inverting differential clock/data input for channel A.
9	CLKA	Input [PD]	Non-inverting differential clock/data input for channel A.
10	SELAA	Input [PU]	Control input. Output amplitude select for channel A.
11	V_{DDQA}	Power	Power supply pin for the channel A outputs QA[0:5]
12	QA0	Output	Differential output pair A0. LVDS interface levels.
13	nQA0	Output	Differential output pair A0. LVDS interface levels.
14	QA1	Output	Differential output pair A1. LVDS interface levels.
15	nQA1	Output	Differential output pair A1. LVDS interface levels.

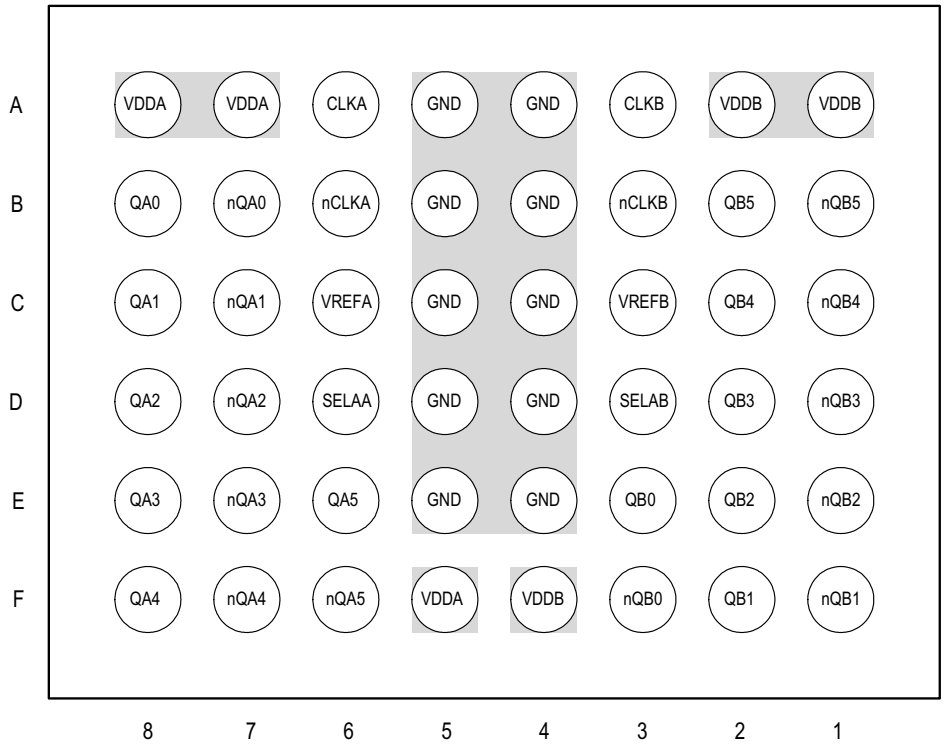
Table 1. 40-VFQFPN Pin Descriptions[a] (Cont.)

Number	Name	Type	Description
16	QA2	Output	Differential output pair A2. LVDS interface levels.
17	nQA2	Output	Differential output pair A2. LVDS interface levels.
18	QA3	Output	Differential output pair A3. LVDS interface levels.
19	nQA3	Output	Differential output pair A3. LVDS interface levels.
20	V_{DDQA}	Power	Power supply pin for the channel A outputs QA[0:5]
21	GND	Power	Power supply ground.
22	QA4	Output	Differential output pair A4. LVDS interface levels.
23	nQA4	Output	Differential output pair A4. LVDS interface levels.
24	QA5	Output	Differential output pair A5. LVDS interface levels.
25	nQA5	Output	Differential output pair A5. LVDS interface levels.
26	QB0	Output	Differential output pair B0. LVDS interface levels.
27	nQB0	Output	Differential output pair B0. LVDS interface levels.
28	QB1	Output	Differential output pair B1. LVDS interface levels.
29	nQB1	Output	Differential output pair B1. LVDS interface levels.
30	GND	Power	Power supply ground.
31	V_{DDQB}	Power	Power supply pin for the channel B outputs QB[0:5].
32	QB2	Output	Differential output pair B2. LVDS interface levels.
33	nQB2	Output	Differential output pair B2. LVDS interface levels.
34	QB3	Output	Differential output pair B3. LVDS interface levels.
35	nQB3	Output	Differential output pair B3. LVDS interface levels.
36	QB4	Output	Differential output pair B4. LVDS interface levels.
37	nQB4	Output	Differential output pair B4. LVDS interface levels.
38	QB5	Output	Differential output pair B5. LVDS interface levels.
39	nQB5	Output	Differential output pair B5. LVDS interface levels.
40	V_{DDQB}	Power	Power supply pin for the channel B outputs QB[0:5].
ePad	GND_EPAD	Power	Exposed pad of package. Connect to ground.

[a] Pull-up (PU) and pull-down (PD) resistors are indicated in parentheses. *Pull-up* and *pull-down* refers to internal input resistors. See Table 6, *DC Input Characteristics,* for typical values.

Pin Assignments for 48-WL-CSP Package

Figure 2. Pin Assignments for 48-WL-CSP, 3.59 x 3.04mm Package – Bottom View



Pin Descriptions for 48-WL-CSP Package

Table 2. 48-WL-CSP Pin Descriptions

Number	Name	Type[a]	Description
Channel A			
A6	CLKA	Input [PD]	Non-inverting and inverting differential clock/data input for channel A.
B6	nCLKA	Input [PU/PD]	
C6	VREFA	Output	Bias voltage reference for the CLKA, nCLKA input pairs.
D6	SELAA	Input [PU]	Control input: Output amplitude select for channel A.
B8, B7	QA0, nQA0	Output	Differential output pair A0. LVDS interface levels.
C8, C7	QA1, nQA1	Output	Differential output pair A1. LVDS interface levels.
D8, D7	QA2, nQA2	Output	Differential output pair A2. LVDS interface levels.
E8, E7	QA3, nQA3	Output	Differential output pair A3. LVDS interface levels.
F8, F7	QA4, nQA4	Output	Differential output pair A4. LVDS interface levels.
E6, F6	QA5, nQA5	Output	Differential output pair A5. LVDS interface levels.
A7, A8, F5	V_{DDA}	Power	Power supply pins for the core, inputs, and outputs QA[0:5] of channel A. A7, A8 and F5 are connected.[b]

Table 2. 48-WL-CSP Pin Descriptions (Cont.)

Number	Name	Type[a]	Description
Channel B			
A3	CLKB	Input [PD]	Non-inverting and inverting differential clock/data input for channel B.
B3	nCLKB	Input [PU/PD]	
C3	VREFB	Output	Bias voltage reference for the CLKB, nCLKB input pairs.
D3	SELAB	Input [PU]	Control input: Output amplitude select for channel B.
E3, F3	QB0, nQB0	Output	Differential output pair B0. LVDS interface levels.
F2, F1	QB1, nQB1	Output	Differential output pair B1. LVDS interface levels.
E2, E1	QB2, nQB2	Output	Differential output pair B2. LVDS interface levels.
D2, D1	QB3, nQB3	Output	Differential output pair B3. LVDS interface levels.
C2, C1	QB4, nQB4	Output	Differential output pair B4. LVDS interface levels.
B2, B1	QB5, nQB5	Output	Differential output pair B5. LVDS interface levels.
A1, A2, F4	V_{DDB}	Power	Power supply pins for the core, inputs and outputs QB[0:5] of channel B. A1, A2 and F4 are connected.
Ground			
A4, A5, B4, B5, C4, C5, D4, D5, E4, E5	GND	Power	Power supply ground.

[a] Internal pull-up (PU) and pull-down (PD) resistors are indicated in parentheses.

[b] V_{DDA} is not connected to V_{DDB}.

Function Tables

Table 3. SELAA Output Amplitude Selection Table

SELAA	QA Output Amplitude (mV)
0	350
1 (default)	500

Table 4. SELAB Output Amplitude Selection Table

SELAB	QB Output Amplitude (mV)
0	350
1 (default)	500

Absolute Maximum Ratings

The absolute maximum ratings are stress ratings only. Stresses greater than those listed below can cause permanent damage to the device. Functional operation of the 8P34S2106 at absolute maximum ratings is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

Table 5. Absolute Maximum Ratings

Item	Rating
Supply voltage, V_{DDX}[a]	4.6V
Inputs, V_I	-0.5V to 3.6V
Outputs, I_O Continuous current Surge current	 10mA 15mA
Input sink/source, I_{REF}	±2mA
Maximum Junction Temperature, $T_{J,MAX}$	125°C
Storage Temperature, T_{STG}	-65°C to 150°C
ESD - Human Body Model[b]	2000V
ESD - Charged Device Model[b]	1500V

[a] V_{DDX} denotes V_{DDA}, V_{DDB}, V_{DDQA}, and V_{DDQB} for the QFN package. V_{DDX} denotes V_{DDA} and V_{DDB} for the WL-CSP package.

[b] According to JEDEC JS-001-2012/JESD22-C101E.

DC Electrical Characteristics

Table 6. DC Input Characteristics

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
C_{IN}	Input capacitance			2		pF
$R_{PULLDOWN}$	Input pull-down resistor			51		kΩ
R_{PULLUP}	Input pull-up resistor			51		kΩ

Table 7. Power Supply DC Characteristics, $V_{DDA} = V_{DDB} = V_{DDQA} = V_{DDQB}$ = 1.8V ± 5%, T_A = -40°C to 85°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
V_{DDX}[a]	Power supply voltage			1.71	1.8	1.89	V
I_{DDX}[a]	Core and output supply current	QA[0:5], QB[0:5] outputs terminated 100Ω between nQx, Qx	500mV amplitude		300	390	mA
			350mV amplitude		210	275	mA

[a] V_{DDX}: For the VFQFPN package, V_{DDA} and V_{DDB} are the core and input supply pins; V_{DDQA} and V_{DDQB} supply the outputs. For the WL-CSP package, V_{DDA} and V_{DDB} supply the circuits of the respective channels.

Table 8. Power Supply DC Characteristics, $V_{DDA} = V_{DDB} = V_{DDQA} = V_{DDQB}$ = 2.1V–2.7V, T_A = -40°C to 85°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
V_{DDX}[a]	Power supply voltage			2.1	2.5	2.7	V
I_{DDX}[a]	Core and output supply current	QA[0:5], QB[0:5] outputs terminated 100Ω between nQx, Qx	500mV amplitude		325	405	mA
			350mV amplitude		230	290	mA

[a] V_{DDX}: For the VFQFPN package, V_{DDA} and V_{DDB} are the core and input supply pins; V_{DDQA} and V_{DDQB} supply the outputs. For the WL-CSP package, V_{DDA} and V_{DDB} supply the circuits of the respective channels.

Table 9. LVCMOS Inputs DC Characteristics, $V_{DDA} = V_{DDB} = V_{DDQA} = V_{DDQB}$ = 1.8V ± 5%, 2.1V-2.7V, T_A = -40°C to 85°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
V_{IH}	Input high voltage	SELAA, SELAB		0.75 · V_{DD}[a]		V_{DD}[a] + 0.3	V
V_{IL}	Input low voltage	SELAA, SELAB		-0.3		0.25 · V_{DD}[a]	V
I_{IH}	Input high current	SELAA, SELAB	V_{IN} = V_{DD}[a] = 1.89V, 2.7V			10	µA
I_{IL}	Input low current	SELAA, SELAB	V_{IN} = 0V, V_{DD}[a] = 1.89V, 2.7V	-150			µA

[a] V_{DD} denotes V_{DDA}, V_{DDB}, V_{DDQA}, and V_{DDQB} for the QFN package. V_{DDX} denotes V_{DDA} and V_{DDB} for the WL-CSP package.

Table 10. Differential Inputs Characteristics, $V_{DDA} = V_{DDB} = V_{DDQA} = V_{DDQB}$ = 1.8V ± 5%, 2.1V-2.7V, T_A = -40°C to 85°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
I_{IH}	Input high current	CLKA, nCLKA CLKB, nCLKB	$V_{IN} = V_{DD}$[a] = 1.89V, 2.7V			150	µA
I_{IL}	Input low current	CLKA, CLKB	V_{IN} = 0V, V_{DD}[a] = 1.89V, 2.7V	-10			µA
		nCLKA, nCLKB	V_{IN} = 0V, V_{DD}[a] = 1.89V, 2.7V	-150			µA
VREFA, B	Reference voltage[b]		I_{REF} = +100µA, V_{DD}[a] = 1.8V	0.90		1.30	V
			I_{REF} = +100µA, V_{DD}[a] = 2.5V	1.50		1.90	V

[a] V_{DD} denotes V_{DDA}, V_{DDB}, V_{DDQA}, and V_{DDQB} for the QFN package. V_{DDX} denotes V_{DDA} and V_{DDB} for the WL-CSP package.

[b] VREF[A:B] specification is applicable to the AC-coupled input interfaces shown in Figure 6 and Figure 7.

Table 11. LVDS DC Characteristics, $V_{DDA} = V_{DDB} = V_{DDQA} = V_{DDQB}$ = 1.8V ±5%, 2.1V–2.7V, T_A = -40°C to +85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
ΔV_{OD}	V_{OD} Magnitude Change				50	mV
ΔV_{OS}	V_{OS} Magnitude Change				50	mV

AC Electrical Characteristics

Table 12. AC Electrical Characteristics, VDDx = 1.8V ± 5%, 2.1V–2.7V, T_A = -40°C to 85°C [a]

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
f_{REF}	Input frequency				2	GHz
$\Delta V/\Delta t$	Input edge rate		1.5			V/ns
t_{PD}	Propagation delay[b], [c]	CLKA to any QAx, CLKB to any nQBx	100	255	400	ps
*t*sk(o)	Output skew[d], [e]			20	40	ps
*t*sk(b)	Output bank skew[e], [f]			10	25	ps
*t*sk(p)	Pulse skew[g]	f_{REF} = 100MHz		5	25	ps
*t*sk(pp)	Part-to-part skew[e], [h]				200	ps

Table 12. AC Electrical Characteristics, VDDx = 1.8V ± 5%, 2.1V–2.7V, T_A = -40°C to 85°C [a] (Cont.)

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
t_{JIT}	Buffer Additive Phase Jitter, RMS; 500mV amplitude; refer to Additive Phase Jitter		f_{REF} = 156.25MHz; square wave, V_{DD} = 1.8V ± 5%, V_{PP} = 0.5V; Integration range: 1kHz – 40MHz		60	80	fs
			f_{REF} = 156.25MHz square wave, V_{DD} = 1.8V ± 5%, V_{PP} = 1V; Integration range: 12kHz – 20MHz		45	60	fs
			f_{REF} = 156.25MHz; square wave, V_{DD} = 2.5V, V_{PP} = 0.5V; Integration range: 1kHz – 40MHz		54	75	fs
			f_{REF} = 156.25MHz square wave, V_{DD} = 2.5V, V_{PP} = 1V; Integration range: 12kHz – 20MHz		40	55	fs
Φ_N(≥30M)	Clock single-side band phase noise		≥30MHz offset from carrier and noise floor, V_{DD} = 1.8V		< -160		dBc/Hz
			≥30MHz offset from carrier and noise floor, V_{DD} = 2.5V		< -165		dBc/Hz
$t_{JIT, SP}$	Spurious suppression, coupling between channels		f_{QA} = 491.52MHz, f_{QB} = 61.44MHz; V_{DD} = 1.8V, measured between neighboring outputs		-59		dB
			f_{QA} = 491.52MHz, f_{QB} = 15.36MHz; V_{DD} = 1.8V, measured between neighboring outputs		-59		dB
			f_{QA} = 491.52MHz, f_{QB} = 61.44MHz; V_{DD} = 2.5V, measured between neighboring outputs		-54		dB
			f_{QA} = 491.52MHz, f_{QB} = 15.36MHz; V_{DD} = 2.5V, measured between neighboring outputs		-67		dB
t_R / t_F	Output Rise/ Fall Time		10% to 90%, outputs loaded with 100Ω, V_{DD} = 1.8V ± 5%		150	400	ps
			20% to 80%, outputs loaded with 100Ω, V_{DD} = 1.8V ± 5%		90	160	ps
			10% to 90%, outputs loaded with 100Ω, V_{DD} = 2.1V - 2.7V		200	420	ps
			20% to 80%, outputs loaded with 100Ω, V_{DD} = 2.1V - 2.7V		110	190	ps
V_{PP}	Input voltage amplitude	CLKA, CLKB		0.15		1.2	V
V_{PP_DIFF}	Differential input voltage amplitude	CLKA, CLKB		0.3		2.4	V

Table 12. AC Electrical Characteristics, VDDx = 1.8V ± 5%, 2.1V–2.7V, T_A = -40°C to 85°C [a] (Cont.)

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{CMR}	Common mode input voltage[i]		1.1		V_{DD}[j] – ($V_{PP/2}$)	V
V_{OD}	Differential output voltage	SELA A, SELAB = 0, R_{OUT} = 100Ω, f_{REF} < 2GHz	247	350	454	mV
		SELA A, SELAB = 1, R_{OUT} = 100Ω, f_{REF} < 2GHz	350	500	650	mV
		SELA A, SELAB = 1, R_{OUT} = 100Ω, f_{REF} < 500MHz	450	550	650	mV
V_{OS}	Offset voltage, V_{DD} = 1.8V ± 5%	SELAA, SELAB = 0	0.61	0.77	0.91	V
		SELAA, SELAB = 1	0.53	0.68	0.82	V
	Offset voltage, V_{DD} = 2.1V	SELAA, SELAB = 0	0.80	1.01	1.20	V
		SELAA, SELAB = 1	0.74	0.95	1.15	V
	Offset voltage, V_{DD} = 2.3V	SELAA, SELAB = 0	1.00	1.21	1.42	V
		SELAA, SELAB = 1	0.95	1.15	1.36	V
	Offset voltage, V_{DD} = 2.5V	SELAA, SELAB = 0	1.30	1.45	1.62	V
		SELAA, SELAB = 1	1.20	1.35	1.55	V
	Offset voltage, V_{DD} = 2.7V	SELAA, SELAB = 0	1.40	1.61	1.82	V
		SELAA, SELAB = 1	1.34	1.55	1.75	V

[a] Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfpm. The device will meet specifications after thermal equilibrium has been reached under these conditions.

[b] Measured from the differential input crossing point to the differential output crossing point.

[c] Input V_{PP} = 400mV.

[d] Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at the differential cross points.

[e] This parameter is defined in accordance with JEDEC Standard 65.

[f] Defined as skew within a bank of outputs at the same voltage and with equal load conditions.

[g] Output pulse skew is the absolute value of the difference of the propagation delay times: $| t_{PLH} - t_{PHL} |$.

[h] Defined as skew between outputs on different devices operating at the same supply voltage, same frequency, same temperature and with equal load conditions. Using the same type of inputs on each device, the outputs are measured at the differential cross points.

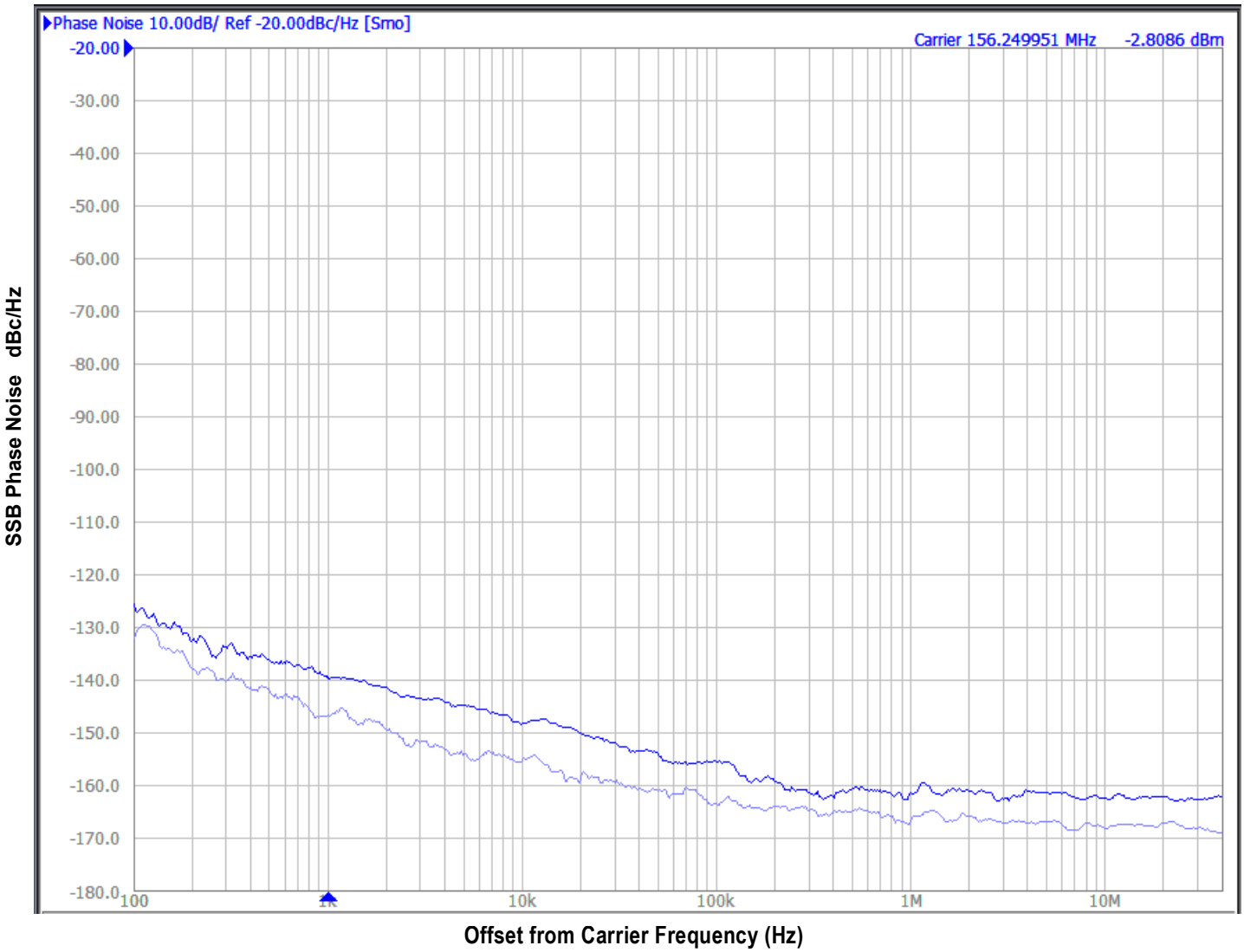
[i] Common Mode Input Voltage is defined as the cross-point voltage.

[j] V_{DDX} denotes V_{DDA}, V_{DDB}, V_{DDQA}, and V_{DDQB} for the QFN package. V_{DDX} denotes V_{DDA} and V_{DDB} for the WL-CSP package.

Additive Phase Jitter

The spectral purity in a band at a specific offset from the fundamental compared to the power of the fundamental is called the *dBc Phase Noise*. This value is normally expressed using a Phase noise plot and is most often the specified plot in many applications. Phase noise is defined as the ratio of the noise power present in a 1Hz band at a specified offset from the fundamental frequency to the power value of the fundamental. This ratio is expressed in decibels (dBm) or a ratio of the power in the 1Hz band to the power in the fundamental. When the required offset is specified, the phase noise is called a *dBc* value, which simply means dBm at a specified offset from the fundamental. By investigating jitter in the frequency domain, we get a better understanding of its effects on the desired application over the entire time record of the signal. It is mathematically possible to calculate an expected bit error rate given a phase noise plot.

Figure 3. Additive Phase Jitter. Frequency: 156.25MHz, Integration range: 12kHz to 20MHz = 45fs Typical



As with most timing specifications, phase noise measurements have issues relating to the limitations of the measurement equipment. The noise floor of the equipment can be higher or lower than the noise floor of the device. Additive phase noise is dependent on both the noise floor of the input source and measurement equipment.

Measured using a Wenzel 156.25MHz Oscillator as the input source.

Applications Information

Recommendations for Unused Input and Output Pins

Inputs

CLK/nCLK Inputs

For applications not requiring the use of the differential input, both CLK and nCLK can be left floating. Though not required, but for additional protection, a 1kΩ resistor can be tied from CLK to ground.

Outputs

LVDS Outputs

All unused LVDS output pairs can be either left floating or terminated with 100Ω across. If they are left floating there should be no trace attached.

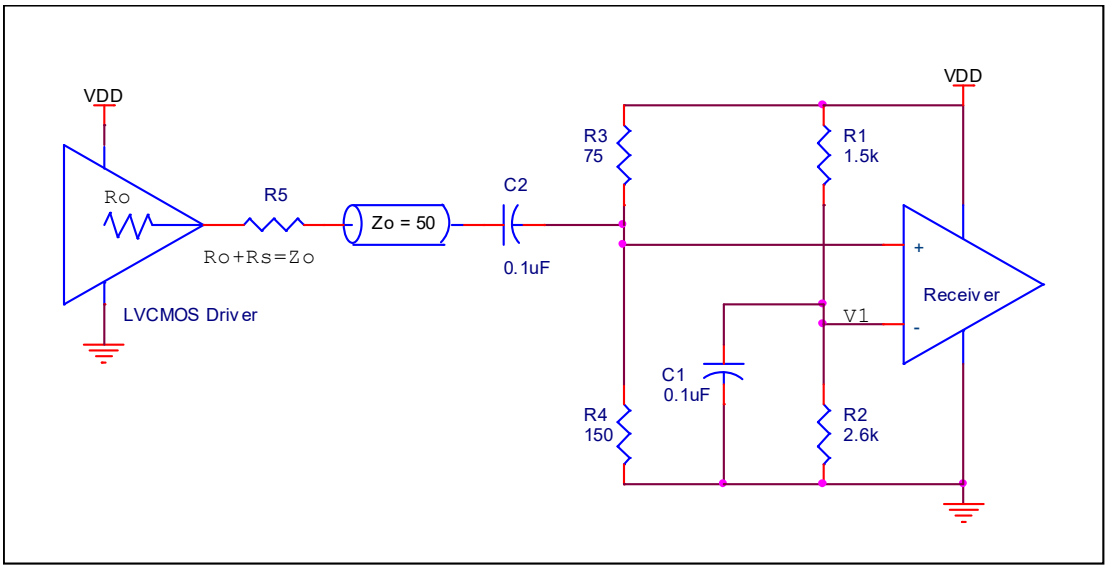
VREFX

The unused VREFA and VREFB pins can be left floating. We recommend that there is no trace attached.

Wiring the Differential Input to Accept Single-Ended Levels

Figure 4 shows an example of how a differential input can be wired to accept single-ended levels. To satisfy the VCMR requirement, the reference voltage V1 is set to 1.2V which is generated by the bias resistors R1 and R2. The bypass capacitor (C1) is used to help filter noise on the DC bias. This bias circuit should be located as close to the input pin as possible. The ratio of R1 and R2 might need to be adjusted to position the V1 to meet the VCRM requirement. For example, if the input clock swing is 1.8V and VDD = 1.8V, R1 and R2 value should be adjusted to set V1 at 1.2V in this example. The values below are for when both the single-ended swing and VDD are at the same voltage. This configuration requires that the sum of the output impedance of the driver (Ro) and the series resistance (Rs) equals the transmission line impedance. In addition, matched termination at the input will attenuate the signal in half. This can be done in one of two ways. First, R3 and R4 in parallel should equal the transmission line impedance and the signal DC offset after AC coupling should be equal to V1, i.e. 1.2V in this example. For most Zo=50Ω applications, R3=75Ω and R4 can be 130Ω. By keeping the same R3/R4 ratio, the values of the resistors can be increased to reduce the loading for slower and weaker LVCMOS driver. When using single-ended signaling, the noise rejection benefits of differential signaling are reduced. Even though the input can handle larger amplitude signaling, it is recommended that the amplitude be reduced. For single-ended applications, the swing can be larger. Make sure the single-ended logic high and logic low signal operates within specification limit. Though some of the recommended components might not be used, the pads should be placed in the layout. They can be utilized for debugging purposes. The datasheet specifications are characterized and guaranteed by using a differential signal.

Figure 4. Example Schematic for Wiring a Differential Input to Accept Single-ended Levels



1.8V Differential Clock Input Interface

The CLK /nCLK accepts LVDS, LVPECL and other differential signals. The differential input signal must meet both the V_{PP} and V_{CMR} input requirements. Figure 5 to Figure 7 show interface examples for the CLK /nCLK input driven by the most common driver types. The input interfaces suggested here are examples only. If the driver is from another vendor, use their termination recommendation. Please consult with the vendor of the driver component to confirm the driver termination requirements.

Figure 5. Differential Input Driven by an LVDS Driver – DC Coupling

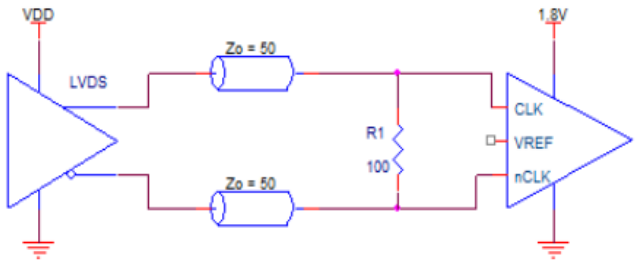


Figure 6. Differential Input Driven by an LVDS Driver – AC Coupling

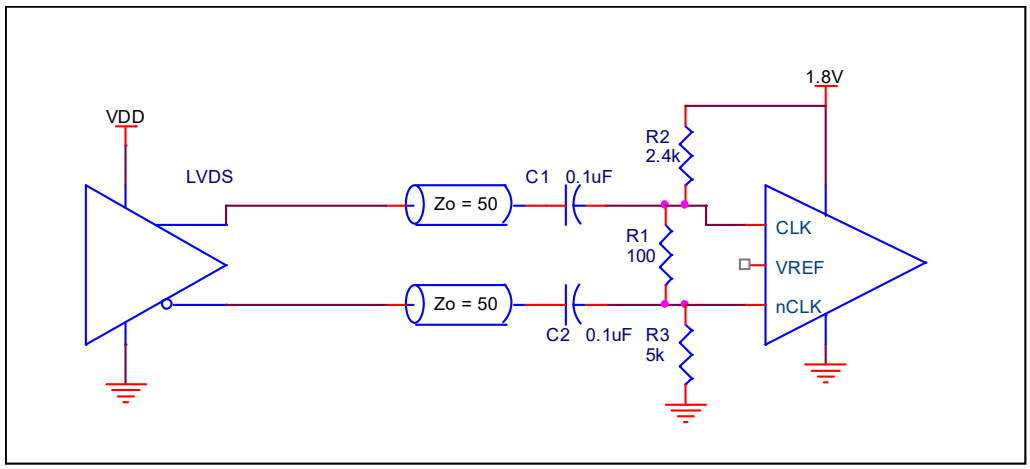
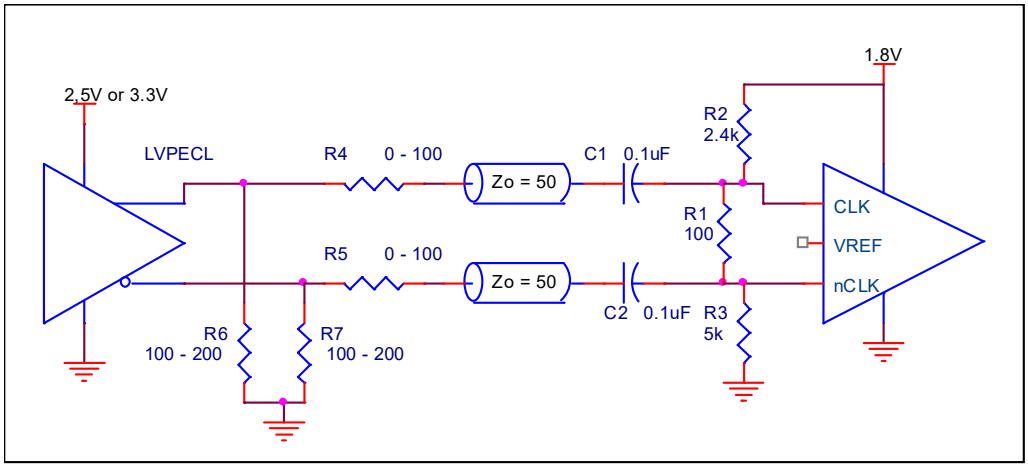


Figure 7. Differential Input Driven by an LVPECL Driver – AC Coupling



LVDS Driver Termination

For a general LVDS interface, the recommended value for the termination impedance (Z_T) is between 90Ω and 132Ω. The actual value should be selected to match the differential impedance (Z_0) of your transmission line. A typical point-to-point LVDS design uses a 100Ω parallel resistor at the receiver and a 100Ω differential transmission-line environment. In order to avoid any transmission-line reflection issues, the components should be surface mounted and must be placed as close to the receiver as possible. Renesas offers a full line of LVDS compliant devices with two types of output structures: current source and voltage source.

The standard termination schematic as shown in Figure 8 can be used with either type of output structure. Figure 9, which can also be used with both output types, is an optional termination with center tap capacitance to help filter common mode noise. The capacitor value should be approximately 50pF. If using a non-standard termination, it is recommended to contact Renesas and confirm if the output structure is current source or voltage source type. In addition, since these outputs are LVDS compatible, the input receiver's amplitude and common-mode input range should be verified for compatibility with the output.

Figure 8. Standard LVDS Termination

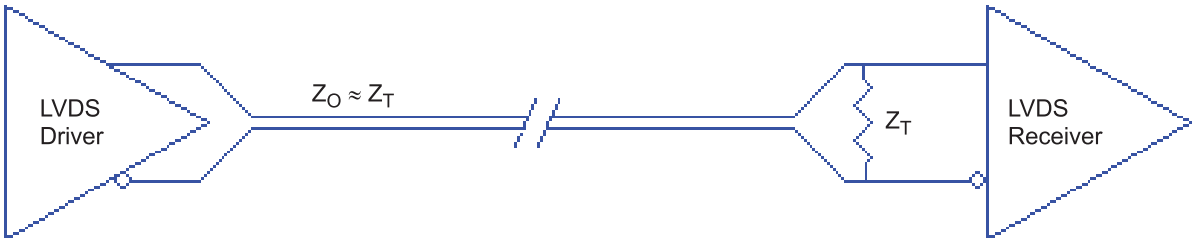
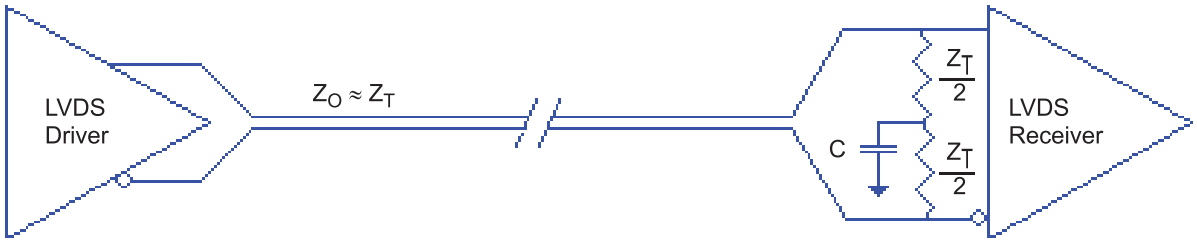


Figure 9. Optional LVDS Termination



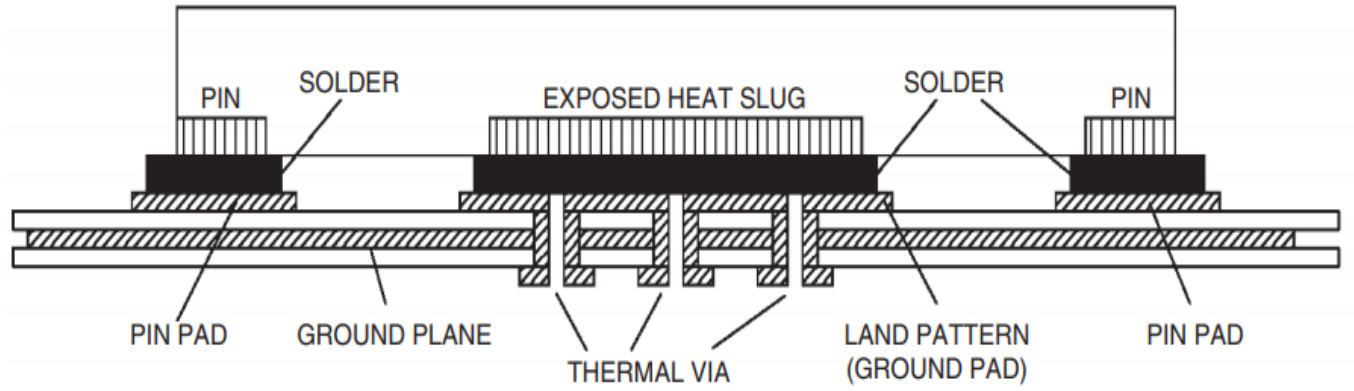
VFQFPN EPAD Thermal Release Path

In order to maximize both the removal of heat from the package and the electrical performance, a land pattern must be incorporated on the Printed Circuit Board (PCB) within the footprint of the package corresponding to the exposed metal pad or exposed heat slug on the package, as shown in Figure 10. The solderable area on the PCB, as defined by the solder mask, should be at least the same size/shape as the exposed pad/slug area on the package to maximize the thermal/electrical performance. Sufficient clearance should be designed on the PCB between the outer edges of the land pattern and the inner edges of pad pattern for the leads to avoid any shorts.

While the land pattern on the PCB provides a means of heat transfer and electrical grounding from the package to the board through a solder joint, thermal vias are necessary to effectively conduct from the surface of the PCB to the ground plane(s). The land pattern must be connected to ground through these vias. The vias act as “heat pipes”. The number of vias (i.e. “heat pipes”) are application specific and dependent upon the package power dissipation as well as electrical conductivity requirements. Thus, thermal and electrical analysis and/or testing are recommended to determine the minimum number needed. Maximum thermal and electrical performance is achieved when an array of vias is incorporated in the land pattern.

It is recommended to use as many vias connected to ground as possible. It is also recommended that the via diameter should be 12 to 13mils (0.30 to 0.33mm) with 1oz copper via barrel plating. This is desirable to avoid any solder wicking inside the via during the soldering process which may result in voids in solder between the exposed pad/slug and the thermal land. Precautions should be taken to eliminate any solder voids between the exposed heat slug and the land pattern. Note: These recommendations are to be used as a guideline only. For further information, please refer to the application note on the *Surface Mount Assembly of Amkor’s Thermally/ Electrically Enhance Leadframe Base Package, Amkor Technology.*

Figure 10. P.C. Assembly for Exposed Pad Thermal Release Path – Side View (Drawing not to Scale)



Case Temperature Considerations for VFQFPN Package

This device supports applications in a natural convection environment which does not have any thermal conductivity through ambient air. The printed circuit board (PCB) is typically in a sealed enclosure without any natural or forced air flow and is kept at or below a specific temperature. The device package design incorporates an exposed pad (ePad) with enhanced thermal parameters which is soldered to the PCB where most of the heat escapes from the bottom exposed pad. For this type of application, it is recommended to use the junction-to-board thermal characterization parameter Ψ_{JB} (Psi-JB) to calculate the junction temperature (T_J) and ensure it does not exceed the maximum allowed junction temperature in Absolute Maximum Ratings.

The junction-to-board thermal characterization parameter, $\Psi_{JB,}$ is calculated using the following equation:

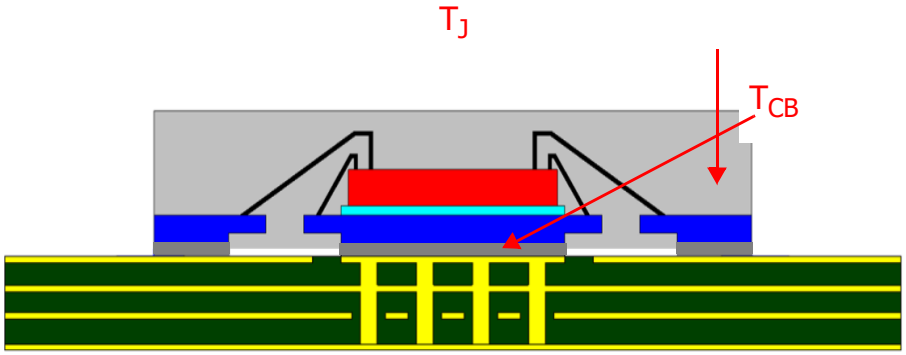
$T_J = T_{CB} + \Psi_{JB} \times P_{D,}$ where

T_J = Junction temperature at steady state condition in (^oC).

T_{CB} = Case temperature (Bottom) at steady state condition in (^oC).

Ψ_{JB} = Thermal characterization parameter to report the difference between junction temperature and the temperature of the board measured at the top surface of the board.

P_D = Power dissipation (W) in desired operating configuration.



The ePad provides a low thermal resistance path for heat transfer to the PCB and represents the key pathway to transfer heat away from the IC to the PCB. It's critical that the connection of the exposed pad to the PCB is properly constructed to maintain the desired IC case temperature (T_{CB}). A good connection ensures that temperature at the exposed pad (T_{CB}) and the board temperature (T_B) are relatively the same. An improper connection can lead to increased junction temperature, increased power consumption and decreased electrical performance. In addition, there could be long-term reliability issues and increased failure rate.

Example Calculation for Junction Temperature (T_J): $T_J = T_{CB} + \Psi_{JB} \times P_D$

Package type	40-VFQFPN
Body size (mm)	6 x 6 x 0.9
ePad size (mm)	4.65 x 4.65
Thermal Via	4 x 4 Matrix
Ψ_{JB}	1.5^{o}C/W
T_{CB}	105^{o}C
P_D	0.71W
VDDx	1.89V

For the variables above, the junction temperature is equal to 106.1^{o}C. Since this is below the maximum junction temperature of 125^{o}C, there are no long term reliability concerns. In addition, since the junction temperature at which the device was characterized using forced convection is 115^{o}C, this device can function without the degradation of the specified AC or DC parameters.

Case Temperature Considerations for WL-CSP Package

This device supports applications in a natural convection environment which does not have any thermal conductivity through ambient air. The printed circuit board (PCB) is typically in a sealed enclosure without any natural or forced air flow and is kept at or below a specific temperature. For this type of application, it is recommended to use the junction-to-board thermal characterization parameter, θ_{JB}, to calculate the junction temperature (T_J) and ensure it does not exceed the maximum allowed junction temperature in Absolute Maximum Ratings.

The junction-to-board thermal characterization parameter, θ_{JB}, is calculated as follows:

$T_J = T_{CB} + \theta_{JB} \times P_D$, where

T_J = Junction temperature at steady state condition in (^oC).

T_{CB} = Case temperature (Bottom) at steady state condition in (^oC).

θ_{JB} = Junction-to-board thermal characterization parameter.

P_D = Power dissipation (W) in desired operating configuration.

Example calculation for junction temperature (T_J): $T_J = T_{CB} + \theta_{JB} \times P_D$

Package type	48-WL-CSP
Body size (mm)	3.59 x 3.04 x 0.6
θ_{JB}	5.86^{o}C/W
T_{CB}	105^{o}C
P_{D_IMAX}	1.0935W
VDDx	2.7V

For the variables above, the junction temperature is equal to 111.41^{o}C. Since this is below the maximum junction temperature of 125^{o}C, there are no long term reliability concerns. In addition, since the junction temperature at which the device was characterized using forced convection is 115^{o}C, this device can function without the degradation of the specified AC or DC parameters.

Power Considerations

This section provides information on power dissipation and junction temperature for the 8P34S2106. Equations and example calculations are also provided.

1. **Power Dissipation.**

The following is the power dissipation for V_{DD} = 1.8V + 5% = 1.89V, which gives worst case results.

Maximum current at 85°C: V_{DD_MAX} = 1.89V: I_{DD_MAX} = 390mA

Maximum current at 85°C, V_{DD_MAX} = 2.7V: I_{DD_MAX} = 405mA

$Power_{_MAX} = V_{DD_MAX} * I_{DD_MAX}$ = 1.89V * 390mA = **737.1mW**

$Power_{_MAX} = V_{DD_MAX} * I_{DD_MAX}$ = 2.7V * 405mA = **1,093.5mW**

2. Junction Temperature.

Junction temperature, Tj, is the temperature at the junction of the bond wire and bond pad directly affects the reliability of the device. The maximum recommended junction temperature is 125°C. Limiting the internal transistor junction temperature, Tj, to 125°C ensures that the bond wire and bond pad temperature remains below 125°C.

The equation for Tj is as follows: $Tj = \theta_{JA} * Pd_total + T_A$

Tj = Junction Temperature

θ_{JA} = Junction-to-Ambient Thermal Resistance

Pd_total = Total Device Power Dissipation (example calculation is in section 1 above)

T_A = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance θ_{JA} must be used. Assuming no air flow and a multi-layer board, the appropriate value is 24.6°C/W per Table 13.

Therefore, Tj for an ambient temperature of 85°C with all outputs switching is:

85°C + 0.7371W * 24.6°C/W = 103.2°C. This is below the limit of 125°C. (40-VFQFPN package, VDDx = 1.89V)

85°C + 1.0935W * 24.6°C/W = 112°C. This is below the limit of 125°C. (40-VFQFPN package, VDDx = 2.7V)

85°C + 0.7371W * 32.32°C/W = 108.9°C. This is below the limit of 125°C. (48-WL-CSP package, VDDx = 1.89V)

85°C + 1.0935W * 32.32°C/W = 120.4°C. This is below the limit of 125°C. (48-WL-CSP package, VDDx = 2.7V)

This calculation is only an example. Tj will obviously vary depending on the number of loaded outputs, supply voltage, air flow and the type of board (multi-layer).

Table 13. Thermal Resistance θ_{JA}, Forced Convection

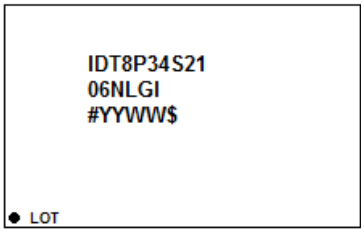
θ_{JA} (°C/W) vs. Air Flow (m/s)			
Meters per Second	**0**	**1**	**2**
40-VFQFPN Multi-Layer PCB, JEDEC Standard Test Boards	24.6	21.2	19.6
48-WL-CSP Multi-Layer PCB, JEDEC Standard Test Boards	32.32	28.35	26.05

Package Outline Drawings

The package outline drawings are located at the end of this document and are accessible from the Renesas website. The package information is the most current data available and is subject to change without revision of this document.

Marking Diagram

40-VFQFPN Package



- Line 1 and line 2 indicates the part number.
- Line 3:
  - "#" indicates stepping.
  - "YYWW" indicates the date code (YY are the last two digits of the year, and "WW" is a work week number that the part was assembled.
  - "$" indicates the mark code.

48-WL-CSP Package

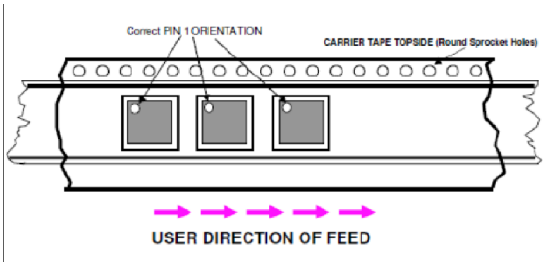
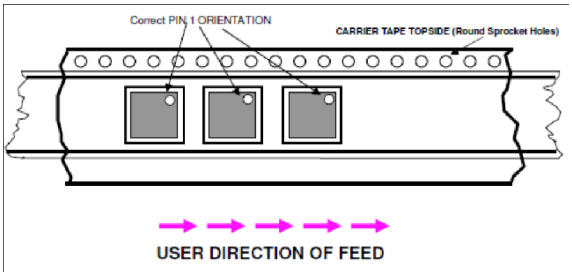


- Line 1 and line 2 indicates the part number.
- Line 3:
  - "#" indicates stepping.
  - "YYWW" indicates the date code (YY are the last two digits of the year, and "WW" is a work week number that the part was assembled.
  - "$" indicates the mark code.

Ordering Information

Part/Order Number	Marking	Package	Shipping Packaging	Temperature
8P34S2106NLGI	IDT8P34S2106NLGI	40-VFQFPN, 6 x 6 x 0.9mm	Tray	-40°C to 85°C
8P34S2106NLGI8	IDT8P34S2106NLGI		Tape & Reel, Pin 1 Orientation: EIA-481-C	
8P34S2106NLGI/W	IDT8P34S2106NLGI		Tape & Reel, Pin 1 Orientation: EIA-481-D/E	
8P34S2106AHGI	IDT8P34S2106AHGI	48-WL-CSP, 3.59 x 3.04 x 0.6mm	Tray	-40°C to 105°C
8P34S2106AHGI8	IDT8P34S2106AHGI8		Tape & Reel, Pin 1 Orientation: EIA-481-D/E	

Table 14. Pin 1 Orientation in Tape and Reel Packaging

Part Number Suffix	Pin 1 Orientation	Illustration
8	Quadrant 1 (EIA-481-C)	
/W	Quadrant 2 (EIA-481-D/E)	

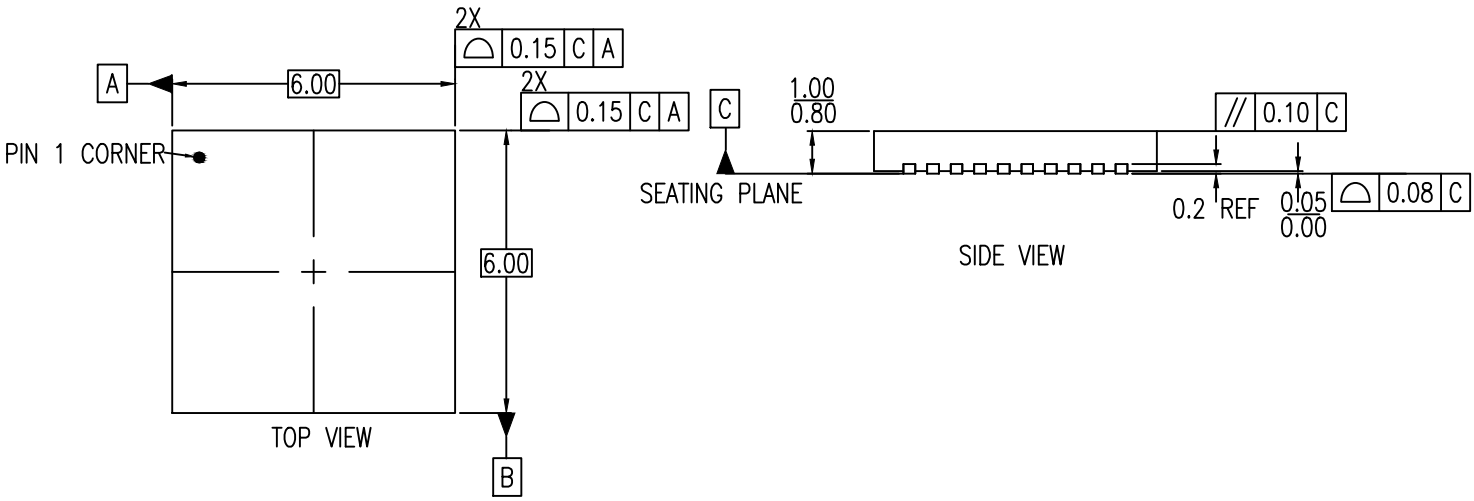
Revision History

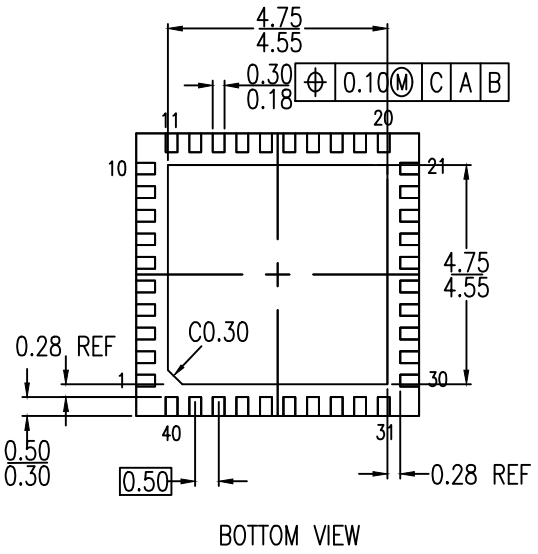
Revision Date	Description of Change
November 9, 2021	Updated Table 12.
May 10, 2021	▪ Updated V_{OD} in Table 12
September 8, 2020	▪ Updated the section Wiring the Differential Input to Accept Single-Ended Levels. ▪ Updated Figures 4, 6 and 7. ▪ Reformatted document template.
January 11, 2019	▪ Updated Package Outline Drawings; however, no mechanical changes ▪ Updated the supported temperature ranges in Ordering Information
July 5, 2017	Added information about the 48-WL-CSP package option.
October 20, 2016	▪ Page 1, Features, added Device current consumption ▪ Page 9, added Additive Phase Jitter ▪ Page 19, added Marking Diagram ▪ Updated datasheet formatting
July 28, 2016	Features Section: corrected phase jitter bullet spec from < 50fs to 45fs.
July 8, 2016	Initial release.

40-VFQFPN Package Outline Drawing

6.0 x 6.0 x 0.9 mm, 0.5mm Pitch, 4.65 x 4.65 mm Epad

NL/NLG40P2, PSC-4115-02, Rev 02, Page 1

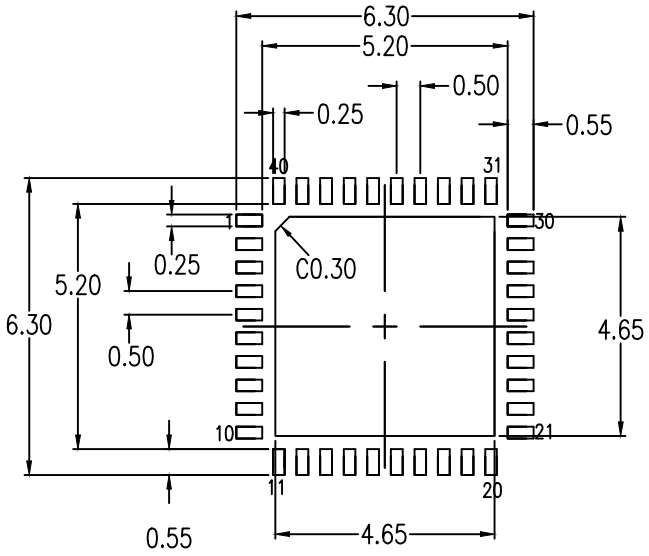




NOTES:

1. ALL DIMENSIONS ARE IN MM. ANGLES IN DEGREES

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BOTTOM VIEW

RECOMMENDED LAND PATTERN DIMENSION

NOTES:
1. ALL DIMENSIONS ARE IN MM. ANGLES IN DEGREES
2. TOP DOWN VIEW–AS VIEWED ON PCB
3. LAND PATTERN RECOMMENDATION IS PER IPC–7351B GENERIC REQUIREMENT FOR SURFACE MOUNT DESIGN AND LAND PATTERN

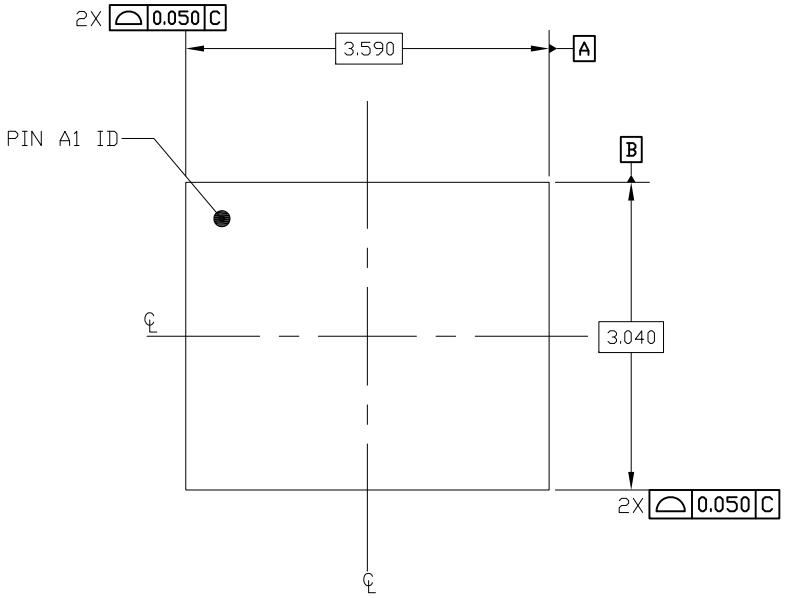
Package Revision History		
Date Created	Rev No.	Description
Jan 22, 2018	Rev 02	Change QFN to VFQFPN
June 1, 2016	Rev 01	Add Chamfer on Epad

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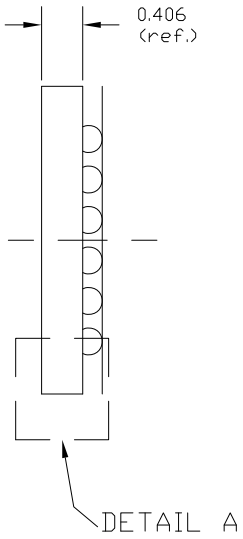
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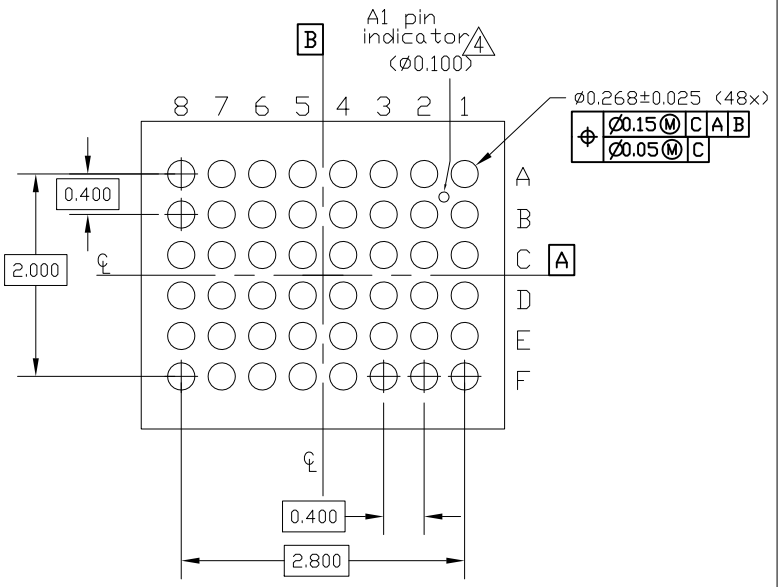
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2. ALL DIMENSIONS ARE IN MILLIMETERS.
3. SEATING PLANE AND PRIMARY DATUM –C– ARE DEFINED BY THE CONTACT POINTS OF THREE OR MORE SOLDER BALLS THAT SUPPORT THE DEVICE WHEN PLACED ON A TOP OF A PLANAR SURFACE.
4. BOTTOM PIN#1 INDICATOR OPTIONAL.

DATE CREATED	REVISIONS HISTORY		
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NOTE: REFER TO DCP FOR OFFICIAL RELEASE DATE			

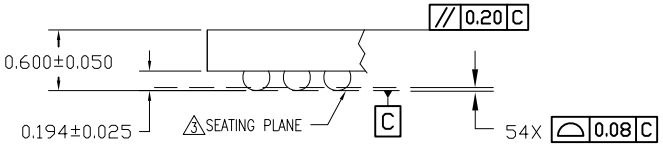


TOP VIEW





BOTTOM VIEW



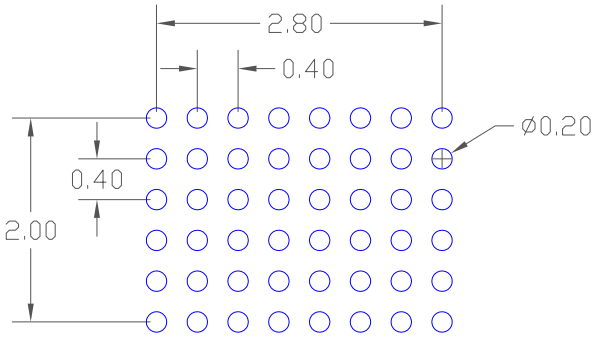
DETAIL A
(ROTATED 90 DEG CW)

TOLERANCES UNLESS OTHERWISE SPECIFIED
DECIMAL :
.X ±
.XX ±
.XXX ±
ANGLE : ±
ANGULAR : ±

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SIZE	DRAWING No.	REV
C	PSC–4669	00
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DATE CREATED	REVISIONS HISTORY		
	REV	DESCRIPTION	AUTHOR
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2. TOP DOWN VIEW, AS VIEW ON PCB.
3. NSMD LAND PATTERN ASSUMED.
4. LAND PATTERN RECOMMENDATION AS PER IPC-7351
   GENERIC REQUIREMENT FOR SURFACE MOUNT DESIGN AND LAND PATTERN.

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(Rev.1.0 Mar 2020)

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