## Description

The device is intended to take 1 or 2 reference clocks, select between them, using a pin or register selection and generate up to 8 outputs that may be the same as the reference frequency or integer-divider versions of it.

The 8P79818 supports two output banks, each with its own divider and power supply. All outputs in one bank would generate the same output frequency, but each output can be individually controlled for output type, output enable or even powered-off.

The device supports a serial port for configuration of the parameters while in operation. The serial port can be selected to use the $I^2C$ or SPI protocol. After power-up, all outputs will come up in LVDS mode and may be programmed to other configurations over the serial port. Outputs may be enabled or disabled under control of the OE input pin.

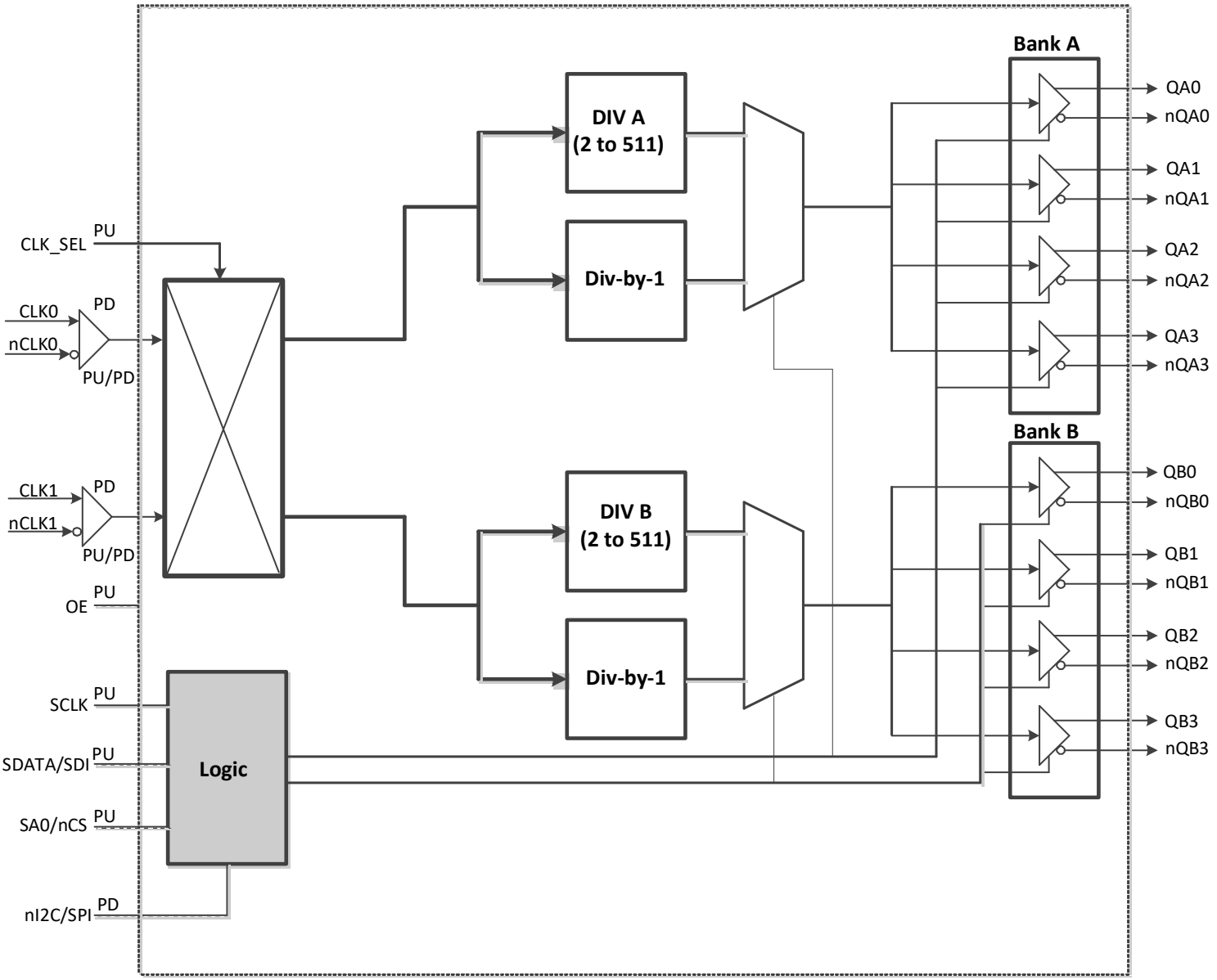
The device can operate over the -40°C to +85°C temperature range.

## Features

- Two differential inputs support LVPECL, LVDS, HCSL or LVCMOS reference clocks
  - Accepts input frequencies ranging from 1PPS (1Hz) to 700MHz
- Select which of the two input clocks is to be used as the reference clock for which divider via pin or register selection
  - Switchover will not generate any runt clock pulses on the output
- Generates eight differential outputs
  or eight LVCMOS outputs, Bank A only
  - Differential outputs selectable as LVPECL, LVDS, CML or HCSL
  - Differential outputs support frequencies from 1PPS to 700MHz
  - LVCMOS outputs support frequencies from 1PPS to 200MHz
  - LVCMOS outputs in the same pair may be inverted or in-phase relative to one another
- Outputs arranged in 2 banks of 4 outputs each
  - Each bank supports a separate power supply of 3.3V, 2.5V or 1.8V
  - 1.5V output voltage is also supported for LVCMOS, Bank A only
  - One divider per output bank, supporting divide ratios of 2...511 or divider bypass
- Output enable control pin
  - Output enable or disable will not cause any runt pulses
- Register programmable via $I^2C$ / SPI serial port
  - Individual output enables, output type selection and output power-down control bits supported
  - Input mux selection control bit
- Core voltage supply of 3.3V, 2.5V or 1.8V
- -40°C to +85°C ambient operating temperature
- Lead-free (RoHS 6) packaging

# Block Diagram

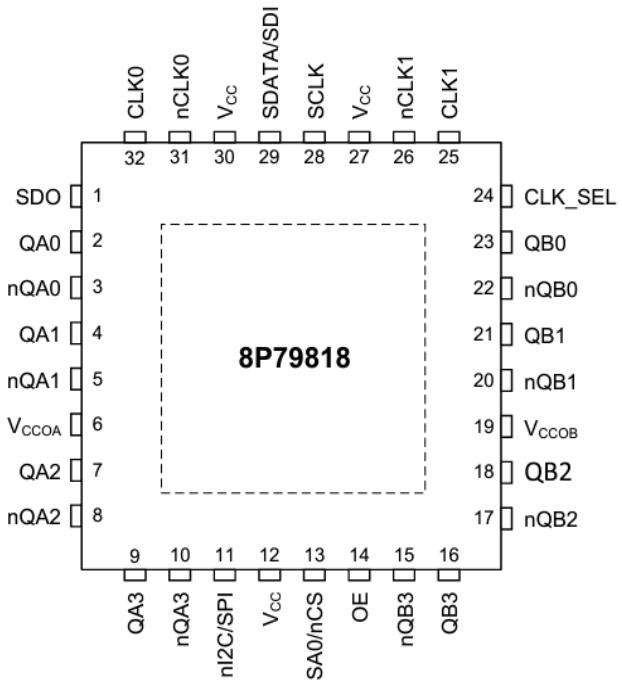
**Figure 1: Block Diagram**




8P79818 transistor count: 33,394

# Pin Assignment

**Figure 2: Pin Assignments for 5mm x 5mm 32-Lead VFQFN Package (Top View)**




# Pin Description and Characteristic Tables

**Table 1: Pin Description**

| Number | Name | Type[a] | Description |
|---|---|---|---|
| 1 | SDO | Output | SPI mode data output signal. Unused in I²C mode. |
| 2 | QA0 | Output | Positive differential clock output. Included in Bank A. Refer to Output Drivers section for details. |
| 3 | nQA0 | Output | Negative differential clock output. Included in Bank A. Refer to Output Drivers section for details. |
| 4 | QA1 | Output | Positive differential clock output. Included in Bank A. Refer to Output Drivers section for details. |
| 5 | nQA1 | Output | Negative differential clock output. Included in Bank A. Refer to Output Drivers section for details. |
| 6 | $V_{CCOA}$ | Power | Output supply for output Bank A. |
| 7 | QA2 | Output | Positive differential clock output. Included in Bank A. Refer to Output Drivers section for details. |
| 8 | nQA2 | Output | Negative differential clock output. Included in Bank A. Refer to Output Drivers section for details. |
| 9 | QA3 | Output | Positive differential clock output. Included in Bank A. Refer to Output Drivers section for details. |
| 10 | nQA3 | Output | Negative differential clock output. Included in Bank A. Refer to Output Drivers section for details. |
| 11 | nI2C/SPI | Input (PD) | Select protocol for serial port:<br>0 = I²C mode<br>1 = SPI mode |
| 12 | $V_{CC}$ | Power | Core logic supply. |
| 13 | SA0/nCS | Input (PU) | SPI chip select input (active low) in SPI mode. Base address bit 0 in I²C mode. |

**Table 1: Pin Description (Cont.)**

| | | | |
|---|---|---|---|
| 14 | OE | Input (PU) | Master output enable control<br>0 = All outputs high-impedance[b]<br>1 = All outputs enabled or disabled under control of register bits |
| 15 | nQB3 | Output | Negative differential clock output. Included in Bank B. Refer to Output Drivers section for details. |
| 16 | QB3 | Output | Positive differential clock output. Included in Bank B. Refer to Output Drivers section for details. |
| 17 | nQB2 | Output | Negative differential clock output. Included in Bank B. Refer to Output Drivers section for details. |
| 18 | QB2 | Output | Positive differential clock output. Included in Bank B. Refer to Output Drivers section for details. |
| 19 | $V_{CCOB}$ | Power | Output supply for output Bank B. |
| 20 | nQB1 | Output | Negative differential clock output. Included in Bank B. Refer to Output Drivers section for details. |
| 21 | QB1 | Output | Positive differential clock output. Included in Bank B. Refer to Output Drivers section for details. |
| 22 | nQB0 | Output | Negative differential clock output. Included in Bank B. Refer to Output Drivers section for details. |
| 23 | QB0 | Output | Positive differential clock output. Included in Bank B. Refer to Output Drivers section for details. |
| 24 | CLK_SEL | Input (PU) | Input clock selection control pin. This pin may be disabled by register control, but if enabled (default) its function is:[c]<br>0 = CLK0 is selected<br>1 = CLK1 is selected |
| 25 | CLK1 | Input (PD) | Non-inverting differential clock input. |
| 26 | nCLK1 | Input (PU/ PD) | Inverting differential clock input. $V_{CC}/2$ when left floating (set by the internal pull-up and pull-down resistors). |
| 27 | $V_{CC}$ | Power | Core logic supply. |
| 28 | SCLK | Input (PU) | Serial port input clock for either SPI or $I^2C$ mode. |
| 29 | SDATA/<br>SDI | Input/Output (PU)<br>Input (PU) | In $I^2C$ mode, this is the bi-directional data signal for the serial port<br>In SPI mode, this is the data input signal. |
| 30 | $V_{CC}$ | Power | Core logic supply. |
| 31 | nCLK0 | Input (PU/ PD) | Inverting differential clock input. $V_{CC}/2$ when left floating (set by the internal pull-up and pull-down resistors). |
| 32 | CLK0 | Input (PD) | Non-inverting differential clock input. |
| EP | $V_{EE}$ | Ground | Must be connected to ground (GND). |

a. Pull-up (PU) and pull-down (PD) resistors are indicated in parentheses. *Pullup* and *Pulldown* refer to internal input resistors. See Table 10, *DC Input/ Output Characteristics,* for typical values.

b. After power up, the selected CLK input need to be active with up to 10 pulses before output is held at high-impedance.

c. After input reference clock switch, up to two clock pulses may be missed.

# Principles of Operation

## Input Selection

The 8P79818 supports two input references: CLK0 and CLK1 that may be driven with differential or single-ended clock signals. Either or both may be used as the source frequency for either output divider under control of the CLK_SEL input pin or under register control.

The CLK_SEL pin is the default selection mechanism and selects whether both dividers are driven by the CLK0, nCLK0 input (CLK_SEL = Low) or by the CLK1, nCLK1 input (CLK_SEL = High).

If the user enables register control via the SEL_REG control bit, then there are 4 selection options available as shown in Table 2.

**Table 2: Input Selection Register Control (SEL_REG = 1)**

| CLK_SEL [1:0] | | Description |
|---|---|---|
| 0 | 0 | Divider A & B both driven from CLK0 |
| 0 | 1 | Divider A driven from CLK1 & Divider B driven from CLK0 |
| 1 | 0 | Divider A driven from CLK0 & Divider B driven from CLK1 |
| 1 | 1 | Divider A & B both driven from CLK1 |

## Output Dividers

Each bank of outputs has its own divider. All outputs in the same bank will be driven by that divider and so will all have the same frequency. Divider A supplies the QA output bank and Divider B supplies the QB output bank. Each divider is capable of being driven by the same or a different input frequency. Each divider can pass that input frequency directly to the outputs or to divide it by any integer from 2 up to 511.

## Output Drivers

The QA[0:3] and QB[0:3] clock outputs are provided with register-controlled output drivers. By selecting the output drive type in the appropriate register, any of these outputs can support LVCMOS, LVPECL, CML, HCSL or LVDS logic levels.

CML operation supports both a 400mV peak-peak swing and an 800mV peak-peak swing selection.

The operating voltage ranges of each output bank is determined by its independent output power pin ($V_{CCOA}$ or $V_{CCOB}$). Output voltage levels of 1.8V, 2.5V or 3.3V are supported for differential operation and LVCMOS operation. In addition, LVCMOS output operation supports 1.5V $V_{CCO}$.

A global OE input pin is provided. If the OE pin is negated (Low), then all outputs will be in a high-impedance state. If the OE pin is asserted (High), then each output will behave as indicated by its individual register enable bit. Using the global OE pin to enable or disable outputs will not result in any ‘runt’ clock pulses on the outputs.

Each output bank may be enabled or disabled using the SYNC_DISx register bit. Using these bits to enable or disable outputs will not result in any ‘runt’ clock pulses on the outputs.

Individual outputs within a bank may be enabled or disabled using the DIS_Qxm register bits. These bits however may result in ‘runt’ pulses on the outputs if the output is otherwise enabled, so it is recommended that the entire bank be disabled via the appropriate SYNC_DISx register bit while an individual output is being enabled using the DIS_Qxm bit to avoid a possible ‘runt’ pulse on the output. If ‘runt’ pulses are not a concern, then the DIS_Qxm bits may be used directly.

### LVCMOS Operation

When a given output is configured to provide LVCMOS levels, then both the Q and nQ outputs will toggle at the selected output frequency. All the previously described configuration and control apply equally to both outputs. Frequency, voltage levels and enable / disable status apply to both the Q and nQ pins.

When configured as LVCMOS, the Q & nQ outputs can be selected to be phase-aligned with each other or inverted relative to one another. Phase-aligned outputs will have increased simultaneous switching currents which can negatively affect phase noise performance and power consumption. It is recommended that use of this selection be kept to a minimum.

### Power-Saving Modes

To allow the device to consume the least power possible for a given application, the following functions are included under register control:

- Any unused output can be individually powered-off.
- If either bank is completely unused, all logic, including the dividers for that bank may be completely powered-off.
- Clock gating on logic that is not being used.

### Device Start-up Behavior

The device will power-up with all outputs enabled in LVDS mode and all dividers bypassed.

## Serial Control Port Description

### Serial Control Port Configuration Description

The device has a serial control port capable of responding as a slave in an $I^2C$ or SPI compatible configuration, to allow access to any of the internal registers for device programming or examination of internal status. All registers are configured to have default values. See the specifics for each register for details. Selection of $I^2C$ versus SPI protocol will be done via the nI2C/SPI input pin.

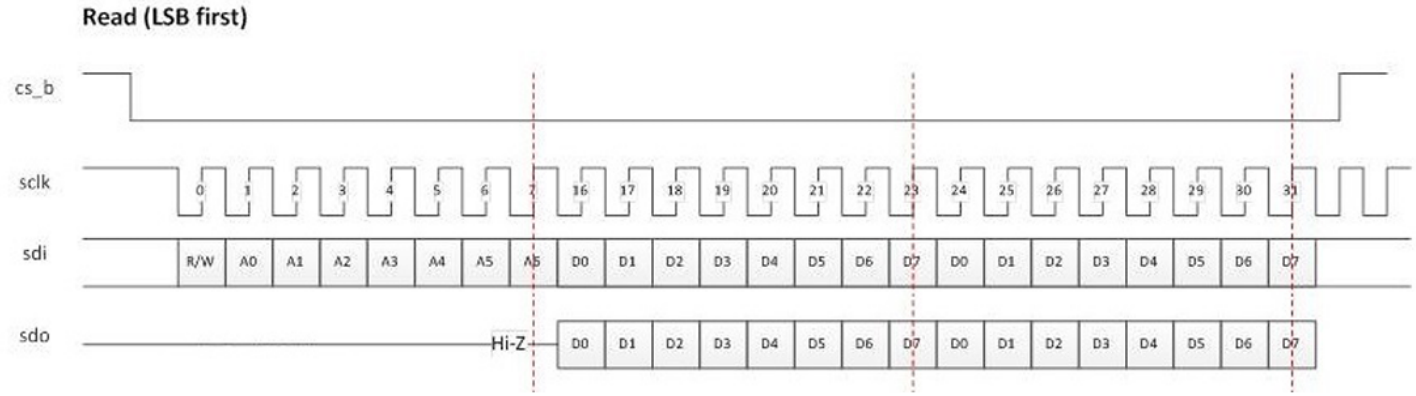
### SPI Mode Operation

SPI mode can be enabled via pin selection from power-up. The following information assumes SPI mode has been selected.

In a read operation (R/W bit is '1'), data on SDO will be clocked out on the falling edge of SCLK.

In a write operation (R/W bit is '0'), data on SDI will be clocked in on the rising edge of SCLK.

**Figure 3: SPI Read Sequencing Diagram**



During SPI Write operations, the user may continue to hold nCS low and provide further bytes of data for up to a total of 16 bytes in a single block write. Data is written directly into the appropriate register as it is received.

**Figure 4: SPI Write Sequencing Diagram**

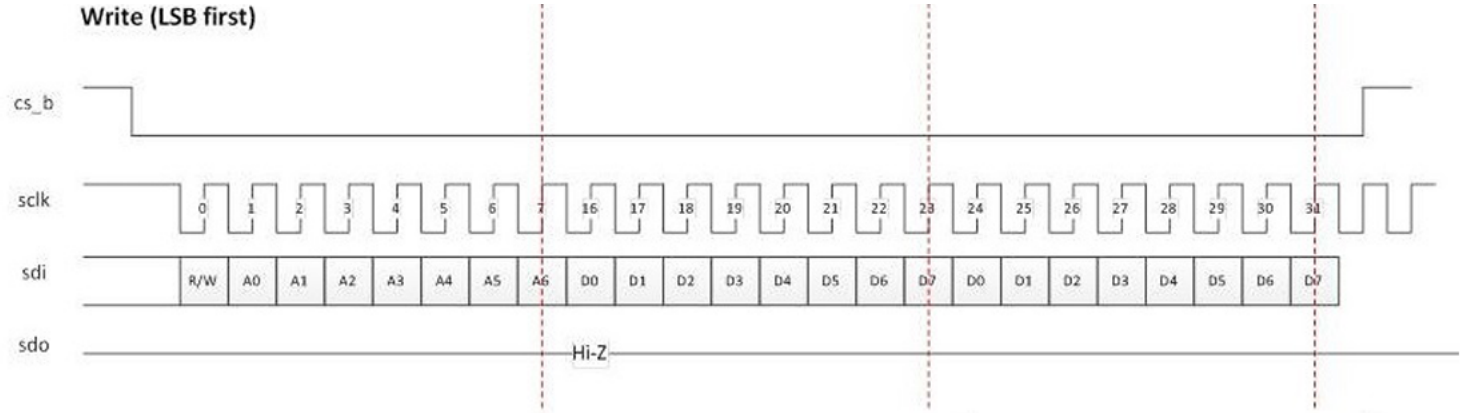



**Figure 5: SPI Read/Write Timing Diagram**

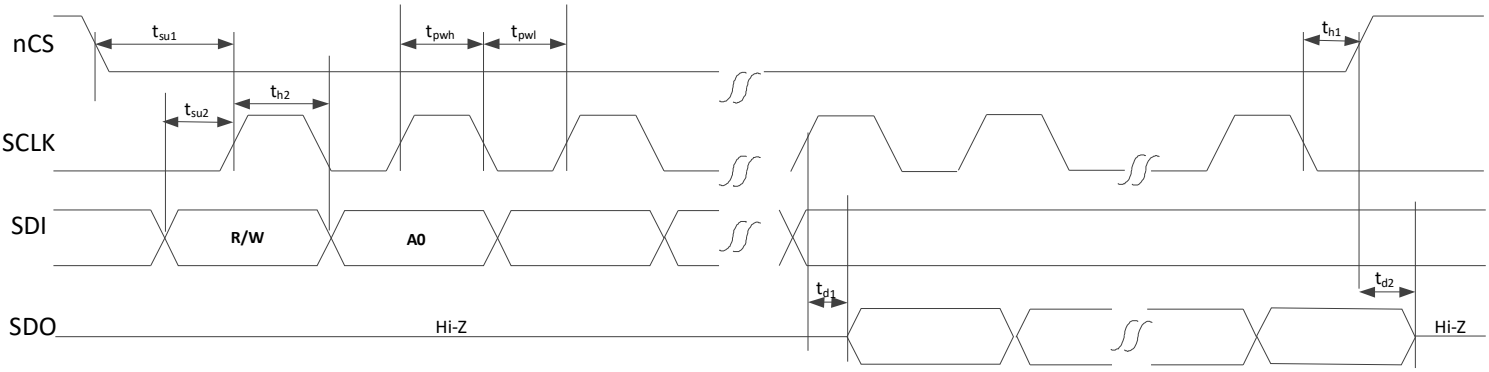



**Table 3: Timing Characteristics in SPI Mode[a]**

| Symbol | Parameter | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| $t_{pw}$ | SCLK Period | 20 | | | ns |
| $t_{pw1}$ | SCLK Pulse Width Low | 8 | | | ns |
| $t_{pw2}$ | SCLK Pulse Width High | 8 | | | ns |
| $t_{su1}$ | Valid nCS to SCLK Rising Setup Time | 10 | | | ns |
| $t_{h1}$ | Valid nCS After Valid SCLK Hold Time (CLKE = 0/1) | 10 | | | ns |
| $t_{su2}$ | Valid SDI to SCLK Rising Setup Time | 5 | | | ns |
| $t_{h2}$ | Valid SDI after valid SCLK Hold Time | 5 | | | ns |
| $t_{d1}$ | SCLK falling (rising in CLKE = 1 case) to Valid Data Delay Time | | | 5 | ns |
| $t_{d2}$ | nCS rising edge to SDO High Impedance Delay Time | | | 10 | ns |
| $t_{csh}$ | Time between Consecutive Read-Read or Read-Write Accesses (nCS rising edge to nCS falling edge) | 20 | | | ns |

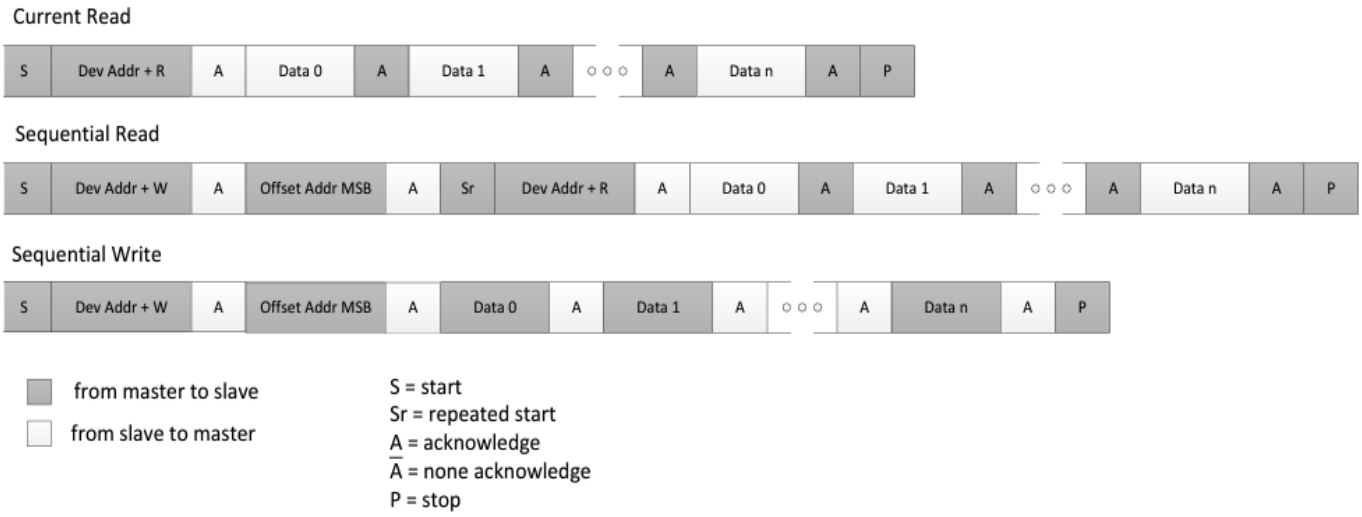
a. Specifications guaranteed by design and characterization.

# I²C Mode Operation

The I²C interface is designed to fully support v1.0 of the I²C specification for *normal* and *fast* mode operation. The device acts as a slave device on the I²C bus at 100kHz or 400kHz using an address of 110110x (binary), where the value of 'x' is set by the SA0/nCS input pin. The interface accepts byte-oriented block write and block read operations. One address byte specifies the register address of the byte position of the first register to write or read. Data bytes (registers) are accessed in sequential order from the lowest to the highest byte (most significant bit first). Read and write block transfers can be stopped after any complete byte transfer. During a write operation, data will be written to the registers directly as each byte is received.

For full electrical I²C compliance, it is recommended to use external pull-up resistors for SDATA and SCLK. The internal pull-up resistors have a size of 51kΩ typical.

**Figure 6: Slave Read and Write Cycle Sequencing**




# Register Descriptions

**Table 4: Register Blocks**

| Register Ranges Offset (Hex) | Register Block Description |
|---|---|
| 0 – 1 | Device control |
| 2 – 5 | Bank A control |
| 6 – 9 | Bank B control |
| A – B | Reserved |
| C – F | Divide ratios |

**Table 5: Device Control Register Bit Field Locations**

| Address (Hex) | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|
| 0 | CLKMODE | CLK_SEL[1:0] | | SEL_REG | Rsvd | Rsvd | Rsvd | DIV_SYNC |
| 1 | BKA_Vx | BKB_Vx | SYNC_DISA | SYNC_DISB | PWR_DNA | PWR_DNB | DIS_DIVA | DIS_DIVB |

| Bit Field Name | Field Type | Default Value | Description |
|---|---|---|---|
| CLKMODE | R/W | 0b | Clock switchover mode selection:<br>0 = Forced clock switch (may result in glitches as clocks switch)<br>1 = Glitch-less clock switch (may remain on original clock source if that source is no longer toggling) |
| CLK_SEL[1:0] | R/W | 00b | Select which input clock is to be used as the reference clock. These bits are only in effect when SEL_REG = 1:<br>00 = CLK0, nCLK0 input drives both Divider A & Divider B<br>01 = CLK1, nCLK1 input drives Divider A & CLK0, nCLK0 drives Divider B<br>10 = CLK0, nCLK0 input drives Divider A & CLK1, nCLK1 drives Divider B<br>11 = CLK1, nCLK1 input drives both Divider A & Divider B |
| SEL_REG | R/W | 0b | Determines if input clock selection is to be performed by pin or register:<br>0 = CLK_SEL input pin controls reference selection mux<br>1 = CLK_SEL register bits controls reference selection mux |
| Rsvd | R/W | – | Reserved. Always write ‘0’ to this bit location. Read values are not defined. |
| DIV_SYNC | R/W | 0b | Divider synchronization control:<br>0 = Dividers running normally<br>1 = Dividers in reset (output clocks halted)<br>1–>0 transition on this bit will synchronize the Bank A & Bank B output dividers |
| BKA_Vx | R/W | 0b | Bank A voltage setting for optimal performance:<br>0 = $V_{CCOA}$ is 3.3V<br>1 = $V_{CCOA}$ is 2.5V,1.8V, and 1.5V |
| BKB_Vx | R/W | 0b | Bank B voltage setting for optimal performance:<br>0 = $V_{CCOB}$ is 3.3V<br>1 = $V_{CCOB}$ is 2.5V,1.8V |
| SYNC_DISA | R/W | 0b | Glitch-free output enable bit for Bank A outputs:<br>0 = Outputs in Bank A are enabled glitch-lessly as indicated by their individual DIS_QAm bits<br>1 = All outputs for Bank A are high-impedance |
| SYNC_DISB | R/W | 0b | Glitch-free output enable bit for Bank B outputs:<br>0 = Outputs in Bank B are enabled glitch-lessly as indicated by their individual DIS_QBm bits<br>1 = All outputs for Bank B are high-impedance |

| Bit Field Name | Field Type | Default Value | Description |
|---|---|---|---|
| PWR_DNA | R/W | 0b | Power-down control for Bank A outputs:<br>0 = All outputs for Bank A are powered (SYNC_DISA should be 1 when powering-up the bank to prevent glitches on the output)<br>1 = All outputs in Bank A are powered-off |
| PWR_DNB | R/W | 0b | Power-down control for Bank B outputs:<br>0 = All outputs for Bank B are powered (SYNC_DISB should be 1 when powering-up the bank to prevent glitches on the output)<br>1 = All outputs in Bank B are powered-off |
| DIS_DIVA | R/W | 0b | Power-down output divider for Bank A (DIVA must be set to 000h to bypass):<br>0 = Output divider for Bank A is powered<br>1 = Output divider for Bank A is powered-down |
| DIS_DIVB | R/W | 0b | Power-down output divider for Bank B (DIVB must be set to 000h to bypass):<br>0 = Output divider for Bank B is powered<br>1 = Output divider for Bank B is powered-down |

**Table 6: Bank A Control Register Bit Field Locations**

| Address (Hex) | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|
| 2 | Rsvd | | | TERM_A | QA_POL3 | QA_POL2 | QA_POL1 | QA_POL0 |
| 3 | Rsvd | | MODE_QA3[2:0] | | | MODE_QA2[2:0] | | |
| 4 | Rsvd | | MODE_QA1[2:0] | | | MODE_QA0[2:0] | | |
| 5 | DIS_QA3 | DIS_QA2 | DIS_QA1 | DIS_QA0 | Rsvd | | | |

| Bit Field Name | Field Type | Default Value | Description |
|---|---|---|---|
| TERM_A | R/W | 0b | Indicates termination used on Bank A outputs when HCSL mode is selected:<br>0 = 33Ω/ 50Ω<br>1 = 50Ω |
| QA_POLm | R/W | 0h | Output polarity selection for output pair nQAm, QAm in LVCMOS mode:<br>0 = nQAm pin is inverted relative to QAm pin when in LVCMOS mode<br>1 = nQAm and QAm pins are in-phase when in LVCMOS mode |
| MODE_QAm[2:0] | R/W | 010b | Output driver mode of operation for output pair QAm, nQAm:<br>000 = high-impedance<br>001 = LVPECL<br>010 = LVDS (default)<br>011 = LVCMOS<br>100 = HCSL<br>101 = CML 400mV swing<br>110 = CML 800mV swing<br>111 = Reserved |
| DIS_QAm | R/W | 0b | Disable output pair QAm, nQAm:<br>0 = Output pair QAm, nQAm is enabled (disable output bank using SYNC_DISA to prevent runt pulses when enabling)<br>1 = Output pair QAm, nQAm is powered-down |
| Rsvd | R/W | – | Reserved. Always write 0 to this bit location. Read values are not defined. |

**Table 7: Bank B Control Register Bit Field Locations**

| Address (Hex) | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|
| 6 | Rsvd | | | TERM_B | Rsvd | Rsvd | Rsvd | Rsvd |
| 7 | Rsvd | | MODE_QB3[2:0] | | | MODE_QB2[2:0] | | |
| 8 | Rsvd | | MODE_QB1[2:0] | | | MODE_QB0[2:0] | | |
| 9 | DIS_QB3 | DIS_QB2 | DIS_QB1 | DIS_QB0 | Rsvd | | | |

| Bit Field Name | Field Type | Default Value | Description |
|---|---|---|---|
| TERM_B | R/W | 0b | Indicates termination used on Bank B outputs when HCSL mode is selected:<br>0 = 33Ω/ 50Ω<br>1 = 50Ω |
| MODE_QBm[2:0] | R/W | 010b | Output driver mode of operation for output pair QBm, nQBm:<br>000 = high-impedance<br>001 = LVPECL<br>010 = LVDS (default)<br>011 = Rsvd<br>100 = HCSL<br>101 = CML 400mV swing<br>110 = CML 800mV swing<br>111 = Reserved |
| DIS_QBm | R/W | 0b | Disable output pair QBm, nQBm:<br>0 = Output pair QBm, nQBm is enabled (disable output bank using SYNC_DISB to prevent runt pulses when enabling)<br>1 = Output pair QBm, nQBm is powered-down |
| Rsvd | R/W | – | Reserved. Always write 0 to this bit location. Read values are not defined. |

**Table 8: Divide Ratio Register Field Locations**

| Address (Hex) | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|
| C | DIVA[7:0] | | | | | | | |
| D | DIVB[7:0] | | | | | | | |
| E | Rsvd | | | | | | DIVB[8] | DIVA[8] |
| F | Rsvd | | | | | | | |

| Bit Field Name | Field Type | Default Value | Description |
|---|---|---|---|
| DIVA[8:0] | R/W | 000h | Divider ratio for Bank A outputs:<br>00h – 01h = Bypass divider and pass reference clock directly to the Bank A outputs<br>02h – 1FFh = ratio to be used by the A divider is value written here. For example writing a 4 in this field will results in a divide ratio of 4 being used. |
| DIVB[8:0] | R/W | 000h | Divider ratio for Bank B outputs:<br>00h – 01h = Bypass divider and pass reference clock directly to the Bank B outputs<br>02h – 1FFh = ratio to be used by the B divider is value written here. For example writing a 4 in this field will results in a divide ratio of 4 being used. |
| Rsvd | R/W | – | Reserved. Always write 0 to this bit location. Read values are not defined. |

# Absolute Maximum Ratings

The absolute maximum ratings are stress ratings only. Stresses greater than those listed below can cause permanent damage to the device. Functional operation of the 8P79818 at absolute maximum ratings is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

**Table 9: Absolute Maximum Ratings**

| Item | Rating |
|---|---|
| Supply voltage, $V_{CCX}$[a] to GND | 3.6V |
| Inputs SCLK, SDATA/SDI, SA0/nCS, CLK_SEL, CLK0, nCLK0, CLK1, nCLK1, OE, nI2C/SPI | –0.5V to 3.6V |
| Outputs, $I_O$ QA[0:3], nQA[0:3], QB[0:3], nQB[0:3]<br>Continuous current<br>Surge current | <br>40mA<br>60mA |
| Outputs, $V_O$ QA[0:3], nQA[0:3], QB[0:3], nQB[0:3] | –0.5V to 3.6V |
| Outputs, $V_O$ SDO, SDATA/SDI | –0.5V to 3.6V |
| Operating junction temperature | 125°C |
| Storage temperature, $T_{STG}$ | –65°C to 150°C |
| Lead temperature (Soldering, 10s) | +260°C |

a. $V_{CCx}$ denotes $V_{CC}$, $V_{CCOA}$, or $V_{CCOB}$.

# DC Characteristics

### Table 10: DC Input/ Output Characteristics

| Symbol | Parameter | | | Test Conditions | Minimum | Typical | Maximum | Units |
|---|---|---|---|---|---|---|---|---|
| $C_{in}$ | Input capacitance | | | | | 0.5 | | pF |
| $C_{PD}$ | Power dissipation capacitance (per output) | LVPECL | QA[0:3], nQA[0:3] QB[0:3], nQB[0:3] | $V_{CCOX}$[a] = 3.465V or 2.625V | | 0.8 | | pF |
| | | LVDS | | | | 1.2 | | pF |
| | | CML 400mV | | | | 0.48 | | pF |
| | | CML 800mV | | | | 0.44 | | pF |
| | | LVCMOS | Bank A | $V_{CCOA}$ = 3.465V or 2.625V | | 2.33 | | pF |
| | | LVPECL | QA[0:3], nQA[0:3] QB[0:3], nQB[0:3] | $V_{CCOX}$ = 1.89V | | 1.4 | | pF |
| | | LVDS | | | | 1.5 | | pF |
| | | CML 400mV | | | | 0.53 | | pF |
| | | CML 800mV | | | | 0.3 | | pF |
| | | LVCMOS | Bank A | $V_{CCOA}$ = 1.89V or 1.575V | | 2.1 | | pF |
| $R_{PULLUP}$ | Input pull-up resistor | | | | | 51 | | kΩ |
| $R_{PULLDOWN}$ | Input pull-down resistor | | | | | 51 | | kΩ |
| $R_{OUT}$ | Output impedance | | QA[3:0], nQA[3:0] | LVCMOS output type selected $V_{CCOA}$ = 3.3V±5% | | 24 | | Ω |
| | | | | LVCMOS output type selected $V_{CCOA}$ = 2.5V±5% | | 15 | | Ω |
| | | | | LVCMOS output type selected $V_{CCOA}$ = 1.8V±5% | | 26 | | Ω |
| | | | | LVCMOS output type selected $V_{CCOA}$ = 1.5V±5% | | 46 | | Ω |

a. $V_{CCOx}$ denotes $V_{CCOA}$ and $V_{CCOB}$.

## Supply Voltage Characteristics ,

**Table 11: Power Supply Characteristics, $V_{CC}$ = 3.3V ±5%, $V_{EE}$ = 0V, $T_A$ = -40°C to +85°C[a], [b], [c]**

| Symbol | Parameter | Test Conditions | Minimum | Typical | Maximum | Units |
|---|---|---|---|---|---|---|
| $V_{CC}$ | Core supply voltage | | 3.135 | | 3.465 | V |
| $V_{CCOA}$, $V_{CCOB}$ | Output supply voltage | | 1.71 | | $V_{CC}$ | V |
| $I_{CC}$ | Core supply current | | | 23 | 26 | mA |
| $I_{CCOA}$ + $I_{CCOB}$ | Output supply current | DIV-by-1 | | 157 | 177 | mA |
| | | DIV A = DIV B = 2 | | 125 | 140 | mA |
| $I_{EE}$ | Power supply current | | | 183 | 206 | mA |

a. Internal dynamic switching current at maximum $f_{OUT}$ is included.

b. All outputs configured for LVEPCL logic levels and not terminated.

c. $V_{CC} \geq V_{CCOA}$ and $V_{CCOB}$.

**Table 12: Power Supply Characteristics, $V_{CC}$ = 2.5V ±5%, $V_{EE}$ = 0V, $T_A$ = -40°C to +85°C[a], [b], [c]**

| Symbol | Parameter | Test Conditions | Minimum | Typical | Maximum | Units |
|---|---|---|---|---|---|---|
| $V_{CC}$ | Core supply voltage | | 2.375 | | 2.625 | V |
| $V_{CCOA}$, $V_{CCOB}$ | Output supply voltage | | 1.71 | | $V_{CC}$ | V |
| $I_{CC}$ | Core supply current | | | 18 | 20 | mA |
| $I_{CCOA}$ + $I_{CCOB}$ | Output supply current | DIV-by-1 | | 156 | 175 | mA |
| | | DIV A = DIV B = 2 | | 124 | 139 | mA |
| $I_{EE}$ | Power supply current | | | 177 | 199 | mA |

a. Internal dynamic switching current at maximum $f_{OUT}$ is included.

b. All outputs configured for LVEPCL logic levels and not terminated.

c. $V_{CC} \geq V_{CCOA}$ and $V_{CCOB}$.

**Table 13: Power Supply Characteristics, $V_{CC}$ = 1.8V ±5%, $V_{EE}$ = 0V, $T_A$ = -40°C to +85°C[a], [b], [c]**

| Symbol | Parameter | Test Conditions | Minimum | Typical | Maximum | Units |
|---|---|---|---|---|---|---|
| $V_{CC}$ | Core supply voltage | | 1.71 | | 1.89 | V |
| $V_{CCOA}$, $V_{CCOB}$ | Output supply voltage | | 1.71 | | $V_{CC}$ | V |
| $I_{CC}$ | Core supply current | | | 14 | 16 | mA |
| $I_{CCOA}$ + $I_{CCOB}$ | Output supply current | DIV-by-1 | | 143 | 160 | mA |
| | | DIV A = DIV B = 2 | | 117 | 132 | mA |
| $I_{EE}$ | Power supply current | | | 161 | 181 | mA |

a. Internal dynamic switching current at maximum $f_{OUT}$ is included.

b. All outputs configured for LVEPCL logic levels and not terminated.

c. $V_{CC} \geq V_{CCOA}$ and $V_{CCOB}$.

**Table 14: Output Supply Current, $V_{CC}$ = 3.3V, 2.5V or 1.8V, $V_{EE}$ = 0V, $T_A$ = 25°C[a], [b]**

| Symbol | Parameter[c] | Test Conditions | $V_{CCOx}$[d] = 3.3V | | | | | $V_{CCOx}$[d] = 2.5V | | | | | $V_{CCOx}$[d] = 1.8V | | | | | $V_{CCOx}$[d] = 1.5V<br>$V_{CCOx}$[d] = 1.5V + 5% | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | LVPECL | LVDS | HCSL | LVCMOS | CML | LVPECL | LVDS | HCSL | LVCMOS | CML (400mV) | LVPECL | LVDS | HCSL | LVCMOS | CML (400mV) | LVCMOS | |
| $I_{CCOA}$ | Bank A output supply current | $V_{CC}$ = 3.3V, $T_A$ = 25°C | 76 | 96 | 73 | 119 | 60 | 75 | 96 | 67 | 92 | 58 | 68 | 87 | 66 | 72 | 53 | 60 | mA |
| | | $V_{CC}$ = 3.3V + 5%, $T_A$ = 85°C | 88 | 114 | 87 | 149 | 70 | 88 | 113 | 85 | 111 | 67 | 80 | 104 | 78 | 86 | 63 | 71 | mA |
| $I_{CCOB}$ | Bank B output supply current | $V_{CC}$ = 3.3V, $T_A$ = 25°C | 76 | 96 | 73 | 119 | 60 | 75 | 96 | 67 | 92 | 58 | 68 | 87 | 66 | 72 | 53 | 60 | mA |
| | | $V_{CC}$ = 3.3V, $T_A$ = 85°C | 88 | 114 | 87 | 149 | 70 | 88 | 113 | 85 | 111 | 67 | 80 | 104 | 78 | 86 | 63 | 71 | mA |

a. All outputs not terminated.

b. $V_{CC} \geq V_{CCOA}$ and $V_{CCOB}$.

c. Internal dynamic switching current at maximum $f_{OUT}$ is included.

d. $V_{CCOx}$ denotes $V_{CCOA}$ and $V_{CCOB}$.

# DC Electrical Characteristics

**Table 15: LVCMOS/LVTTL Control / Status Signals DC Characteristics, $V_{EE}$ = 0V, $T_A$ = -40°C to +85°C**

| Symbol | Parameter | | Test Conditions | Minimum | Typical | Maximum | Units |
|---|---|---|---|---|---|---|---|
| $V_{IH}$ | Input high voltage | | $V_{CC}$ = 3.3V | 2.20 | | $V_{CC}$ +0.3 | V |
| | | | $V_{CC}$ = 2.5V | 1.85 | | $V_{CC}$ +0.3 | V |
| | | | $V_{CC}$ = 1.8V | 1.25 | | $V_{CC}$ +0.3 | V |
| $V_{IL}$ | Input low voltage | | $V_{CC}$ = 3.3V | –0.3 | | 0.8 | V |
| | | | $V_{CC}$ = 2.5V | –0.3 | | 0.7 | V |
| | | | $V_{CC}$ = 1.8V | –0.3 | | 0.7 | V |
| $I_{IH}$ | Input high current | SA0/nCS, SDATA/SDI, SCLK, CLK_SEL, OE | $V_{CC}$ = $V_{IN}$ = 3.465V, 2.625V or 1.89V | | | 5 | µA |
| | | nI2C/SPI | | | | 150 | µA |
| $I_{IL}$ | Input low current | SA0/nCS, SDATA/SDI, SCLK, CLK_SEL,OE | $V_{CC}$ = 3.465V, 2.625V or 1.89V, $V_{IN}$ = 0V | –150 | | | µA |
| | | nI2C/SPI | | –5 | | | µA |
| $V_{OH}$ | Output high voltage | SDATA/SDI, SDO | $V_{CC}$ = 3.3V ±5%, $I_{OH}$ = –5mA | 2.6 | | | V |
| | | | $V_{CC}$ = 2.5V ±5%, $I_{OH}$ = –5mA | 1.8 | | | V |
| | | | $V_{CC}$ = 1.8V ±5%, $I_{OH}$ = –5mA | | | | V |
| $V_{OL}$ | Output low voltage | SDATA/SDI, SDO | $V_{CC}$ = 3.3V ±5% or 2.5V ±5% or 1.8V ±5%, $I_{OL}$ = 5mA | | | 0.5 | V |

**Table 16: Differential Input DC Characteristics, $V_{CC}$ = 3.3V±5%, 2.5V±5% or 1.8V±5%, $V_{EE}$ = 0V, $T_A$ = -40°C to +85°C**

| Symbol | Parameter | | Test Conditions | Minimum | Typical | Maximum | Units |
|---|---|---|---|---|---|---|---|
| $I_{IH}$ | Input high current | CLKx, nCLKx[a] | $V_{CC}$ = $V_{IN}$ = 3.465V or 2.625V | | | 150 | µA |
| $I_{IL}$ | Input low current | CLKx[a] | $V_{CC}$ = 3.465V or 2.625V, $V_{IN}$ = 0V | –5 | | | µA |
| | | nCLKx[a] | $V_{CC}$ = 3.465V or 2.625V, $V_{IN}$ = 0V | –150 | | | µA |
| $V_{PP}$ | Peak-to-peak voltage[b] | | | 0.15 | | 1.3 | V |
| $V_{CMR}$ | Common mode input voltage[b], [c] | | | 0 | | $V_{CC}$ | V |

a. CLKx denotes CLK0, CLK1. nCLKx denotes nCLK0, nCLK1.

b. $V_{IL}$ should not be less than –0.3V. $V_{IH}$ should not be higher than $V_{CC}$.

c. Common mode voltage is defined as the cross-point.

**Table 17: LVPECL DC and AC Characteristics, $V_{CC}$ = 3.3V±5%, 2.5V±5% or 1.8V±5%, $V_{EE}$ = 0V, $T_A$ = -40°C to +85°C**

| Symbol | Parameter | | $V_{CCOx}$[a] = 3.3V±5% | | | $V_{CCOx}$[a] = 2.5V±5% | | | $V_{CCOx}$[a] = 1.8V±5% | | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| $V_{OH}$ | Output high voltage[b] | Qx, nQx[c] | $V_{CCOx}$ - 1.30 | | $V_{CCOx}$ - 0.80 | $V_{CCOx}$ - 1.35 | | $V_{CCOx}$ - 0.80 | $V_{CCOx}$ - 1.50 | | $V_{CCOx}$ - 0.90 | V |
| $V_{OL}$ | Output low voltage | Qx, nQx[c] | $V_{CCOx}$ - 2.00 | | $V_{CCOx}$ - 1.75 | $V_{CCOx}$ - 2.00 | | $V_{CCOx}$ - 1.75 | $V_{EE}$ | | 0.25 | V |
| $V_{OUT}$ | Output voltage swing, $f_{OUT}$ < 500MHz | Qx, nQx[c] | 0.5 | 0.8 | 1.2 | 0.5 | 0.8 | 1.2 | 0.35 | 0.6 | 1.0 | V |
| | Output voltage swing, $f_{OUT}$ < 700MHz | Qx, nQx[c] | 0.3 | 0.65 | 1.05 | 0.3 | 0.65 | 1.05 | 0.25 | 0.45 | 0.7 | V |

a. $V_{CCOx}$ denotes $V_{CCOA}$ and $V_{CCOB}$.

b. Outputs terminated with 50Ω to $V_{CCOx}$ – 2V when $V_{CCOx}$ = 3.3V±5% or 2.5V±5%. Outputs terminated with 50Ω to ground when $V_{CCOx}$ = 1.8V±5%.

c. Qx denotes QA0, QA1, QA2, QA3, QB0, QB1, QB2, QB3. nQx denotes nQA0, nQA1, nQA2, nQA3, nQB0, nQB1, nQB2, nQB3.

**Table 18: LVDS DC and AC Characteristics, $V_{CC}$ = 3.3V ±5%, 2.5V ±5% or 1.8V ±5%, $V_{CCOA}$ = $V_{CCOB}$ = 3.3V ±5%, 2.5V ±5% or 1.8V ±5%, $T_A$ = -40°C to +85°C**

| Symbol | Parameter | | Test Conditions | Minimum | Typical | Maximum | Units |
|---|---|---|---|---|---|---|---|
| $V_{OD}$ | Differential output voltage | Qx, nQx[a] | Terminated 100Ω across Qx and nQx | 247 | | 480 | mV |
| $\Delta V_{OD}$ | $V_{OD}$ magnitude change | Qx, nQx[a] | | | | 50 | mV |
| $V_{OS}$ | Offset voltage | Qx, nQx[a] | | 1.125 | | 1.375 | V |
| $\Delta V_{OS}$ | $V_{OS}$ magnitude change | Qx, nQx[a] | | | | 50 | mV |

a. Qx denotes QA0, QA1, QA2, QA3, QB0, QB1, QB2, QB3.nQx denotes nQA0, nQA1, nQA2, nQA3, nQB0, nQB1, nQB2, nQB3.

**Table 19: CML (400mV Swing) DC and AC Characteristics, $V_{CC}$ = 3.3V ±5%, 2.5V ±5% or 1.8V ±5%, $V_{CCOA}$ = $V_{CCOB}$ = 3.3V ±5%, 2.5V ±5% or 1.8V ±5%, $T_A$ = -40°C to +85°C**

| Symbol | Parameter | | Test Conditions | Minimum | Typical | Maximum | Units |
|---|---|---|---|---|---|---|---|
| $V_{OH}$ | Output high voltage | Qx, nQx[a] | Terminated with 50Ω to $V_{CCOx}$[b] | $V_{CCOx}$[b] – 0.10 | | $V_{CCOx}$[b] | V |
| $V_{OL}$ | Output low voltage | Qx, nQx[a] | | $V_{CCOx}$[b] – 0.50 | | $V_{CCOx}$[b] – 0.30 | V |
| $V_{OUT}$ | Output voltage swing | Qx, nQx[a] | | 300 | | 500 | mV |

a. Qx denotes QA0, QA1, QA2, QA3, QB0, QB1, QB2, QB3.nQx denotes nQA0, nQA1, nQA2, nQA3, nQB0, nQB1, nQB2, nQB3.

b. $V_{CCOx}$ denotes $V_{CCOA}$ and $V_{CCOB}$.

**Table 20: CML (800mV Swing) DC and AC Characteristics, $V_{CC}$ = 3.3V ±5%, 2.5V ±5% or 1.8V ±5%, $V_{CCOA}$ = $V_{CCOB}$ = 3.3V ±5%, 2.5V ±5% or 1.8V ±5%, $T_A$ = -40°C to +85°C**

| Symbol | Parameter | | Test Conditions | Minimum | Typical | Maximum | Units |
|---|---|---|---|---|---|---|---|
| $V_{OH}$ | Output high voltage | Qx, nQx[a] | Terminated with 50Ω to $V_{CCOx}$[b] | $V_{CCOx}$[b] – 0.10 | | $V_{CCOx}$ | V |
| $V_{OL}$ | Output low voltage | Qx, nQx[a] | | $V_{CCOx}$[b] – 0.95 | | $V_{CCOx}$[b] – 0.70 | V |
| $V_{OUT}$ | Output voltage swing | Qx, nQx[a] | | 575 | | 1000 | mV |

a. Qx denotes QA0, QA1, QA2, QA3, QB0, QB1, QB2, QB3.nQx denotes nQA0, nQA1, nQA2, nQA3, nQB0, nQB1, nQB2, nQB3.

b. $V_{CCOx}$ denotes $V_{CCOA}$ and $V_{CCOB}$.

**Table 21: LVCMOS Clock Outputs DC Characteristics, $V_{CC}$ = 3.3V±5%, 2.5V±5% or 1.8V±5%, $V_{EE}$ = 0V, $T_A$ = -40°C to +85°C**

| Symbol | Parameter | Test Conditions | $V_{CCOA}$ = 3.3V±5% | | | $V_{CCOA}$ = 2.5V±5% | | | $V_{CCOA}$ = 1.8V ±5% | | | $V_{CCOA}$ = 1.5V ±5% | | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| $V_{OH}$ | Output high voltage QAx, nQAx[a] | $I_{OH}$ = –8mA | 2.6 | | | 1.1 | | | 1.1 | | | 1.1 | | | V |
| $V_{OL}$ | Output low voltage QAx, nQAx[a] | $I_{OL}$ = 8mA | | | 0.5 | | | 0.5 | | | 0.5 | | | 0.5 | V |

a. QAm denotes QA0, QA1, QA2, QA3. nQAm denotes nQA0, nQA1, nQA2, nQA3.

**Table 22: Input Frequency Characteristics, $V_{CC}$ = 3.3V±5%, 2.5V±5% or 1.8V±5%, $T_A$ = -40°C to +85°C**

| Symbol | Parameter | | Test Conditions | Minimum | Typical | Maximum | Units |
|---|---|---|---|---|---|---|---|
| $f_{IN}$ | Input frequency, CLKx, nCLKx | LVPECL, LVDS, HCSL, CML | | 1PPS | | 700MHz | |
| | | LVCMOS | | 1PPS | | 200MHz | |
| idc | Input duty cycle[a] | | | | 50 | | % |
| $f_{SCLK}$ | Serial port clock SCLK | $I^2C$ operation | | 100 | | 400 | kHz |
| | | SPI operation | | | | 50 | MHz |

a. Any deviation from a 50% duty cycle on the input may be reflected in the output duty cycle.

# AC Electrical Characteristics

**Table 23: AC Characteristics, $V_{CC}$ = 3.3V ±5%, 2.5V ±5% or 1.8V ±5%, $V_{CCOA}$ = $V_{CCOB}$ = 3.3V ±5%, 2.5V ±5% or 1.8V ±5%, $T_A$ = -40°C to +85°C**

| Symbol | Parameter[a] | | Test Conditions | | Minimum | Typical | Maximum | Units |
|---|---|---|---|---|---|---|---|---|
| $f_{OUT}$ | Output frequency | LVPECL, LVDS | | | 1PPS | | 700MHz | |
| | | HCSL, CML[b] | | | | | | |
| | | LVCMOS | | | 1PPS | | 200MHz | |
| $t_{PD}$ | Propagation Delay | LVPECL | VCCOx = 1.8V ± 5% | | 0.85 | 1.90 | 2.70 | ns |
| | | | VCCOx = 2.5V ± 5% | | 1.10 | 1.78 | 2.50 | |
| | | | VCCOx = 3.3V ± 5% | | 1.25 | 1.75 | 2.30 | |
| | | LVDS | VCCOx = 1.8V ± 5% | | 0.72 | 1.90 | 2.85 | ns |
| | | | VCCOx = 2.5V ± 5% | | 1.25 | 1.80 | 2.30 | |
| | | | VCCOx = 3.3V ± 5% | | 1.25 | 1.75 | 2.30 | |
| | | HCSL | VCCOx = 1.8V ± 5% | | 0.71 | 1.90 | 2.80 | ns |
| | | | VCCOx = 2.5V ± 5% | | 1.30 | 1.85 | 2.35 | |
| | | | VCCOx = 3.3V ± 5% | | 1.30 | 1.80 | 2.35 | |
| | | CML_800mV | VCCOx = 1.8V ± 5% | | 1.25 | 1.80 | 2.35 | ns |
| | | | VCCOx = 2.5V ± 5% | | 1.30 | 1.75 | 2.15 | |
| | | | VCCOx = 3.3V ± 5% | | 1.30 | 1.70 | 2.10 | |
| | | CML_400mV | VCCOx = 1.8V ± 5% | | 1.15 | 1.85 | 2.50 | ns |
| | | | VCCOx = 2.5V ± 5% | | 1.00 | 1.75 | 2.40 | |
| | | | VCCOx = 3.3V ± 5% | | 1.00 | 1.70 | 2.40 | |
| | | LVCMOS | VCCOx = 1.5V ± 5% | | 1.80 | 2.85 | 4.45 | ns |
| | | | VCCOx = 1.8V ± 5% | | 1.85 | 2.45 | 3.75 | |
| | | | VCCOx = 2.5V ± 5% | | 1.70 | 2.25 | 4.70 | |
| | | | VCCOx = 3.3V ± 5% | | 1.60 | 2.20 | 2.85 | |
| $t_R$ / $t_F$ | Output rise and fall times | LVPECL | 20% to 80% | | 125 | | 700 | ps |
| | | LVDS | $V_{CCOx}$[c] = 3.3V | 20% to 80% | 125 | | 550 | ps |
| | | | $V_{CCOx}$[c] = 2.5V | 20% to 80% | | | | |
| | | | $V_{CCOx}$[c] = 1.8V | 20% to 80% | 175 | | 550 | ps |
| | | CML, 400mV | 20% to 80% | | 100 | | 675 | ps |
| | | CML, 800mV | 20% to 80% | | 125 | | 825 | ps |
| | | LVCMOS | $V_{CCOA}$ = 3.3V | 20% to 80% | 200 | | 800 | ps |
| | | | $V_{CCOA}$ = 2.5V | 20% to 80% | | | | |
| | | | $V_{CCOA}$ = 1.8V | 20% to 80% | | | | |
| | | | $V_{CCOA}$ = 1.5V | 20% to 80% | | 650 | 1300 | ps |

**Table 23: AC Characteristics, $V_{CC}$ = 3.3V ±5%, 2.5V ±5% or 1.8V ±5%, $V_{CCOA}$ = $V_{CCOB}$ = 3.3V ±5%, 2.5V ±5% or 1.8V ±5%, $T_A$ = -40°C to +85°C (Cont.)**

| Symbol | Parameter[a] | | Test Conditions | | Minimum | Typical | Maximum | Units |
|---|---|---|---|---|---|---|---|---|
| $t_{sk}(b)$ | Bank skew[d][e][f] | LVPECL | | | | 15 | 50 | ps |
| | | LVDS | | | | 20 | 60 | ps |
| | | CML | | | | 10 | 35 | ps |
| | | HCSL | | | | 10 | 35 | ps |
| | | LVCMOS | | | | 50 | 100 | ps |
| $t_{sk}(bb)$ | Bank-to-bank skew[g][h][i] | LVPECL | Both banks with LVPECL outputs | | | | 120 | ps |
| | | LVDS | Both banks with LVDS outputs | | | | 100 | ps |
| odc | Output duty cycle[j] | LVPECL, LVDS, HCSL, CML | Even divide ratios | | 45 | 50 | 55 | % |
| | | LVPECL, LVDS, HCSL, CML | Odd divide ratios / bypass | | 43 | 50 | 57 | % |
| | | LVCMOS | $V_{CCOA}$ = 3.3V, 2.5V, or 1.8V | Even divide ratios | 45 | 50 | 55 | % |
| | | | | Odd divide ratios / bypass | 40 | 50 | 60 | % |
| | | LVCMOS | $V_{CCOA}$ = 1.5V | Even divide ratios | 40 | 50 | 60 | % |
| | | | | Odd divide ratios / bypass | 38 | 50 | 62 | % |
| $MUX_{ISOL}$ | Mux isolation | | 156.25MHz, $V_{SWING}$ = 800mV | | | 61 | | dB |
| | Noise floor | | Offset >10MHz from156.25MHz carrier | | | -154 | | dBc/Hz |

a. Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500lfpm. The device will meet specifications after thermal equilibrium has been reached under these conditions.

b. CML denotes CML 400mV and CML 800mV, unless otherwise stated.

c. $V_{CCOx}$ denotes $V_{CCOA}$ and $V_{CCOB}$.

d. This parameter is guaranteed by characterization. Not tested in production.

e. This parameter is defined in accordance with JEDEC Standard 65.

f. Defined as skew within a bank of outputs at the same supply voltage and with equal load conditions.

g. This parameter is guaranteed by characterization. Not tested in production.

h. This parameter is defined in accordance with JEDEC Standard 65.

i. Defined as skew within a bank of outputs at the same supply voltage and with equal load conditions.

j. Measured using 50% duty cycle on input reference.

**Table 24: HCSL AC Characteristics, $V_{CC}$ = 3.3V ±5%, 2.5V ±5% or 1.8V ±5%, $V_{CCOA}$ = $V_{CCOB}$ = 3.3V ±5%, 2.5V ±5% or 1.8V ±5%, $T_A$ = -40°C to +85°C**

| Symbol | Parameter[a] | Test Conditions[b] | Minimum | Typical | Maximum | Units |
|---|---|---|---|---|---|---|
| $t_{SLEW}$ | Rise/ fall edge rate[c] | $V_{CCOx}$ = 3.3V or 2.5V | 0.6 | | 4 | V/ns |
| | | $V_{CCOx}$ = 1.8V | 0.45 | | 4 | V/ns |
| $V_{MAX}$ | Absolute max. output voltage[d], [e] | $V_{CCOx}$ = 3.3V, 2.5V, 1.8V | | | 1150 | mV |
| $V_{MIN}$ | Absolute min. output voltage[d], [f] | $V_{CCOx}$ = 3.3V, 2.5V, 1.8V | –150 | | | mV |
| $V_{CROSS}$ | Absolute crossing voltage[g], [h] | $V_{CCOx}$ = 3.3V, 2.5V, 1.8V | | | 550 | mV |
| $\Delta V_{CROSS}$ | Total variation of $V_{CROSS}$ over all edges[g], [i] | $V_{CCOx}$ = 3.3V, 2.5V, 1.8V | | | 140 | mV |

a. Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500lfpm. The device will meet specifications after thermal equilibrium has been reached under these conditions.

b. $V_{CCOx}$ denotes $V_{CCOA}$ and $V_{CCOB}$.

c. Measured from –150mV to +150mV on the differential waveform (derived from Qx minus nQx). The signal must be monotonic through the measurement region for rise and fall time. The 300mV measurement window is centered on the differential zero crossing.

d. Measurement taken from single ended waveform.

e. Defined as the maximum instantaneous voltage including overshoot.

f. Defined as the minimum instantaneous voltage including undershoot.

g. Measured at crossing point where the instantaneous voltage value of the rising edge of Qm equals the falling edge of nQm.

h. Refers to the total variation from the lowest crossing point to the highest, regardless of which edge is crossing. Refers to all crossing points for this measurement.

i. Defined as the total variation of all crossing voltages of rising Qm and falling nQm, This is the maximum allowed variance in $V_{CROSS}$ for any particular system.

**Table 25: Additive Jitter, $V_{CC}$ = 3.3V, 2.5V or 1.8V, $V_{CCOA}$ = $V_{CCOB}$ = 3.3V, 2.5V, 1.8V or 1.5V (1.5V only supported for LVCMOS outputs), $T_A$ = 25°C**

| Symbol | Parameter | | Test Conditions[a] | | Minimum | Typical | Maximum | Units |
|---|---|---|---|---|---|---|---|---|
| $t_{jit}(f)$ | RMS additive jitter (random); Integration range: 12kHz – 20MHz | LVPECL | $f_{OUT}$ = 156.25MHz | $V_{CCOx}$[b] = 3.3V or 2.5V | | 77 | 92 | fs |
| | | | | $V_{CCOx}$[b] = 1.8V | | 90 | 117 | fs |
| | | | $f_{OUT}$ = 625MHz | $V_{CCOx}$[b] = 3.3V or 2.5V | | 50 | 60 | fs |
| | | | | $V_{CCOx}$[b] = 1.8V | | 60 | 84 | fs |
| | | LVDS | $f_{OUT}$ = 156.25MHz | $V_{CCOx}$[b] = 3.3V or 2.5V | | 85 | 104 | fs |
| | | | | $V_{CCOx}$[b] = 1.8V | | 126 | 185 | fs |
| | | | $f_{OUT}$ = 625MHz | $V_{CCOx}$[b] = 3.3V or 2.5V | | 48 | 61 | fs |
| | | | | $V_{CCOx}$[b] = 1.8V | | 57 | 84 | fs |
| | | HCSL | $f_{OUT}$ = 156.25MHz | $V_{CCOx}$[b] = 3.3V or 2.5V | | 92 | 132 | fs |
| | | | | $V_{CCOx}$[b] = 1.8V | | 92 | 133 | fs |
| | | | $f_{OUT}$ = 625MHz | $V_{CCOx}$[b] = 3.3V or 2.5V | | 61 | 73 | fs |
| | | | | $V_{CCOx}$[b] = 1.8V | | 67 | 93 | fs |
| | | LVCMOS | $f_{OUT}$ = 156.25MHz | $V_{CCOA}$ = 3.3V or 2.5V | | 98 | 166 | fs |
| | | | | $V_{CCOA}$ = 1.8V | | 128 | 204 | fs |
| | | | | $V_{CCOA}$ = 1.5V | | 198 | 314 | fs |

a. All outputs configured for the specific output type, as shown in the table.

b. $V_{CCOx}$ denotes $V_{CCOA}$ and $V_{CCOB}$.

# Applications Information

## Recommendations for Unused Input and Output Pins

### Inputs:

#### *CLK/nCLK Inputs*

For applications not requiring the use of the differential input, both CLK and nCLK can be left floating. Though not required, but for additional protection, a 1kΩ resistor can be tied from CLK to ground.

#### *LVCMOS Control Pins*

All control pins have internal pullups and pulldowns; additional resistance is not required but can be added for additional protection. A 1kΩ resistor can be used.

### Outputs:

#### *LVCMOS Outputs*

All unused LVCMOS outputs can be left floating. It is recommended that there is no trace attached.

#### *LVPECL Outputs*

All unused LVPECL outputs can be left floating. We recommend that there is no trace attached. Both sides of the differential output pair should either be left floating or terminated.

#### *LVDS Outputs*

All unused LVDS output pairs can be either left floating or terminated with 100Ω across. If they are left floating, there should be no trace attached.

#### *Differential Outputs*

All unused Differential outputs can be left floating. It is recommended that there is no trace attached.

# Power Dissipation and Thermal Considerations

The 8P79818 is a multi-functional, high speed device that targets a wide variety of clock frequencies and applications. Since this device is highly programmable with a broad range of features and functionality, the power consumption will vary as each of these features and functions is enabled.

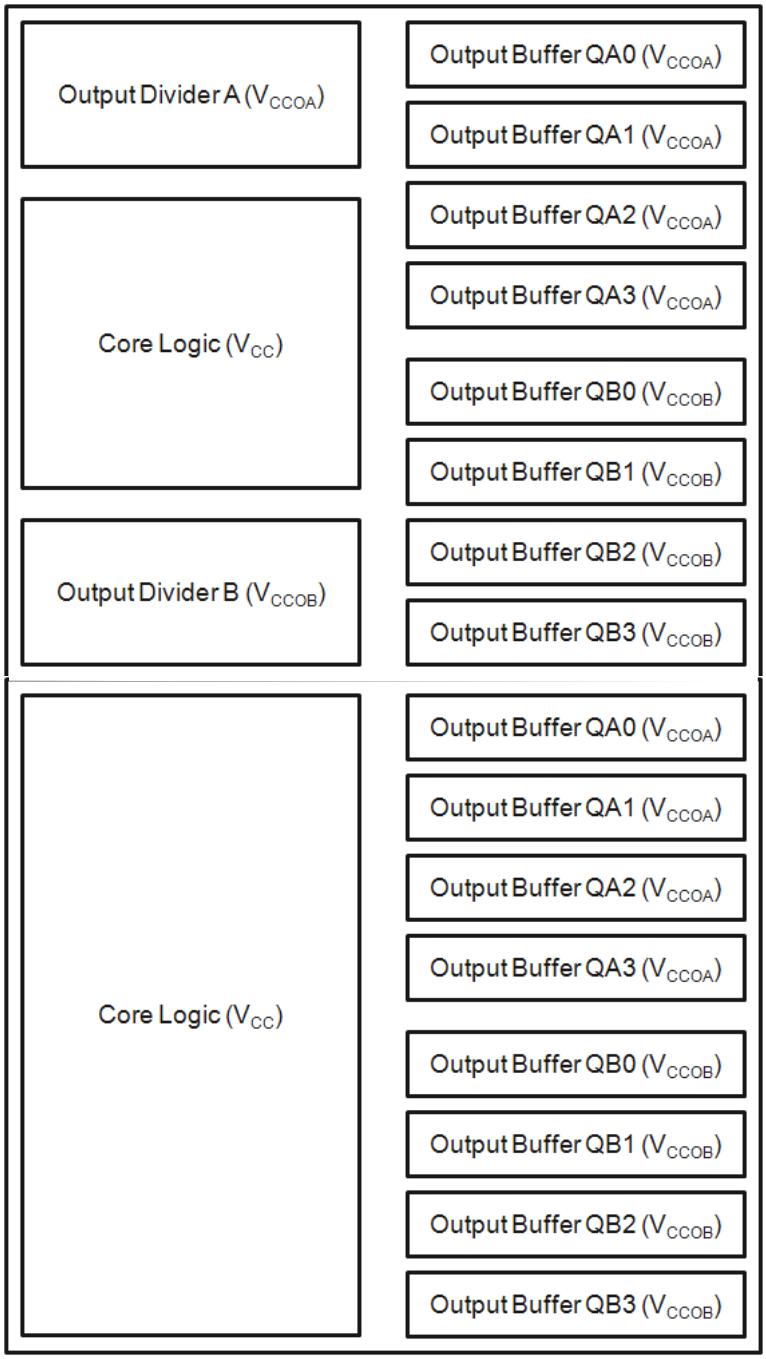
The 8P79818 device was designed and characterized to operate within the ambient industrial temperature range of -40°C to +85°C. The ambient temperature represents the temperature around the device, not the junction temperature. When using the device in extreme cases, such as maximum operating frequency and high ambient temperature, external air flow may be required in order to ensure a safe and reliable junction temperature. Extreme care must be taken to avoid exceeding 125°C junction temperature.

The power calculation examples below were generated using a maximum ambient temperature and supply voltage. For many applications, the power consumption will be much lower. Please contact Renesas technical support for any concerns on calculating the power dissipation for your own specific configuration.

## Power Domains

The 8P79818 device has a number of separate power domains that can be independently enabled and disabled via register accesses (all power supply pins must still be connected to a valid supply voltage). Figure 7 below indicates the individual domains and the associated power pins.

**Figure 7: 8P79818 Power Domains**



## Power Consumption Calculation

Determining total power consumption involves several steps:

1.Determine the power consumption using maximum current values for core voltage from Table 11, Table 12 and Table 13, Page 17 for the appropriate case of how many dividers are enabled.

2.Determine the nominal power consumption of each enabled output path.

a. This consists of a base amount of power that is independent of operating frequency, as shown in Table 27 through Table 43 (depending on the chosen output protocol).

b. Then there is a variable amount of power that is related to the output frequency. This can be determined by multiplying the output frequency by the FQ_Factor shown in Table 27 through Table 43.

3.All of the above totals are then summed.

## Example Calculations

**Table 26: Example 1. Common Customer Configuration (3.3V Core Voltage)**

| Bank | Configuration | Frequency (MHz) | $V_{CCO}$ |
|---|---|---|---|
| Bank A | LVDS | 125 | 3.3V |
| Bank B | LVDS | 125 | 2.5V |

- Core supply current, $I_{CC}$ = 24.7mA (max.)
- Output supply current, Bank A = 0.06 ∗ 125 + 71.615 = 79.115mA
- Output supply current, Bank B = 0.06 ∗ 125 + 71.615 = 79.115mA
- Total device current = 24.7mA + 79.115mA + 79.115mA = 182.93mA
- Total device power = 3.465V ∗ 183.93mA = 633.934mW

With an ambient temperature of 85°C and no airflow, the junction temperature is:

$T_J$ = 85°C + 35.23°C/W ∗ 0.634W = 107.3°C

# Thermal Considerations

Once the total power consumption has been determined, it is necessary to calculate the maximum operating junction temperature for the device under the environmental conditions it will operate in. Thermal conduction paths, air flow rate and ambient air temperature are factors that can affect this. The thermal conduction path refers to whether heat is to be conducted away via a heat-sink, via airflow or via conduction into the PCB through the device pads (including the ePAD). Thermal conduction data is provided for typical scenarios in Table 44, Page 30. Please contact Renesas for assistance in calculating results under other scenarios.

## Current Consumption Data and Equations

**Table 27: 3.3V LVDS Output Calculation Table**

| LVDS | FQ_Factor (mA/MHz), per output | Base_Current (mA) |
|---|---|---|
| Qx, nQx[a] | 0.06 | 71.615 |

a. Qx denotes QA0, QA1, QA2, QA3, QB0, QB1, QB2, QB3. nQx denotes nQA0, nQA1, nQA2, nQA3, nQB0, nQB1, nQB2, nQB3.

**Table 28: 2.5V LVDS Output Calculation Table**

| LVDS | FQ_Factor (mA/MHz), per output | Base_Current (mA) |
|---|---|---|
| Qx, nQx[a] | 0.06 | 71.544 |

a. Qx denotes QA0, QA1, QA2, QA3, QB0, QB1, QB2, QB3. nQx denotes nQA0, nQA1, nQA2, nQA3, nQB0, nQB1, nQB2, nQB3.

**Table 29: 1.8V LVDS Output Calculation Table**

| LVDS | FQ_Factor (mA/MHz), per output | Base_Current (mA) |
|---|---|---|
| Qx, nQx[a] | 0.1 | 50.284 |

a. Qx denotes QA0, QA1, QA2, QA3, QB0, QB1, QB2, QB3. nQx denotes nQA0, nQA1, nQA2, nQA3, nQB0, nQB1, nQB2, nQB3.

**Table 30: 3.3V LVPECL Output Calculation Table**

| LVPECL | FQ_Factor (mA/MHz), per output | Base_Current (mA) |
|---|---|---|
| Qx, nQx[a] | 0.05 | 53.475 |

a. Qx denotes QA0, QA1, QA2, QA3, QB0, QB1, QB2, QB3. nQx denotes nQA0, nQA1, nQA2, nQA3, nQB0, nQB1, nQB2, nQB3.

**Table 31: 2.5V LVPECL Output Calculation Table**

| LVPECL | FQ_Factor (mA/MHz), per output | Base_Current (mA) |
|---|---|---|
| Qx, nQx[a] | 0.04 | 20.874 |

a. Qx denotes QA0, QA1, QA2, QA3, QB0, QB1, QB2, QB3. nQx denotes nQA0, nQA1, nQA2, nQA3, nQB0, nQB1, nQB2, nQB3.

**Table 32: 1.8V LVPECL Output Calculation Table**

| LVPECL | FQ_Factor (mA/MHz), per output | Base_Current (mA) |
|---|---|---|
| Qx, nQx[a] | 0.04 | 19.962 |

a. Qx denotes QA0, QA1, QA2, QA3, QB0, QB1, QB2, QB3. nQx denotes nQA0, nQA1, nQA2, nQA3, nQB0, nQB1, nQB2, nQB3.

**Table 33: 3.3V HCSL Output Calculation Table**

| HCSL | FQ_Factor (mA/MHz), per output | Base_Current (mA) |
|---|---|---|
| Qx, nQx[a] | 0.05 | 54.911 |

a. Qx denotes QA0, QA1, QA2, QA3, QB0, QB1, QB2, QB3. nQx denotes nQA0, nQA1, nQA2, nQA3, nQB0, nQB1, nQB2, nQB3.

**Table 34: 3.3V CML Output (400mV) Calculation Table**

| CML | FQ_Factor (mA/MHz), per output | Base_Current (mA) |
|---|---|---|
| Qx, nQx[a] | 0.03 | 51.889 |

a. Qx denotes QA0, QA1, QA2, QA3, QB0, QB1, QB2, QB3. nQx denotes nQA0, nQA1, nQA2, nQA3, nQB0, nQB1, nQB2, nQB3.

**Table 35: 2.5V CML Output (400mV) Calculation Table**

| CML | FQ_Factor (mA/MHz), per output | Base_Current (mA) |
|---|---|---|
| Qx, nQx[a] | 0.02 | 49.220 |

a. Qx denotes QA0, QA1, QA2, QA3, QB0, QB1, QB2, QB3. nQx denotes nQA0, nQA1, nQA2, nQA3, nQB0, nQB1, nQB2, nQB3.

**Table 36: 1.8V CML Output (400mV) Calculation Table**

| CML | FQ_Factor (mA/MHz), per output | Base_Current (mA) |
|---|---|---|
| Qx, nQx[a] | 0.02 | 47.326 |

a. Qx denotes QA0, QA1, QA2, QA3, QB0, QB1, QB2, QB3. nQx denotes nQA0, nQA1, nQA2, nQA3, nQB0, nQB1, nQB2, nQB3.

**Table 37: 3.3V CML Output (800mV) Calculation Table**

| CML | FQ_Factor (mA/MHz), per output | Base_Current (mA) |
|---|---|---|
| Qx, nQx[a] | 0.02 | 51.474 |

a. Qx denotes QA0, QA1, QA2, QA3, QB0, QB1, QB2, QB3. nQx denotes nQA0, nQA1, nQA2, nQA3, nQB0, nQB1, nQB2, nQB3.

**Table 38: 2.5V CML Output (800mV) Calculation Table**

| CML | FQ_Factor (mA/MHz), per output | Base_Current (mA) |
|---|---|---|
| Qx, nQx[a] | 0.02 | 48.906 |

a. Qx denotes QA0, QA1, QA2, QA3, QB0, QB1, QB2, QB3. nQx denotes nQA0, nQA1, nQA2, nQA3, nQB0, nQB1, nQB2, nQB3.

**Table 39: 1.8V CML Output (800mV) Calculation Table**

| CML | FQ_Factor (mA/MHz), per output | Base_Current (mA) |
|---|---|---|
| Qx, nQx[a] | 0.02 | 47.334 |

a. Qx denotes QA0, QA1, QA2, QA3, QB0, QB1, QB2, QB3. nQx denotes nQA0, nQA1, nQA2, nQA3, nQB0, nQB1, nQB2, nQB3.

**Table 40: 3.3V LVCMOS Output Calculation Table**

| LVCMOS | Base_Current (mA) |
|---|---|
| Qx, nQx[a] | 62.289 |

a. Qx denotes QA0, QA1, QA2, QA3, QB0, QB1, QB2, QB3. nQx denotes nQA0, nQA1, nQA2, nQA3, nQB0, nQB1, nQB2, nQB3.

**Table 41: 2.5V LVCMOS Output Calculation Table**

| LVCMOS | Base_Current (mA) |
|---|---|
| Qx, nQx[a] | 51.097 |

a. Qx denotes QA0, QA1, QA2, QA3, QB0, QB1, QB2, QB3. nQx denotes nQA0, nQA1, nQA2, nQA3, nQB0, nQB1, nQB2, nQB3.

**Table 42: 1.8V LVCMOS Output Calculation Table**

| LVCMOS | Base_Current (mA) |
|---|---|
| Qx, nQx[a] | 47.745 |

a. Qx denotes QA0, QA1, QA2, QA3, QB0, QB1, QB2, QB3. nQx denotes nQA0, nQA1, nQA2, nQA3, nQB0, nQB1, nQB2, nQB3.

**Table 43: 1.5V LVCMOS Output Calculation Table**

| LVCMOS | Base_Current (mA) |
|---|---|
| Qx, nQx[a] | 41.485 |

a. Qx denotes QA0, QA1, QA2, QA3, QB0, QB1, QB2, QB3. nQx denotes nQA0, nQA1, nQA2, nQA3, nQB0, nQB1, nQB2, nQB3.

Applying the values to the following equation will yield output current by frequency: (mA) = FQ_Factor * Frequency (MHz) + Base_Current

where:

Qx Current is the specific output current according to output type and frequency

FQ_Factor is used for calculating current increase due to output frequency

Base_Current is the base current for each output path independent of output frequency

The second step is to multiply the power dissipated by the thermal impedance to determine the maximum power gradient, using the following equation:

$T_J = T_A + (\theta_{JA} * Pd_{total})$

where:

$T_J$ is the junction temperature (°C)

$T_A$ is the ambient temperature (°C)

$\theta_{JA}$ is the thermal resistance value from Table 44, Page 30, dependent on ambient airflow (°C/W)

$Pd_{total}$ is the total power dissipation of the 8P79818 under usage conditions, including power dissipated due to loading (W)

Note that for LVPECL outputs the power dissipation through the load is assumed to be 27.95mW. When selecting LVCMOS outputs, power dissipation through the load will vary based on a variety of factors including termination type and trace length. For these examples, power dissipation through loading will be calculated using $C_{PD}$ (found in Table 10, Page 15) and output frequency:

$Pd_{OUT} = C_{PD} * f_{OUT} * V_{CCO}^2$

where:

$Pd_{out}$ is the power dissipation of the output (W)

$C_{PD}$ is the power dissipation capacitance (pF)

$f_{OUT}$ is the output frequency of the selected output (MHz)

$V_{CCO}$ is the voltage supplied to the appropriate output (V)

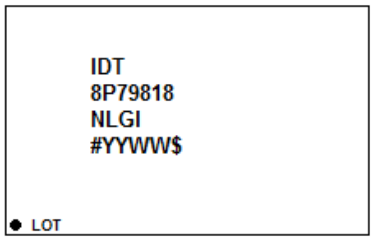
**Table 44: $\theta_{JA}$ vs. Air Flow Table for a 32-lead 5mm x 5mm VFQFN**

| $\theta_{JA}$ vs. Air Flow | | | |
|---|---|---|---|
| Meters per Second | 0 | 1 | 2 |
| Multi-Layer PCB, JEDEC Standard Test Boards | 35.23°C/W | 31.6°C/W | 30.0°C/W |

## Package Outline Drawings

The package outline drawings are located at the end of this document and are accessible from the Renesas website (see Ordering Information for POD links). The package information is the most current data available and is subject to change without revision of this document.

## Marking Diagram



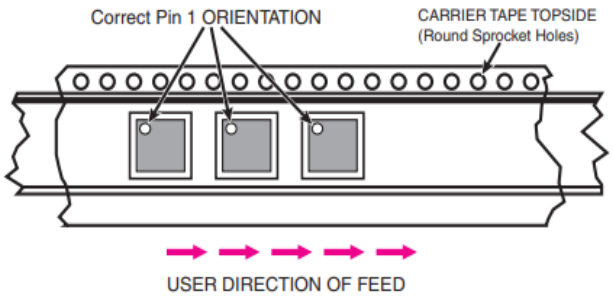
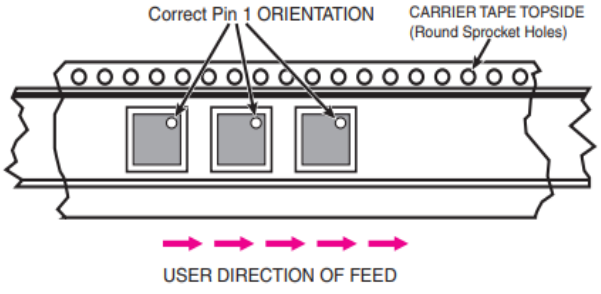

- Line 1 is the prefix of the part number.
- Line 2 and Line 3 is the part number.
- Line 4:
  - "#" denotes the stepping number.
  - "YY" are the last digits of the year and "WW" is the work week that the part was assembled.
  - "$" denotes mark code.

## Ordering Information

**Table 45: Ordering Information**

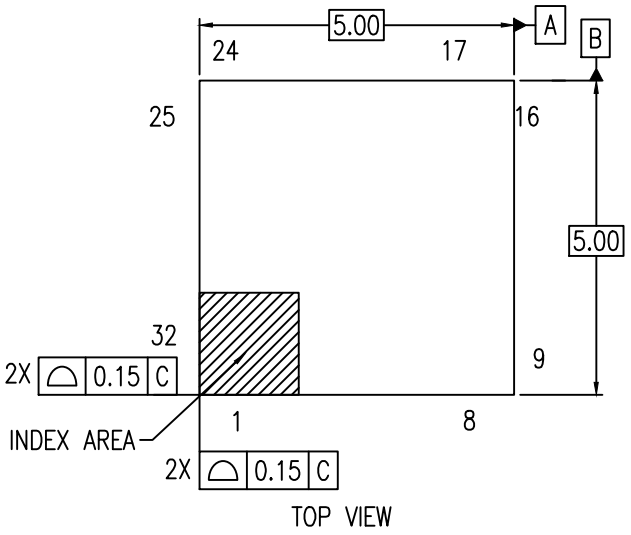
| Part Number | Marking | Package | Carrier Type | Temperature Range |
|---|---|---|---|---|
| 8P79818NLGI | IDT8P79818NLGI | 32-lead VFQFN, Lead Free | Tray | -40°C to +85°C |
| 8P79818NLGI8 | IDT8P79818NLGI | | Tape & Reel | -40°C to +85°C |
| 8P79818NLGI/W | IDT8P79818NLGI | | Tape & Reel | -40°C to +85°C |

**Table 46: Pin 1 Orientation in Tape and Reel Packaging**

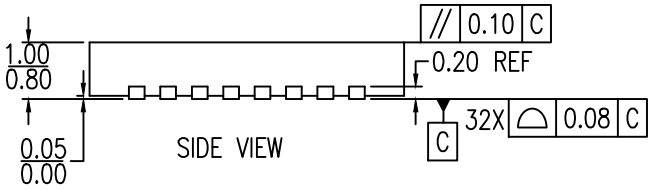
| Part Number Suffix | Pin 1 Orientation | Illustration |
|---|---|---|
| NLGI8 | Quadrant 1 (EIA-481-C) |  |
| NLGI/W | Quadrant 2 (EIA-481-D) |  |

# Revision History

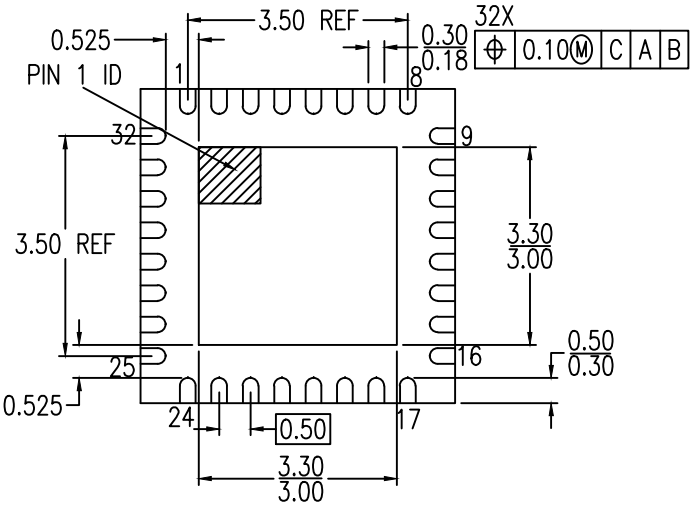
| Revision Date | Description of Change |
|---|---|
| November 19, 2021 | ▪ Added footnote ‘c’ to Table 1. |
| November 9, 2021 | ▪ Added Bank-to-Bank Skew to Table 23<br>▪ Added footnote ‘b’ to Table 1<br>▪ Completed other minor changes |
| July 29, 2021 | ▪ Added output voltage swing in Table 17 |
| June 25, 2021 | ▪ Added propagation delay specifications to AC Characteristics table.<br>▪ Updated Package Outline Drawings section.<br>▪ Rebranded datasheet. |
| December 19, 2016 | Initial datasheet. |



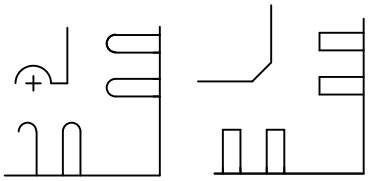

TOP VIEW




SIDE VIEW



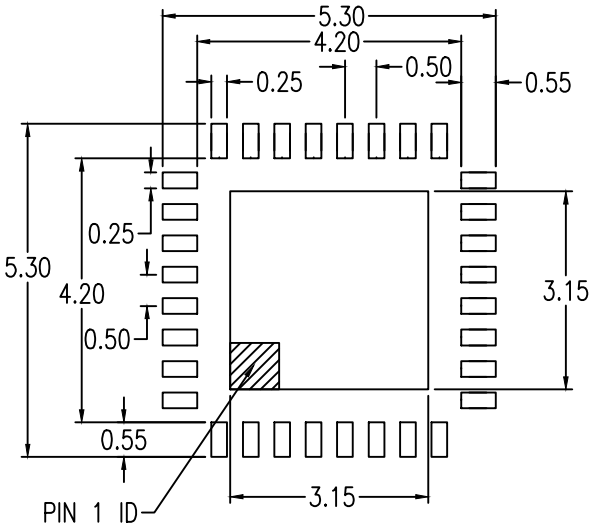

BOTTOM VIEW



PIN #1 ID OPTION

NOTE:
1. ALL DIMENSION ARE IN MM. ANGLES IN DEGREES.
2. COPLANARITY APPLIE TO THE EXPOSED PAD AS WELL AS THE TERMINALS. COPLANARITY SHALL NOT EXCEED 0.08 MM.
3. WARPAGE SHALL NOT EXCEED 0.10 MM.
4. PIN LOCATION IS UNDENTIFIED BY EITHER CHAMFER OR NOTCH.

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RECOMMENDED LAND PATTERN DIMENSION

1. ALL DIMENSIONS ARE IN MM. ANGLES IN DEGREES.
2. TOP DOWN VIEW. AS VIEWED ON PCB.
3. LAND PATTERN RECOMMENDATION PER IPC-7351B GENERIC REQUIREMENT FOR SURFACE MOUNT DESIGN AND LAND PATTERN.

| Package Revision History | | |
|---|---|---|
| Date Created | Rev No. | Description |
| April 12, 2018 | Rev 02 | New Format |
| Feb 8, 2016 | Rev 01 | Added "k: Value |

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(Rev.1.0 Mar 2020)


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