Description

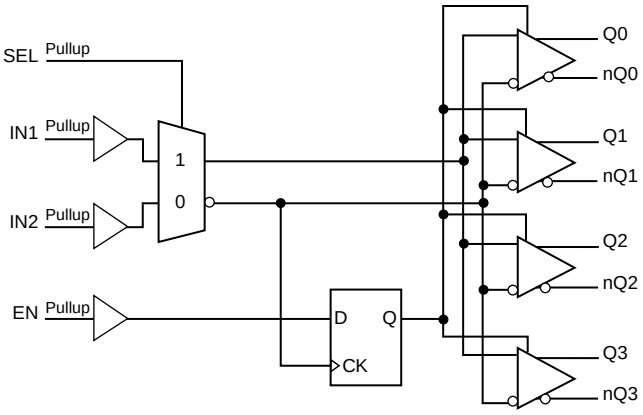
The 8S89834I is a high speed 2-to-4 LVCMOS/LVTTL-to-LVPECL/ECL Clock Multiplexer. The 8S89834I is optimized for high speed and very low output skew, making it suitable for use in demanding applications such as SONET, 1 Gigabit and 10 Gigabit Ethernet, and Fibre Channel. The device also has an output enable pin which may be useful for system test and debug purposes.

The 8S89834I is packaged in a small 3mm x 3mm 16-pin VFQFN package which makes it ideal for use in space-constrained applications.

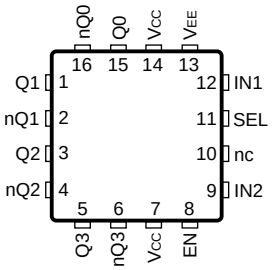
Features

- Four differential LVPECL/ECL output pairs
- Two LVCMOS/LVTTL clock inputs
- Maximum output frequency: 1GHz
- Output skew: 30ps (maximum)
- Part-to-part skew: 100ps (maximum)
- Propagation delay: 550ps (maximum)
- Additive phase jitter, RMS: 0.12ps (typical)
- Full 3.3V and 2.5V operating supply modes
- -40°C to 85°C ambient operating temperature
- Available in lead-free (RoHS 6) package

Block Diagram



Pin Assignment



8S89834I

16-Lead VFQFN
3mm x 3mm x 0.925mm package body
K Package
Top View

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Table 1. Pin Descriptions

Number	Name	Type		Description
1, 2	Q1, nQ1	Output		Differential output pair. LVPECL/ECL interface levels.
3, 4	Q2, nQ2	Output		Differential output pair. LVPECL/ECL interface levels.
5, 6	Q3, nQ3	Output		Differential output pair. LVPECL/ECL interface levels.
7, 14	V_{cc}	Power		Positive supply pins.
8	EN	Input	Pullup	Synchronizing clock enable. When LOW, Q outputs will go LOW and nQ outputs will go HIGH on the next LOW transition at IN inputs. Input threshold is V_{CC}/2V. Includes a 37kΩ pullup resistor. Default state is HIGH when left floating. The internal latch is clocked on the falling edge of the input signal IN1, IN2. LVTTL/LVCMOS interface levels.
9	IN2	Input	Pullup	Single-ended clock input. LVCMOS/LVTTL interface levels.
10	nc	Unused		No connect.
11	SEL	Input	Pullup	Select clock input. When LOW, selects IN2 and when HIGH selects IN1. LVCMOS/LVTTL interface levels.
12	IN1	Input	Pullup	Single-ended clock input. LVCMOS/LVTTL interface levels.
13	V_{EE}	Power		Negative supply pin.
15, 16	Q0, nQ0	Output		Differential output pair. LVPECL/ECL interface levels.

NOTE: *Pullup* refers to internal input resistors. See Table 2, *Pin Characteristics,* for typical values.

Table 2. Pin Characteristics

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
R_{PULLUP}	Input Pullup Resistor			37		kΩ

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Function Tables

Table 3A. Control Input Function Table

Inputs		Outputs	
EN	**Selected Source**	**Q[0:3]**	**nQ[0:3]**
0	IN1, IN2	Disabled; LOW	Disabled; HIGH
1	IN1, IN2	Enabled	Enabled

NOTE: EN switches, the clock outputs are disabled or enabled following a falling input clock edge as shown in *Figure 1.*

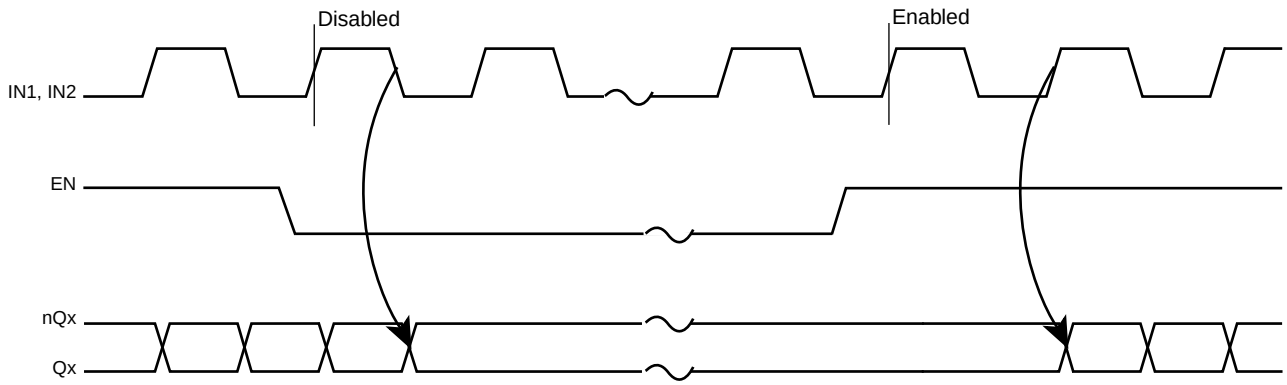


Figure 1. EN Timing Diagram

Table 3B. Truth Table

Inputs			Outputs	
IN1, IN2	**IN1, IN2**	**EN**	**Q[0:3]**	**nQ[0:3]**
0	X	1	0	1
1	X	1	1	0
X	0	1	0	1
X	1	1	1	0
X	X	0	0(NOTE 1)	1(NOTE 1)

NOTE 1: On next negative transition of the input signal (IN).

Table 3C. SEL Control Function Table

SEL	Input Selected
0	IN2
1	IN1

.

Absolute Maximum Ratings

Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics or AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Item	Rating
Supply Voltage, V_{CC}	4.6V (LVPECL mode, V_{EE} = 0V)
Negative Supply Voltage, V_{EE}	-4.6V (ECL mode, V_{CC} = 0V)
Inputs, V_I (LVPECL mode)	-0.5V to V_{CC} + 0.5V
Inputs, V_I (ECL mode)	0.5V to V_{EE} - 0.5V
Outputs, I_O Continuos Current Surge Current	 50mA 100mA
Operating Temperature Range, T_A	-40°C to +85°C
Package Thermal Impedance, θ_{JA}, (Junction-to-Ambient)	74.7°C/W (0 mps)
Storage Temperature, T_{STG}	-65°C to 150°C

DC Electrical Characteristics

Table 4A. Power Supply DC Characteristics, V_{CC} = 3.3V ± 10%, V_{EE} = 0V, T_A = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{CC}	Positive Supply Voltage		2.97	3.3	3.63	V
I_{EE}	Power Supply Current				52	mA

Table 4B. Power Supply DC Characteristics, V_{CC} = 2.5V ± 5%, V_{EE} = 0V, T_A = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{CC}	Positive Supply Voltage		2.375	2.5	2.625	V
I_{EE}	Power Supply Current				52	mA

Table 4C. LVCMOS/LVTTL DC Characteristics, V_{CC} = 2.5V ± 5% or 3.3V ± 10%, V_{EE} = 0V, T_A = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{IH}	Input High Voltage	V_{CC} = 3.3V	2.2		V_{CC} + 0.3	V
		V_{CC} = 2.5V	1.7		V_{CC} + 0.3	V
V_{IL}	Input Low Voltage	V_{CC} = 3.3V	-0.3		0.8	V
		V_{CC} = 2.5V	-0.3		0.7	V
I_{IH}	Input High Current	V_{CC} = V_{IN} = 3.63V or 2.625V			10	µA
I_{IL}	Input Low Current	V_{CC} = 3.63V or 2.625V, V_{IN} = 0V	-150			µA

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Table 4D. LVPECL DC Characteristics, V_{CC} = 3.3V ± 10% or 2.5V ± 5%, V_{EE} = 0V, T_A = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{OH}	Output High Voltage; NOTE 1		V_{CC} – 1.145		V_{CC} – 0.80	V
V_{OL}	Output Low Voltage; NOTE 1		V_{CC} – 1.945		V_{CC} – 1.60	V
V_{OUT}	Output Voltage Swing		0.6		1.0	V
V_{DIFF_OUT}	Differential Output Voltage Swing		1.2		2.0	V

NOTE 1: Outputs terminated with 50Ω to V_{CC} - 2V.

AC Electrical Characteristics

Table 5. AC Characteristics, V_{CC} = 2.5V ± 5% or or 3.3V ± 10%, T_A = -40°C to 85°C

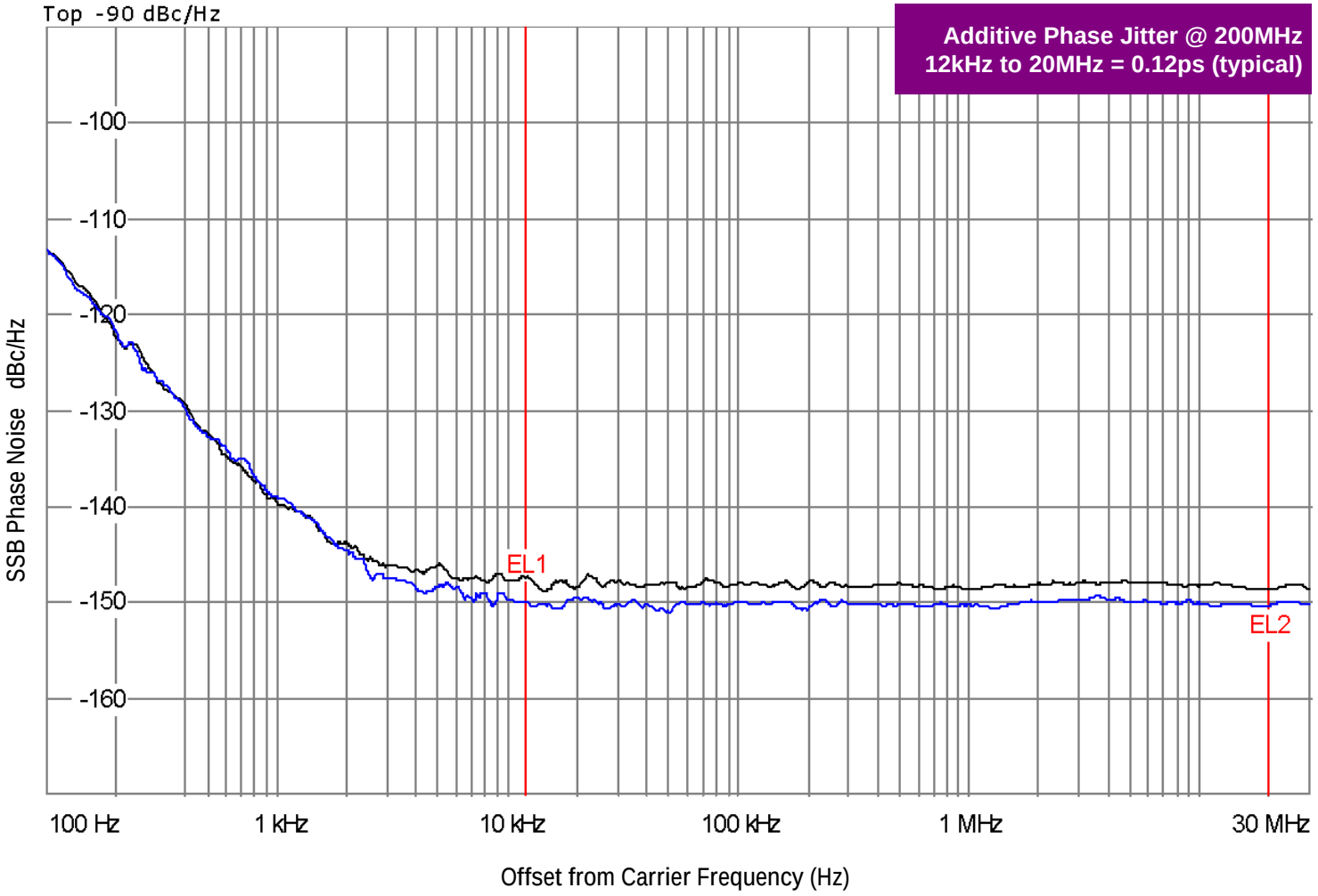
Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
f_{MAX}	Maximum Frequency					1	GHz
t_{PLH}	Propagation Delay; Low-to-High; NOTE 1			250		550	ps
t_{PHL}	Propagation Delay; High-to-Low; NOTE 1			300		550	ps
t_{SW}	Switchover Time	SEL to Q		300		550	ps
*t*sk(o)	Output Skew; NOTE 2, 3					30	ps
*t*sk(pp)	Part-to-Part Skew; NOTE 3, 4					100	ps
*t*jit	Buffer Additive Phase Jitter, RMS; refer to Additive Phase Jitter Section		200MHz Integration Range: (12kHz - 20MHz)		0.12		ps
t_S	Clock Enable Setup Time	EN to IN1, IN2		300			ps
t_H	Clock Enable Hold Time	EN to IN1, IN2		500			ps
t_R / t_F	Output Rise/Fall Time		20% to 80%	50		250	ps
odc	Output Duty Cycle		f_{MAX} < 622MHz	48		52	%
			$f_{MAX} \geq$ 622MHz	45		55	%

NOTE: Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfpm. The device will meet specifications after thermal equilibrium has been reached under these conditions.
All parameters are measured at ≤ 1GHz unless otherwise noted.
NOTE 1: Measured from V_{CC}/2 of the input to the differential output crossing point.
NOTE 2: Defined as skew between outputs at the same supply voltage and with equal load conditions.
Measured at the output differential cross points.
NOTE 3: This parameter is defined in accordance with JEDEC Standard 65.
NOTE 4: Defined as skew between outputs on different devices operating at the same supply voltage, same frequency and with equal load conditions. Using the same type of inputs on each device, the outputs are measured at the differential cross points.

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Additive Phase Jitter

The spectral purity in a band at a specific offset from the fundamental compared to the power of the fundamental is called the *dBc Phase Noise.* This value is normally expressed using a Phase noise plot and is most often the specified plot in many applications. Phase noise is defined as the ratio of the noise power present in a 1Hz band at a specified offset from the fundamental frequency to the power value of the fundamental. This ratio is expressed in decibels (dBm) or a ratio of the power in the 1Hz band to the power in the fundamental. When the required offset is specified, the phase noise is called a *dBc* value, which simply means dBm at a specified offset from the fundamental. By investigating jitter in the frequency domain, we get a better understanding of its effects on the desired application over the entire time record of the signal. It is mathematically possible to calculate an expected bit error rate given a phase noise plot.

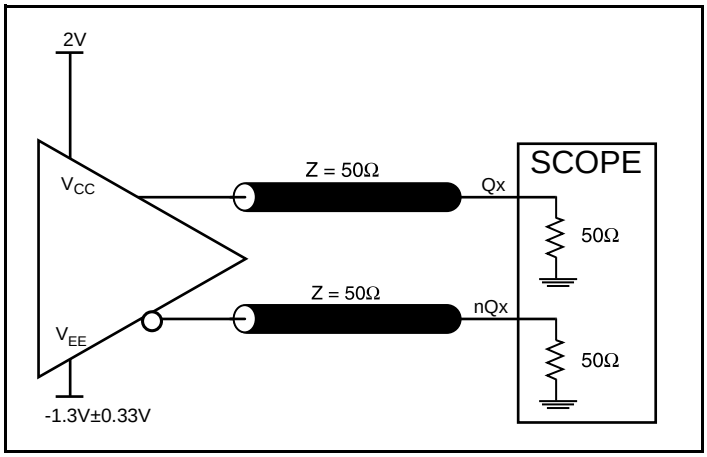


As with most timing specifications, phase noise measurements has issues relating to the limitations of the equipment. Often the noise floor of the equipment is higher than the noise floor of the device. This is illustrated above. The device meets the noise floor of what is shown, but can actually be lower. The phase noise is dependent on the input source and measurement equipment.

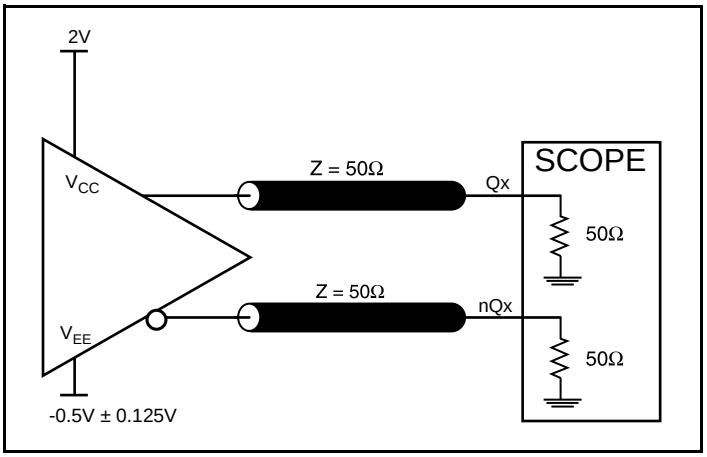
The source generator “IFR2042 10kHz – 56.4GHz Low Noise Signal Generator as external input to an Agilent 8133A 3GHz Pulse Generator”.

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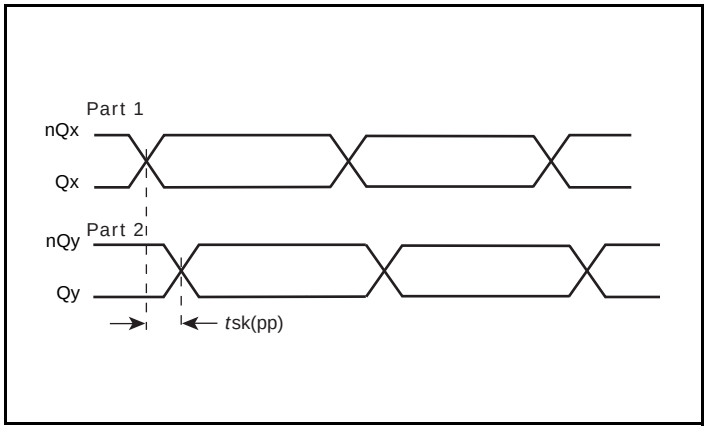
Parameter Measurement Information



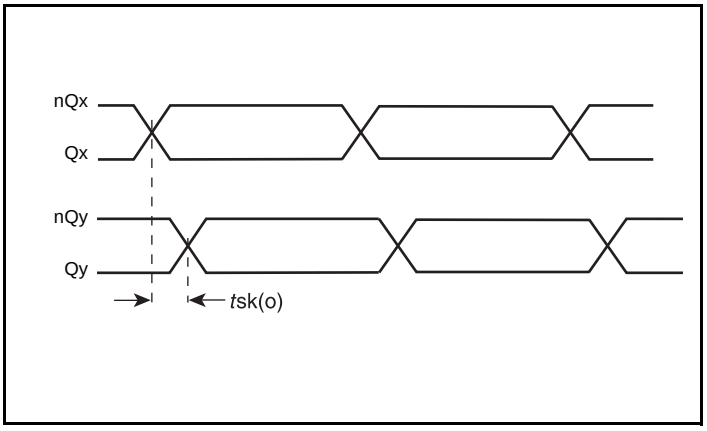
3.3V LVPECL Output Load AC Test Circuit



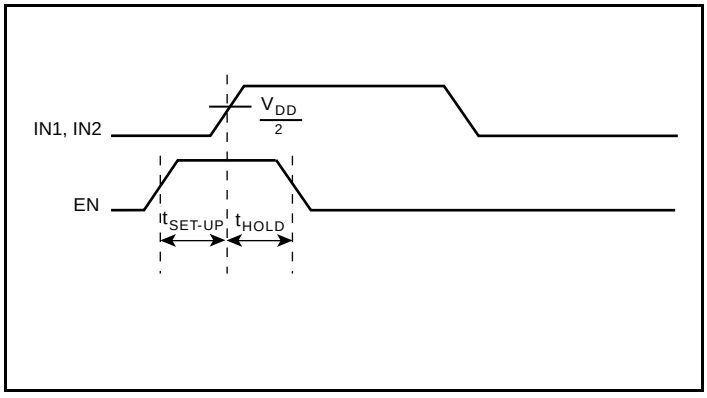
2.5V LVPECL Output Load AC Test Circuit



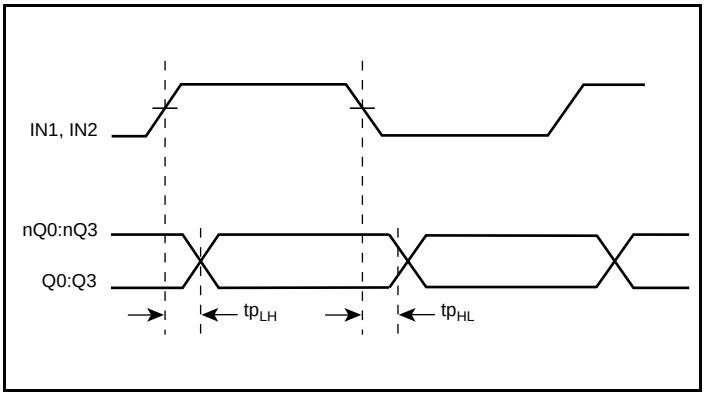
Part-to-Part Skew



Output Skew

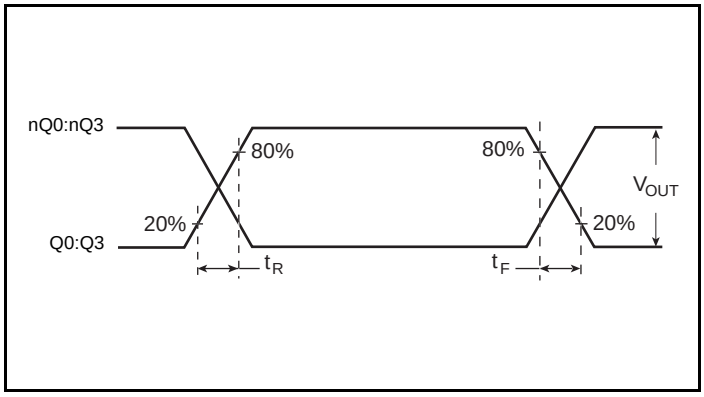


Setup & Hold Time

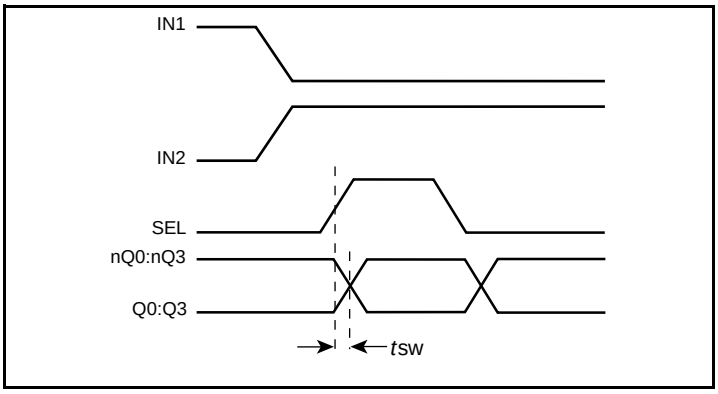


Propagation Delay

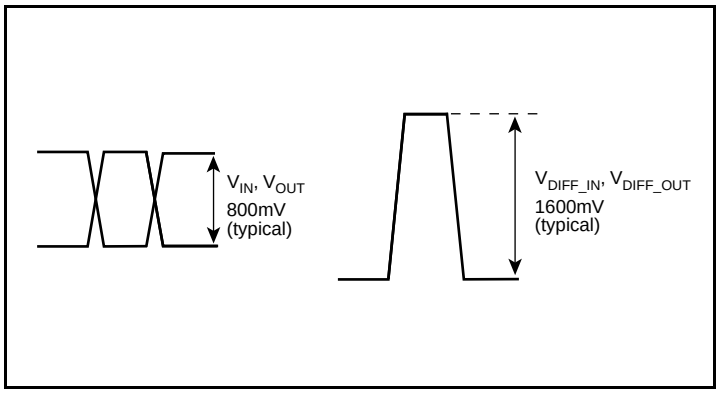
Parameter Measurement Information, continued



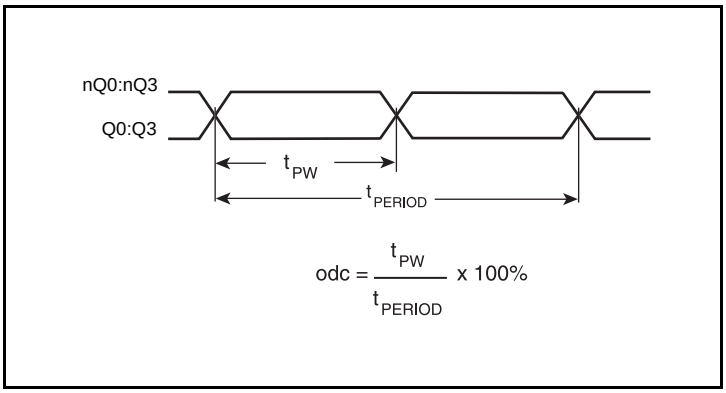
Output Rise/Fall Time



Switch Over



Differential Output Voltage Swing



Output Duty Cycle/Pulse Width/Period

Application Information

Recommendations for Unused Input and Output Pins

Inputs:

IN Inputs

For applications not requiring the use of a clock input, it can be left floating. Though not required, but for additional protection, a 1kΩ resistor can be tied from the IN input to ground.

LVCMOS Control Pins

All control pins have internal pullups; additional resistance is not required but can be added for additional protection. A 1kΩ resistor can be used.

Outputs:

LVPECL Outputs

All unused LVPECL outputs can be left floating. We recommend that there is no trace attached. Both sides of the differential output pair should either be left floating or terminated.

VFQFN EPAD Thermal Release Path

In order to maximize both the removal of heat from the package and the electrical performance, a land pattern must be incorporated on the Printed Circuit Board (PCB) within the footprint of the package corresponding to the exposed metal pad or exposed heat slug on the package, as shown in *Figure 2.* The solderable area on the PCB, as defined by the solder mask, should be at least the same size/shape as the exposed pad/slug area on the package to maximize the thermal/electrical performance. Sufficient clearance should be designed on the PCB between the outer edges of the land pattern and the inner edges of pad pattern for the leads to avoid any shorts.

While the land pattern on the PCB provides a means of heat transfer and electrical grounding from the package to the board through a solder joint, thermal vias are necessary to effectively conduct from the surface of the PCB to the ground plane(s). The land pattern must be connected to ground through these vias. The vias act as “heat pipes”. The number of vias (i.e. “heat pipes”) are application specific and dependent upon the package power dissipation as well as electrical conductivity requirements. Thus, thermal and electrical analysis and/or testing are recommended to determine the minimum number needed. Maximum thermal and electrical performance is achieved when an array of vias is incorporated in the land pattern. It is recommended to use as many vias connected to ground as possible. It is also recommended that the via diameter should be 12 to 13mils (0.30 to 0.33mm) with 1oz copper via barrel plating. This is desirable to avoid any solder wicking inside the via during the soldering process which may result in voids in solder between the exposed pad/slug and the thermal land. Precautions should be taken to eliminate any solder voids between the exposed heat slug and the land pattern. Note: These recommendations are to be used as a guideline only. For further information, please refer to the Application Note on the Surface Mount Assembly of Amkor’s Thermally/ Electrically Enhance Leadframe Base Package, Amkor Technology.

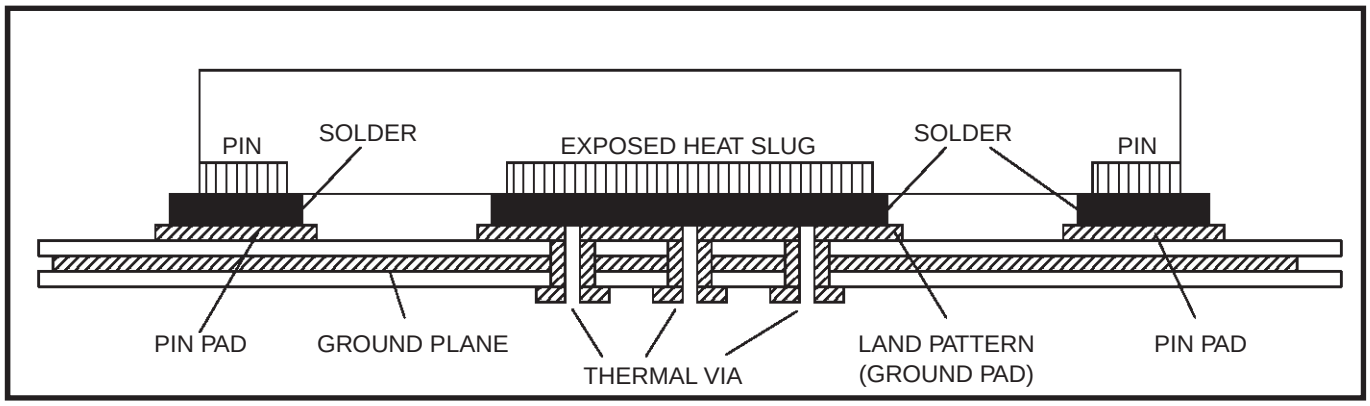


Figure 2. P.C. Assembly for Exposed Pad Thermal Release Path – Side View (drawing not to scale)

Termination for 3.3V LVPECL Outputs

The clock layout topology shown below is a typical termination for LVPECL outputs. The two different layouts mentioned are recommended only as guidelines.

The differential outputs are low impedance follower outputs that generate ECL/LVPECL compatible outputs. Therefore, terminating resistors (DC current path to ground) or current sources must be used for functionality. These outputs are designed to drive 50Ω transmission lines. Matched impedance techniques should be used to maximize operating frequency and minimize signal distortion. *Figures 3A and 3B* show two different layouts which are recommended only as guidelines. Other suitable clock layouts may exist and it would be recommended that the board designers simulate to guarantee compatibility across all printed circuit and clock component process variations.

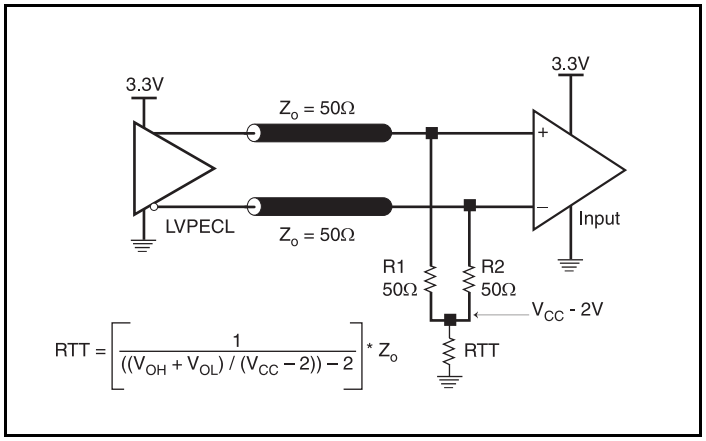


Figure 3A. 3.3V LVPECL Output Termination

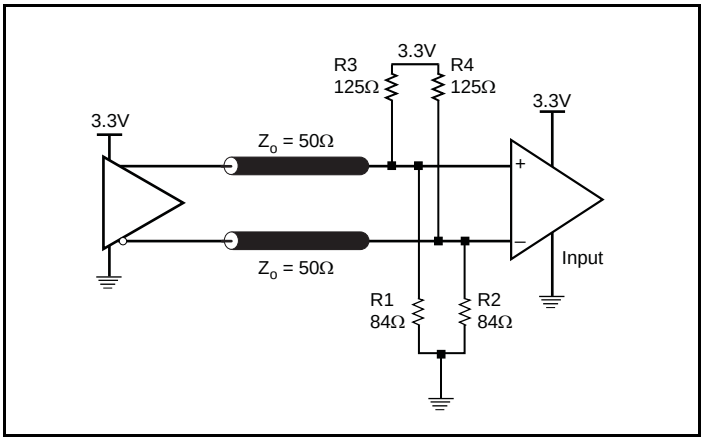


Figure 3B. 3.3V LVPECL Output Termination

Termination for 2.5V LVPECL Outputs

Figure 4A and *Figure 4B* show examples of termination for 2.5V LVPECL driver. These terminations are equivalent to terminating 50Ω to V_{CC} – 2V. For V_{CC} = 2.5V, the V_{CC} – 2V is very close to ground level. The R3 in Figure 4B can be eliminated and the termination is shown in *Figure 4C.*

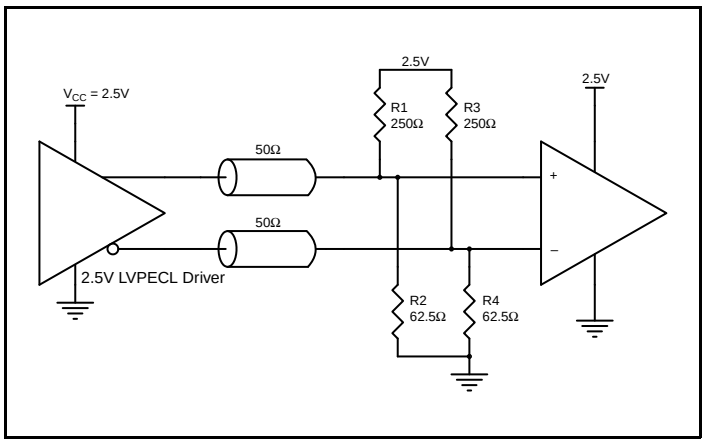


Figure 4A. 2.5V LVPECL Driver Termination Example

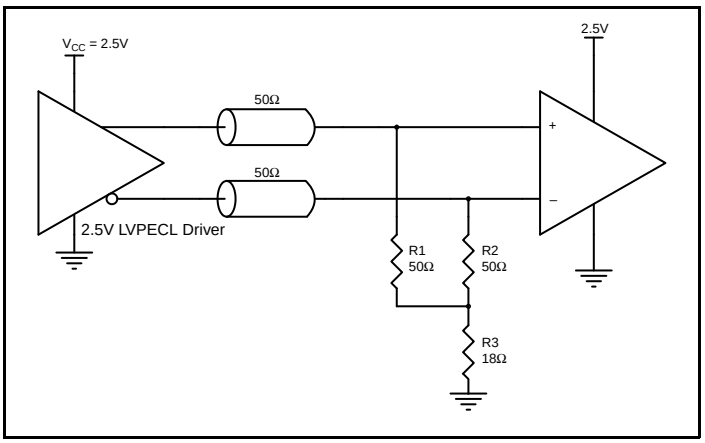


Figure 4B. 2.5V LVPECL Driver Termination Example

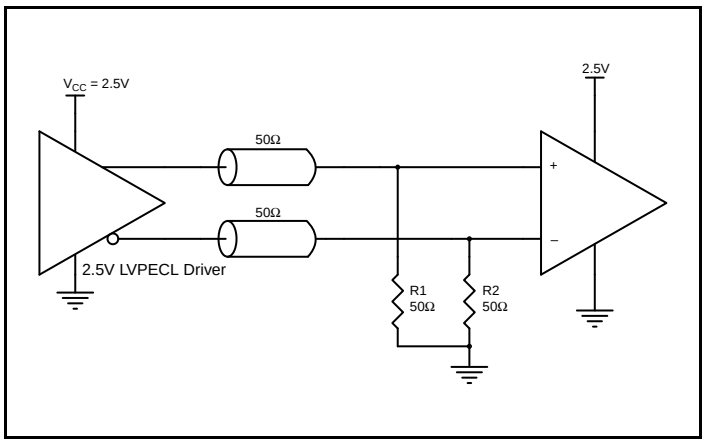


Figure 4C. 2.5V LVPECL Driver Termination Example

Power Considerations

This section provides information on power dissipation and junction temperature for the 8S89834I.
Equations and example calculations are also provided.

1. Power Dissipation.

The total power dissipation for the 8S89834I is the sum of the core power plus the power dissipated in the load(s).
The following is the power dissipation for V_{CC} = 3.63V, which gives worst case results.

NOTE: Please refer to Section 3 for details on calculating power dissipated in the load.

- Power $(core)_{MAX} = V_{CC_MAX} * I_{EE_MAX}$ = 3.63V * 52mA = **188.76mW**
- Power $(outputs)_{MAX}$ = **32mW w/Loaded Output pair**
  If all outputs are loaded, the total power is 4 * 32mW = **128mW**

Total Power$_{_MAX}$ = (3.63V, with all outputs switching) = 188.76mW + 128mW = **316.76mW**

2. Junction Temperature.

Junction temperature, Tj, is the temperature at the junction of the bond wire and bond pad directly affects the reliability of the device. The maximum recommended junction temperature is 125°C. Limiting the internal transistor junction temperature, Tj, to 125°C ensures that the bond wire and bond pad temperature remains below 125°C.

The equation for Tj is as follows: $Tj = \theta_{JA} * Pd_total + T_A$

Tj = Junction Temperature

θ_{JA} = Junction-to-Ambient Thermal Resistance

Pd_total = Total Device Power Dissipation (example calculation is in section 1 above)

T_A = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance θ_{JA} must be used. Assuming no air flow and a multi-layer board, the appropriate value is 74.7°C/W per Table 6 below.

Therefore, Tj for an ambient temperature of 85°C with all outputs switching is:

85°C + 0.317W * 74.7°C/W = 108.7°C. This is well below the limit of 125°C.

This calculation is only an example. Tj will obviously vary depending on the number of loaded outputs, supply voltage, air flow and the type of board (multi-layer).

Table 6. Thermal Resistance θ_{JA} for 16 Lead VFQFN, Forced Convection

θ_{JA} **vs. Air Flow**			
Meters per Second	**0**	**1**	**2.5**
Multi-Layer PCB, JEDEC Standard Test Boards	74.7°C/W	65.3°C/W	58.5°C/W

3. Calculations and Equations.

The purpose of this section is to calculate the power dissipation for the LVPECL output pairs.

LVPECL output driver circuit and termination are shown in *Figure 5.*

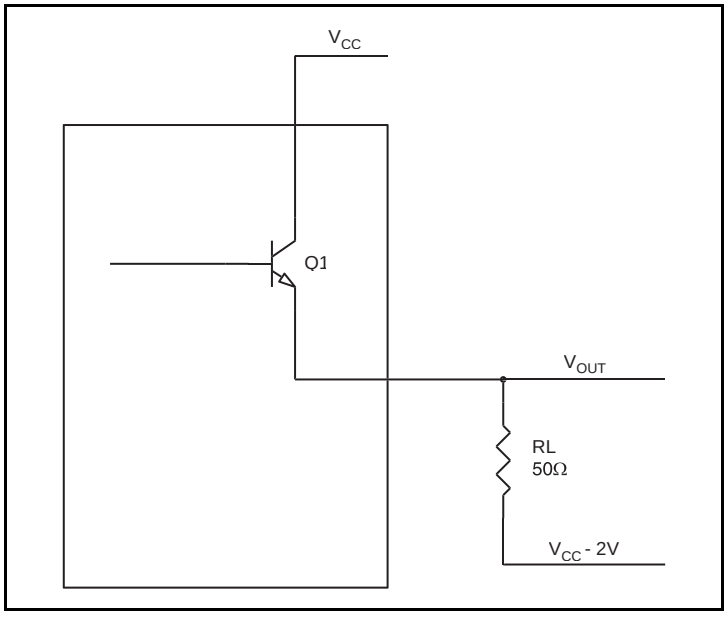


Figure 5. LVPECL Driver Circuit and Termination

To calculate worst case power dissipation into the load, use the following equations which assume a 50Ω load, and a termination voltage of V_{CC} – 2V.

- For logic high, $V_{OUT} = V_{OH_MAX} = \mathbf{V_{CC_MAX} - 0.80V}$
  $(V_{CC_MAX} - V_{OH_MAX}) = \mathbf{0.80V}$
- For logic low, $V_{OUT} = V_{OL_MAX} = \mathbf{V_{CC_MAX} - 1.60V}$
  $(V_{CC_MAX} - V_{OL_MAX}) = \mathbf{1.60V}$

Pd_H is power dissipation when the output drives high.

Pd_L is the power dissipation when the output drives low.

$Pd_H = [(V_{OH_MAX} – (V_{CC_MAX} – 2V))/R_L] * (V_{CC_MAX} – V_{OH_MAX}) = [(2V – (V_{CC_MAX} – V_{OH_MAX}))/R_L] * (V_{CC_MAX} – V_{OH_MAX}) =$
$[(2V – 0.80V)/50\Omega] * 0.80V =$ **19.20mW**

$Pd_L = [(V_{OL_MAX} – (V_{CC_MAX} – 2V))/R_L] * (V_{CC_MAX} – V_{OL_MAX}) = [(2V – (V_{CC_MAX} – V_{OL_MAX}))/R_L] * (V_{CO_MAX} – V_{OL_MAX}) =$
$[(2V – 1.60V)/50\Omega] * 1.60V =$ **12.80mW**

Total Power Dissipation per output pair = Pd_H + Pd_L = **32mW**

Reliability Information

Table 6. θ_{JA} vs. Air Flow Table for a 16 Lead VFQFN

θ_{JA} by Velocity			
Meters per Second	**0**	**1**	**2.5**
Multi-Layer PCB, JEDEC Standard Test Boards	74.7°C/W	65.3°C/W	58.5°C/W

Transistor Count

The transistor count for 8S89834I is: 351
This device is pin and function compatible and a suggested replacement for 889834.

Package Outline Drawings

The package outline drawings are located in the last section of this document. The package information is the most current data available and is subject to change without notice or revision of this document.

Ordering Information

Table 8. Ordering Information

Part/Order Number	Marking	Package	Shipping Packaging	Temperature
8S89834AKILF	834A	“Lead-Free” 16 Lead VFQFN	Tube	-40°C to 85°C
8S89834AKILFT	834A	“Lead-Free” 16 Lead VFQFN	Tape & Reel	-40°C to 85°C

Revision History

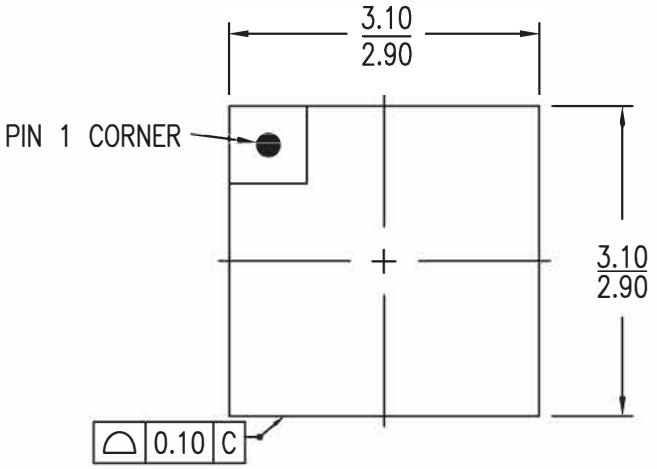
Revision Date	Description of Change
September 22, 2017	▪ Updated the package outline drawings; however, no mechanical changes ▪ Completed other minor improvements
January 27, 2016	▪ Removed ICS from part numbers where needed. ▪ General Description - Deleted ICS chip. ▪ Ordering Information - Deleted quantity from tape and reel. Deleted LF note below table. ▪ Updated header and footer.

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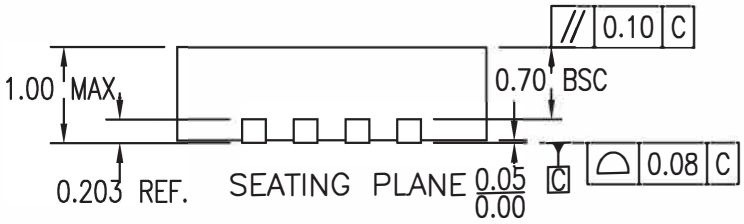
16L-QFN Package Outline Drawing

3.0 x 3.0 x 1.0 mm, 0.5 mm Pitch, 1.70 x 1.70 mm Epad

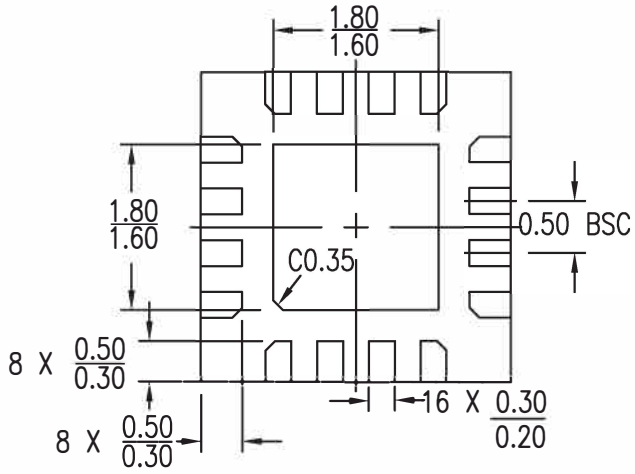
NL/NLG16P2, PSC-4169-02, Rev 03, Page 1



TOP VIEW



SIDE VIEW

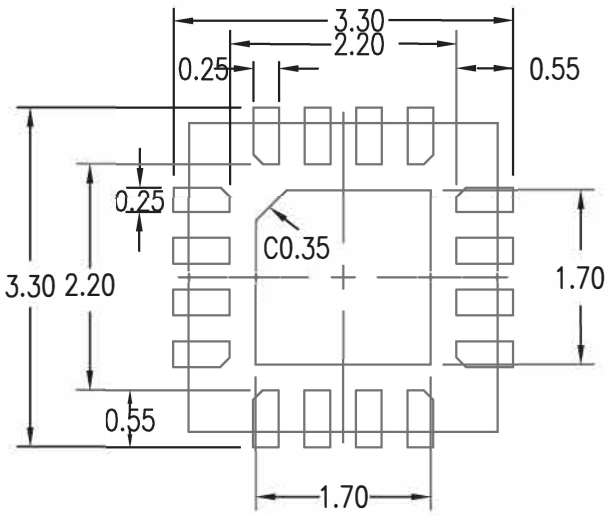


BOTTOM VIEW

NOTES:

1. ALL DIMENSIONS ARE IN mm.ANGLES IN DEGREES

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3.30
2.20
0.25
0.55
0.25
C0.35
3.30
2.20
1.70
0.55
1.70

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(Rev.1.0 Mar 2020)

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