Description

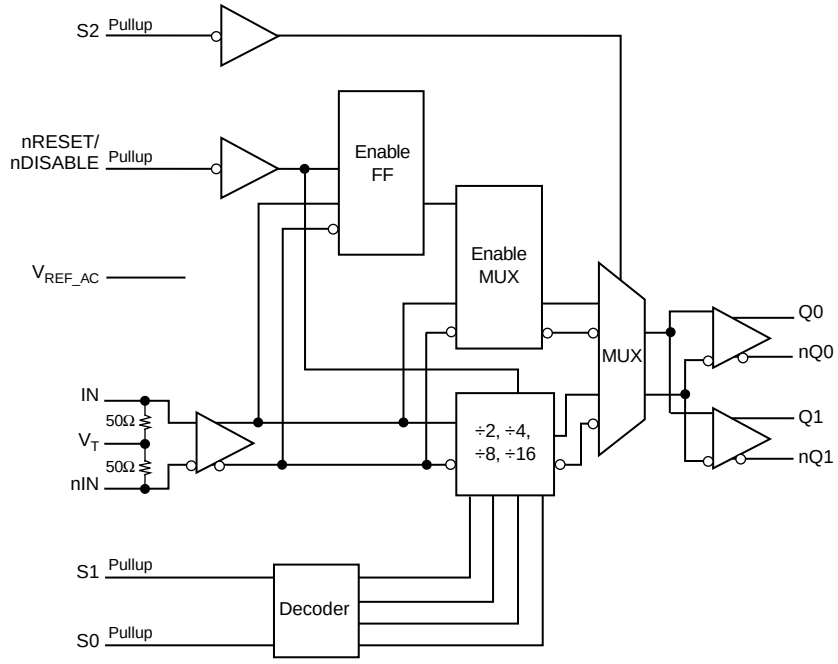
The 8S89875I is a high speed Differential-to-LVDS Buffer/Divider w/Internal Termination. The 8S89875I has selectable ÷1, ÷2, ÷4, ÷8, ÷16 output divider. The clock input has internal termination resistors, allowing it to interface with several differential signal types while minimizing the number of required external components.

The device is packaged in a small, 3mm x 3mm VFQFN package, making it ideal for use on space-constrained boards.

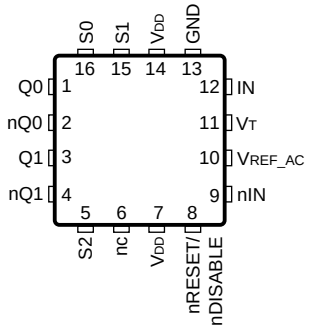
Features

- Two LVDS output pairs
- Frequency divide select options: ÷1, ÷2, ÷4, ÷8, ÷16
- IN, nIN input can accept the following differential input levels: LVPECL, LVDS, CML
- Input frequency: 2.5GHz (maximum)
- Cycle-to-cycle jitter, RMS: 4.1ps (maximum)
- Total jitter: 18ps (maximum)
- Output skew: 15ps (maximum)
- Part-to-part skew: 280ps (maximum)
- Propagation delay: 1000ps (maximum)
- Full 2.5V supply mode
- -40°C to 85°C ambient operating temperature
- Available in lead-free (RoHS 6) package
- Pin compatible with the obsolete device, 889875AK

Block Diagram



Pin Assignment



8S89875I

16-Lead VFQFN
3mm x 3mm x 0.9mm package body
K Package
Top View

Table 1. Pin Descriptions

Number	Name	Type		Description
1, 2	Q0, nQ0	Output		Differential output pair. Divide by 1, 2, 4, 8, or 16. Unused outputs must be terminated with 100Ω across the differential pair. LVDS interface levels.
3, 4	Q1, nQ1	Output		Differential output pair. Divide by 1, 2, 4, 8, or 16. Unused outputs must be terminated with 100Ω across the differential pair. LVDS interface levels.
5, 15, 16	S2, S1, S0	Input	Pullup	Select pins. Internal 37kΩ pullup resistor. Logic HIGH if left disconnected. Input threshold is V_{DD}/2. LVCMOS/LVTTL interface levels.
6	nc	Unused		No connect.
7, 14	V_{DD}	Power		Power supply pins.
8	nRESET/ nDISABLE	Input	Pullup	Synchronizing enable/disable pin. When LOW, resets the divider (divided by 2, 4, 8 or 16 mode) and sets the Qx outputs to a logic 0. When HIGH, the dividers and Qx outputs are enabled. The reset and disable function occurs on the next high-to-low clock input transition. Input threshold is V_{DD}/2V. Includes a 37kΩ pull-up resistor. LVTTL / LVCMOS interface levels.
9	nIN	Input		Inverting differential LVPECL clock input. R_T = 50Ω termination to V_T.
10	V_{REF_AC}	Output		Reference voltage for AC-coupled applications. Equal to V_{DD} – 1.35V (approx.). Maximum sink/source current is 2mA.
11	V_T	Input		Termination center-tap input.
12	IN	Input		Non-inverting LVPECL differential clock input. R_T = 50Ω termination to V_T.
13	GND	Power		Power supply ground.

NOTE: *Pullup* refers to internal input resistors. See Table 2, *Pin Characteristics,* for typical values.

Table 2. Pin Characteristics

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
R_{PULLUP}	Input Pullup Resistor			37		kΩ

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Function Tables

Table 3A. Control Input Function Table

Input	Outputs	
nRESET	**Q0, Q1**	**nQ0, nQ1**
0	Disabled; LOW	Disabled; HIGH
1 (default)	Enabled	Enabled

NOTE: After nRESET switches, the clock outputs are disabled or enabled following a falling input clock edge as shown in *Figure 1.*

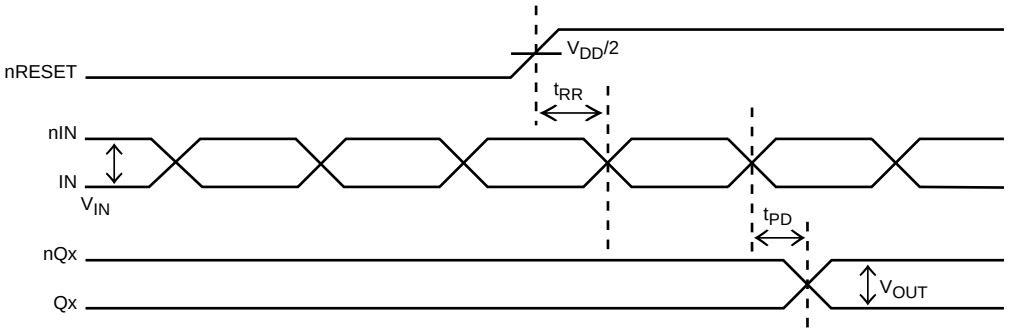


Figure 1. nRESET Timing Diagram

Table 3B. Truth Table

Inputs				Outputs
nRESET/nDISABLE	**S2**	**S1**	**S0**	**Q0, nQ0; Q1, nQ1**
1	0	X	X	Reference Clock (pass through)
1	1	0	0	Reference Clock ÷2
1	1	0	1	Reference Clock ÷4
1	1	1	0	Reference Clock ÷8
1	1	1	1	Reference Clock ÷16 (default)
0(NOTE 1)	X	X	X	Qx = LOW, nQx = HIGH; Clock disabled

NOTE 1: nReset/nDisable function is asserted on the next clock input (IN, nIN) high-to-low transition.

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Absolute Maximum Ratings

NOTE: Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics or AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Item	Rating
Supply Voltage, V_{DD}	4.6V
Inputs, V_I	-0.5V to V_{DD} + 0.5V
Outputs, I_O Continuous Current Surge Current	 10mA 15mA
Input Current, IN, nIN	±50mA
V_T Current, I_{VT}	±100mA
Input Sink/Source, I_{REF_AC}	±2mA
Operating Temperature Range, T_A	-40°C to +85°C
Package Thermal Impedance, θ_{JA}, (Junction-to-Ambient)	74.7°C/W (0 mps)
Storage Temperature, T_{STG}	-65°C to 150°C

NOTE: I_{OUT} refers to output current supplied by the 8S89875I only.

DC Electrical Characteristics

Table 4A. Power Supply DC Characteristics, V_{DD} = 2.5V ± 5%, T_A = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{DD}	Positive Supply Voltage		2.375	2.5	2.625	V
I_{DD}	Power Supply Current				68	mA

Table 4B. LVCMOS/LVTTL DC Characteristics, V_{DD} = 2.5V ± 5%, T_A = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{IH}	Input High Voltage		1.7		V_{DD} + 0.3	V
V_{IL}	Input Low Voltage		-0.3		0.7	V
I_{IH}	Input High Current	V_{DD} = V_{IN} = 2.625V			10	µA
I_{IL}	Input Low Current	V_{DD} = 2.625V, V_{IN} = 0V	-150			µA

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Table 4C. Differential DC Characteristics, V_{DD} = 2.5V ± 5%, T_A = -40°C to 85°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
R_{IN}	Differential Input Resistance	(IN, nIN)		80	100	120	Ω
V_{IH}	Input High Voltage	(IN, nIN)		1.2		V_{DD} + 0.05	V
V_{IL}	Input Low Voltage	(IN, nIN)		0		V_{DD} – 0.15	V
V_{IN}	Input Voltage Swing			0.15		1.2	V
V_{DIFF_IN}	Differential Input Voltage Swing			0.3			V
I_{IN}	Input Current	(IN, nIN)				45	mA
V_{REF_AC}	Bias Voltage			V_{DD} – 1.45	V_{DD} – 1.35	V_{DD} – 1.25	V

Table 4D. LVDS DC Characteristics, V_{DD} = 2.5V ± 5%, T_A = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{OUT}	Output Voltage Swing		247		454	mV
V_{OH}	Output High Voltage		1.4		1.95	V
V_{OL}	Output Low Voltage		1.05		1.55	V
V_{OCM}	Output Common Mode Voltage		1.15		1.45	V
ΔV_{OCM}	Change in Common Mode Voltage				50	mV

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AC Electrical Characteristics

Table 5. AC Characteristics, V_{DD} = 2.5V ± 5%, T_A = -40°C to 85°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
f_{IN}	Input Frequency					2.5	GHz
t_{PD}	Propagation Delay; NOTE 1	IN-to-Q		460		1000	ps
*t*sk(o)	Output Skew; NOTE 2, 3					15	ps
*t*sk(pp)	Part-to-Part Skew; NOTE 3, 4					280	ps
*t*jit(cc)	Additive Cycle-to-Cycle Jitter, RMS; NOTE 5					4.1	ps
*t*jit(j)	Additive Total Jitter; NOTE 6, 7					18	ps
t_{RR}	Reset Recovery Time			600			ps
t_R / t_F	Output Rise/Fall Time			60		250	ps

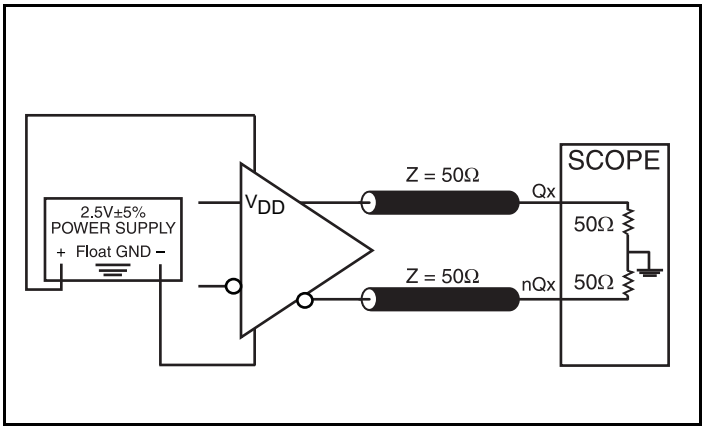
NOTE: Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfpm. The device will meet specifications after thermal equilibrium has been reached under these conditions.
All parameters characterized at ≤ 1.7GHz unless otherwise noted.
NOTE 1: Measured from the differential input crossing point to the differential output crossing point.
NOTE 2: Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at the output differential cross points.
NOTE 3: This parameter is defined in accordance with JEDEC Standard 65.
NOTE 4: Defined as skew between outputs on different devices operating at the same supply voltage, same temperature, same frequency and with equal load conditions. Using the same type of inputs on each device, the outputs are measured at the differential cross points.

NOTE 5: Additive Cycle-to-cycle jitter is calculated by: $\sqrt{\mathrm{tjit(cc)output}^2 - \mathrm{tjit(cc)input}^2}$.

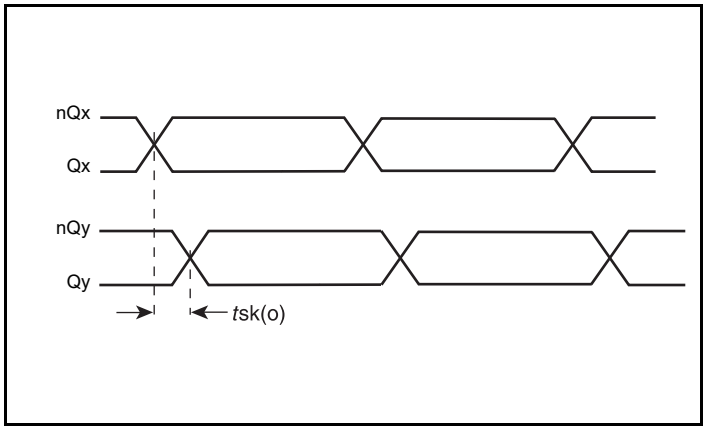
NOTE 6: Total Jitter was obtained using the dual-Dirac model and is calculated by: [RMS Multiplier * Random Jitter (R_J)] + Deterministic Jitter (D_J). The RMS multiplier of 14.26 used in the specification above corresponds to a bit error rate (BER) of 10E–12.
NOTE 7: Additive Total Jitter is the difference between the Total Jitter of the input and the output.

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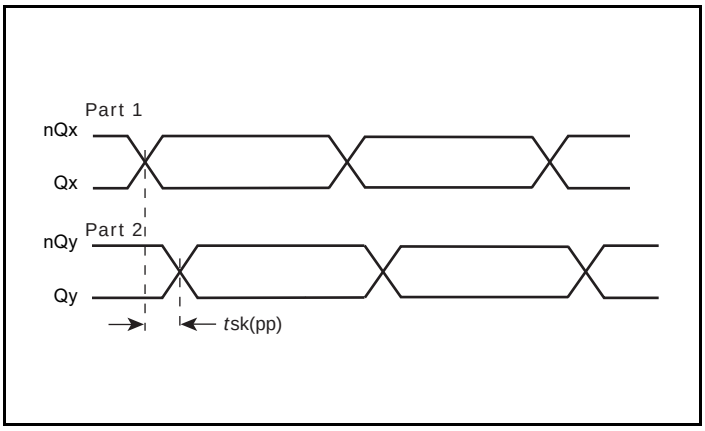
Parameter Measurement Information



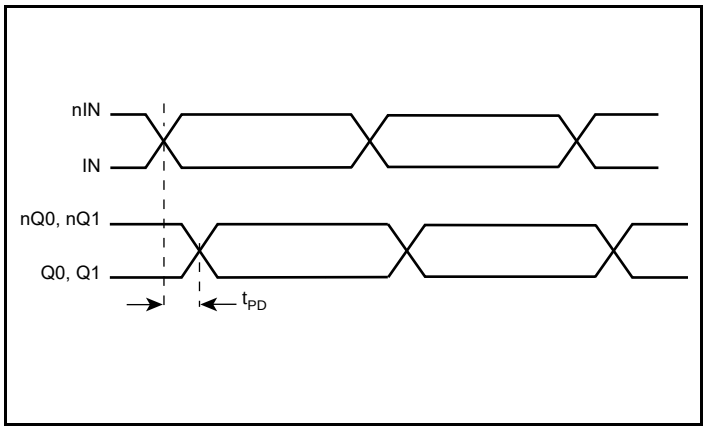
LVDS Output Load AC Test Circuit



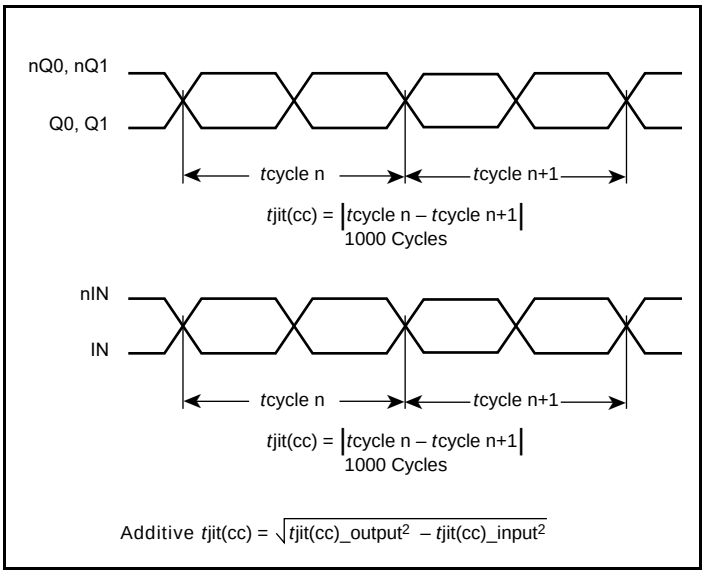
Output Skew



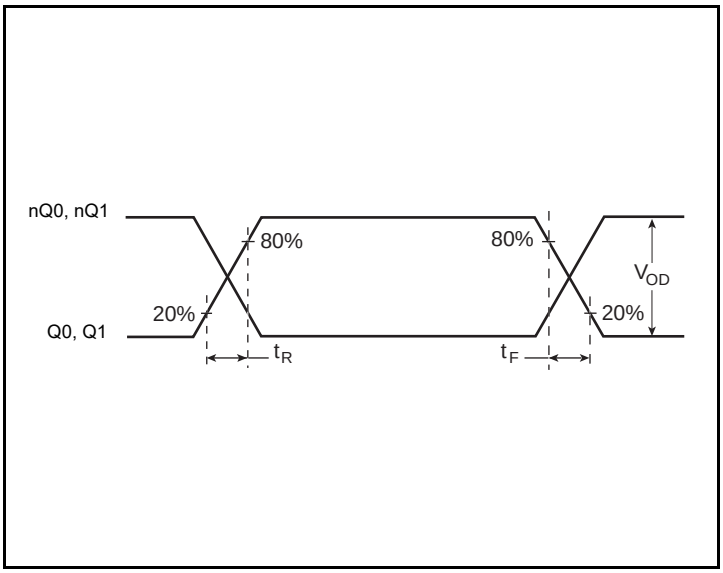
Part-to-Part Skew



Propagation Delay

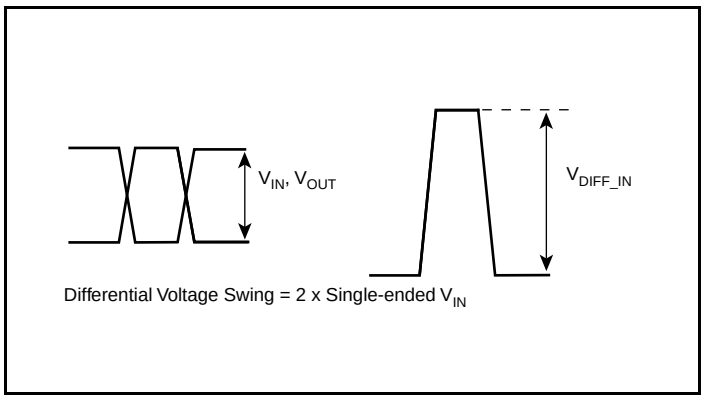


Additive Cycle-to-Cycle Jitter, RMS

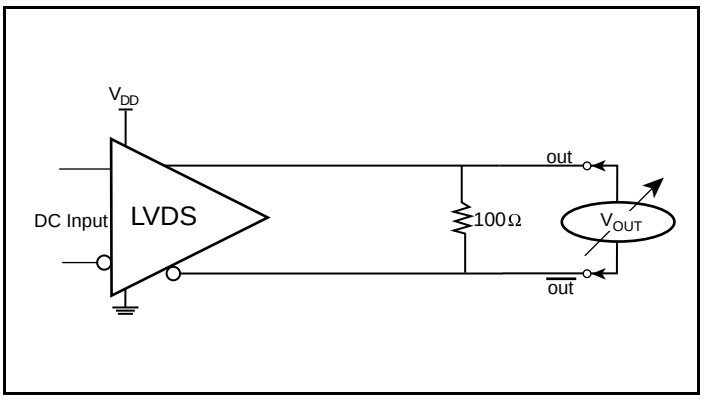


Output Rise/Fall Time

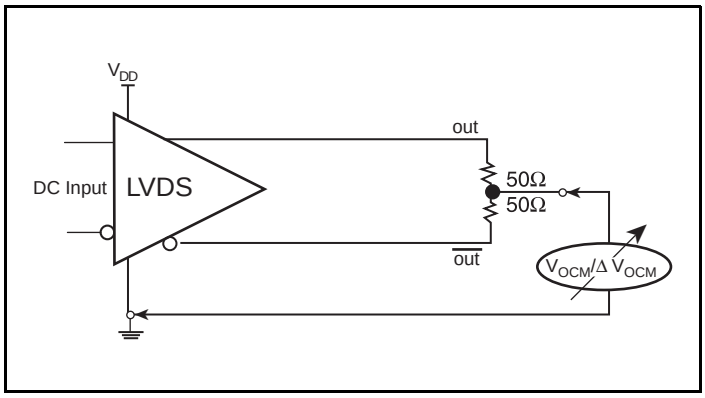
Parameter Measurement Information, continued



Single-Ended & Differential Input Voltage Swing



Differential Output Voltage Setup



Offset Voltage Setup

Applications Information

Recommendations for Unused Input Pins

Inputs:

LVCMOS Select Pins

All control pins have internal pullups; additional resistance is not required but can be added for additional protection. A 1kΩ resistor can be used.

Outputs:

LVDS Outputs

All unused LVDS output pairs can be either left floating or terminated with 100Ω across. If they are left floating, we recommend that there is no trace attached.

2.5V LVPECL Input with Built-In 50Ω Termination Interface

The IN /nIN with built-in 50Ω terminations accept LVDS, LVPECL, CML and other differential signals. Both signals must meet the V_{IN} and V_{IH} input requirements. *Figures 2A to 2D* show interface examples for the IN /nIN with built-in 50Ω termination input driven by the most common driver types. The input interfaces suggested here are examples only. If the driver is from another vendor, use their termination recommendation. Please consult with the vendor of the driver component to confirm the driver termination requirements.

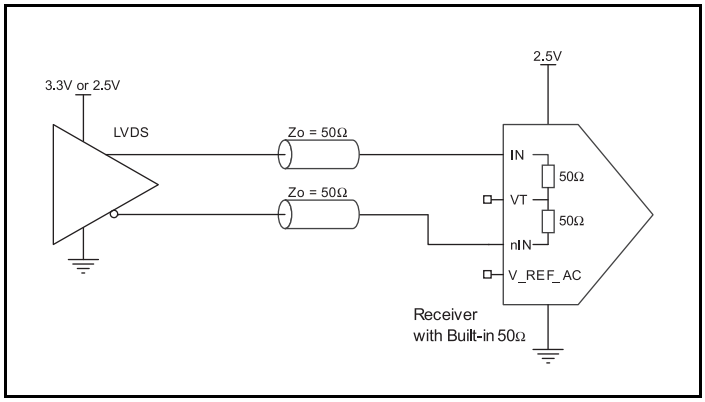


Figure 2A. IN/nIN Input with Built-In 50Ω Driven by an LVDS Driver

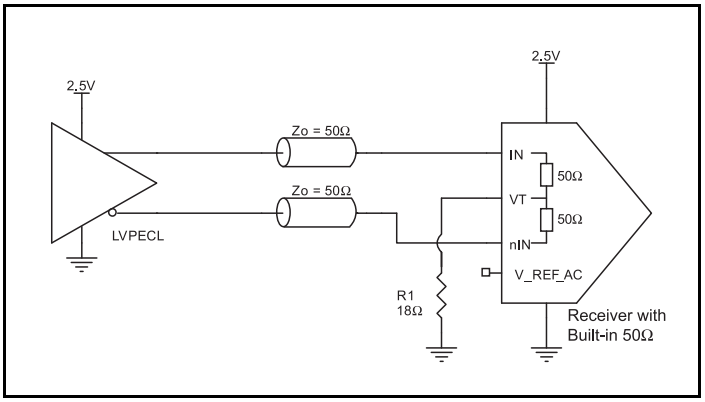


Figure 2B. IN/nIN Input with Built-In 50Ω Driven by an LVPECL Driver

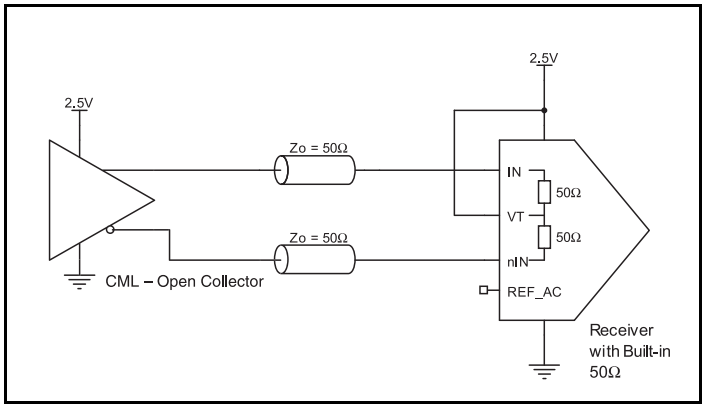


Figure 2C. IN/nIN Input with Built-In 50Ω Driven by a CML Driver

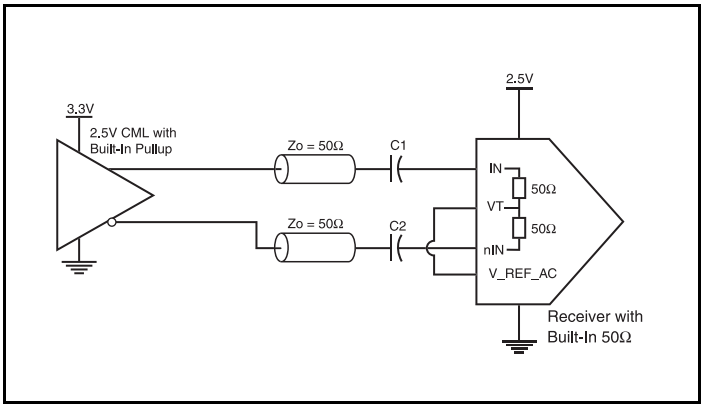


Figure 2D. IN/nIN Input with Built-In 50Ω Driven by a CML Driver with Built-In 50Ω Pullup

VFQFN EPAD Thermal Release Path

In order to maximize both the removal of heat from the package and the electrical performance, a land pattern must be incorporated on the Printed Circuit Board (PCB) within the footprint of the package corresponding to the exposed metal pad or exposed heat slug on the package, as shown in *Figure 3.* The solderable area on the PCB, as defined by the solder mask, should be at least the same size/shape as the exposed pad/slug area on the package to maximize the thermal/electrical performance. Sufficient clearance should be designed on the PCB between the outer edges of the land pattern and the inner edges of pad pattern for the leads to avoid any shorts.

While the land pattern on the PCB provides a means of heat transfer and electrical grounding from the package to the board through a solder joint, thermal vias are necessary to effectively conduct from the surface of the PCB to the ground plane(s). The land pattern must be connected to ground through these vias. The vias act as “heat pipes”. The number of vias (i.e. “heat pipes”) are application specific

and dependent upon the package power dissipation as well as electrical conductivity requirements. Thus, thermal and electrical analysis and/or testing are recommended to determine the minimum number needed. Maximum thermal and electrical performance is achieved when an array of vias is incorporated in the land pattern. It is recommended to use as many vias connected to ground as possible. It is also recommended that the via diameter should be 12 to 13mils (0.30 to 0.33mm) with 1oz copper via barrel plating. This is desirable to avoid any solder wicking inside the via during the soldering process which may result in voids in solder between the exposed pad/slug and the thermal land. Precautions should be taken to eliminate any solder voids between the exposed heat slug and the land pattern. Note: These recommendations are to be used as a guideline only. For further information, please refer to the Application Note on the Surface Mount Assembly of Amkor’s Thermally/ Electrically Enhance Leadframe Base Package, Amkor Technology.

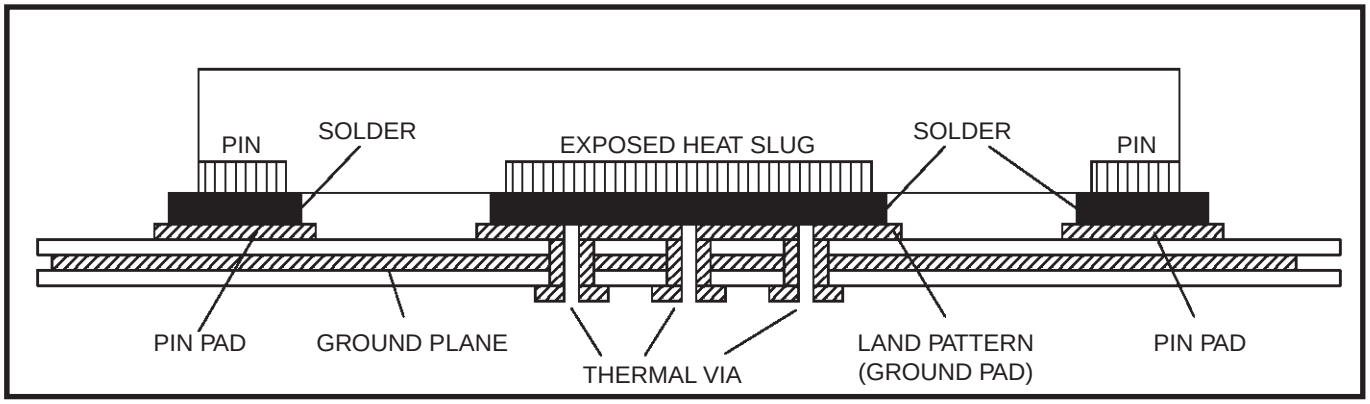


Figure 3. P.C. Assembly for Exposed Pad Thermal Release Path – Side View (drawing not to scale)

LVDS Driver Termination

A general LVDS interface is shown in *Figure 4.* Standard termination for LVDS type output structure requires both a 100Ω parallel resistor at the receiver and a 100Ω differential transmission line environment. In order to avoid any transmission line reflection issues, the 100Ω resistor must be placed as close to the receiver as possible. IDT offers a full line of LVDS compliant devices with two types of output structures: current source and voltage source. The standard termination schematic as shown in Figure 4 can be used with either type of output structure. If using a non-standard termination, it is recommended to contact IDT and confirm if the output is a current source or a voltage source type structure. In addition, since these outputs are LVDS compatible, the amplitude and common mode input range of the input receivers should be verified for compatibility with the output.

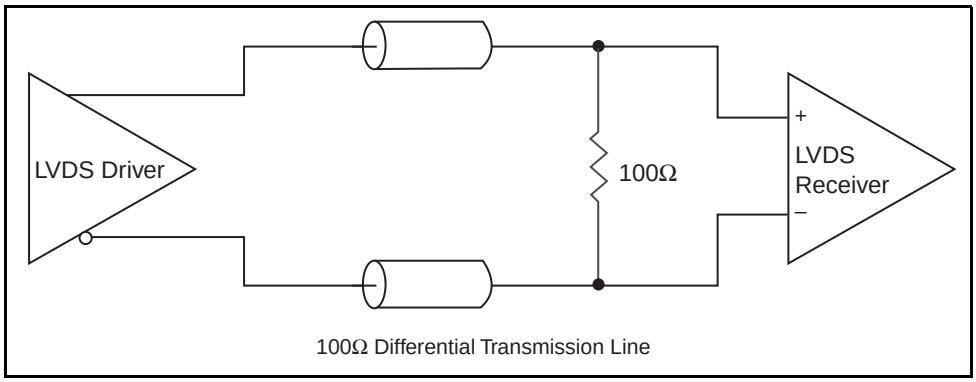


Figure 4. Typical LVDS Driver Termination

Schematic Example

Figure 5 shows a schematic example of the 8S89875I. This schematic provides examples of input and output handling. The 8S89875I input has built-in 50Ω termination resistors. The input can directly accept various types of differential signals without AC coupling. For AC coupling termination, the 8S89875I also provides the V_{REF_AC} pin for proper offset bias. This example shows the 8S89875I input driven by a 2.5V LVPECL driver. The 8S89875I outputs are LVDS drivers. In this example, we assume the traces are long transmission lines and the receivers of the LVDS drivers have high input impedance without built-in termination.

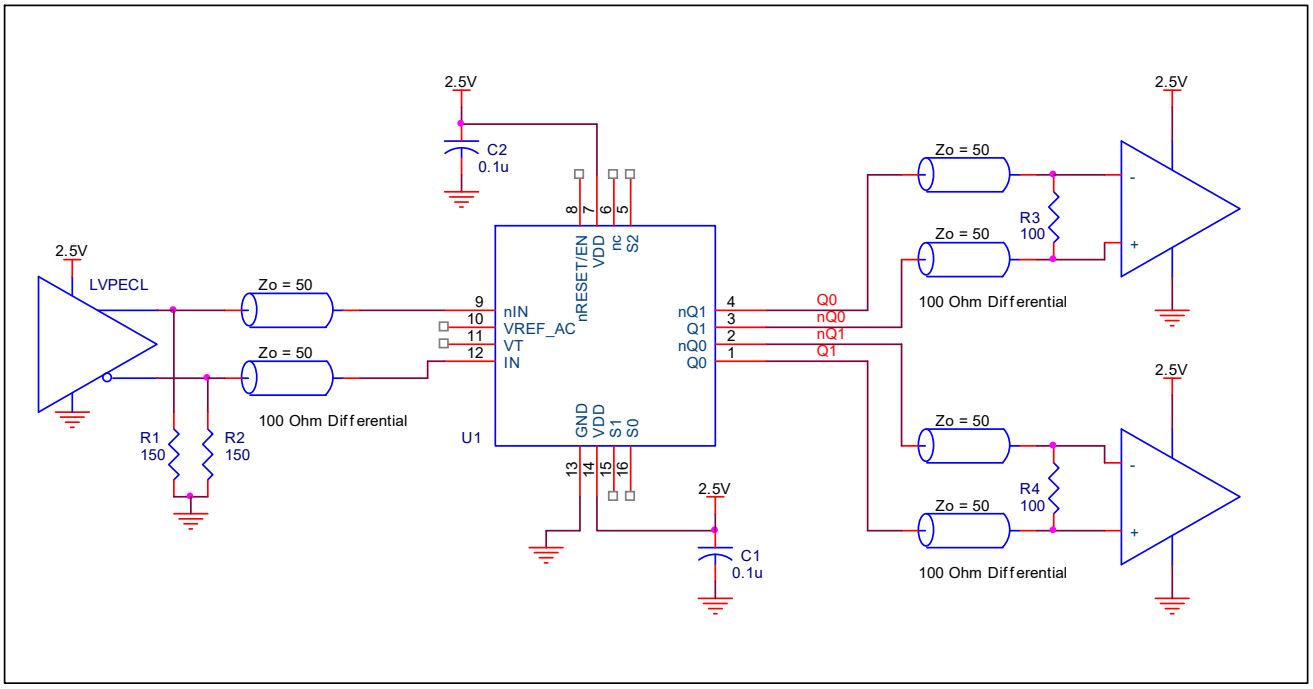


Figure 5. 8S89875I Schematic Example

Power Considerations

This section provides information on power dissipation and junction temperature for the 8S89875I.
Equations and example calculations are also provided.

1. Power Dissipation.

The total power dissipation for the 8S89875I is the sum of the core power plus the power dissipated in the load(s).
The following is the power dissipation for V_{DD} = 2.5V + 5% = 2.625V, which gives worst case results.

- Power$__{MAX}$ = V_{DD_MAX} * I_{DD_MAX} = 2.625V *68mA = **178.5mW**
- Power Dissipation for internal termination R_T
  Power $(R_T)_{MAX}$ = $(V_{IN_MAX})^2$ / R_{T_MIN} = $(1.2V)^2$ / 80Ω = **18mW**

Total Power$__{MAX}$ (2.625V, with all outputs switching) = 178.5mW + 18mW + 18mW = **196.5mW**

2. Junction Temperature.

Junction temperature, Tj, is the temperature at the junction of the bond wire and bond pad, and directly affects the reliability of the device. The maximum recommended junction temperature is 125°C. Limiting the internal transistor junction temperature, Tj, to 125°C ensures that the bond wire and bond pad temperature remains below 125°C.

The equation for Tj is as follows: Tj = θ_{JA} * Pd_total + T_A

Tj = Junction Temperature

θ_{JA} = Junction-to-Ambient Thermal Resistance

Pd_total = Total Device Power Dissipation (example calculation is in section 1 above)

T_A = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance θ_{JA} must be used. Assuming no air flow and a multi-layer board, the appropriate value is 74.7°C/W per Table 6 below.

Therefore, Tj for an ambient temperature of 85°C with all outputs switching is:

85°C + 0.197W * 74.7°C/W = 99.7°C. This is below the limit of 125°C.

This calculation is only an example. Tj will obviously vary depending on the number of loaded outputs, supply voltage, air flow and the type of board (multi-layer).

Table 6. Thermal Resistance θ_{JA} for 16 Lead VFQFN, Forced Convection

θ_{JA} by Velocity			
Meters per Second	**0**	**1**	**2.5**
Multi-Layer PCB, JEDEC Standard Test Boards	74.7°C/W	65.3°C/W	58.5°C/W

Reliability Information

Table 7. θ_{JA} vs. Air Flow Table for a 16 Lead VFQFN

θ_{JA} by Velocity			
Meters per Second	**0**	**1**	**2.5**
Multi-Layer PCB, JEDEC Standard Test Boards	74.7°C/W	65.3°C/W	58.5°C/W

Transistor Count

The transistor count for 8S89875I is: 506

Package Outline Drawings

The package outline drawings are located at the end of this document. The package information is the most current data available and is subject to change without notice or revision of this document.

Ordering Information

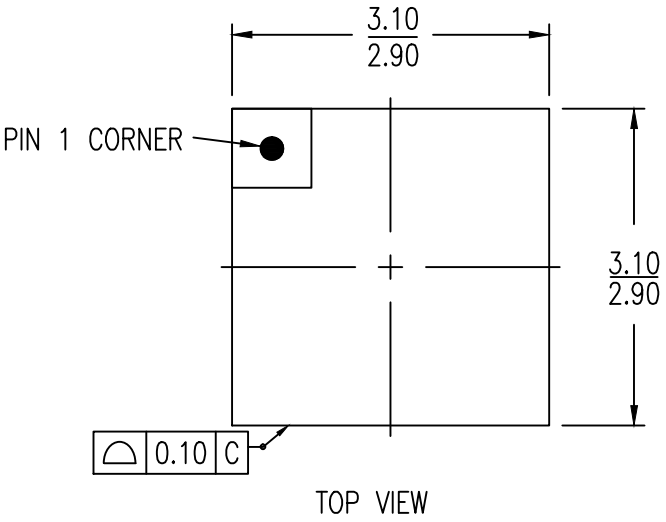
Table 8. Ordering Information

Part/Order Number	Marking	Package	Shipping Packaging	Temperature
8S89875AKILF	875A	“Lead-Free” 16 Lead VFQFN	Tube	-40°C to 85°C
8S89875AKILFT	875A	“Lead-Free” 16 Lead VFQFN	Tape & Reel	-40°C to 85°C

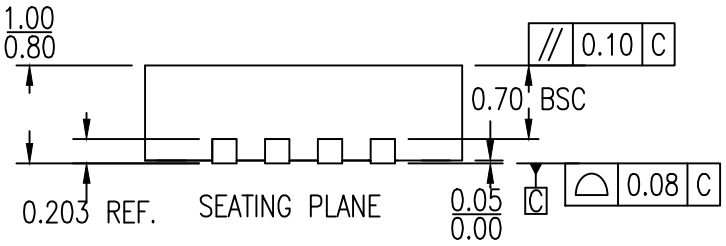
Revision History

Revision Date	Description of Change
January 11, 2018	▪ Updated the package outline drawings; however, no mechanical changes
February 9, 2016	▪ Removed ICS from the part number where needed. ▪ Ordering Information - removed LF note below table. Removed quantity from tape and reel. ▪ Updated header and footer.

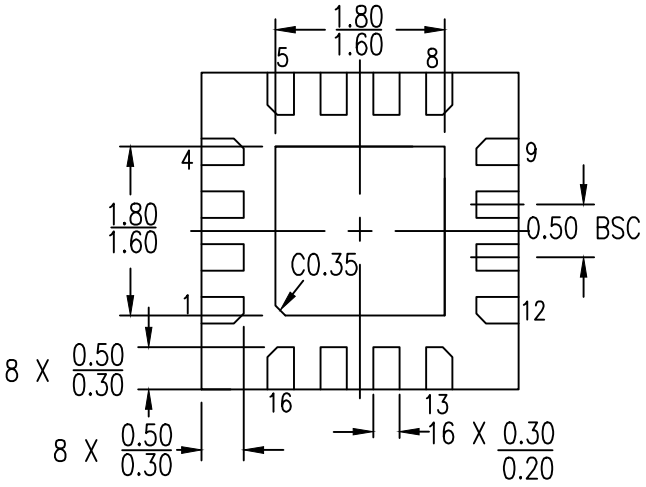
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TOP VIEW



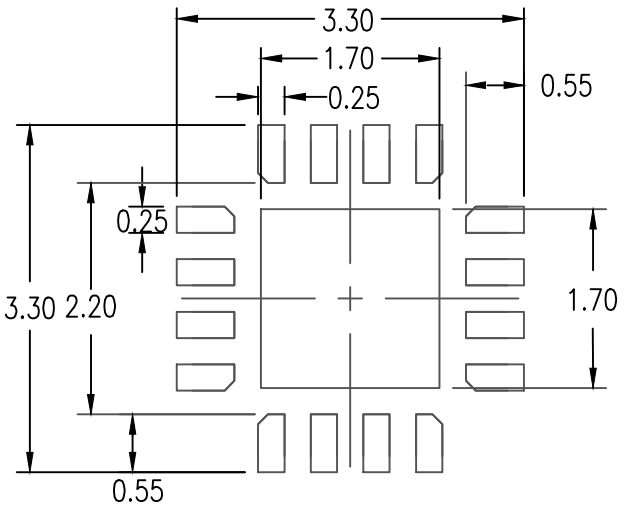
SIDE VIEW



BOTTOM VIEW

NOTES:
1. ALL DIMENSIONS ARE IN mm. ANGLES IN DEGREES

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RECOMMENDED LAND PATTERN DIMENSION

NOTES:
1. ALL DIMENSIONS ARE IN mm. ANGLES IN DEGREES
2. TOP DOWN VIEW–AS VIEWED ON PCB
3. LAND PATTERN RECOMMENDATION IS PER IPC–7351B GENERIC REQUIREMENT FOR SURFACE MOUNT DESIGN AND LAND PATTERN

Package Revision History		
Date Created	Rev No.	Description
Oct 25, 2017	Rev 04	Remove Bookmak at Pdf Format & Update Thickness Tolerance
Aug 15, 2017	Rev 03	Update Epad Range

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