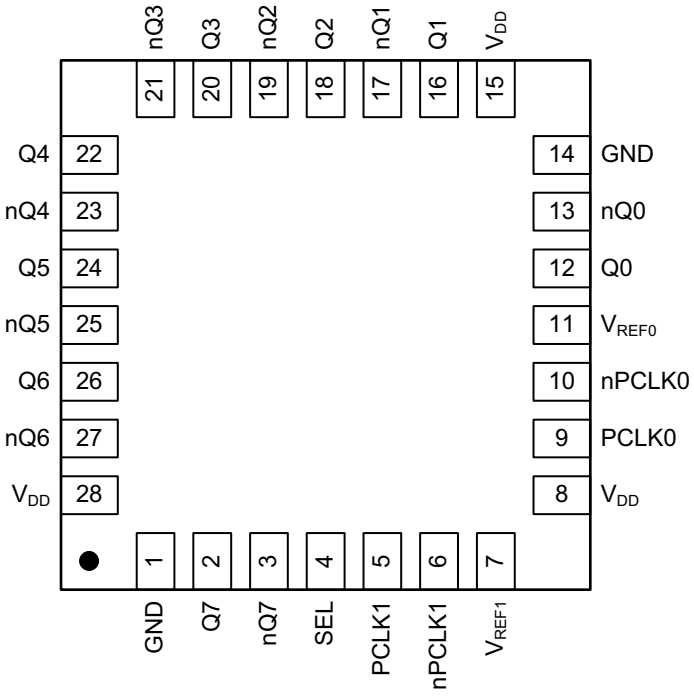
General Description

The IDT8SLVD1208-33I is a high-performance differential LVDS fanout buffer. The device is designed for the fanout of high-frequency, very low additive phase-noise clock and data signals. The IDT8SLVD1208-33I is characterized to operate from a 3.3V power supply. Guaranteed output-to-output and part-to-part skew characteristics make the IDT8SLVD1208-33I ideal for those clock distribution applications demanding well-defined performance and repeatability. Two selectable differential inputs and eight low skew outputs are available. The integrated bias voltage reference enables easy interfacing of single-ended signals to the device inputs. The device is optimized for low power consumption and low additive phase noise.

Features

- Eight low skew, low additive jitter LVDS output pairs
- Two selectable, differential clock input pairs
- Differential PCLK, nPCLK pairs can accept the following differential input levels: LVDS, LVPECL
- Maximum input clock frequency: 2GHz (maximum)
- LVCMOS/LVTTL interface levels for the control select input
- Output skew: 8ps (typical)
- Propagation delay: 240ps (typical)
- Low additive phase jitter, RMS; f_{REF} = 156.25MHz, V_{PP} = 1V, 10kHz - 20MHz: 82fs (typical)
- Maximum device current consumption (I_{DD}): 190mA (maximum) @ 3.465V
- 3.3V supply voltage
- Lead-free (RoHS 6), 28-Lead VFQFN package
- -40°C to 85°C ambient operating temperature

Pin Assignment



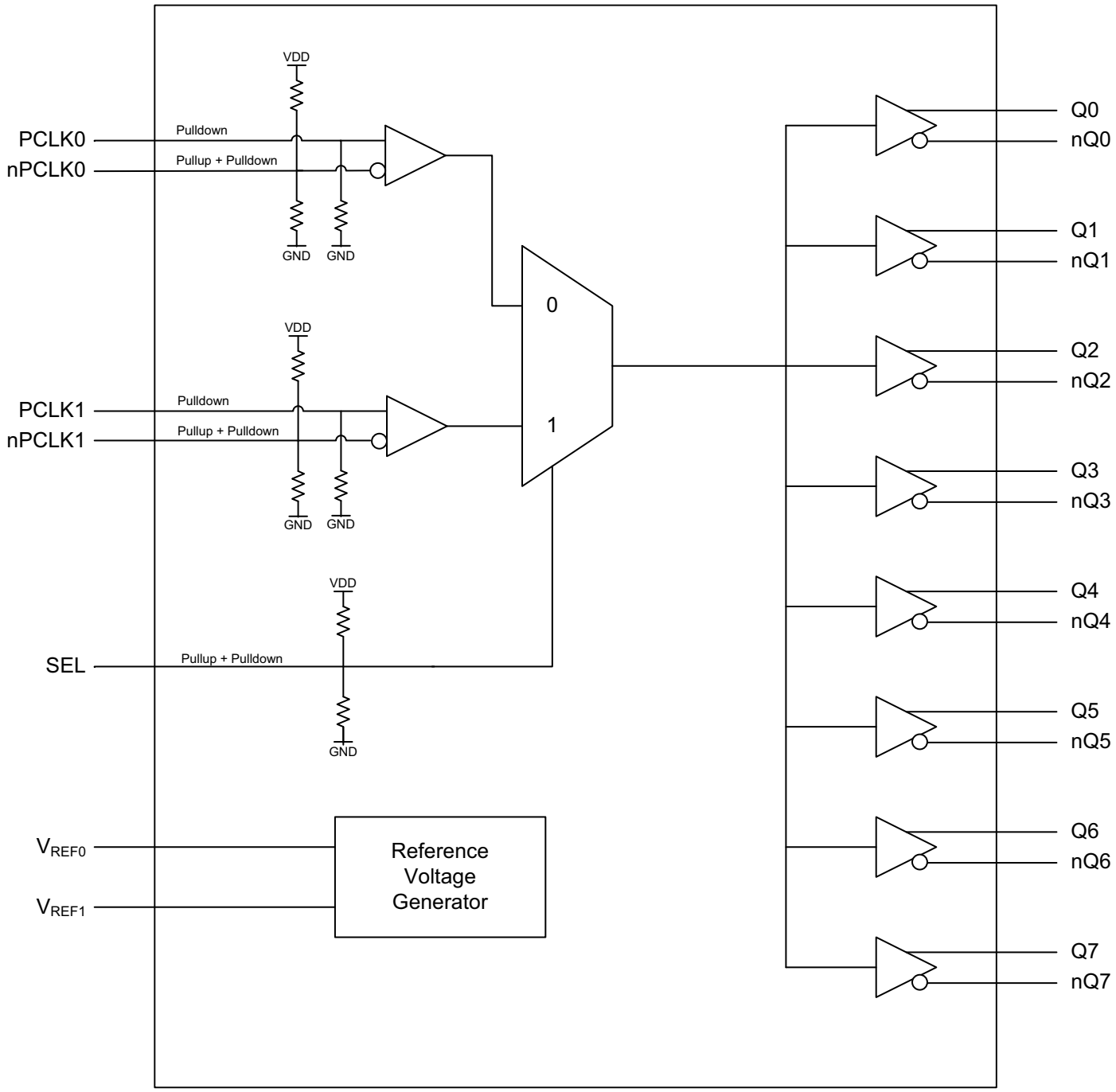
IDT8SLVD1208-33I

28 lead VFQFN
5.0mm x 5.0mm x 0.925mm package body
E-Pad size 3.25mm x 3.25 mm
NB Package

Top View

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Block Diagram



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Pin Descriptions and Characteristics

Table 1. Pin Descriptions

Number	Name	Type		Description
1,14	GND	Power		Power supply pin.
4	SEL	Input	Pullup/ Pulldown	Reference select control pin. See Table 3 for function. LVCMOS/LVTTL interface levels.
5	PCLK1	Input	Pulldown	Non-inverting differential clock/data input.
6	nPCLK1	Input	Pullup/ Pulldown	Inverting differential clock/data input. $V_{DD}/2$ default when left floating.
8,15,28	V_{DD}	Power		Power supply pin.
9	PCLK0	Input	Pulldown	Non-inverting differential clock/data input.
10	nPCLK0	Input	Pullup/ Pulldown	Inverting differential clock/data input. $V_{DD}/2$ default when left floating.
11	V_{REF0}	Output		Bias voltage reference for the PCLK0, nPCLK0 inputs.
7	V_{REF1}	Output		Bias voltage reference for the PCLK1, nPCLK1 inputs.
12, 13	Q0, nQ0	Output		Differential clock output pair. LVDS interface levels.
16, 17	Q1, nQ1	Output		Differential clock output pair. LVDS interface levels.
18, 19	Q2, nQ2	Output		Differential clock output pair. LVDS interface levels.
20, 21	Q3, nQ3	Output		Differential clock output pair. LVDS interface levels.
22, 23	Q4, nQ4	Output		Differential clock output pair. LVDS interface levels.
24, 25	Q5, nQ5	Output		Differential clock output pair. LVDS interface levels.
26, 27	Q6, nQ6	Output		Differential clock output pair. LVDS interface levels.
2, 3	Q7, nQ7	Output		Differential clock output pair. LVDS interface levels.

NOTE: *Pulldown* and *Pullup* refers to internal input resistors. See Table 2, *Pin Characteristics,* for typical values.

Table 2. Pin Characteristics

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
C_{IN}	Input Capacitance			2		pF
$R_{PULLDOWN}$	Input Pulldown Resistor			51		kΩ
R_{PULLUP}	Input Pullup Resistor			51		kΩ

Function Table

Table 3. SEL Input Selection Function Table

Input SEL	Operation
0	PCLK0, nPCLK0 is the selected differential clock input.
1	PCLK1, nPCLK1 is the selected differential clock input.
Open	Input buffers are disabled and outputs are static.

NOTE: SEL is an asynchronous control.

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Absolute Maximum Ratings

NOTE: Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics or AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Item	Rating
Supply Voltage, V_{DD}	4.6V
Inputs, V_I	-0.5V to V_{DD} + 0.5V
Outputs, I_O (LVPECL) Continuous Current Surge Current	 10mA 15mA
Input Sink/Source, I_{REF}	±2mA
Maximum Junction Temperature, $T_{J,MAX}$	125°C
Storage Temperature, T_{STG}	-65°C to 150°C
ESD - Human Body Model, NOTE 1	2000V
ESD - Charged Device Model, NOTE 1	1500V

NOTE 1: According to JEDEC/JS-001-2012/ 22-C101E.

DC Electrical Characteristics

Table 4A. Power Supply DC Characteristics, V_{DD} = 3.3V ± 5%, T_A = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{DD}	Power Supply Voltage		3.135	3.3	3.465	V
I_{DD}	Power Supply Current	Q0 to Q7 terminated 100Ω between nQx, Qx		170	190	mA

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Table 4B. LVCMOS/LVTTL DC Characteristics, V_{DD} = 3.3V ± 5%, T_A = -40°C to 85°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
V_{MID}	Input voltage - open pin		Open		V_{DD} / 2		V
V_{IH}	Input High Voltage	SEL		0.7 * V_{DD}		V_{DD} + 0.3	V
V_{IL}	Input Low Voltage	SEL		-0.3		0.2 * V_{DD}	V
I_{IH}	Input High Current	SEL	V_{DD} = V_{IN} = 3.465V			150	µA
I_{IL}	Input Low Current	SEL	V_{DD} = 3.465V, V_{IN} = 0V	-150			µA

Table 4C. Differential Inputs Characteristics, V_{DD} = 3.3V ± 5%, T_A = -40°C to 85°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
I_{IH}	Input High Current	PCLK0, nPCLK0 PCLK1, nPCLK1	V_{IN} = V_{DD} = 3.465V			150	µA
I_{IL}	Input Low Current	PCLK0, PCLK1	V_{IN} = 0V, V_{DD} = 3.465V	-10			µA
		nPCLK0, nPCLK1	V_{IN} = 0V, V_{DD} = 3.465V	-150			µA
V_{REF0}, V_{REF1}	Reference Voltage for Input Bias		I_{REFx} = ±1mA	V_{DD} – 1.5	V_{DD} – 1.25	V_{DD} – 1.15	V
V_{PP}	Peak-to-Peak Voltage; NOTE 1		f_{REF} < 1.5 GHz	0.1		1.5	V
			f_{REF} > 1.5 GHz	0.2		1.5	V
V_{CMR}	Common Mode Input Voltage; NOTE 1, 2			1.0		V_{DD} – 0.6	V

NOTE 1: V_{IL} should not be less than -0.3V.
NOTE 2: Common mode input voltage is defined as crosspoint voltage.

Table 4D. LVDS DC Characteristics, V_{DD} = 3.3V ± 5%, T_A = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{OD}	Differential Output Voltage	Outputs loaded with 100Ω	247		454	mV
ΔV_{OD}	V_{OD} Magnitude Change				50	mV
V_{OS}	Offset Voltage		1.125		1.55	V
ΔV_{OS}	V_{OS} Magnitude Change				50	mV

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AC Electrical Characteristics

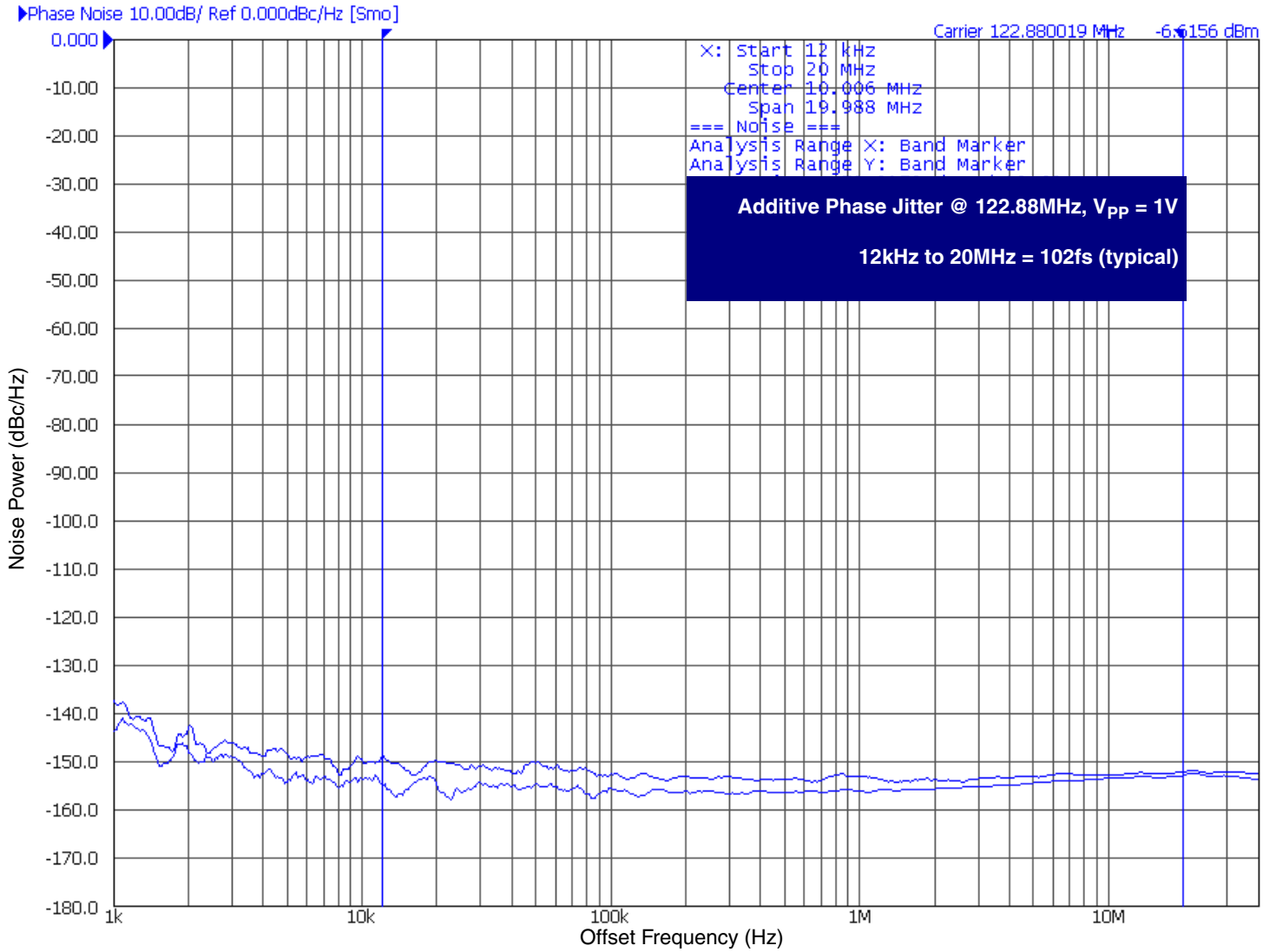
Table 5. AC Electrical Characteristics, V_{DD} = 3.3V ± 5%, T_A = -40°C to 85°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
f_{REF}	Input Frequency	PCLK[0:1], nPCLK[0:1]				2	GHz
ΔV/Δt	Input Edge Rate	PCLK[0:1], nPCLK[0:1]		1.5			V/ns
t_{PD}	Propagation Delay; NOTE 1		PCKx, nPCLKx to any Qx, nQx for V_{PP} = 0.1V or 0.3V	150	240	330	ps
*t*sk(o)	Output Skew; NOTE 2, 3					40	ps
*t*sk(i)	Input Skew; NOTE 3					60	ps
*t*sk(p)	Pulse Skew		f_{REF} = 100MHz			25	ps
*t*sk(pp)	Part-to-Part Skew; NOTE 3, 4					230	ps
t_{JIT}	Buffer Additive Phase Jitter, RMS; refer to Additive Phase Jitter Section		f_{REF} = 122.88MHz Square Wave, V_{PP} = 1V, Integration Range: 1kHz – 40MHz		134	185	fs
			f_{REF} = 122.88MHz Square Wave, V_{PP} = 1V, Integration Range: 10kHz – 20MHz		102	140	fs
			f_{REF} = 122.88MHz Square Wave, V_{PP} = 1V, Integration Range: 12kHz – 20MHz		102	140	fs
			f_{REF} = 156.25MHz Square Wave, V_{PP} = 1V, Integration Range: 1kHz – 40MHz		112	190	fs
			f_{REF} = 156.25MHz Square Wave, V_{PP} = 1V, Integration Range: 10kHz – 20MHz		82	150	fs
			f_{REF} = 156.25MHz Square Wave, V_{PP} = 1V, Integration Range: 12kHz – 20MHz		82	150	fs
			f_{REF} = 156.25MHz Square Wave, V_{PP} = 0.5V, Integration Range: 1kHz – 40MHz		103	160	fs
			f_{REF} = 156.25MHz Square Wave, V_{PP} = 0.5V, Integration Range: 10kHz – 20MHz		78	150	fs
			f_{REF} = 156.25MHz Square Wave, V_{PP} = 0.5V, Integration Range: 12kHz – 20MHz		78	150	fs
t_R / t_F	Output Rise/ Fall Time		20% to 80% outputs loaded with 100Ω	30	100	300	ps
$MUX_{ISOLATION}$	Mux Isolation; NOTE 5		f_{REF} = 100MHz		-82		dB

NOTE: Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfpm. The device will meet specifications after thermal equilibrium has been reached under these conditions.
NOTE 1: Measured from the differential input crosspoint to the differential output crosspoint.
NOTE 2: Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at the differential crosspoint.
NOTE 3: This parameter is defined in accordance with JEDEC Standard 65.
NOTE 4: Defined as skew between outputs on different devices operating at the same supply voltage, same frequency, same temperature and with equal load conditions. Using the same type of inputs on each device, the outputs are measured at the differential crosspoint.
NOTE 5: Qx, nQx outputs measured differentially. See *MUX Isolation diagram* in the *Parameter Measurement Information section.*

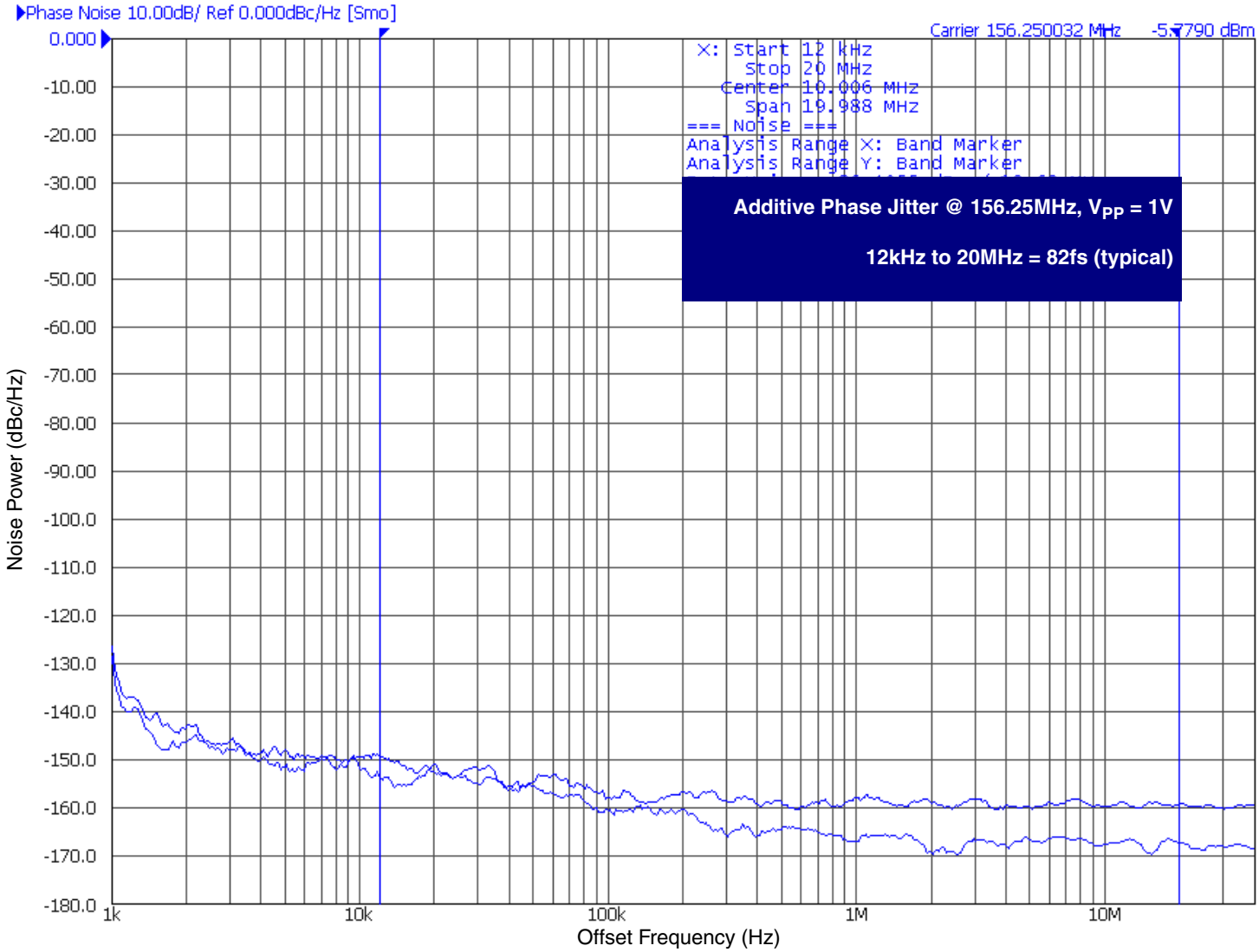
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Typical Phase Noise at 122.88MHz



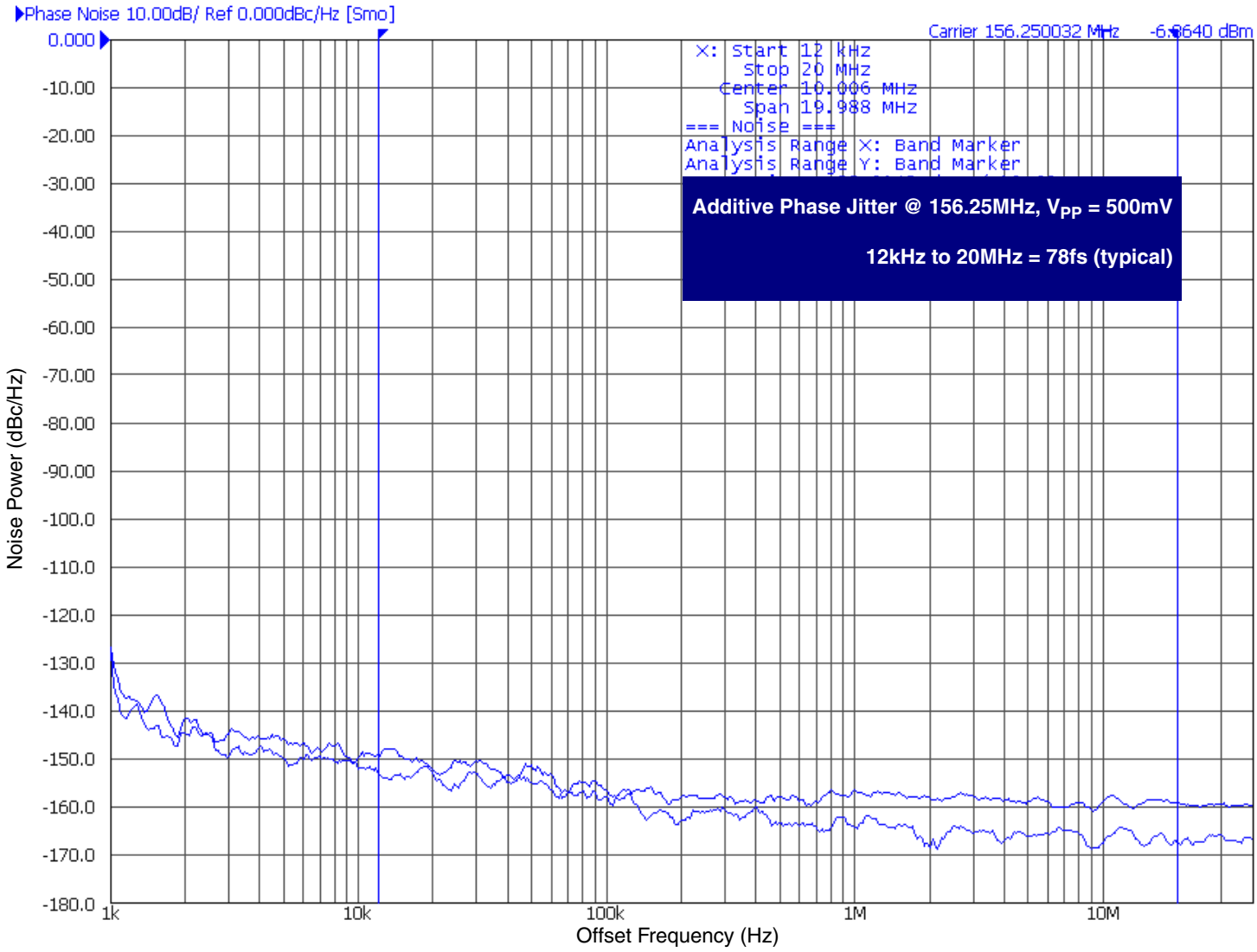
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Typical Phase Noise at 156.25MHz



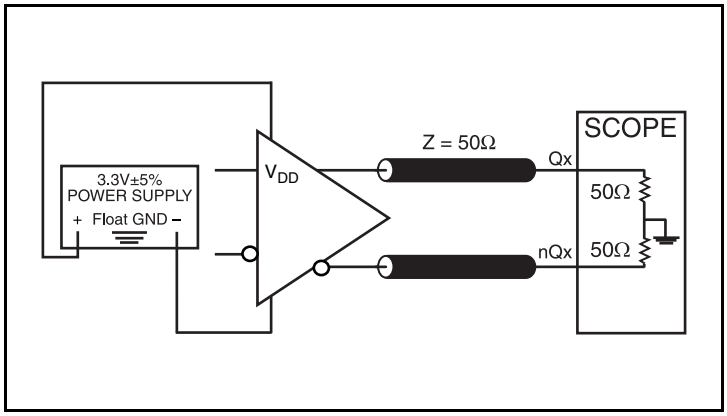
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Typical Phase Noise at 156.25MHz

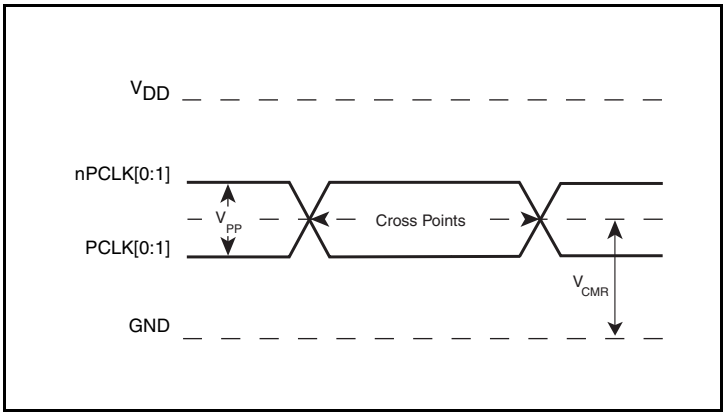


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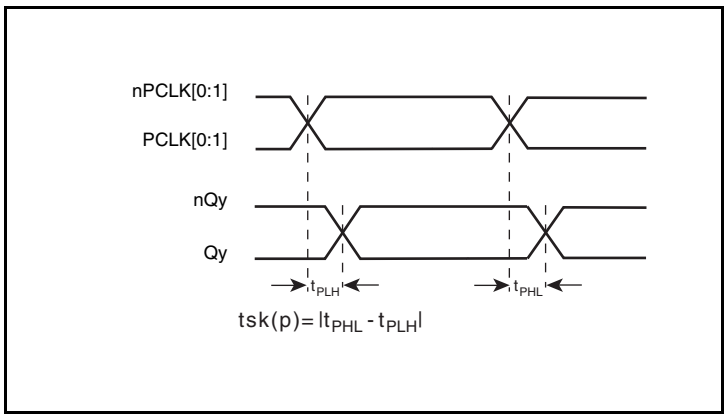
Parameter Measurement Information



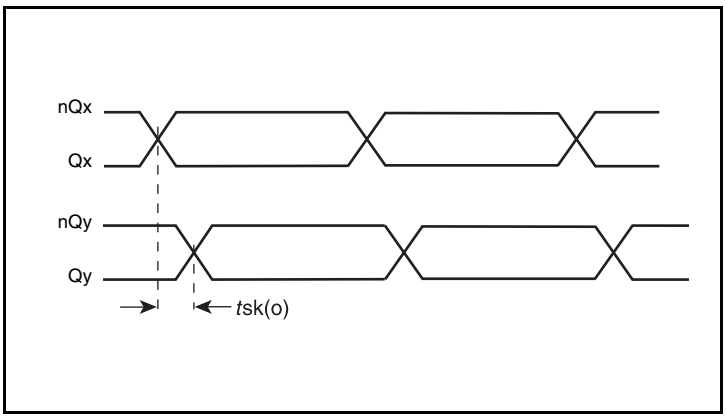
3.3V LVDS Output Load Test Circuit



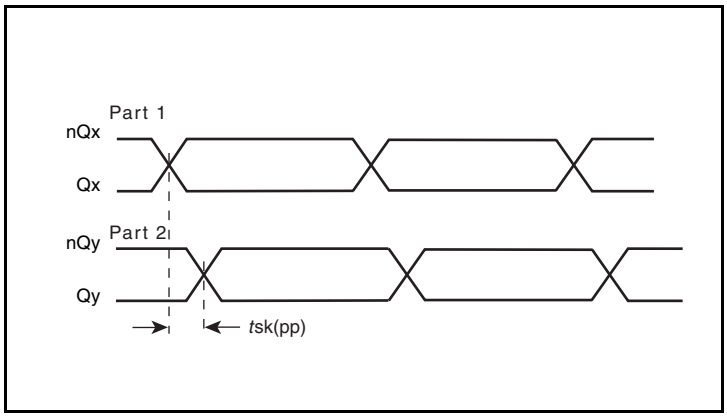
Differential Input Level



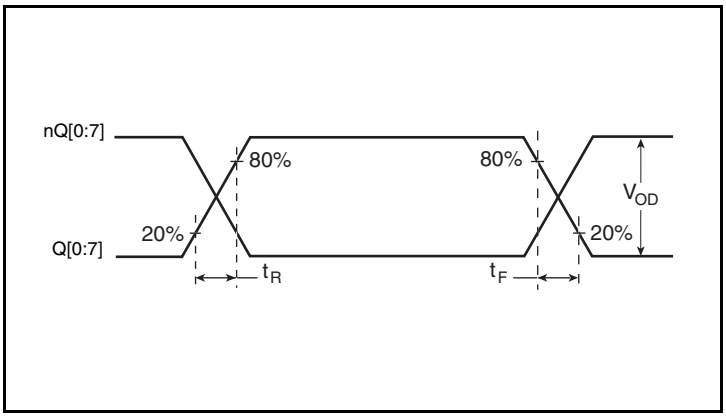
Pulse Skew



Output Skew



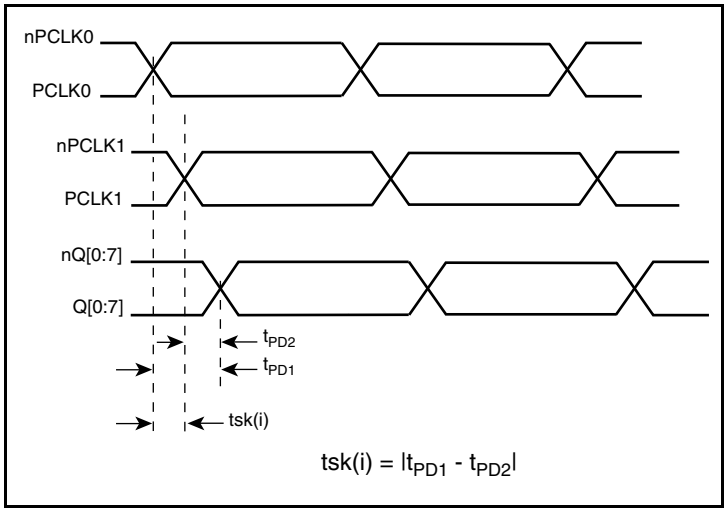
Part-to-Part Skew



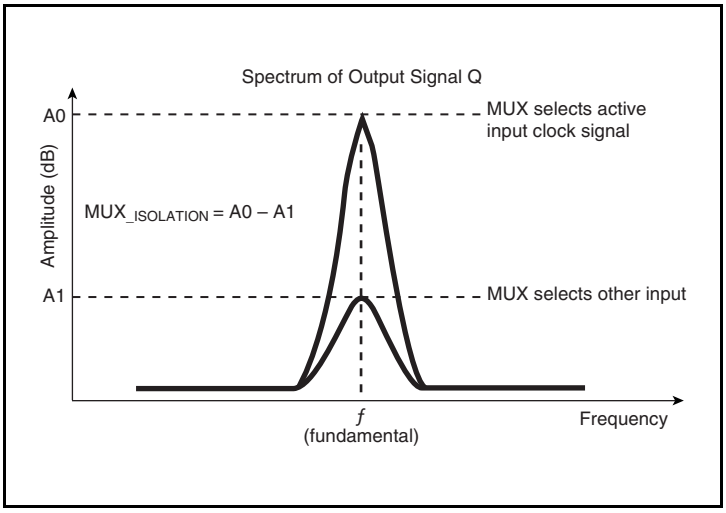
Output Rise/Fall Time

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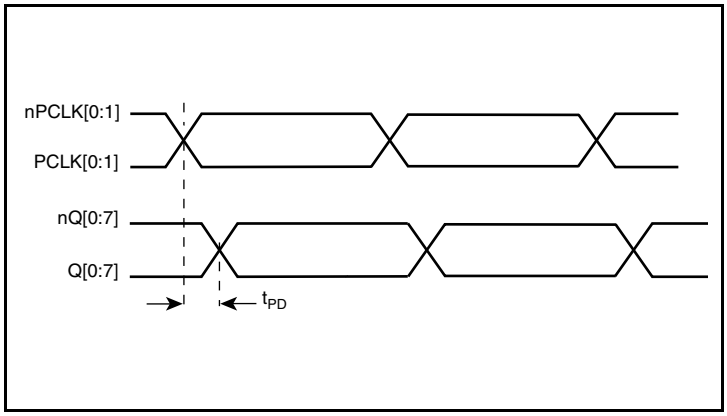
Parameter Measurement Information, continued



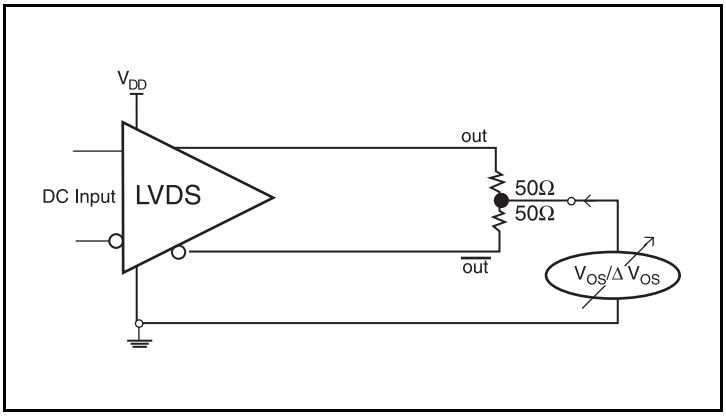
Input Skew



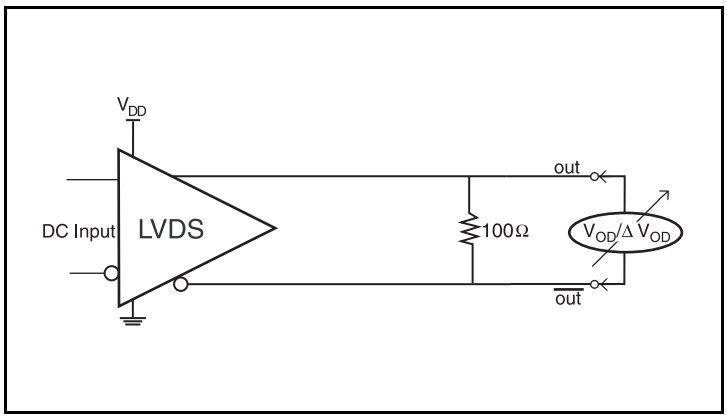
MUX Isolation



Propagation Delay



Offset Voltage Setup



Differential Output Voltage Setup

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Applications Information

Recommendations for Unused Input and Output Pins

Inputs:

PCLK/nPCLK Inputs

For applications not requiring the use of a differential input, both the PCLK and nPCLK pins can be left floating. Though not required, but for additional protection, a 1kΩ resistor can be tied from PCLK to ground.

Outputs:

LVDS Outputs

All unused LVDS output pairs can be either left floating or terminated with 100Ω across. If they are left floating, there should be no trace attached.

Wiring the Differential Input to Accept Single-Ended Levels

Figure 1 shows how a differential input can be wired to accept single ended levels. The reference voltage V1 = V_{DD}/2 is generated by the bias resistors R1 and R2. The bypass capacitor (C1) is used to help filter noise on the DC bias. This bias circuit should be located as close to the input pin as possible. The ratio of R1 and R2 might need to be adjusted to position the V1 in the center of the input voltage swing. For example, if the input clock swing is 2.5V and V_{DD} = 2.5V, R1 and R2 value should be adjusted to set V1 at 1.25V. The values below are for when both the single ended swing and V_{DD} are at the same voltage. This configuration requires that the sum of the output impedance of the driver (Ro) and the series resistance (Rs) equals the transmission line impedance. In addition, matched termination at the input will attenuate the signal in half. This can be done in one of two ways. First, R3 and R4 in parallel should equal the transmission line impedance. For most 50Ω applications, R3 and R4 can be 100Ω. The values of the resistors can be increased to reduce the loading for slower and weaker LVCMOS driver. When using single-ended signaling, the noise rejection benefits of differential signaling are reduced. Even though the differential input can handle full rail LVCMOS signaling, it is recommended that the amplitude be reduced. The datasheet specifies a lower differential amplitude, however this only applies to differential signals. For single-ended applications, the swing can be larger, however V_{IL} cannot be less than -0.3V and V_{IH} cannot be more than V_{DD} + 0.3V. Though some of the recommended components might not be used, the pads should be placed in the layout. They can be utilized for debugging purposes. The datasheet specifications are characterized and guaranteed by using a differential signal.

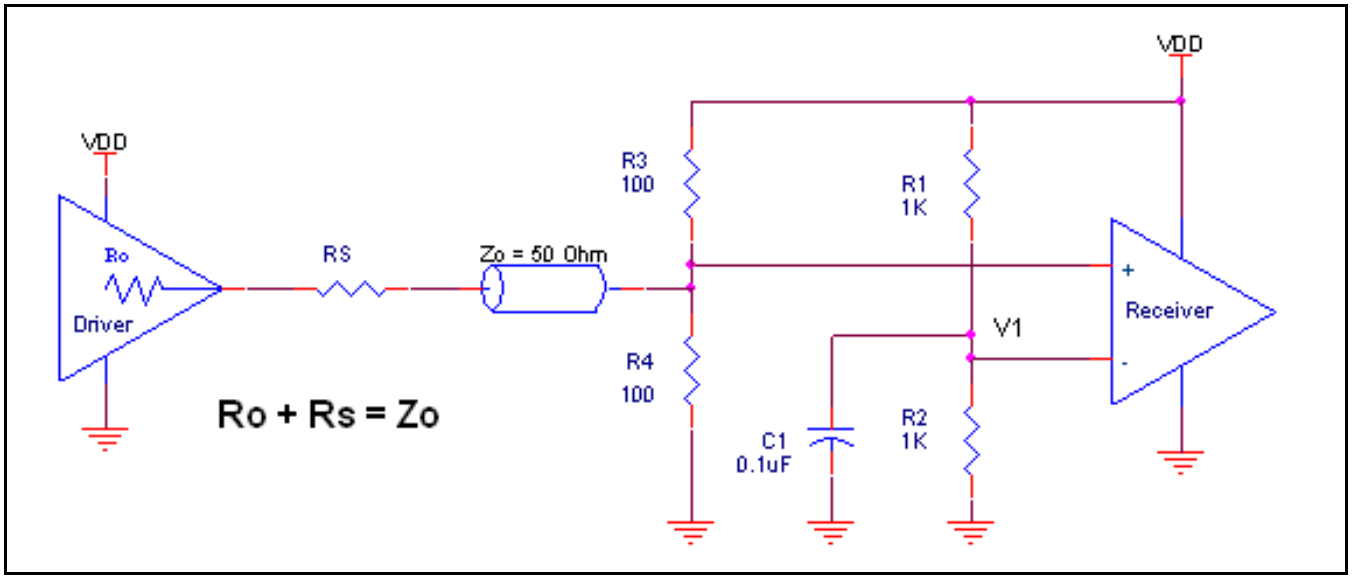


Figure 1. Recommended Schematic for Wiring a Differential Input to Accept Single-ended Levels

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3.3V LVPECL Clock Input Interface

The PCLK /nPCLK accepts LVPECL, LVDS and other differential signals. Both differential outputs must meet the V_{PP} and V_{CMR} input requirements. *Figures 2A to 2E* show interface examples for the PCLK/ nPCLK input driven by the most common driver types. The input interfaces suggested here are examples only. If the driver is from another vendor, use their termination recommendation. Please consult with the vendor of the driver component to confirm the driver termination requirements.

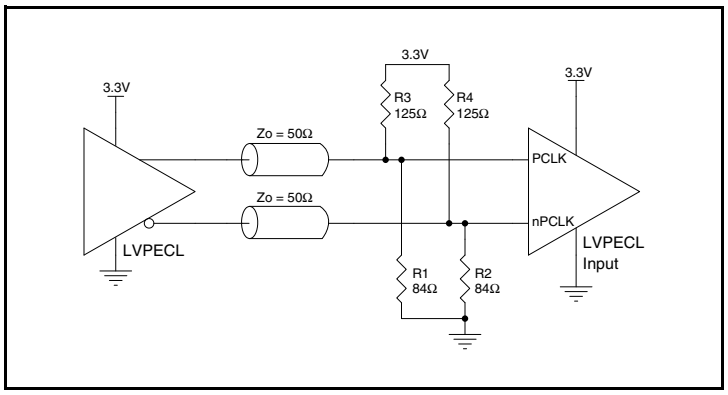


Figure 2A. PCLK/nPCLK Input Driven by a 3.3V LVPECL Driver

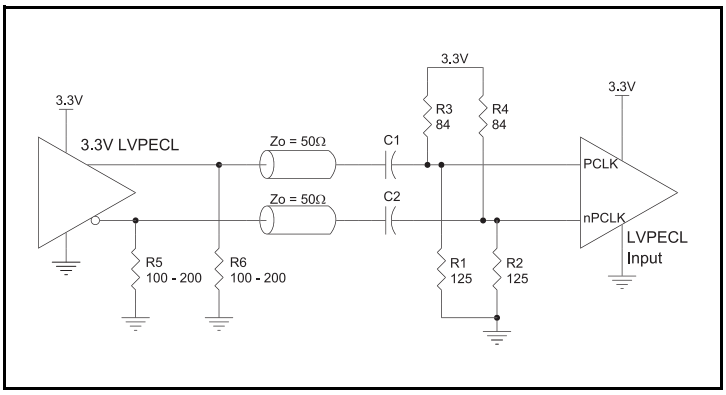


Figure 2B. PCLK/nPCLK Input Driven by a 3.3V LVPECL Driver with AC Couple

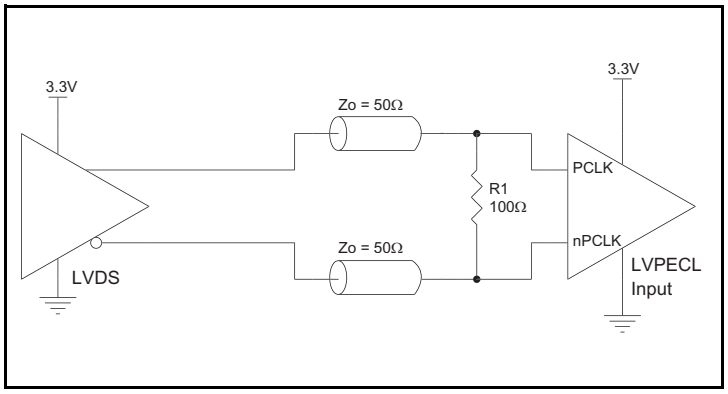


Figure 2C. PCLK/nPCLK Input Driven by a 3.3V LVDS Driver

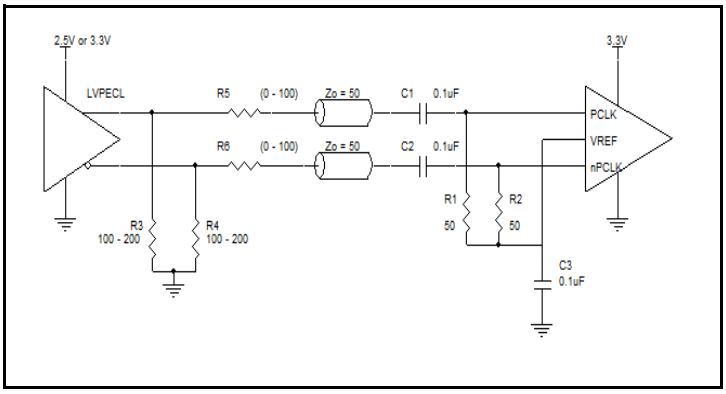


Figure 2D. PCLK/nPCLK Input Driven by a 3.3V LVPECL Driver with AC Coupling

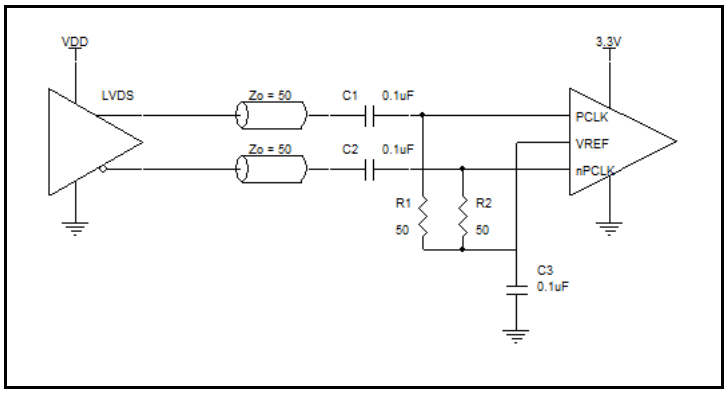


Figure 2E. PCLK/nPCLK Input Driven by a 3.3V LVDS Driver with AC Coupling

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LVDS Driver Termination

For a general LVDS interface, the recommended value for the termination impedance (Z_T) is between 90Ω and 132Ω. The actual value should be selected to match the differential impedance (Z_0) of your transmission line. A typical point-to-point LVDS design uses a 100Ω parallel resistor at the receiver and a 100Ω differential transmission-line environment. In order to avoid any transmission-line reflection issues, the components should be surface mounted and must be placed as close to the receiver as possible. IDT offers a full line of LVDS compliant devices with two types of output structures: current source and voltage source. The standard termination schematic as shown in *Figure 3A* can be used with either type of output structure. *Figure 3B*, which can also be used with both output types, is an optional termination with center tap capacitance to help filter common mode noise. The capacitor value should be approximately 50pF. If using a non-standard termination, it is recommended to contact IDT and confirm if the output structure is current source or voltage source type. In addition, since these outputs are LVDS compatible, the input receiver's amplitude and common-mode input range should be verified for compatibility with the output.

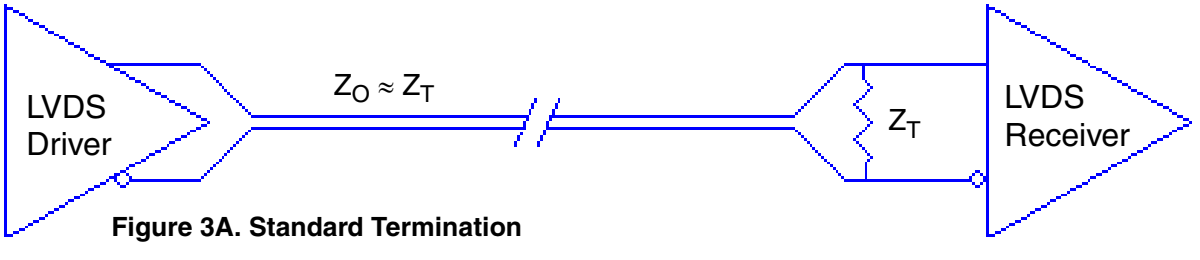


Figure 3A. Standard Termination

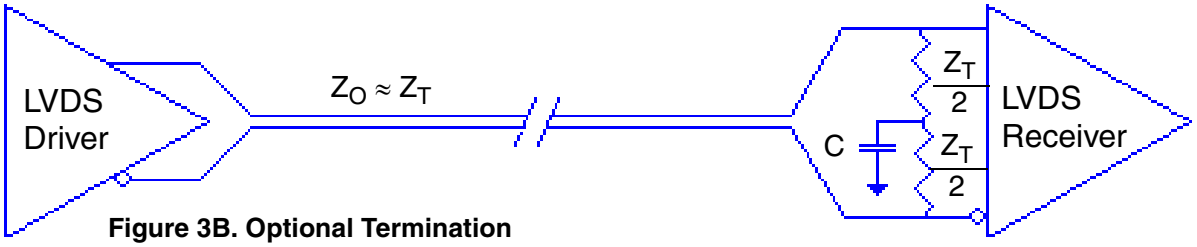


Figure 3B. Optional Termination

LVDS Termination

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VFQFN EPAD Thermal Release Path

In order to maximize both the removal of heat from the package and the electrical performance, a land pattern must be incorporated on the Printed Circuit Board (PCB) within the footprint of the package corresponding to the exposed metal pad or exposed heat slug on the package, as shown in *Figure 4.* The solderable area on the PCB, as defined by the solder mask, should be at least the same size/shape as the exposed pad/slug area on the package to maximize the thermal/electrical performance. Sufficient clearance should be designed on the PCB between the outer edges of the land pattern and the inner edges of pad pattern for the leads to avoid any shorts.

While the land pattern on the PCB provides a means of heat transfer and electrical grounding from the package to the board through a solder joint, thermal vias are necessary to effectively conduct from the surface of the PCB to the ground plane(s). The land pattern must be connected to ground through these vias. The vias act as “heat pipes”. The number of vias (i.e. “heat pipes”) are application specific and dependent upon the package power dissipation as well as electrical conductivity requirements. Thus, thermal and electrical analysis and/or testing are recommended to determine the minimum number needed. Maximum thermal and electrical performance is achieved when an array of vias is incorporated in the land pattern. It is recommended to use as many vias connected to ground as possible. It is also recommended that the via diameter should be 12 to 13mils (0.30 to 0.33mm) with 1oz copper via barrel plating. This is desirable to avoid any solder wicking inside the via during the soldering process which may result in voids in solder between the exposed pad/slug and the thermal land. Precautions should be taken to eliminate any solder voids between the exposed heat slug and the land pattern. Note: These recommendations are to be used as a guideline only. For further information, please refer to the Application Note on the Surface Mount Assembly of Amkor’s Thermally/ Electrically Enhance Leadframe Base Package, Amkor Technology.

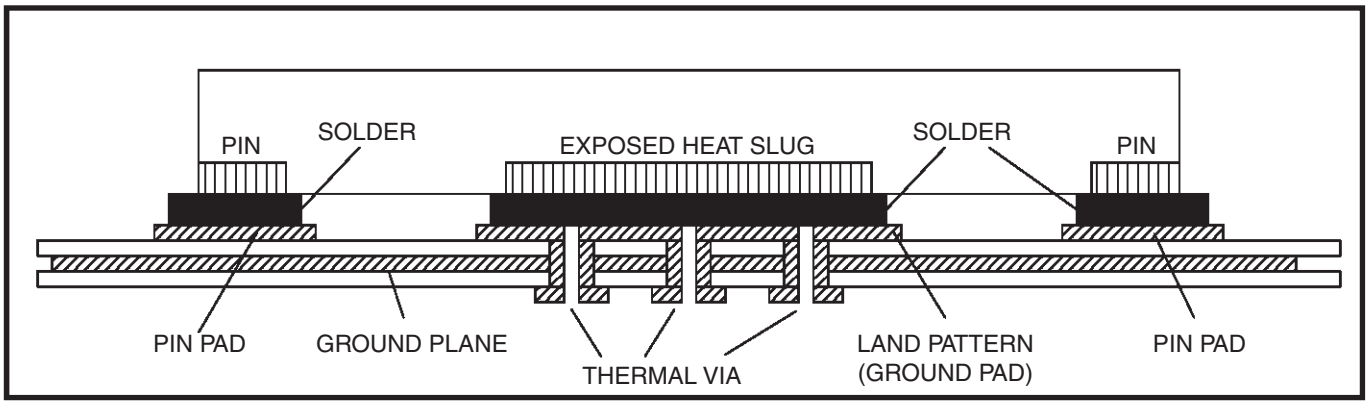


Figure 4. P.C. Assembly for Exposed Pad Thermal Release Path – Side View (drawing not to scale)

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Power Considerations

This section provides information on power dissipation and junction temperature for the IDT8SLVD1208-33I. Equations and example calculations are also provided.

1. Power Dissipation.

The total power dissipation for the IDT8SLVD1208-33I is the sum of the core power plus the output power dissipation into the load. The following is the power dissipation for V_{DD} = 3.3V + 5% = 3.465V, which gives worst case results.

The maximum current at 85°C is as follows:

I_{DD_MAX} = 190mA

- Power $_{(core)MAX}$ = V_{DD_MAX} * I_{DD_MAX} = 3.465V * 190mA = **658.4mW**

Total Power$_{_MAX}$ = 658.4mW

2. Junction Temperature.

Junction temperature, Tj, is the temperature at the junction of the bond wire and bond pad directly affects the reliability of the device. The maximum recommended junction temperature is 125°C. Limiting the internal transistor junction temperature, Tj, to 125°C ensures that the bond wire and bond pad temperature remains below 125°C.

The equation for Tj is as follows: Tj = θ_{JA} * Pd_total + TA

Tj = Junction Temperature

θ_{JA} = Junction-to-Ambient Thermal Resistance

Pd_total = Total Device Power Dissipation (example calculation is in section 1 above)

T_A = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance θ_{JA} must be used. Assuming no air flow and a multi-layer board, the appropriate value is 46.2°C/W per Table 6 below.

Therefore, Tj for an ambient temperature of 85°C with all outputs switching is:

85°C + 0.658W * 46.2°C/W = 115.4°C. This is below the limit of 125°C.

This calculation is only an example. Tj will obviously vary depending on the number of loaded outputs, supply voltage, air flow and the type of board (multi-layer).

Table 6. Thermal Resistance θ_{JA} for 28 Lead VFQFN, Forced Convection

θ_{JA} at 0 Air Flow			
Meters per Second	**0**	**1**	**2**
Multi-Layer PCB, JEDEC Standard Test Boards	46.2°C/W	39.4C/W	37.1°C/W

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Reliability Information

Table 7. θ_{JA} vs. Air Flow Table for a 28 Lead VFQFN

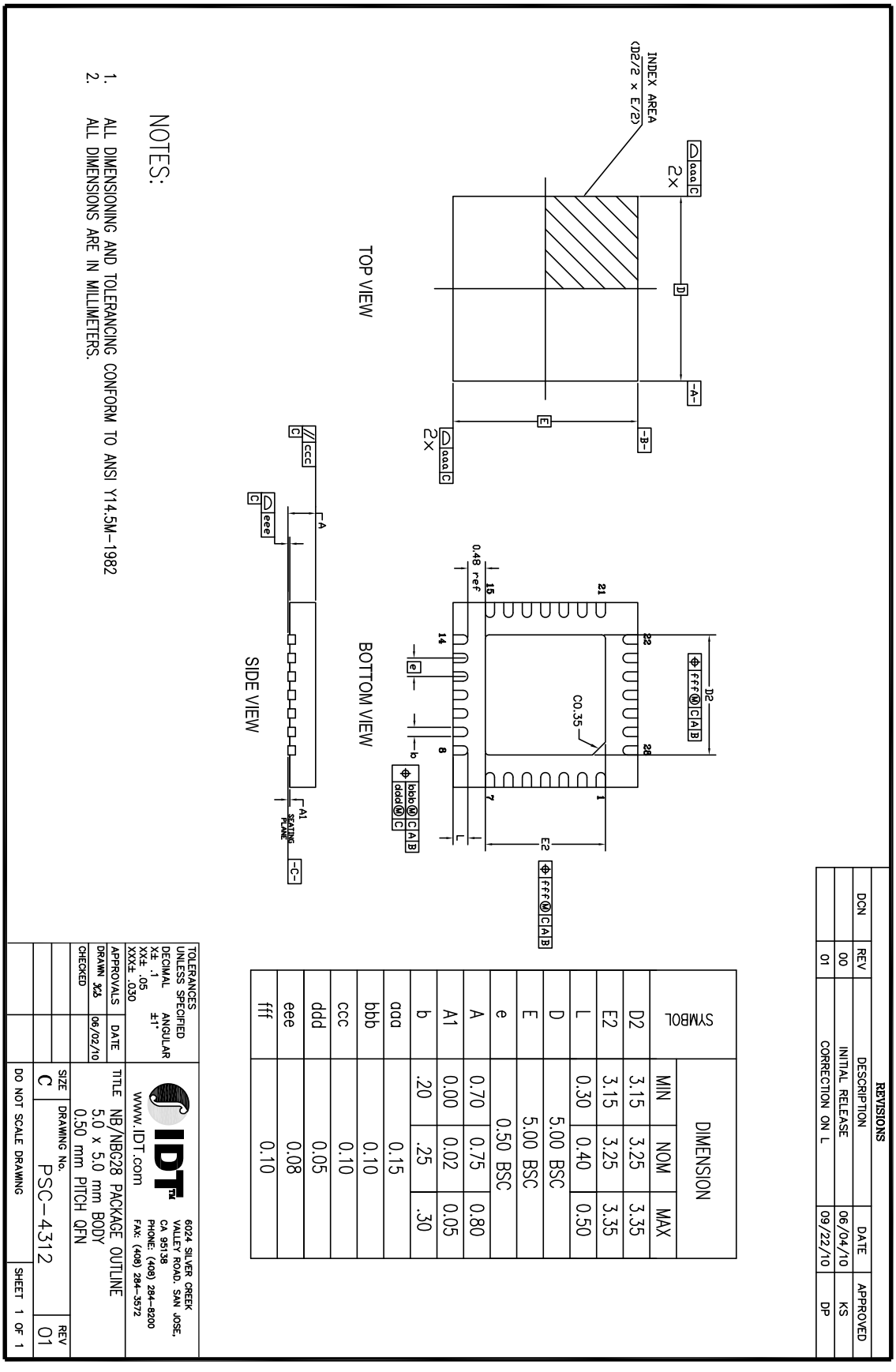
θ_{JA} at 0 Air Flow			
Meters per Second	**0**	**1**	**2.5**
Multi-Layer PCB, JEDEC Standard Test Boards	46.2°C/W	39.4C/W	37.1°C/W

Transistor Count

The transistor count for the IDT8SLVD1208-33I is: 489

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28 Lead VFQFN Package Outline and Package Dimensions



SYMBOL	DIMENSION		
	MIN	NOM	MAX
D2	3.15	3.25	3.35
E2	3.15	3.25	3.35
L	0.30	0.40	0.50
D		5.00 BSC	
E		5.00 BSC	
e		0.50 BSC	
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
b	.20	.25	.30
aaa		0.15	
bbb		0.10	
ccc		0.10	
ddd		0.05	
eee		0.08	
fff		0.10	

NOTES:

1. ALL DIMENSIONING AND TOLERANCING CONFORM TO ANSI Y14.5M-1982
2. ALL DIMENSIONS ARE IN MILLIMETERS.

REVISIONS

DCN	REV	DESCRIPTION	DATE	APPROVED
	00	INITIAL RELEASE	06/04/10	KS
	01	CORRECTION ON L	09/22/10	DP

TOLERANCES UNLESS SPECIFIED
DECIMAL ANGULAR
X± .1 ±1°
XX± .05
XXX± .030

APPROVALS | DATE
DRAWN JCS | 06/02/10
CHECKED

IDT™ 6024 SILVER CREEK VALLEY ROAD. SAN JOSE. CA 95138
WWW.IDT.COM PHONE: (408) 284-8200 FAX: (408) 284-3572

TITLE NB/NBG28 PACKAGE OUTLINE 5.0 x 5.0 mm BODY 0.50 mm PITCH QFN

SIZE C | DRAWING No. PSC-4312 | REV 01

DO NOT SCALE DRAWING | SHEET 1 OF 1

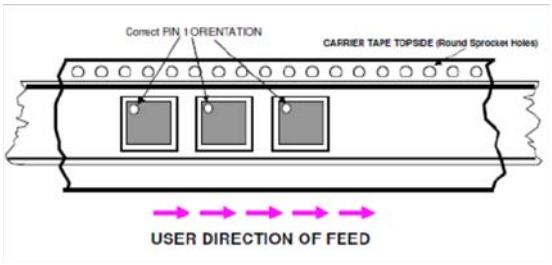
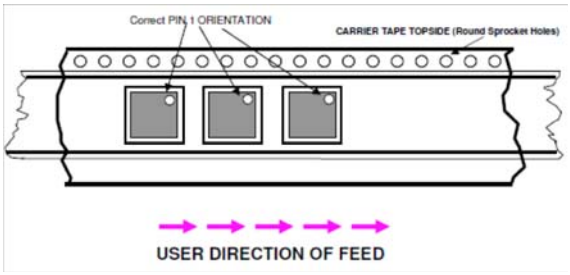
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Ordering Information

Table 8. Ordering Information

Part/Order Number	Marking	Package	Shipping Packaging	Temperature
8SLVD1208-33NBGI	VD120833NBGI	“Lead-Free” 28 Lead VFQFN	Tray	-40°C to 85°C
8SLVD1208-33NBGI8	VD120833NBGI	“Lead-Free” 28 Lead VFQFN	Tape & Reel, pin 1 orientation: EIA-481-C	-40°C to 85°C
8SLVD1208-33NBGI/W	VD120833NBGI	“Lead-Free” 28 Lead VFQFN	Tape & Reel, pin 1 orientation: EIA-481-D	-40°C to 85°C

Table 9. Pin 1 Orientation in Tape and Reel Packaging

Part Number Suffix	Pin 1 Orientation	Illustration
8	Quadrant 1 (EIA-481-C)	
/W	Quadrant 2 (EIA-481-D)	

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Revision History Sheet

Rev	Table	Page	Description of Change	Date
A		13	3.3V LVPECL Clock Input Interface application note - added figures 2D and 2E.	2/12/2014

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