Low Phase Noise, 1-to-12, 3.3V, 2.5V LVPECL Output Fanout Buffer

8SLVP1212

DATASHEET

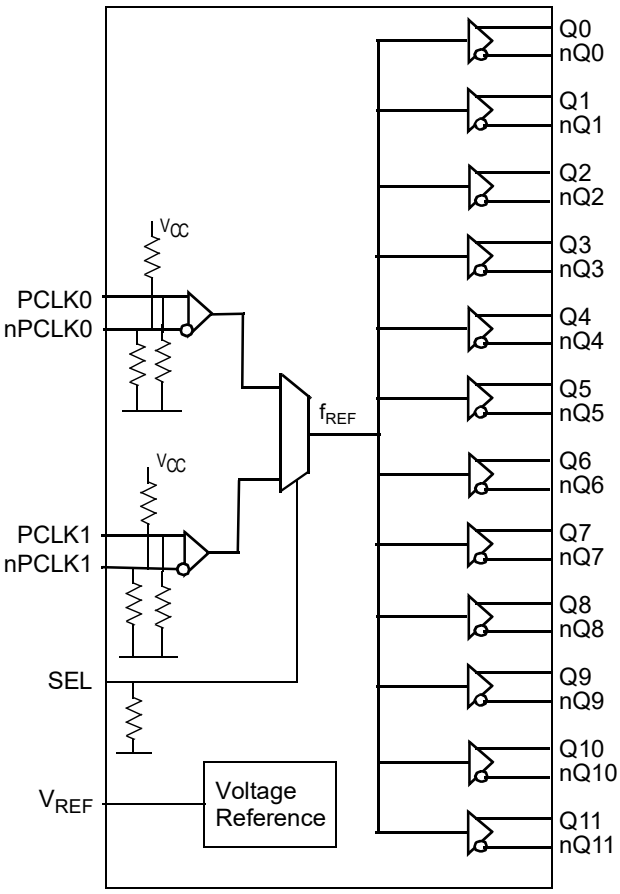
Description

The 8SLVP1212 is a high-performance, 12 output differential LVPECL fanout buffer. The device is designed for the fanout of high-frequency, very low additive phase-noise clock and data signals. The 8SLVP1212 is characterized to operate from a 3.3V and 2.5V power supply. Guaranteed output-to-output and part-to-part skew characteristics make the 8SLVP1212 ideal for those clock distribution applications demanding well-defined performance and repeatability. Two selectable differential inputs and twelve low skew outputs are available. The integrated bias voltage generators enables easy interfacing of single-ended signals to the device inputs. The device is optimized for low power consumption and low additive phase noise.

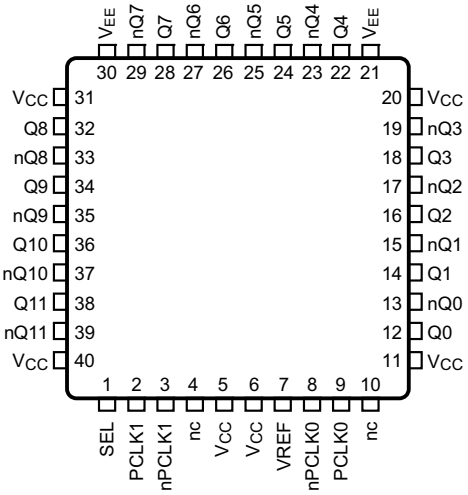
Features

- Twelve low skew, low additive jitter LVPECL outputs
- Two selectable, differential clock inputs
- Differential pairs can accept the following differential input levels: LVDS, LVPECL, CML
- Maximum input clock frequency: 2GHz
- LVCMOS interface levels for the control input (input select)
- Output skew: 33ps (maximum)
- Propagation delay: 550ps (maximum)
- Low additive phase jitter, RMS at f_{REF} = 156.25MHz, V_{PP} = 1V, 12kHz–20MHz: 60fs (maximum)
- Full 3.3V and 2.5V supply voltage
- Device current consumption (I_{EE}): 131mA (maximum)
- Available in Lead-free (RoHS 6), 40-VFQFPN package
- -40°C to +85°C ambient operating temperature
- Differential PCLK0, nPCLK0 and PCLK1, nPCLK1 pairs can also accept single-ended LVCMOS levels. See Applications section Wiring the Differential Input Levels to Accept Single-ended Levels (Figure 1A and Figure 1B)
- Supports PCI Express Gen1–5

Block Diagram



Pin Assignment



8SLVP1212

40-VFQFPN
6 x 6 x 0.9 mm package body,
Top View

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Table 1. Pin Descriptions

Number	Name	Type		Description
1	SEL	Input	Pulldown	Reference select control. See Table 3A for function. LVCMOS/LVTTL interface levels.
2	PCLK1	Input	Pulldown	Non-inverting LVPECL differential clock/data input.
3	nPCLK1	Input	Pulldown/Pullup	Inverting LVPECL differential clock/data input.
4, 10	nc	Unused		Do not connect.
5, 6, 11, 20, 31, 40	V_{CC}	Power		Power supply pins.
7	V_{REF}	Output		Bias voltage reference.
8	nPCLK0	Input	Pulldown/Pullup	Inverting LVPECL differential clock/data input.
9	PCLK0	Input	Pulldown	Non-inverting LVPECL differential clock/data input.
12, 13	Q0, nQ0	Output		Differential output pair 0. LVPECL interface levels.
14, 15	Q1, nQ1	Output		Differential output pair 1. LVPECL interface levels.
16, 17	Q2, nQ2	Output		Differential output pair 2. LVPECL interface levels.
18, 19	Q3, nQ3	Output		Differential output pair 3. LVPECL interface levels.
21, 30	V_{EE}	Power		Negative power supply pins.
22, 23	Q4, nQ4	Output		Differential output pair 4. LVPECL interface levels.
24, 25	Q5, nQ5	Output		Differential output pair 5. LVPECL interface levels.
26, 27	Q6, nQ6	Output		Differential output pair 6. LVPECL interface levels.
28, 29	Q7, nQ7	Output		Differential output pair 7. LVPECL interface levels.
32, 33	Q8, nQ8	Output		Differential output pair 8. LVPECL interface levels.
34, 35	Q9, nQ9	Output		Differential output pair 9. LVPECL interface levels.
36, 37	Q10, nQ10	Output		Differential output pair 10. LVPECL interface levels.
38, 39	Q11, nQ11	Output		Differential output pair 11. LVPECL interface levels.

NOTE: *Pulldown* and *Pullup* refers to an internal input resistors. See Table 2, *Pin Characteristics,* for typical values.

Table 2. Pin Characteristics

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
C_{IN}	Input Capacitance			2		pF
$R_{PULLDOWN}$	Input Pulldown Resistor			51		kΩ
R_{PULLUP}	Input Pullup Resistor			51		kΩ

Function Table

Table 3. SEL Input Section Function Table

Input	
SEL	Operation
0 (default)	PCLK0, nPCLK0 is the selected differential clock input
1	PCLK1, nPCLK1 is the selected differential clock input

NOTE: SEL is an asynchronous control.

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Absolute Maximum Ratings

NOTE: Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of the product at these conditions or any conditions beyond those listed in the *DC Characteristics or AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Item	Rating
Supply Voltage, V_{CC}	4.6V
Inputs, V_I	-0.5V to V_{CC} + 0.5V
Outputs, I_O (LVPECL) Continuous Current Surge Current	 50mA 100mA
Maximum Junction Temperature, $T_{J,MAX}$	125 °C
Storage Temperature, T_{STG}	-65°C to 150°C
ESD - Human Body Model (NOTE 1)	2000V
ESD - Charged Device Model (NOTE 1)	500V

NOTE 1: According to JEDEC/JESD 22-A114/22-C101. ESD ratings are target specifications.

DC Electrical Characteristics

Table 4A. Power Supply DC Characteristics, V_{CC} = 3.3V ± 5%, V_{EE} = 0V, T_A = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{CC}	Power Supply Voltage		3.135	3.3V	3.465	V
I_{EE}	Power Supply Current			110	131	mA
I_{CC}	Power Supply Current	Q[0:11] terminated 50Ω ±1% to V_{CC} – 2V		490	550	mA

Table 4B. Power Supply DC Characteristics, V_{CC} = 2.5V ± 5%, V_{EE} = 0V, T_A = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{CC}	Power Supply Voltage		2.375	2.5V	2.625	V
I_{EE}	Power Supply Current			104	124	mA
I_{CC}	Power Supply Current	Q[0:11] terminated 50Ω ±1% to V_{CC} – 2V		490	550	mA

Table 4C. LVCMOS/LVTTL DC Characteristics, V_{CC} = 3.3V ± 5% or 2.5V ± 5%, V_{EE} = 0V, T_A = -40°C to 85°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
V_{IH}	Input High Voltage		V_{CC} = 3.465V	2.2		V_{CC} + 0.3	V
			V_{CC} = 2.625V	1.7		V_{CC} + 0.3	V
V_{IL}	Input Low Voltage		V_{CC} = 3.465V	-0.3		0.8	V
			V_{CC} = 2.625V	-0.3		0.7	V
I_{IH}	Input High Current	SEL	V_{CC} = V_{IN} = 3.465V or 2.625V			150	µA
I_{IL}	Input Low Current	SEL	V_{CC} = 3.465V or 2.625V, V_{IN} = 0V	-10			µA

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Table 4D. LVPECL DC Characteristics, V_{CC} = 3.3V ± 5%, V_{EE} = 0V, T_A = -40°C to 85°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
I_{IH}	Input High Current	PCLK0, nPCLK0 PCLK1, nPCLK1	V_{CC} = V_{IN} = 3.465V			150	µA
I_{IL}	Input Low Current	PCLK0, PCLK1	V_{CC} = 3.465V, V_{IN} = 0V	-10			µA
		nPCLK0, nPCLK1	V_{CC} = 3.465V, V_{IN} = 0V	-150			µA
V_{REF}	Reference Voltage for Input Bias; NOTE 1		I_{REF} = 2mA	V_{CC} – 1.6	V_{CC} – 1.26	V_{CC} – 1.1	V
V_{OH}	Output High Voltage; NOTE 2			V_{CC} – 1.26	V_{CC} – 0.84	V_{CC} – 0.6	V
V_{OL}	Output Low Voltage; NOTE 2			V_{CC} – 1.7	V_{CC} – 1.5	V_{CC} – 1.28	V

NOTE: Input and output parameters vary 1:1 with V_{CC}.
NOTE 1: V_{REF} is for 3.3V±5% V_{CC} only. To obtain a bias voltage for V_{CC} = 2.5V±5% application, an external voltage supply is recommended.
NOTE 2: Outputs terminated with 50Ω to V_{CC} – 2V.

Table 4E. LVPECL DC Characteristics, V_{CC} = 2.5V ± 5%, V_{EE} = 0V, T_A = -40°C to 85°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
I_{IH}	Input High Current	PCLK0, nPCLK0 PCLK1, nPCLK1	V_{CC} = V_{IN} = 2.625V			150	µA
I_{IL}	Input Low Current	PCLK0, PCLK1	V_{CC} = 2.625V, V_{IN} = 0V	-10			µA
		nPCLK0, nPCLK1	V_{CC} = 2.625V, V_{IN} = 0V	-150			µA
V_{REF}	Reference Voltage for Input Bias; NOTE 1		I_{REF} = 2mA	V_{CC} – 1.6	V_{CC} – 1.26	V_{CC} – 1.1	V
V_{OH}	Output High Voltage; NOTE 2			V_{CC} – 1.26	V_{CC} – 0.84	V_{CC} – 0.6	V
V_{OL}	Output Low Voltage; NOTE 2			V_{CC} – 1.7	V_{CC} – 1.47	V_{CC} – 1.28	V

NOTE: Input and output parameters vary 1:1 with V_{CC}.
NOTE 1: V_{REF} is for 3.3V±5% V_{CC} only. To obtain a bias voltage for V_{CC} = 2.5V±5% application, an external voltage supply is recommended.
NOTE 2: Outputs terminated with 50Ω to V_{CC} – 2V.

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AC Electrical Characteristics

Table 5. AC Electrical Characteristics, V_{CC} = 3.3V ± 5% or 2.5V ± 5%, V_{EE} = 0V, T_A = -40°C to 85°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
f_{REF}	Input Frequency	PCLK[0:1], nPCLK[0:1]				2	GHz
ΔV/Δt	Input Edge Rate	PCLK[0:1], nPCLK[0:1]		1.5			V/ns
t_{PD}	Propagation Delay; NOTE 1		PCLKx, nPCLKx to any Qx, nQx for V_{PP} = 0.1V or 0.3V	230	360	550	ps
$MUX_{_ISOLATION}$	MUX Isolation		f_{REF} = 100MHz		70		dB
*t*sk(o)	Output Skew; NOTE 2, 3				17	33	ps
*t*sk(p)	Pulse Skew		f_{REF} = 100MHz		10	50	ps
*t*sk(pp)	Part-to-Part Skew; NOTE 3, 4					150	ps
t_{JIT}	Buffer Additive Phase Jitter, RMS; refer to Additive Phase Jitter Section		f_{REF} = 122.88MHz, Square Wave, V_{PP} = 0.8V, Integration Range: 1kHz– 40MHz		90		fs
			f_{REF} = 122.88MHz, Square Wave, V_{PP} = 0.8V, Integration Range: 10kHz – 20MHz		60		fs
			f_{REF} = 122.88MHz, Square Wave, V_{PP} = 0.8V, Integration Range: 12kHz – 20MHz		55		fs
			f_{REF} = 156.25MHz, Square Wave, V_{PP} = 1V, Integration Range: 1kHz– 40MHz		61	76	fs
			f_{REF} = 156.25MHz, Square Wave, V_{PP} = 1V, Integration Range: 10kHz – 20MHz		45	60	fs
			f_{REF} = 156.25MHz, Square Wave, V_{PP} = 1V, Integration Range: 12kHz – 20MHz		45	60	fs
			f_{REF} = 156.25MHz Square Wave, V_{PP} = 0.5V, Integration Range: 1kHz– 40MHz		60	90	fs
			f_{REF} = 156.25MHz, Square Wave, V_{PP} = 0.5V, Integration Range: 10kHz – 20MHz		45	80	fs
			f_{REF} = 156.25MHz, Square Wave, V_{PP} = 0.5V, Integration Range: 12kHz – 20MHz		45	80	fs
t_R / t_F	Output Rise/ Fall Time		20% to 80%	70	110	170	ps
V_{PP}	Differential Input Voltage; NOTE 5, 7		f < 1.5GHz	0.1		1.5	V
			f > 1.5GHz	0.2		1.5	V
V_{CMR}	Common Mode Input Voltage; NOTE 5, 6, 7			1.0		V_{CC} – 0.3	V
V_O(pp)	Output Voltage Swing, Peak-to-Peak		V_{CC} = 3.3V ± 5%, $f_{REF} \le$ 2GHz	0.45	0.68	0.90	V
			V_{CC} = 2.5V ± 5%, $f_{REF} \le$ 2GHz	0.45	0.68	0.90	V
V_{DIFF_OUT}	Differential Output Voltage Swing, Peak-to-Peak		V_{CC} = 3.3V ± 5%, $f_{REF} \le$ 2GHz	0.9	1.36	1.8	V
			V_{CC} = 2.5V ± 5%, $f_{REF} \le$ 2GHz	0.9	1.36	1.8	V

NOTES on next page.

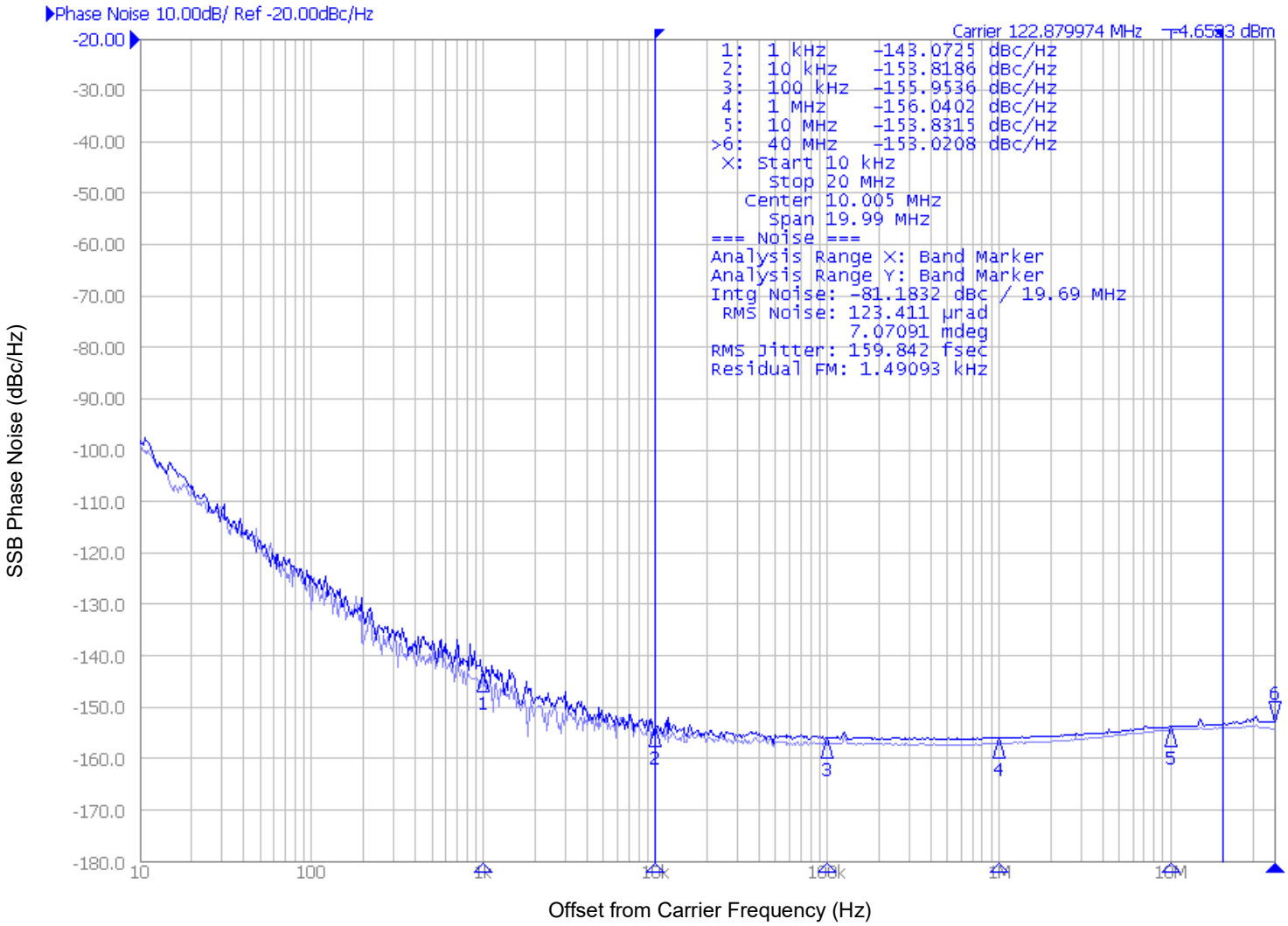
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NOTE: Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfpm. The device will meet specifications after thermal equilibrium has been reached under these conditions.
NOTE 1: Measured from the differential input crosspoint to the differential output crosspoint.
NOTE 2: Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at the differential crosspoints.
NOTE 3: This parameter is defined in accordance with JEDEC Standard 65.
NOTE 4: Defined as skew between outputs on different devices operating at the same supply voltage, same frequency, same temperature and with equal load conditions. Using the same type of inputs on each device, the outputs are measured at the differential crosspoints.
NOTE 5: V_{IL} should not be less than -0.3V. V_{IH} should not be higher than V_{CC}.
NOTE 6: Common mode input voltage is defined at the crosspoint.
NOTE 7: For single-ended LVCMOS input applications, please refer to the Applications Information, Wiring the Differential Input to accept single-ended levels, Figures 1A and 1B.

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Additive Phase Jitter (3.3V at 122.88MHz)

The spectral purity in a band at a specific offset from the fundamental compared to the power of the fundamental is called the ***dBc Phase Noise.*** This value is normally expressed using a Phase noise plot and is most often the specified plot in many applications. Phase noise is defined as the ratio of the noise power present in a 1Hz band at a specified offset from the fundamental frequency to the power value of the fundamental. This ratio is expressed in decibels (dBm) or a ratio of the power in the 1Hz band to the power in the fundamental. When the required offset is specified, the phase noise is called a ***dBc*** value, which simply means dBm at a specified offset from the fundamental. By investigating jitter in the frequency domain, we get a better understanding of its effects on the desired application over the entire time record of the signal. It is mathematically possible to calculate an expected bit error rate given a phase noise plot.



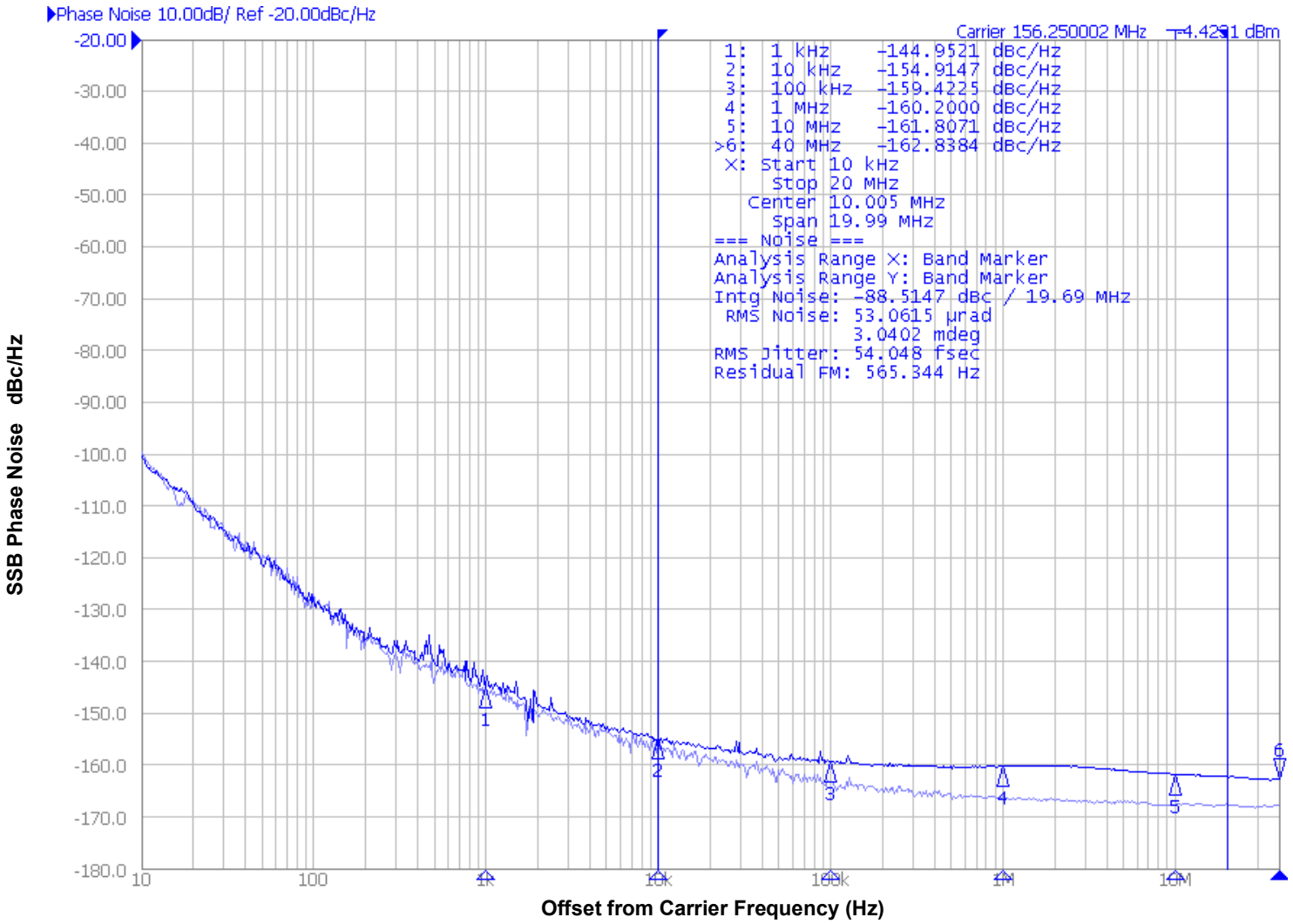
As with most timing specifications, phase noise measurements have issues relating to the limitations of the measurement equipment. The noise floor of the equipment can be higher or lower than the noise floor of the device. Additive phase noise is dependent on both the noise floor of the input source and measurement equipment.

Measured using a Wenzel 122.88MHz Oscillator as the input source.

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Additive Phase Jitter (3.3V at 156.25MHz)

The spectral purity in a band at a specific offset from the fundamental compared to the power of the fundamental is called the ***dBc Phase Noise.*** This value is normally expressed using a Phase noise plot and is most often the specified plot in many applications. Phase noise is defined as the ratio of the noise power present in a 1Hz band at a specified offset from the fundamental frequency to the power value of the fundamental. This ratio is expressed in decibels (dBm) or a ratio of the power in the 1Hz band to the power in the fundamental. When the required offset is specified, the phase noise is called a ***dBc*** value, which simply means dBm at a specified offset from the fundamental. By investigating jitter in the frequency domain, we get a better understanding of its effects on the desired application over the entire time record of the signal. It is mathematically possible to calculate an expected bit error rate given a phase noise plot.

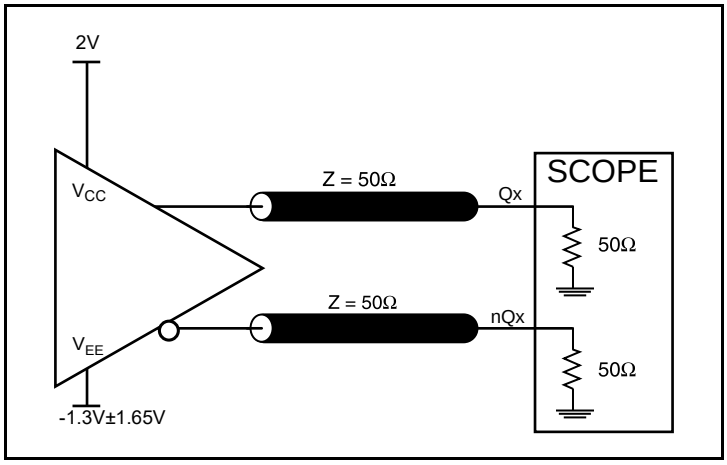


As with most timing specifications, phase noise measurements have issues relating to the limitations of the measurement equipment. The noise floor of the equipment can be higher or lower than the noise floor of the device. Additive phase noise is dependent on both the noise floor of the input source and measurement equipment.

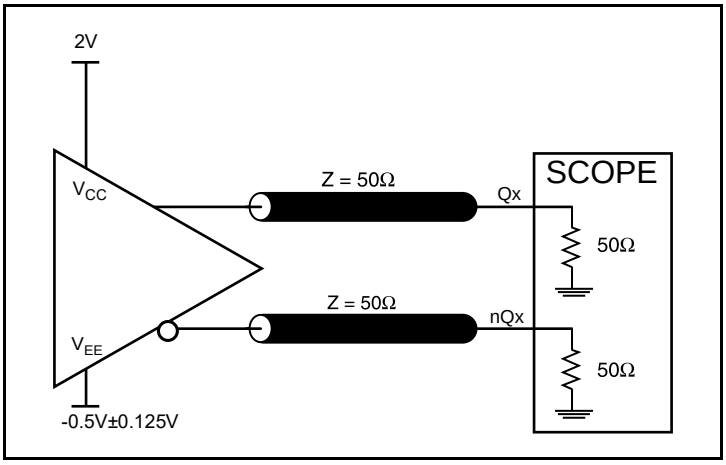
Measured using a Wenzel 156.25MHz Oscillator as the input source.

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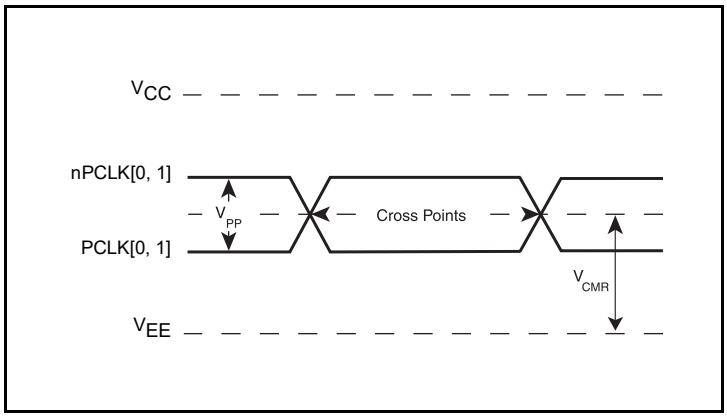
Parameter Measurement Information



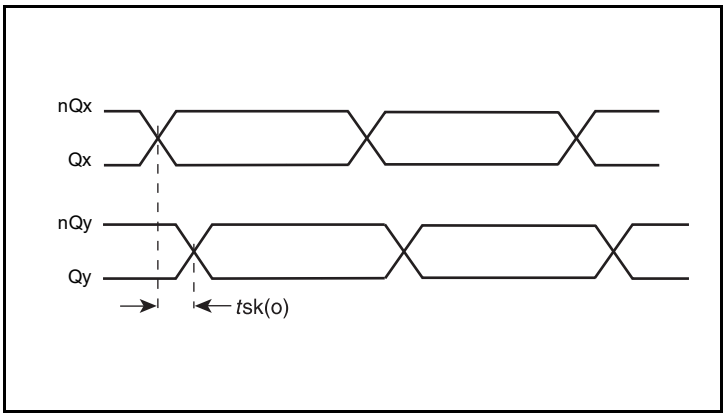
3.3V LVPECL Output Load AC Test Circuit



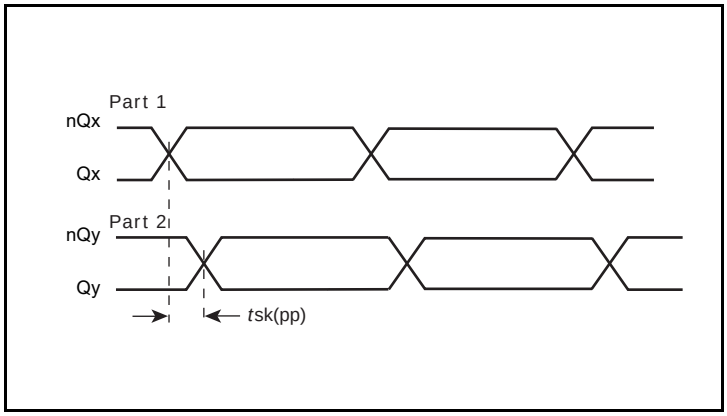
2.5V LVPECL Output Load AC Test Circuit



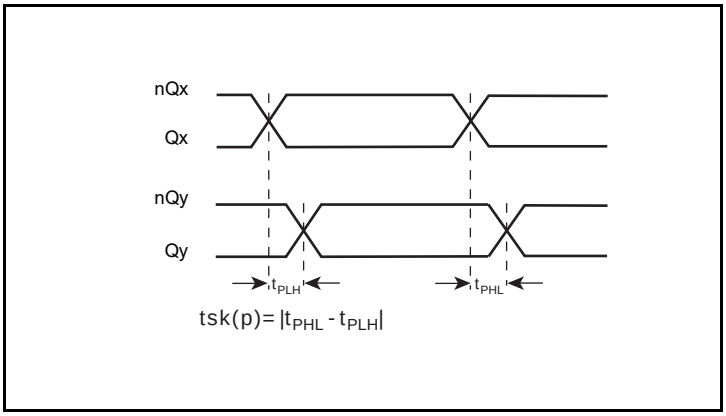
Differential Input Level



Output Skew



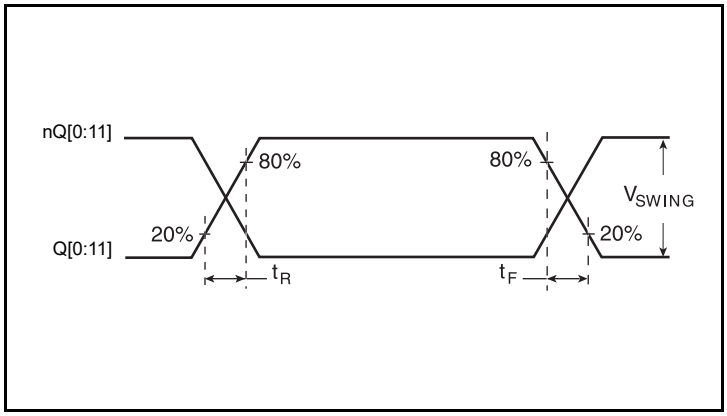
Part-to-Part Skew



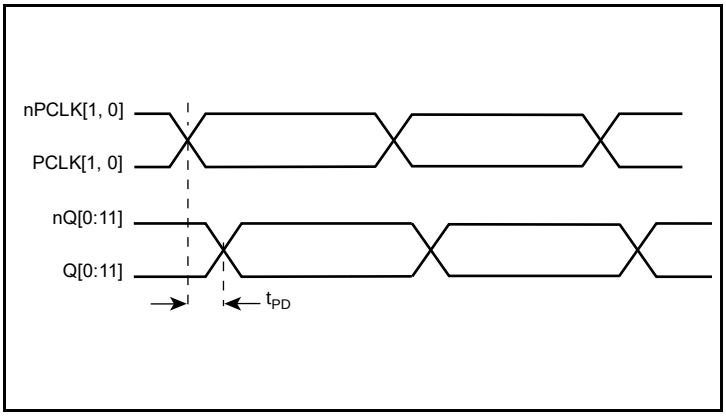
Pulse Skew

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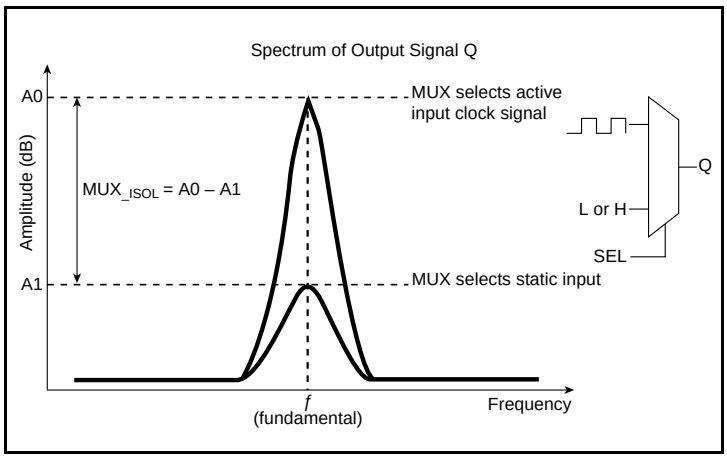
Parameter Measurement Information, continued



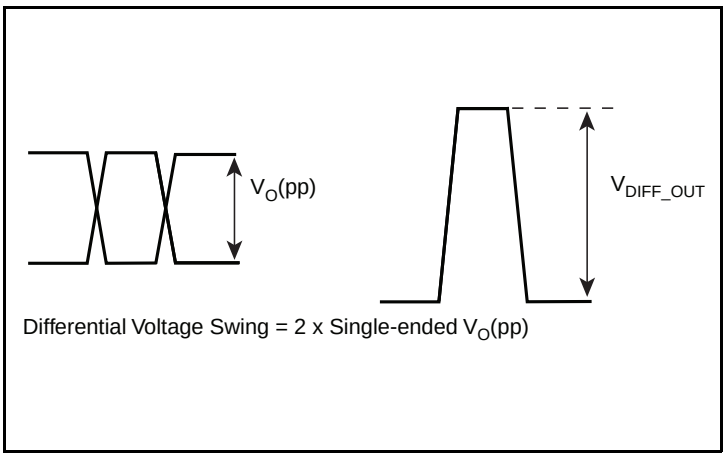
Output Rise/Fall Time



Propagation Delay



MUX Isolation



Output Voltage Swing

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Applications Information

Wiring the Differential Input to Accept Single-Ended Levels

The 8SLVP1212 inputs can be interfaced to LVPECL, LVDS, CML or LVCMOS drivers. *Figure 1A* illustrates how to dc couple a single LVCMOS input to the 8SLVP1212. The value of the series resistance RS is calculated as the difference between the transmission line impedance and the driver output impedance. This resistor should be placed close to the LVCMOS driver. To avoid cross-coupling of single-ended LVCMOS signals, apply the LVCMOS signals to no more than one PCLK input.

A practical method to implement Vth is shown in *Figure 1B* below. The reference voltage Vth = V1 = V_{CC}/2, is generated by the bias resistors R1 and R2. The bypass capacitor (C1) is used to help filter noise on the DC bias. This bias circuit should be located as close to the input pin as possible.

The ratio of R1 and R2 might need to be adjusted to position the V1 in the center of the input voltage swing. For example, if the input clock swing is 2.5V and V_{CC} = 3.3V, R1 and R2 value should be adjusted to set V1 at 1.25V. The values below apply when both the single-ended swing and V_{CC} are at the same voltage.

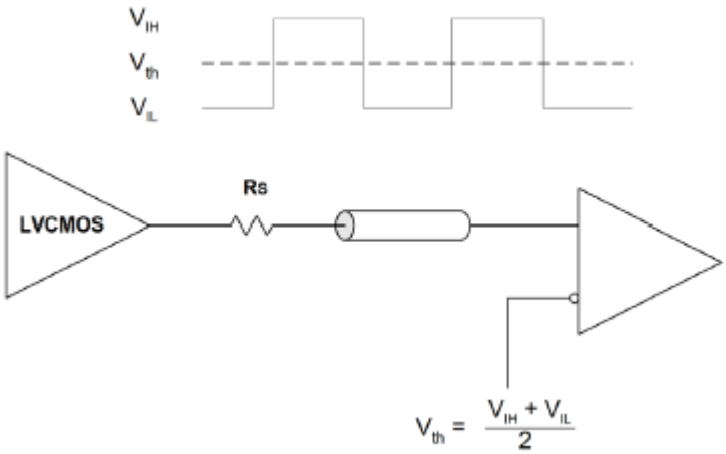


Figure 1A. DC-Coupling a Single LVCMOS Input to the 8SLVP1212

When using single-ended signaling, the noise rejection benefits of differential signaling are reduced. Even though the differential input can handle full rail LVCMOS signaling, it is recommended that the amplitude be reduced, particularly if both input references are LVCMOS to minimize cross talk. The datasheet specifies a lower differential amplitude, however this only applies to differential signals. For single-ended applications, the swing can be larger, however V_{IL} cannot be less than -0.3V and V_{IH} cannot be more than V_{CC} + 0.3V.

Figure 1B shows a way to attenuate the PCLK input level by a factor of two as well as matching the transmission line between the LVCMOS driver and the IDT8SLVP1212I at both the source and the load. This configuration requires that the sum of the output impedance of the driver (Ro) and the series resistance (Rs) equals the transmission line impedance. R3 and R4 in parallel should equal the transmission line impedance; for most 50Ω applications, R3 and R4 will be 100Ω. The values of the resistors can be increased to reduce the loading for slower and weaker LVCMOS driver.

Though some of the recommended components of Figure 1B might not be used, the pads should be placed in the layout so that they can be utilized for debugging purposes. The datasheet specifications are characterized and guaranteed by using a differential signal.

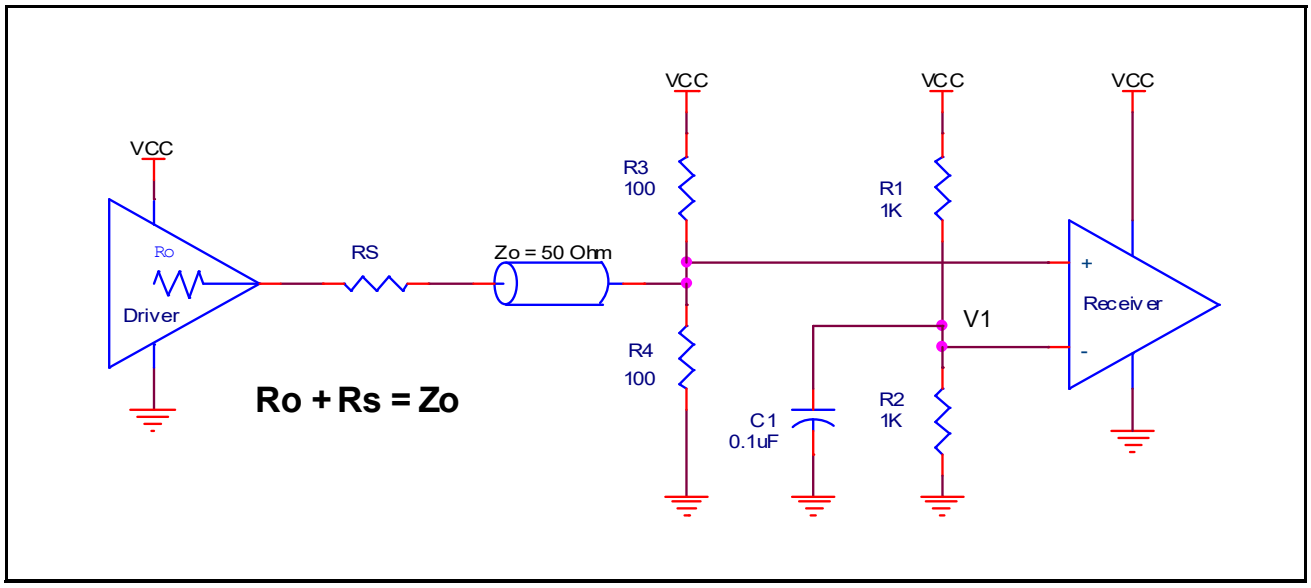


Figure 1B. Alternative DC Coupling a Single LVCMOS Input to the 8SLVP1212

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Recommendations for Unused Input and Output Pins

Inputs:

PCLKx/nPCLKx Inputs

For applications not requiring the use of a differential input, both the PCLKx and nPCLKx pins can be left floating. Though not required, but for additional protection, a 1kΩ resistor can be tied from PCLKx to ground. For applications

Outputs:

LVPECL Outputs

All unused LVPECL outputs can be left floating. We recommend that there is no trace attached. Both sides of the differential output pair should either be left floating or terminated.

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3.3V LVPECL Clock Input Interface

The PCLK /nPCLK accepts LVPECL, LVDS, CML and other differential signals. Both differential outputs must meet the V_{PP} and V_{CMR} input requirements. *Figures 2A to 2E* show interface examples for the PCLK/ nPCLK input driven by the most common driver types.

The input interfaces suggested here are examples only. If the driver is from another vendor, use their termination recommendation. Please consult with the vendor of the driver component to confirm the driver termination requirements.

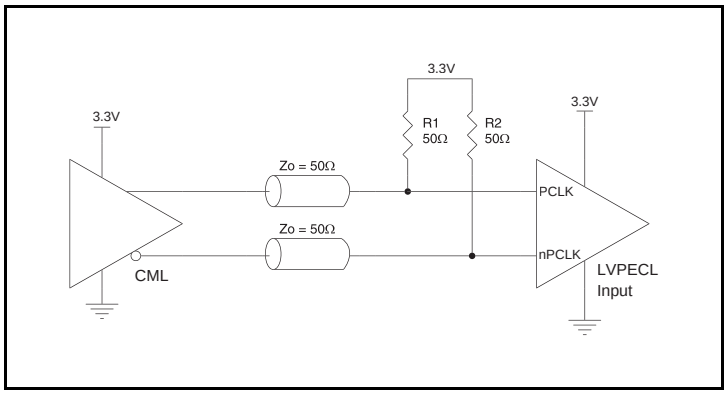


Figure 2A. PCLK/nPCLK Input Driven by a CML Driver

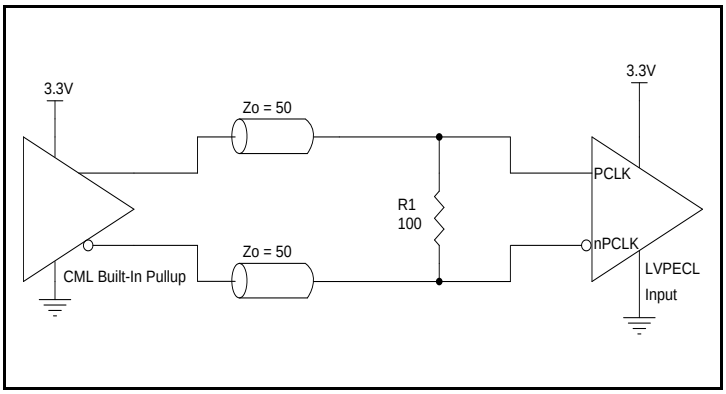


Figure 2B. PCLK/nPCLK Input Driven by a Built-In Pullup CML Driver

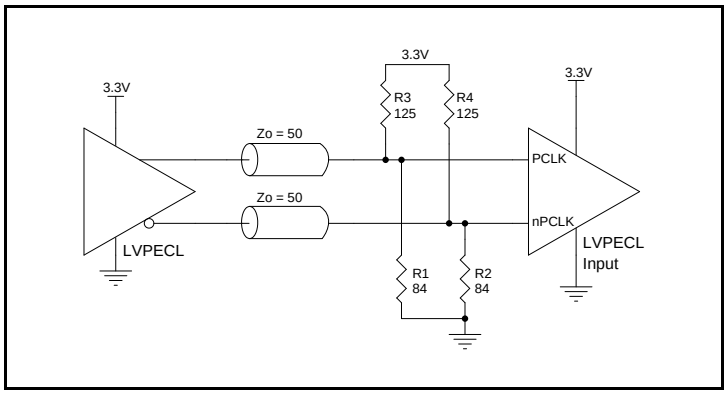


Figure 2C. PCLK/nPCLK Input Driven by a 3.3V LVPECL Driver

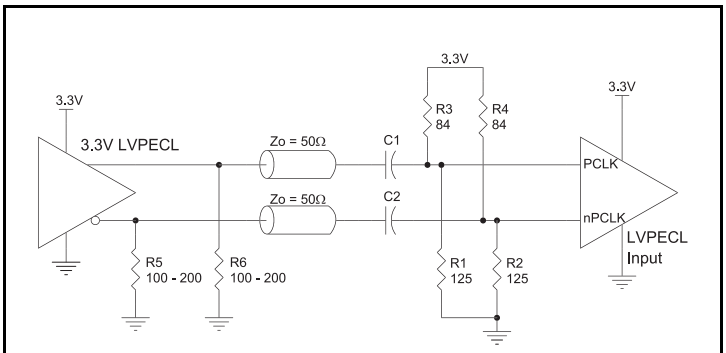


Figure 2D. PCLK/nPCLK Input Driven by a 3.3V LVPECL Driver with AC Couple

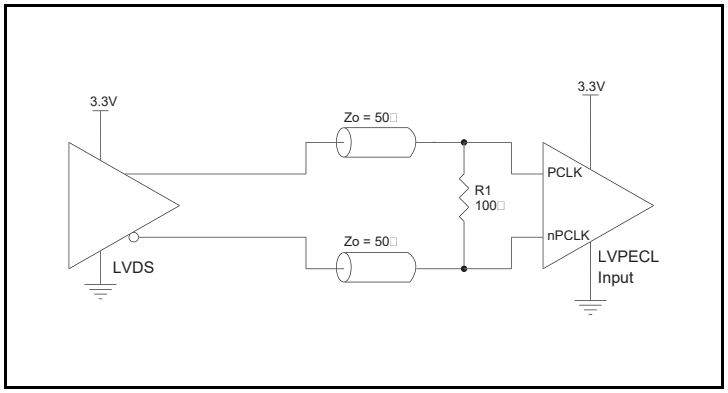


Figure 2E. PCLK/nPCLK Input Driven by a 3.3V LVDS Driver

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2.5V LVPECL Clock Input Interface

The PCLK /nPCLK accepts LVPECL, LVDS, CML and other differential signals. Both differential outputs must meet the V_{PP} and V_{CMR} input requirements. *Figures 3A to 3E* show interface examples for the PCLK/ nPCLK input driven by the most common driver types.

The input interfaces suggested here are examples only. If the driver is from another vendor, use their termination recommendation. Please consult with the vendor of the driver component to confirm the driver termination requirements.

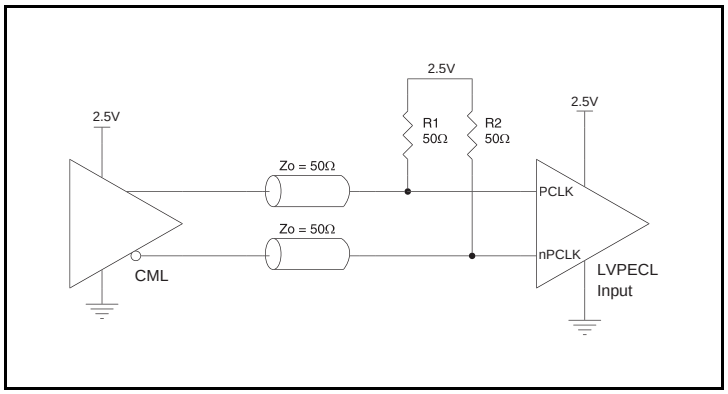


Figure 3A. PCLK/nPCLK Input Driven by a CML Driver

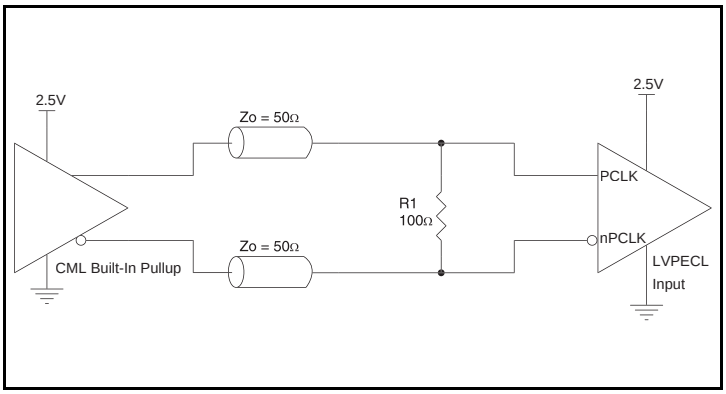


Figure 3B. PCLK/nPCLK Input Driven by a Built-In Pullup CML Driver

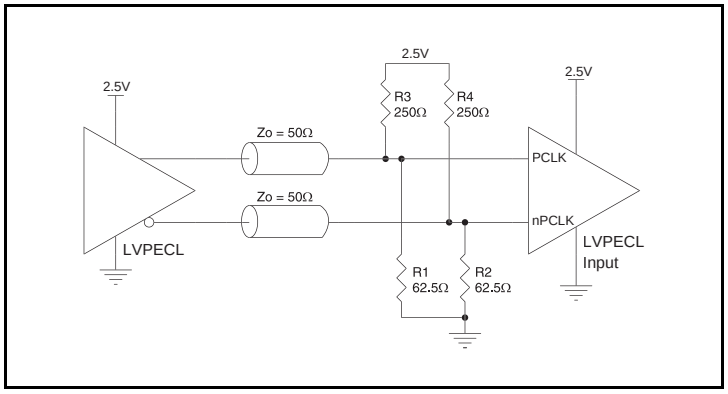


Figure 3C. PCLK/nPCLK Input Driven by a 2.5V LVPECL Driver

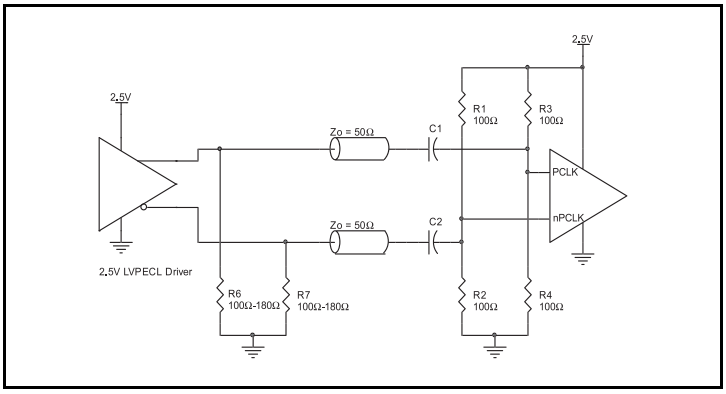


Figure 3D. PCLK/nPCLK Input Driven by a 2.5V LVPECL Driver with AC Couple

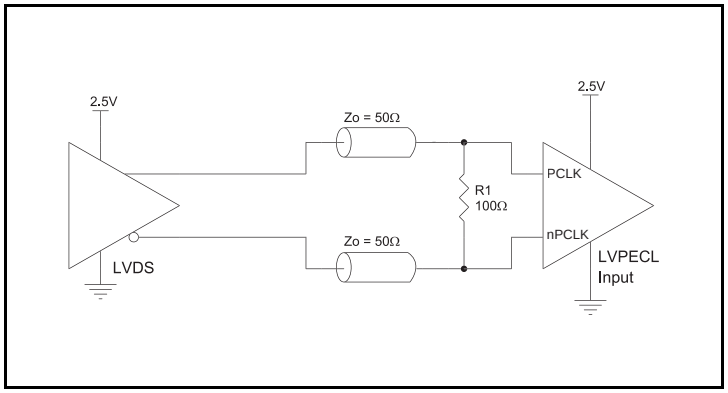


Figure 3E. PCLK/nPCLK Input Driven by a 2.5V LVDS Driver

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VFQFN EPAD Thermal Release Path

In order to maximize both the removal of heat from the package and the electrical performance, a land pattern must be incorporated on the Printed Circuit Board (PCB) within the footprint of the package corresponding to the exposed metal pad or exposed heat slug on the package, as shown in *Figure 4*. The solderable area on the PCB, as defined by the solder mask, should be at least the same size/shape as the exposed pad/slug area on the package to maximize the thermal/electrical performance. Sufficient clearance should be designed on the PCB between the outer edges of the land pattern and the inner edges of pad pattern for the leads to avoid any shorts.

While the land pattern on the PCB provides a means of heat transfer and electrical grounding from the package to the board through a solder joint, thermal vias are necessary to effectively conduct from the surface of the PCB to the ground plane(s). The land pattern must be connected to ground through these vias. The vias act as “heat pipes”. The number of vias (i.e. “heat pipes”) are application specific and dependent upon the package power dissipation as well as electrical conductivity requirements. Thus, thermal and electrical analysis and/or testing are recommended to determine the minimum number needed. Maximum thermal and electrical performance is achieved when an array of vias is incorporated in the land pattern. It is recommended to use as many vias connected to ground as possible. It is also recommended that the via diameter should be 12 to 13mils (0.30 to 0.33mm) with 1oz copper via barrel plating. This is desirable to avoid any solder wicking inside the via during the soldering process which may result in voids in solder between the exposed pad/slug and the thermal land. Precautions should be taken to eliminate any solder voids between the exposed heat slug and the land pattern. Note: These recommendations are to be used as a guideline only. For further information, please refer to the Application Note on the Surface Mount Assembly of Amkor’s Thermally/ Electrically Enhance Leadframe Base Package, Amkor Technology.

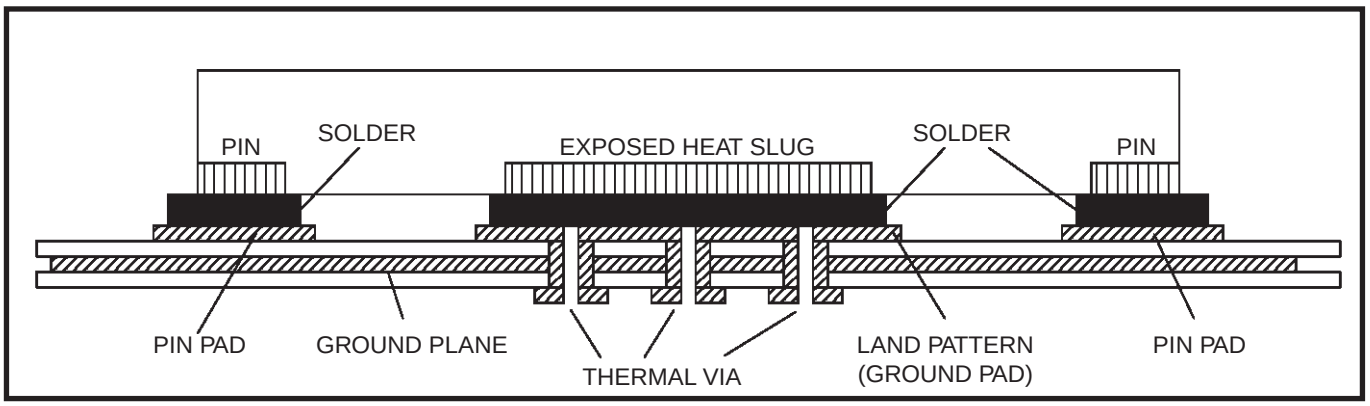


Figure 4. P.C. Assembly for Exposed Pad Thermal Release Path – Side View (drawing not to scale)

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Termination for 3.3V LVPECL Outputs

The clock layout topology shown below is a typical termination for LVPECL outputs. The two different layouts mentioned are recommended only as guidelines.

The differential outputs are a low impedance follower output that generate ECL/LVPECL compatible outputs. Therefore, terminating resistors (DC current path to ground) or current sources must be used for functionality. These outputs are designed to drive 50Ω transmission lines. Matched impedance techniques should be used to maximize operating frequency and minimize signal distortion. *Figures 5A and 5B* show two different layouts which are recommended only as guidelines. Other suitable clock layouts may exist and it would be recommended that the board designers simulate to guarantee compatibility across all printed circuit and clock component process variations.

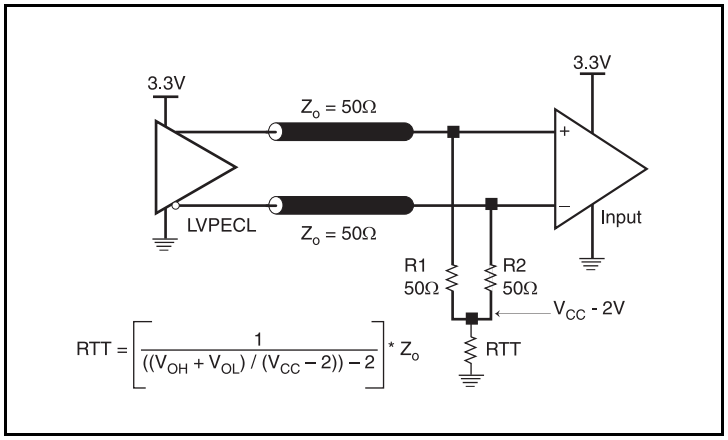


Figure 5A. 3.3V LVPECL Output Termination

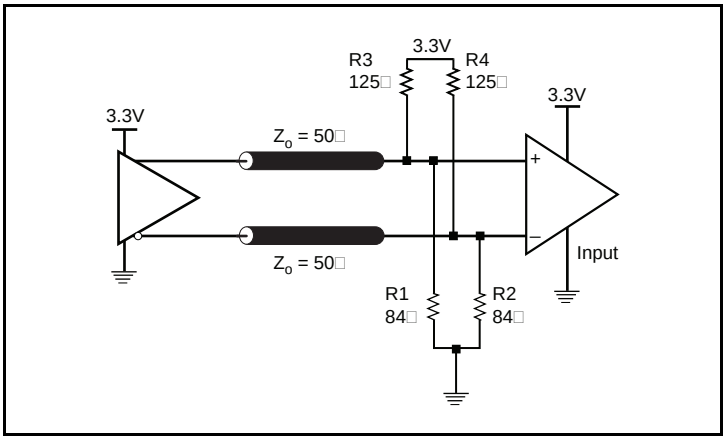


Figure 5B. 3.3V LVPECL Output Termination

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Termination for 2.5V LVPECL Outputs

Figure 6A and *Figure 6B* show examples of termination for 2.5V LVPECL driver. These terminations are equivalent to terminating 50Ω to V_{CC} – 2V. For V_{CC} = 2.5V, the V_{CC} – 2V is very close to ground level. The R3 in Figure 6B can be eliminated and the termination is shown in *Figure 6C*.

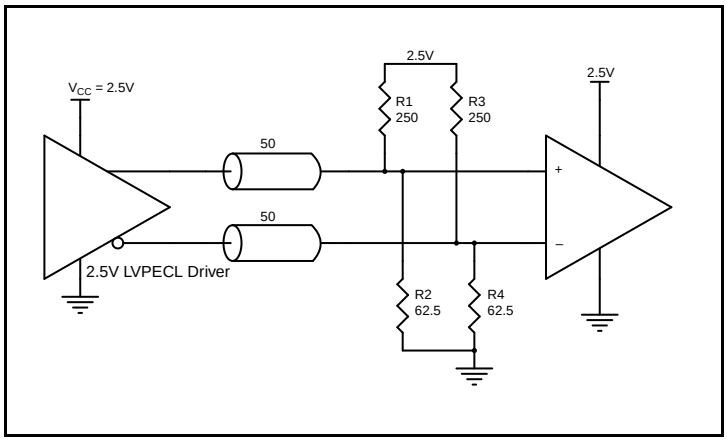


Figure 6A. 2.5V LVPECL Driver Termination Example

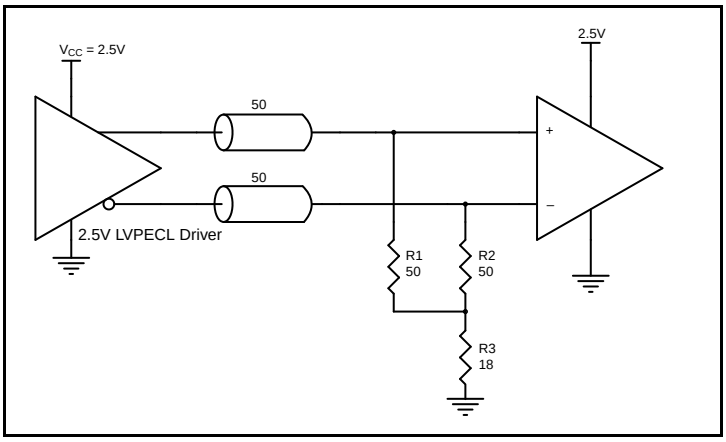


Figure 6B. 2.5V LVPECL Driver Termination Example

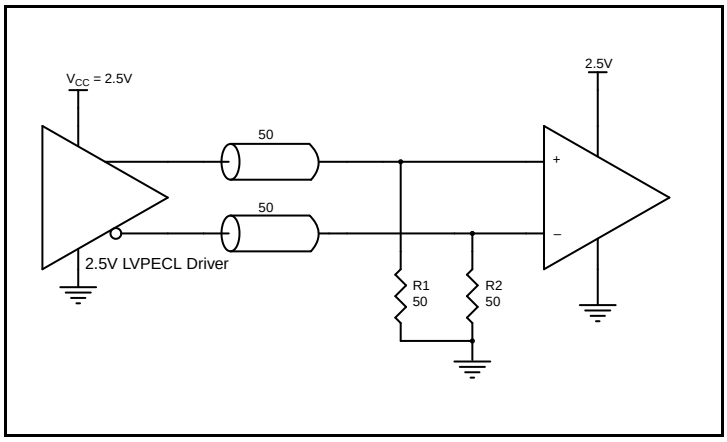


Figure 6C. 2.5V LVPECL Driver Termination Example

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Termination for Q, nQ LVPECL Outputs AC-Coupled into HCSL-Receiver

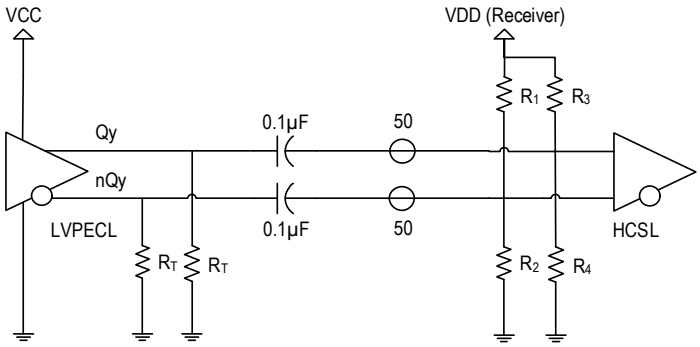


Figure 7. LVPECL Output AC-Coupled into HCSL Receiver

Table 6. Termination Resistors

	V_{CC} = 2.5V	V_{CC} = 3.3V
R_T	100Ω	180Ω

Table 7. HCSL Receiver Voltage Bias

	V_{DD} = 2.5V	V_{DD} = 3.3V
R_1, R_3	357Ω	470Ω
R_2, R_4	58Ω	56Ω

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Power Considerations

This section provides information on power dissipation and junction temperature for the 8SLVP1212.
Equations and example calculations are also provided.

1. Power Dissipation.

The total power dissipation for the 8SLVP1212 is the sum of the core power plus the power dissipation in the load(s).
The following is the power dissipation for V_{CC} = 3.3V + 5% = 3.465V, which gives worst case results.

NOTE: Please refer to Section 3 for details on calculating power dissipation in the load.

- Power $(core)_{MAX} = V_{CC_MAX} * I_{EE_MAX}$ = 3.465V * 131mA = **453.9mW**
- Power $(outputs)_{MAX}$ = **35.2mW/Loaded Output pair**
  If all outputs are loaded, the total power is 12 * 35.2mW = **422.4mW**

Total Power$_{MAX}$ (3.465V, with all outputs switching) = 453.9mW + 422.4mW = **876.3mW**

2. Junction Temperature.

Junction temperature, Tj, is the temperature at the junction of the bond wire and bond pad, and directly affects the reliability of the device. The maximum recommended junction temperature is 125°C. Limiting the internal transistor junction temperature, Tj, to 125°C ensures that the bond wire and bond pad temperature remains below 125°C.

The equation for Tj is as follows: $Tj = \theta_{JA} * Pd_total + T_A$

Tj = Junction Temperature

θ_{JA} = Junction-to-Ambient Thermal Resistance

Pd_total = Total Device Power Dissipation (example calculation is in section 1 above)

T_A = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance θ_{JA} must be used. Assuming no air flow and a multi-layer board, the appropriate value is 38.1°C/W per Table 6 below.

Therefore, Tj for an ambient temperature of 85°C with all outputs switching is:

85°C + 0.876W * 38.1°C/W = 118.4°C. This is below the limit of 125°C.

This calculation is only an example. Tj will obviously vary depending on the number of loaded outputs, supply voltage, air flow and the type of board (multi-layer).

Table 8. Thermal Resistance θ_{JA} for a 40-Lead VFQFN

θ_{JA} **at 0 Air Flow**			
Meters per Second	**0**	**1**	**2**
Multi-Layer PCB, JEDEC Standard Test Boards	38.1°C/W	32.0°C/W	29.9°C/W

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3. Calculations and Equations.

The purpose of this section is to calculate the power dissipation for the LVPECL output pair.

The LVPECL output driver circuit and termination are shown in *Figure 8.*

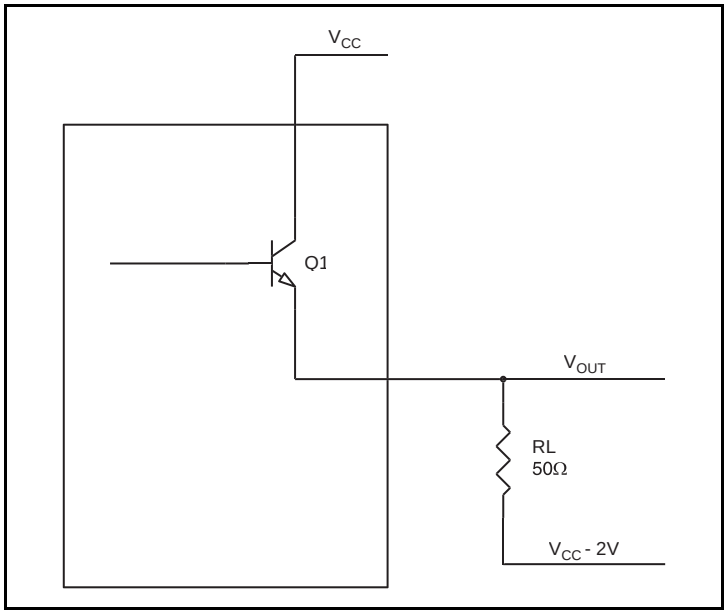


Figure 8. LVPECL Driver Circuit and Termination

To calculate power dissipation per output pair due to loading, use the following equations which assume a 50Ω load, and a termination voltage of V_{CC} – 2V.

- For logic high, $V_{OUT} = V_{OH_MAX} = \mathbf{V_{CC_MAX} – 0.6V}$
  $(V_{CC_MAX} – V_{OH_MAX}) = \mathbf{0.6V}$
- For logic low, $V_{OUT} = V_{OL_MAX} = \mathbf{V_{CC_MAX} – 1.28V}$
  $(V_{CC_MAX} – V_{OL_MAX}) = \mathbf{1.28V}$

Pd_H is power dissipation when the output drives high.

Pd_L is the power dissipation when the output drives low.

$Pd_H = [(V_{OH_MAX} – (V_{CC_MAX} – 2V))/R_L] * (V_{CC_MAX} – V_{OH_MAX}) = [(2V - (V_{CC_MAX} – V_{OH_MAX}))/R_L] * (V_{CC_MAX} – V_{OH_MAX}) =$
$[(2V – 0.6V)/50\Omega] * 0.6V =$ **16.8mW**

$Pd_L = [(V_{OL_MAX} – (V_{CC_MAX} – 2V))/R_L] * (V_{CC_MAX} – V_{OL_MAX}) = [(2V – (V_{CC_MAX} – V_{OL_MAX}))/R_L] * (V_{CC_MAX} – V_{OL_MAX}) =$
$[(2V – 1.28V)/50\Omega] * 1.28V =$ **18.4mW**

Total Power Dissipation per output pair = Pd_H + Pd_L = **35.2mW**

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Reliability Information

Table 9. θ_{JA} vs. Air Flow Table for a 40-VFQFPN

θ_{JA} at 0 Air Flow			
Meters per Second	**0**	**1**	**2**
Multi-Layer PCB, JEDEC Standard Test Boards	38.1°C/W	32.0°C/W	29.9°C/W

Transistor Count

The transistor count for the 8SLVP1212 is: 7748

Package Outline Drawings

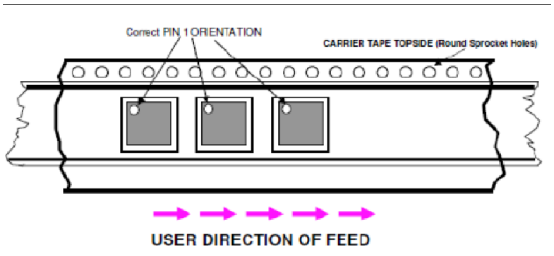
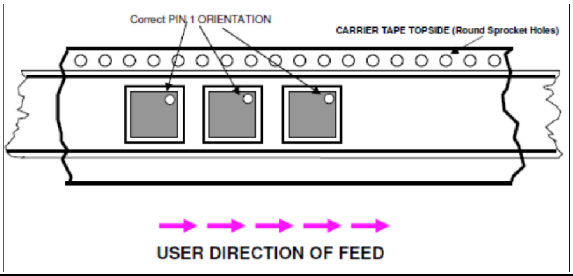
The package outline drawings are located at the end of this document and are accessible from the Renesas website (see Ordering Information for POD links). The package information is the most current data available and is subject to change without revision of this document.

Ordering Information

Table 10. Ordering Information

Part/Order Number	Marking	Package	Shipping Packaging	Temperature
8SLVP1212ANLGI	IDT8SLVP1212ANLGI	6.0 × 6.0 mm 40-VFQFPN	Tray	-40°C to +85°C
8SLVP1212ANLGI8	IDT8SLVP1212ANLGI		Tape & Reel, pin 1 orientation: EIA-481-C	-40°C to +85°C
8SLVP1212ANLGI/W	IDT8SLVP1212ANLGI		Tape & Reel, pin 1 orientation: EIA-481-D	-40°C to +85°C

Table 11. Pin 1 Orientation in Tape and Reel Packaging

Part Number Suffix	Pin 1 Orientation	Illustration
8	Quadrant 1 (EIA-481-C)	
/W	Quadrant 2 (EIA-481-D)	

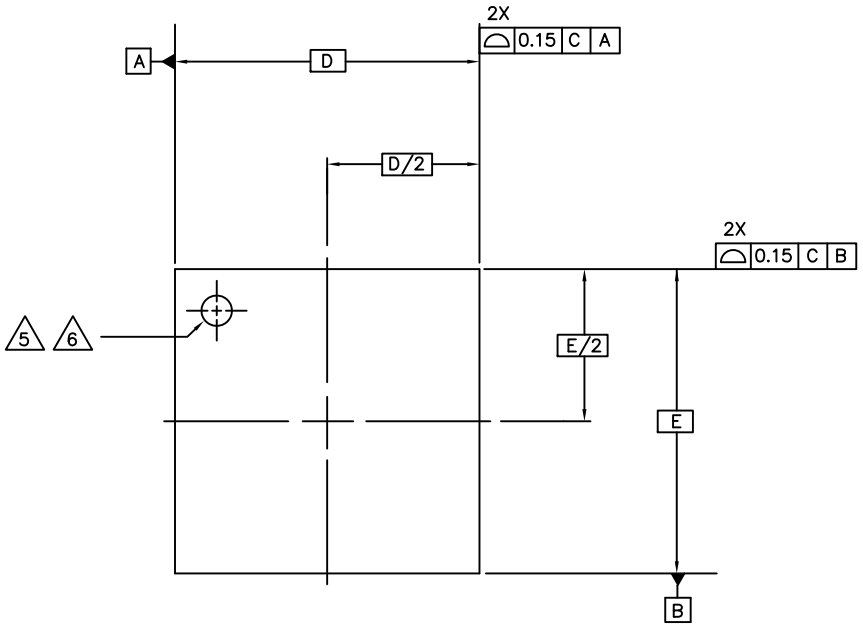
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Revision History Sheet

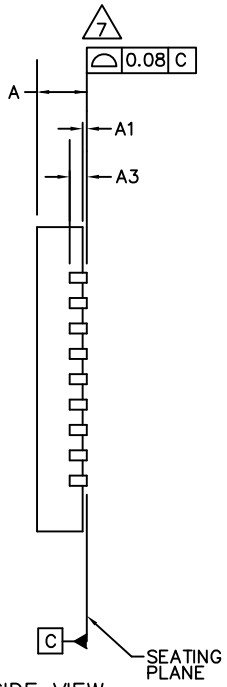
Date	Description of Change
May 20, 2021	• Added Termination for Q, nQ LVPECL Outputs AC-Coupled into HCSL-Receiver section. • Added Features bullet: Supports PCI Express Gen1–5.
January 28, 2014	Changed Note 5 to read "V_{IL} should not be less than -0.3V. V_{IH} should not be higher than V_{CC}."
January 30, 2013	• Added Features Bullet: Differential PCLKA, nPCLKA and PCLKB, nPCLKB pairs can also accept single-ended LVCMOS levels. • Added NOTE 7 to V_{PP}, V_{CMR}. • Updated the "Wiring the Differential Input to Accept Single-Ended Levels" note.

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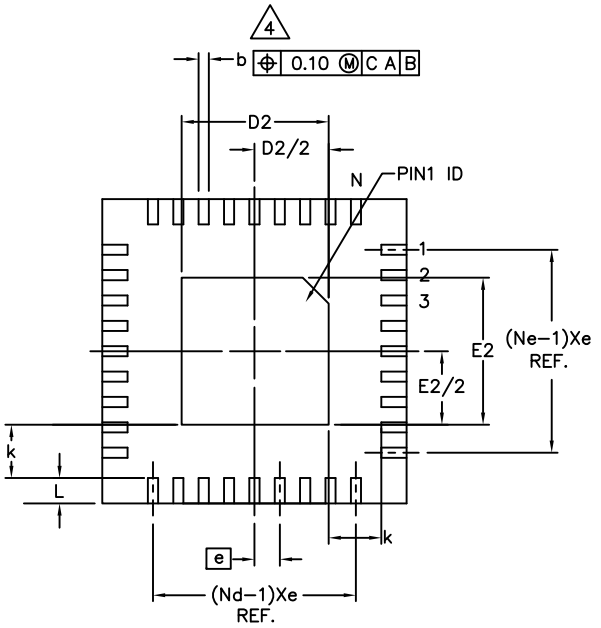
REVISIONS			
REV	DESCRIPTION	DATE	APPROVED
00	INITIAL RELEASE	02/4/16	JH



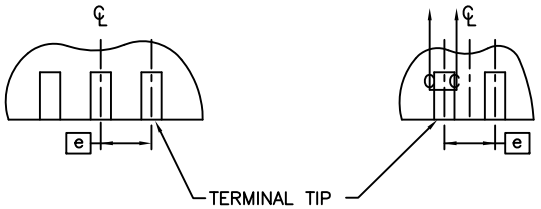
TOP VIEW



SIDE VIEW

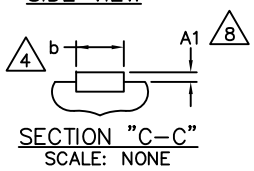


BOTTOM VIEW

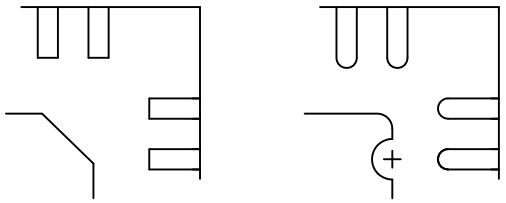


FOR ODD TERMINAL/SIDE

FOR EVEN TERMINAL/SIDE



SECTION "C–C"
SCALE: NONE



PIN #1 ID AND TIE BAR MARK OPTION

TOLERANCES UNLESS SPECIFIED DECIMAL ANGULAR XX± ± XXX± XXXX±		IDT™ www.IDT.com	6024 SILVERCREEK VALLEY ROAD SAN JOSE CA.95138 PHONE: (408) 284–8200 FAX: (408) 284–8591
APPROVALS	DATE	TITLE	NL/NLG 40 PACKAGE OUTLINE 6.0 X 6.0 mm BODY EPAD 2.90 x 2.90 mm QFN
DRAWN PSC	02/4/16		
CHECKED			
		SIZE C	DRAWING No. PSC–4115–01 REV 00
		DO NOT SCALE DRAWING	SHEET 1 OF 3

REVISIONS			
REV	DESCRIPTION	DATE	APPROVED
00	INITIAL RELEASE	02/4/16	JH

NOTES:

1. DIMENSIONING & TOLERANCING CONFORM TO ASME Y14.5M. – 1994.
2. N IS THE NUMBER OF TERMINALS.
   Nd IS THE NUMBER OF TERMINALS IN X–DIRECTION &
   Ne IS THE NUMBER OF TERMINALS IN Y–DIRECTION.
3. ALL DIMENSIONS ARE IN MILLIMETERS.
4. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.20 AND 0.30mm FROM TERMINAL TIP.
5. THE PIN #1 IDENTIFIER MUST EXIST ON THE TOP SURFACE OF THE PACKAGE BY USING INDENTATION MARK OR OTHER FEATURE OF PACKAGE BODY.
6. EXACT SHAPE AND SIZE OF THIS FEATURE IS OPTIONAL.
7. APPLIED TO EXPOSED PAD AND TERMINALS. EXCLUDE EMBEDDED PART OF EXPOSED PAD FROM MEASURING.
8. APPLIED ONLY FOR TERMINALS.
9. THIS OUTLINES CONFORMS TO JEDEC PUBLICATION 95 REGISTRATION MO–220, VARIATION VJJC–3 & VJJD–5 WITH THE EXCEPTION OF D2 & E2.

SYMBOL	DIMENSION			NOTE
	MIN	NOM	MAX	
b	0.18	0.25	0.30	4
D		6.00 BSC		
E		6.00 BSC		
D2	2.80	2.90	3.00	
E2	2.80	2.90	3.00	
L	0.30	0.40	0.50	
e		0.50 BSC		
k		1.15 REF.		
N		40		2
A	0.80	0.90	1.00	
A1	0.00	0.02	0.05	7
A3		0.2 REF		
Nd		10		2
Ne		10		2

TOLERANCES UNLESS SPECIFIED
DECIMAL ANGULAR
XX± ±
XXX±
XXXX±

APPROVALS DATE
DRAWN RdC 02/4/16
CHECKED

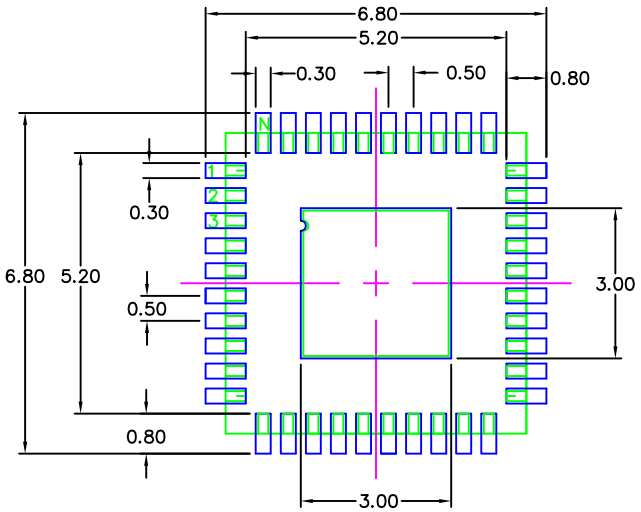
IDT™ www.IDT.com
6024 SILVERCREEK VALLEY ROAD
SAN JOSE CA.95138
PHONE: (408) 284–8200
FAX: (408) 284–8591

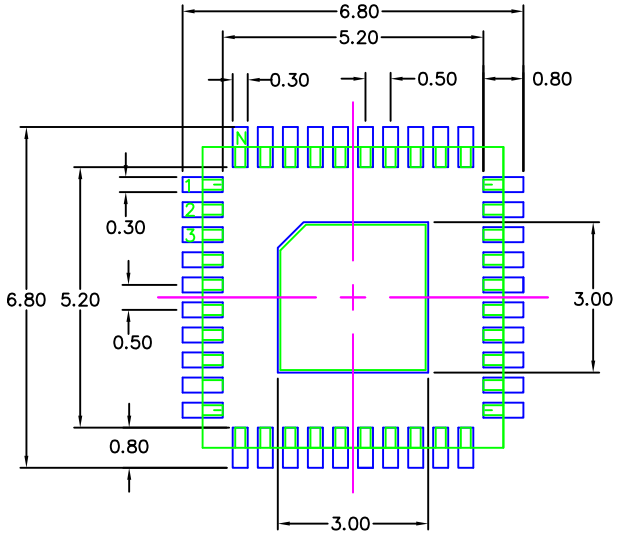
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6.0 X 6.0 mm BODY
EPAD 2.90 x 2.90 mm QFN

SIZE C | DRAWING No. PSC–4115–01 | REV 00

DO NOT SCALE DRAWING |

REVISIONS			
REV	DESCRIPTION	DATE	APPROVED
00	INITIAL RELEASE	02/4/16	JH





RECOMMENDED LAND PATTERN

NOTES:

1. ALL DIMENSIONS ARE IN mm. ANGLES IN DEGREES.
2. TOP DOWN VIEW. AS VIEWED ON PCB.
3. COMPONENT OUTLINE SHOWS FOR REFERENCE IN GREEN.
4. LAND PATTERN IN BLUE. NSMD PATTERN ASSUMED.
5. LAND PATTERN RECOMMENDATION PER IPC-7351B GENERIC REQUIREMENT FOR SURFACE MOUNT DESIGN AND LAND PATTERN.

TOLERANCES UNLESS SPECIFIED DECIMAL ANGULAR XX± ± XXX± XXXX±		IDT™ www.IDT.com	6024 SILVERCREEK VALLEY ROAD SAN JOSE CA.95138 PHONE: (408) 284-8200 FAX: (408) 284-8591
APPROVALS	DATE	TITLE	NL/NLG 40 PACKAGE OUTLINE 6.0 X 6.0 mm BODY EPAD 2.90 x 2.90 mm QFN
DRAWN RdC	02/4/16		
CHECKED			
		SIZE C	DRAWING No. PSC-4115-01 REV 00
		DO NOT SCALE DRAWING	SHEET 3 OF 3

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(Rev.1.0 Mar 2020)

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