Description

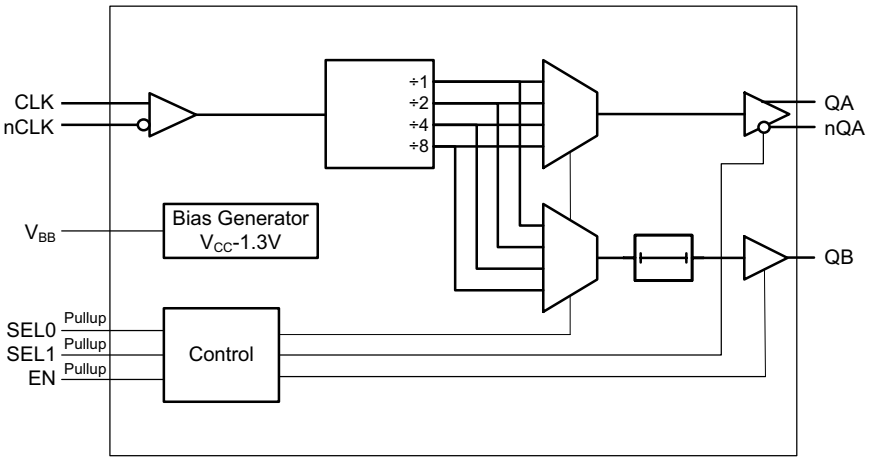
The 8T73S1802 is a fully integrated clock fanout buffer and frequency divider. The input signal is frequency-divided and then fanned out to one differential LVPECL and one LVCMOS output. Each of the outputs can select its individual divider value from the range of ÷1, ÷2, ÷4 and ÷8. Three control inputs EN, SEL0 and SEL1 (3-level logic) are available to select the frequency dividers and the output enable/disable state. The single-ended LVCMOS output is phase-delayed by 650ps to minimize coupling of LVCMOS switching into the differential output during its signal transition.

The 8T73S1802 is optimized to deliver very low phase noise clocks. The V_{BB} output generates a common-mode voltage reference for the differential clock input so that connecting the V_{BB} pin to an unused input (nCLK) enables to use of single-ended input signals. The extended temperature range supports wireless infrastructure, telecommunication and networking end equipment requirements. The 8T73S1802 can be used with a 3.3V or a 2.5V power supply. The device is a member of the high-performance clock family from IDT.

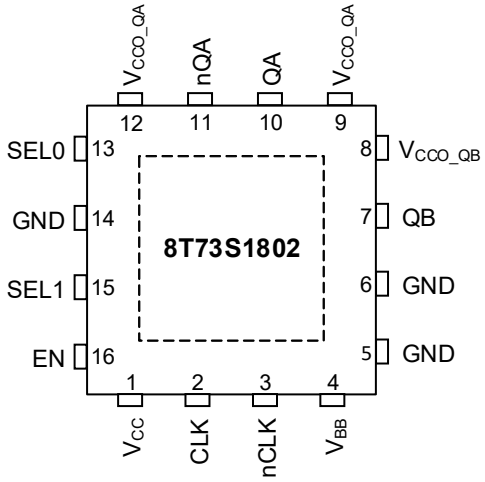
Features

- High-performance fanout buffer clock and fanout buffer
- Input clock signal is distributed to one LVPECL and one LVCMOS output
- Configurable output dividers for both LVPECL and LVCMOS outputs
- Supports clock frequencies up to 1000MHz (LVPECL) and up to 200MHz (LVCMOS)
- Flexible differential input supports LVPECL, LVDS and CML
- V_{BB} generator output supports single-ended input signal applications
- Optimized for low phase noise
- 650ps delay between LVCMOS and LVPECL minimizes coupling between outputs
- Supply voltage: 3.3V or 2.5V
- -40°C to 85°C ambient operating temperature
- 16 VFQFPN package (3 x 3 mm)

Block Diagram



Pin Assignment



16-pin, 3mm x 3mm VFQFPN Package

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Pin Description and Pin Characteristic Tables

Table 1. Pin Assignment

Pin Number	Name	Type[1]		Description
1	V_{CC}	Power		Power supply voltage for the device core and the inputs.
2	CLK	Input		Non-inverting differential clock input. Compatible with LVPECL, LVDS and CML signals.
3	nCLK	Input		Inverting differential clock input. Compatible with LVPECL, LVDS and CML signals.
4	V_{BB}	Output		Bias voltage generator output. Use to bias the nCLK input in single-ended input applications. V_{BB} = V_{CC} - 1.3V.
5	GND	Power		Ground supply voltage (GND) and ground return path. Connect to board GND (0V).
6	GND	Power		Ground supply voltage (GND) and ground return path. Connect to board GND (0V).
7	QB	Output		LVCMOS clock output QB. LVCMOS/LVTTL interface levels. If this pin is disabled by connecting its power supply pin V_{CCO_QB} to GND, QB must be left open or connected to GND.
8	V_{CCO_QB}	Power		Positive supply voltage for the QB output. The QB output (if not connected) can be disabled by connecting this pin to GND.
9	V_{CCO_QA}	Power		Positive supply voltage for the QA, nQA output. The QA, nQA output (if not connected) can be disabled by connecting this pin to GND.
10	QA	Output		Differential clock output QA. LVPECL interface levels. If this pin is disabled by connecting its power supply pins V_{CCO_QA} to GND, QA and nQA must be left open or connected to GND.
11	nQA	Output		Differential clock output QA. LVPECL interface levels. If this pin is disabled by connecting its power supply pins V_{CCO_QA} to GND, QA and nQA must be left open or connected to GND.
12	V_{CCO_QA}	Power		Positive supply voltage for the QA, nQA output. The QA, nQA output (if not connected) can be disabled by connecting this pin to GND.
13	SEL0	Input	60kΩ Pullup	Configuration pins. 3-Level interface. See Table 3 for function and Table 4D for interface levels.
14	GND	Power		Ground supply voltage (GND) and ground return path. Connect to board GND (0V).
15	SEL1	Input	60kΩ Pullup	Configuration pins. 3-Level interface. See Table 3 for function and Table 4D for interface levels.
16	EN	Input	60kΩ Pullup	Configuration pin. 3-Level interface. See Table 3 for function and Table 4D for interface levels.

NOTE 1. *Pullup* refers to internal input resistors. See Table 2, *Pin Characteristics,* for typical values.

Table 2. Pin Characteristics

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
C_{IN}	Input Capacitance			2		pF
C_{PD}	Power Dissipation Capacitance			5.4		pF
R_{PULLUP}	Input Pullup Resistor		42	60	78	kΩ
R_{OUT}	LVCMOS Output Resistance	V_{CCO_QB} = 2.375V		38		Ω
		V_{CCO_QB} = 3.465V		28		Ω

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Principles Of Operation

Control Pins

The control input pins SEL0, SEL1 and EN are 3-level inputs with internal 60kΩ resistors that pull the input to the V_{CC} level when left open. Each input has three logic states: low (0), mid ($V_{CC}/2$) and high (1). Connect a control input to GND for achieving the low (0) state. For the high (1) state, connect the input to V_{CC} or leave the input open. For the mid state, connect an external 60kΩ resistor from the input to GND. See Table 4D for the 3-state input min and max levels.

Operation Modes

The device offers a many combinations of divider values and output enable states. See Table 3 for the supported modes.

Table 3. Operation Modes[1]

Input[2 3 4]			Output Divider	
EN	**SEL1**	**SEL0**	**QA (LVPECL)**	**QB (LVCMOS)**
0	X	X	Disabled	Disabled
MID	0	0	÷4	÷4
		MID	÷1	÷1
		1	÷2	÷2
	MID	MID	÷8	÷1
		1	÷1	÷2
	1	0	÷4	÷8
1	0	0	÷1	÷4
		1	÷2	÷4
	1	0	÷8	÷4
		1	Disable	÷4

NOTE 1. In the default state (control input left open), QA is disabled and QB = ÷4.
NOTE 2. 0 = Low, MID = $V_{CC}/2$, 1 = High; X = either 0, MID or 1.
NOTE 3. 0 = Low, MID = $V_{CC}/2$, 1 = High; X = either 0, MID or 1.
NOTE 4. Unspecified EN, SEL1, SEL0 input logic states are reserved and should not be used.

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Absolute Maximum Ratings

NOTE: Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of the product at these conditions or any conditions beyond those listed in the *DC Characteristics or AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Item	Rating
Supply Voltage, V_{CC}	3.6V
Inputs, V_I	-0.5V to V_{CC} + 0.5V
Outputs, V_O (LVCMOS)	-0.5V to V_{CCO_QB} + 0.5V
Outputs, I_O (LVPECL) Continuous Current Surge Current	 10mA 15mA
Maximum Junction Temperature, T_{J_MAX}	125°C
Storage Temperature, T_{STG}	-65°C to 150°C
ESD - Human Body Model[1]	2000V
ESD - Charged Device Model	1500V

NOTE 1. According to JEDEC/JESD 22-A114/22-C101.

Electrical Characteristics

Table 4A. 3.3V Power Supply Characteristics, V_{CC} = V_{CCO_QA} = V_{CCO_QB} = 3.0V to 3.465V, T_A = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{CC}	Power Supply Voltage		3.0	3.3	3.465	V
V_{CCO_QA}, V_{CCO_QB}	Output Supply Voltage		3.0	3.3	3.465	V
I_{CC}	Power Supply Current[1]	All outputs enabled and terminated with 50Ω to V_{CC} – 2V on LVPECL outputs and 10pF on LVCMOS output; f = 800MHz for LVPECL outputs and 200MHz for LVCMOS, V_{CC} = 3.3V		120		mA
		Outputs enabled, no load; f = 800MHz for LVPECL outputs and 200MHz for LVCMOS, V_{CC} = 3.465V			104	mA
I_{CCZ}	Power Supply Current[1]	Outputs Disabled, EN = 0, f_{IN} = 0Hz, V_{CC} = 3.465V			8.2	mA
I_{EE}	Power Supply Current	All outputs enabled and terminated with 50Ω to V_{CC} – 2V on LVPECL outputs and 10pF on LVCMOS output; f = 800MHz for LVPECL outputs and 200MHz for LVCMOS		92	109	mA

NOTE 1. I_{CC} includes output current.

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Table 4B. 2.5V Power Supply Characteristics, V_{CC} = V_{CCO_QA} = V_{CCO_QB} = 2.5V ± 5%, T_A = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{CC}	Power Supply Voltage		2.375	2.5	2.625	V
V_{CCO_QA}, V_{CCO_QB}	Output Supply Voltage		2.375	2.5	2.625	V
I_{CC}	Power Supply Current[1]	All outputs enabled and terminated with 50Ω to V_{CC} – 2V on LVPECL outputs and 10pF on LVCMOS output; f = 800MHz for LVPECL outputs and 200MHz for LVCMOS, V_{CC} = 2.5V		114		mA
		Outputs enabled, no load; f = 800MHz for LVPECL outputs and 200MHz for LVCMOS, V_{CC} = 2.625V			96	mA
I_{CCZ}	Power Supply Current[1]	Outputs Disabled, EN = 0, f_{IN} = 0Hz, V_{CC} = 2.625V			1.5	mA
I_{EE}	Power Supply Current	All outputs enabled and terminated with 50Ω to V_{CC} – 2V on LVPECL outputs and 10pF on LVCMOS output; f = 800MHz for LVPECL outputs and 200MHz for LVCMOS		85	99	mA

NOTE 1. I_{CC} includes output current.

Table 4C. Differential Characteristics, V_{CC} = V_{CCO_QA} = 3.0V to 3.465V or 2.5V±5%, T_A = -40°C to 85°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
I_{IH}	Input High Current	CLK, nCLK	V_{CC} = V_{IN} = V_{CC_MAX}			65	µA
I_{IL}	Input Low Current	CLK, nCLK	V_{CC} = V_{CC_MAX}, V_{IN} = 0V	-10			µA
R_{IN}	Input Impedance	CLK, nCLK			22		kΩ
V_{BB}	Reference Voltage for Input Bias		I_{BB} = -0.2mA	V_{CC} – 1.4		V_{CC} – 1.2	V
V_{OH}	Output High Voltage[1]			V_{CCO_QA} – 1.18		V_{CCO_QA} – 0.81	V
V_{OL}	Output Low Voltage[1]			V_{CCO_QA} – 1.98		V_{CCO_QA} – 1.55	V
I_{OZH}	Output Disabled Leakage Current[2]		V_{CC} = $V_{CCO_QA_MAX}$ V_O = V_{CC}-0.8V			40	µA
I_{OZL}	Output Disabled Leakage Current[2]		V_{CC} = $V_{CCO_QA_MAX}$ V_O = 0V			5	µA

NOTE 1. QA, nQA Outputs terminated with 50Ω to V_{CC} – 2V.

NOTE 2. Maximum voltage applied to a disabled (high-impedance) output is 3.465V.

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Table 4D. Single-Ended Characteristics, V_{CC} = V_{CCO_QB} = 3.0V to 3.465V or 2.5V±5%, T_A = -40°C to 85°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
V_{IH}	Input High Voltage[1]			0.9 x V_{CC}			V
V_{IM}	Input Mid Voltage[1]		V_{CC} = 3.0V to 3.465V	0.35 x V_{CC}		0.65 x V_{CC}	V
			V_{CC} = 2.5V ±5%	0.4 x V_{CC}		0.6 x V_{CC}	V
V_{IL}	Input High Voltage[1]			-0.3		0.1 x V_{CC}	V
I_{IH}	Input High Current[1]		V_{IN} = V_{CC}			5	µA
I_{IL}	Input Low Current[1]		V_{IN} = 0V, V_{CC} = 3.0V to 3.465V	-85		-38	µA
			V_{IN} = 0V, V_{CC} = 2.5V ±5%	-62		-30	µA
V_{OH}	High-Level Voltage	QB	V_{CC} = 3.0V to V_{CC_MAX}, I_{OH} = -100µA	V_{CCO_QB} – 0.1			V
			V_{CC} = 3.0V, I_{OH} = -6mA	2.4			V
			V_{CC} = 3.0V, I_{OH} = -12mA	2			V
V_{OL}	Low-Level Voltage	QB	V_{CC} = 3.0V to V_{CC_MAX}, I_{OL} = 100µA			0.1	V
			V_{CC} = 3.0V, I_{OL} = 6mA			0.5	V
			V_{CC} = 3.0V, I_{OL} = 12mA			0.8	V
I_{OH}	High-Level Current	QB	V_{CC} = 3.3V, V_O = 1.65V		-39		mA
I_{OL}	Low-Level Current	QB	V_{CC} = 3.3V, V_O = 1.65V		44		mA
I_{OZ}	Output Disabled Leakage Current		V_{CC} = V_{CC_MAX}, V_O = V_{CC} or V_O = 0V	-5		5	µA

NOTE 1. Single-ended input: SEL1, SEL0, EN.

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AC Electrical Characteristics

Table 5. AC Characteristics, V_{CC} = V_{CCO_QA} = V_{CCO_QB} = 3.0V to 3.465V or 2.5V±5%, T_A = -40°C to 85°C[1, 2]

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
f_{IN}	Input Frequency	CLK				1000	MHz
f_{OUT}	Output Frequency	QA				1000	MHz
		QB				200	MHz
V_{PP}	Peak-to-Peak Input Voltage[3]			0.15		1.3	V
V_{CMR}	Common Mode Input Voltage[4, 5]			1.0		V_{CC} – V_{PP} /2	V
V_O(pp)	Single-ended Output Voltage Swing, Peak-to-Peak	QA		0.5			V
V_{DIFF_OUT}	Differential Output Voltage Swing, Peak-to-Peak	QA		1.0			V
t_{PD}	Propagation Delay	CLK to QA	(Any Divider)	150	450	700	ps
		CLK to QB	(Any Divider)	900	1100	1500	ps
t_{DIS}	Output Disable Time		EN to Outputs Disabled (High-Impedance)		15		ns
t_{EN}	Output Enable Time		EN to Outputs Enabled		400		ns
*t*sk(o)	Output Skew[6, 7]	QA to QB	when QA and QB have the same Output Divider		650	1000	ps
*t*sk(pp)	Part-to-Part Skew	QA			50		ps
		QB			300		ps
*t*sk(p)	Pulse Skew	QA				100	ps
t(odc)	Output Duty Cycle Distortion[8]	QA[9]	f_{IN} = 800MHz	-50	0	50	ps
		QB	f_{IN} = 200MHz, N = 1	-225		225	ps
			f_{IN} = 200MHz, N = 2, 4, 8	-150		150	ps
t_R / t_F	Output Rise/Fall Time, Differential	QA	20% to 80%		120	350	ps
ΔV/Δt	Output Slew Rate	QB	20% to 80%, V_{CCO_QB} = 3.3V	1.4	5		V/ns
		QB	20% to 80%, V_{CCO_QB} = 2.5V	1.4	3		V/ns
*t*jit	Additive Phase Jitter	QA	200MHz – 1GHz, Integration Range: 12kHz - 20MHz			150	fs
		QA	200MHz – 1GHz, Integration Range: 50kHz - 40MHz			250	fs
		QB	250MHz, Integration Range: 12kHz - 20MHz			250	fs
		QB	250MHz, Integration Range: 50kHz - 40MHz			400	fs

NOTE 1. Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfpm. The device will meet specifications after thermal equilibrium has been reached under these conditions.

NOTE 2. QA is terminated 50Ω to V_T = V_{CC} - 2V, the QB load is terminated 50Ω to V_{CC}/2.

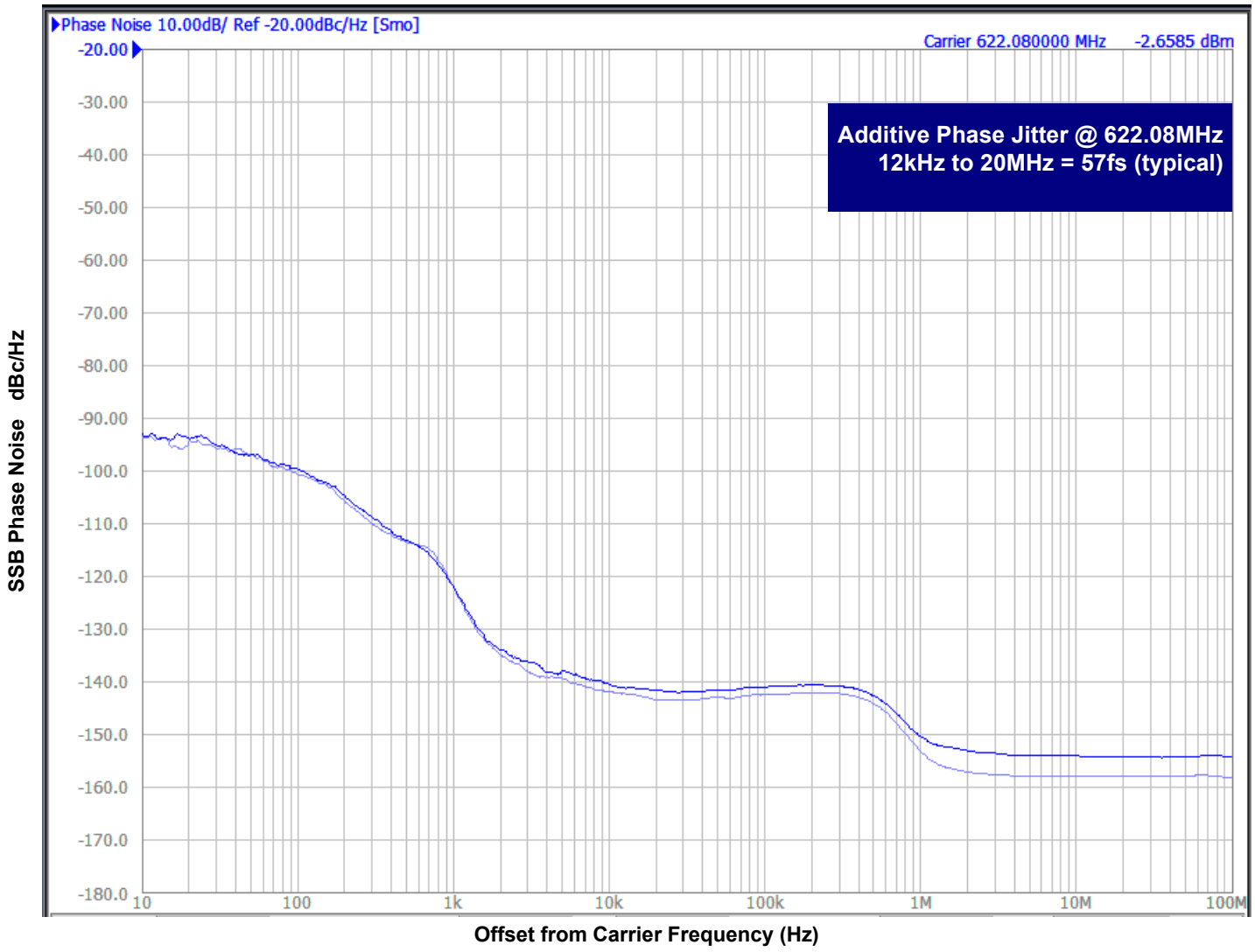
NOTE 3. For single-ended LVCMOS input applications, refer to the Applications section *Wiring the Differential Input Levels to Accept Single-ended Levels.*

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NOTE 4. V_{IL} should not be less than -0.3V. V_{IH} should not be higher than V_{CC}.
NOTE 5. Common mode input voltage is defined as the crosspoint.
NOTE 6. This parameter is defined in accordance with JEDEC standard 65.
NOTE 7. Defined as skew between outputs at the same supply voltage and with equal load conditions.
NOTE 8. Input CLK driven by an ideal clock input signal.
NOTE 9. Crosspoint to crosspoint distortion.

Additive Phase Jitter

The spectral purity in a band at a specific offset from the fundamental compared to the power of the fundamental is called the ***dBc Phase Noise.*** This value is normally expressed using a Phase noise plot and is most often the specified plot in many applications. Phase noise is defined as the ratio of the noise power present in a 1Hz band at a specified offset from the fundamental frequency to the power value of the fundamental. This ratio is expressed in decibels (dBm) or a ratio of the power in the 1Hz band to the power in the fundamental. When the required offset is specified, the phase noise is called a ***dBc*** value, which simply means dBm at a specified offset from the fundamental. By investigating jitter in the frequency domain, we get a better understanding of its effects on the desired application over the entire time record of the signal. It is mathematically possible to calculate an expected bit error rate given a phase noise plot.



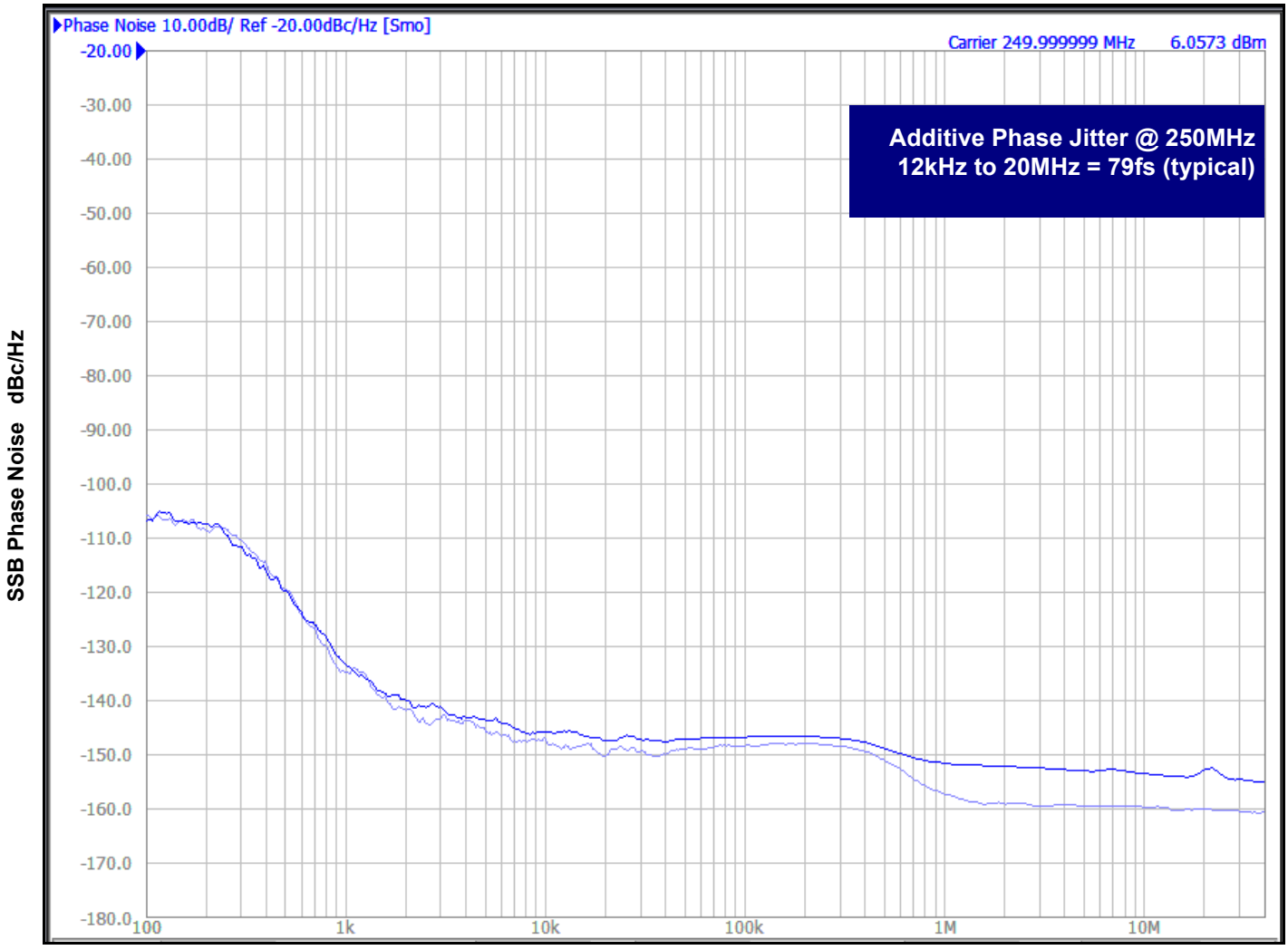
As with most timing specifications, phase noise measurements have issues relating to the limitations of the measurement equipment. The noise floor of the equipment can be higher or lower than the noise floor of the device. Additive phase noise is dependent on both the noise floor of the input source and measurement equipment.

The additive phase jitter for this device was measured using a Rhode & Schwarz SMA100 input source and an Agilent E5052 Phase noise analyzer.

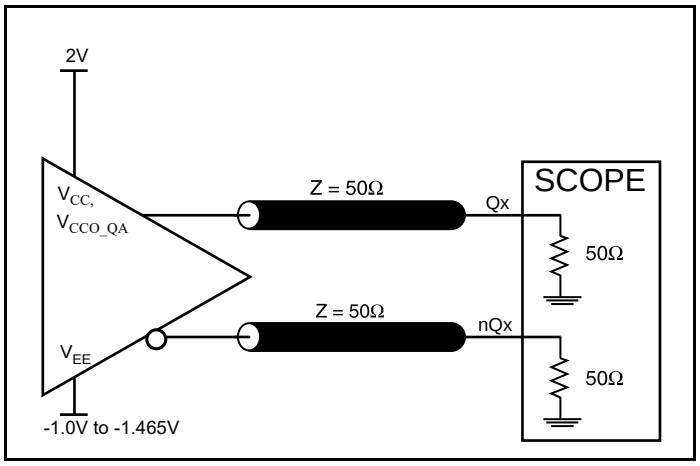
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Additive Phase Jitter

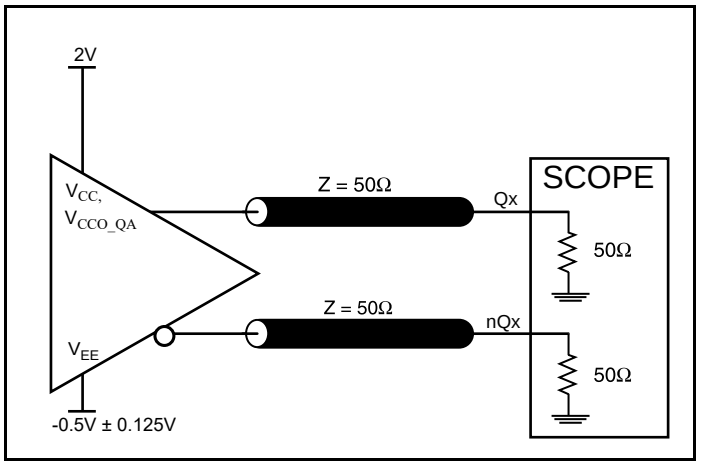
The spectral purity in a band at a specific offset from the fundamental compared to the power of the fundamental is called the ***dBc Phase Noise.*** This value is normally expressed using a Phase noise plot and is most often the specified plot in many applications. Phase noise is defined as the ratio of the noise power present in a 1Hz band at a specified offset from the fundamental frequency to the power value of the fundamental. This ratio is expressed in decibels (dBm) or a ratio of the power in the 1Hz band to the power in the fundamental. When the required offset is specified, the phase noise is called a ***dBc*** value, which simply means dBm at a specified offset from the fundamental. By investigating jitter in the frequency domain, we get a better understanding of its effects on the desired application over the entire time record of the signal. It is mathematically possible to calculate an expected bit error rate given a phase noise plot.



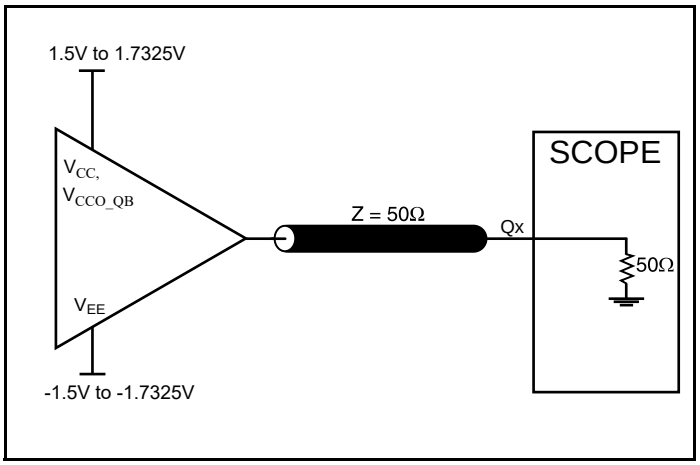
Parameter Measurement Information



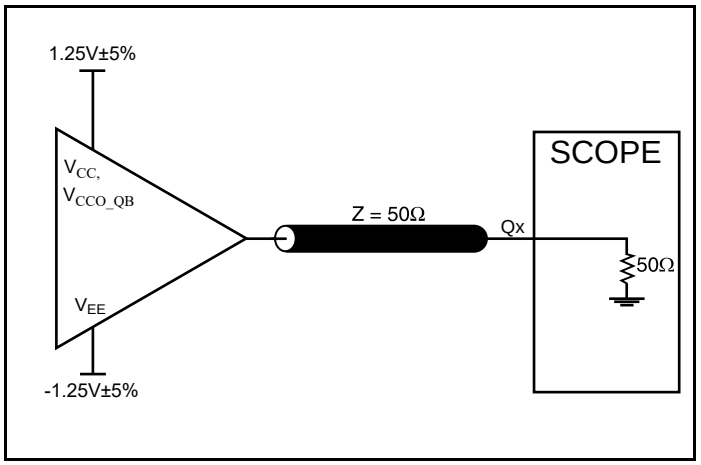
3.3 Core/3.3V LVPECL Output Load AC Test Circuit



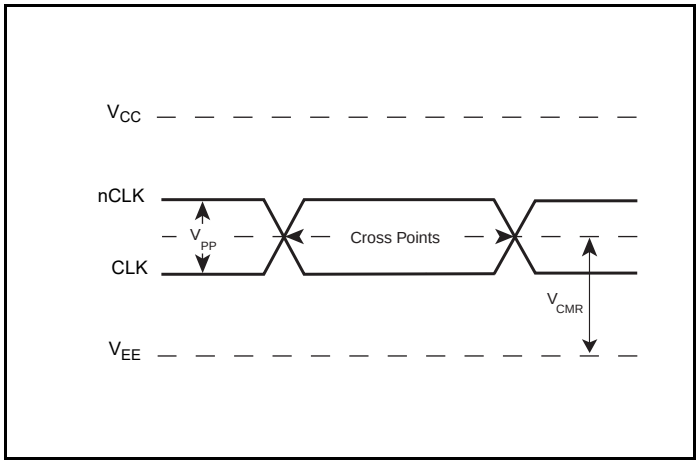
2.5V Core/2.5V LVPECL Output Load AC Test Circuit



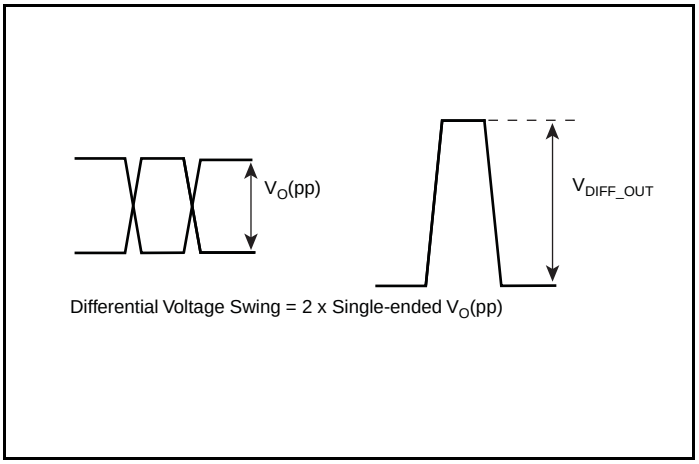
3.3 Core/3.3V LVCMOS Output Load AC Test Circuit



2.5V Core/2.5V LVCMOS Output Load AC Test Circuit

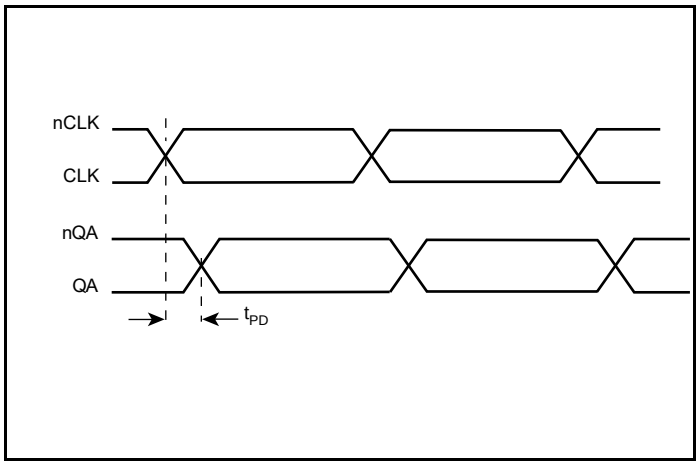


Differential Input Level

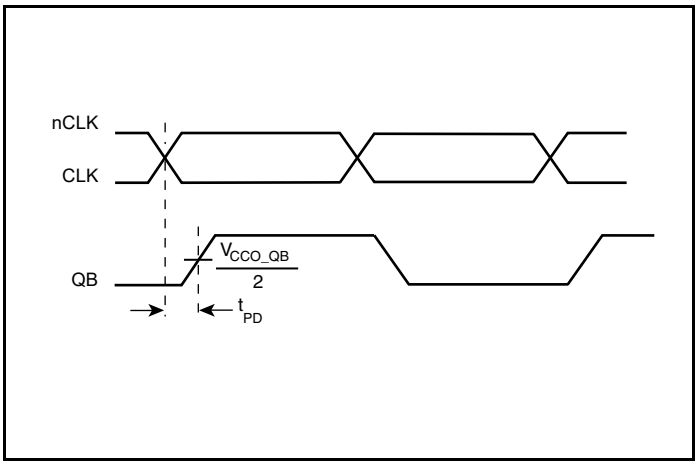


Single-Ended & Differential Output Voltage Swing

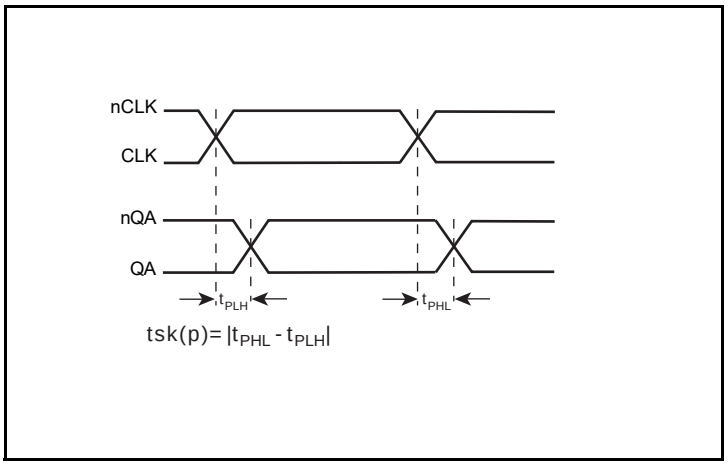
Parameter Measurement Information, continued



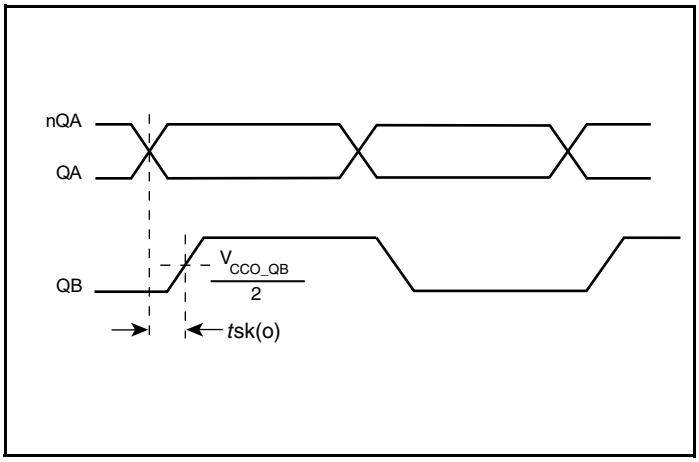
LVPECL Propagation Delay



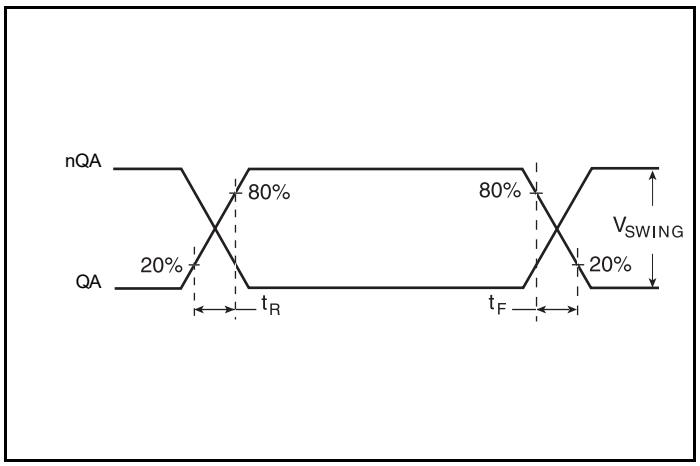
LVCMOS Propagation Delay



LVPECL Pulse Skew



Output Skew



Output Rise/Fall Time

Applications Information

3.3V LVPECL Clock Input Interface

The CLK /nCLK accepts LVPECL, LVDS, CML and other differential signals. Both V_{SWING} and V_{OH} must meet the V_{PP} and V_{CMR} input requirements. *Figure 1A to Figure 1E* show interface examples for the CLK/nCLK input driven by the most common driver types. The input interfaces suggested here are examples only. If the driver is from another vendor, use their termination recommendation. Please consult with the vendor of the driver component to confirm the driver termination requirements.

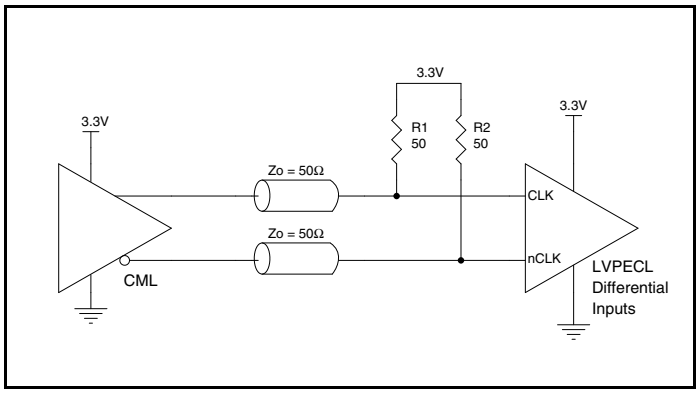


Figure 1A. CLK/nCLK Input Driven by a CML Driver

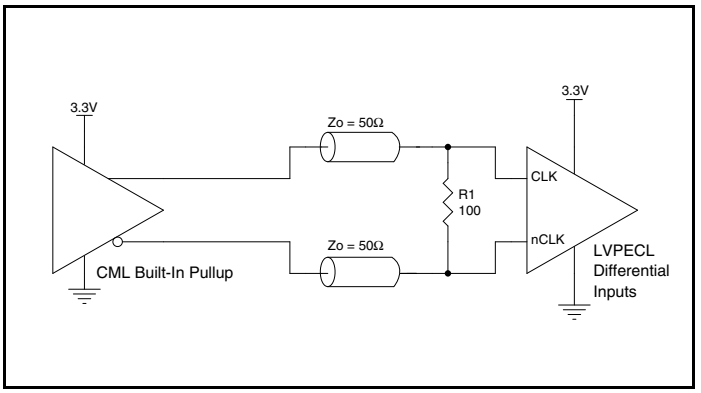


Figure 1D. CLK/nCLK Input Driven by a Built-In Pullup CML Driver

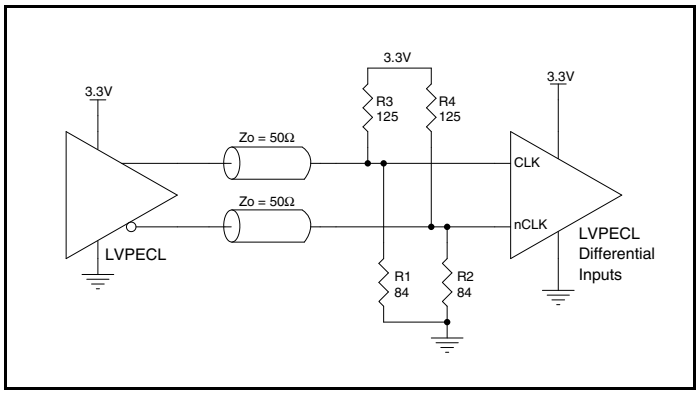


Figure 1B. CLK/nCLK Input Driven by a 3.3V LVPECL Driver

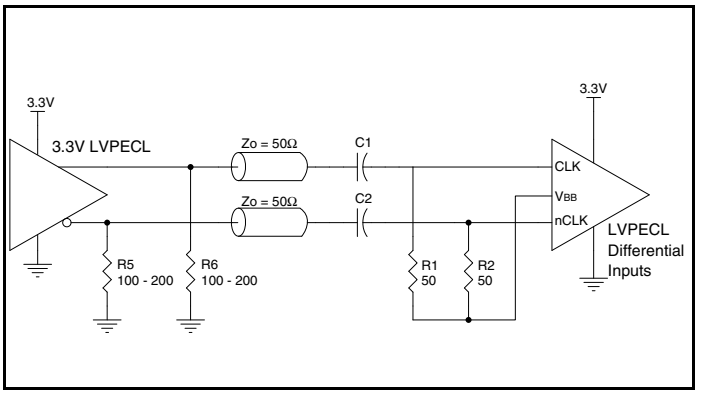


Figure 1E. CLK/nCLK Input Driven by a 3.3V LVPECL Driver with AC Couple

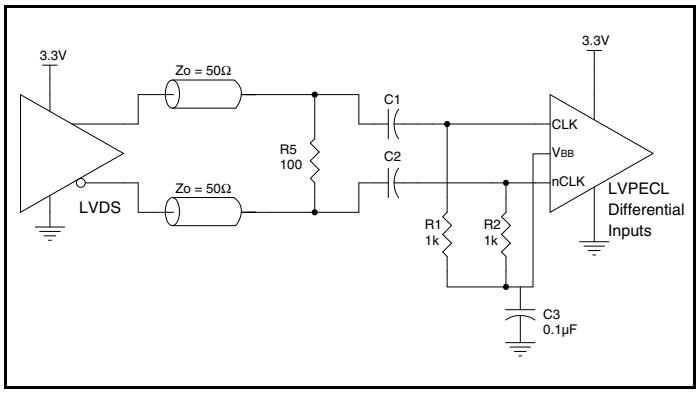


Figure 1C. CLK/nCLK Input Driven by a 3.3V LVDS Driver

2.5V LVPECL Clock Input Interface

The CLK /nCLK accepts LVPECL, LVDS, CML and other differential signals. Both V_{SWING} and V_{OH} must meet the V_{PP} and V_{CMR} input requirements. *Figure 2A to Figure 2E* show interface examples for the CLK/nCLK input driven by the most common driver types. The input interfaces suggested here are examples only. If the driver is from another vendor, use their termination recommendation. Please consult with the vendor of the driver component to confirm the driver termination requirements.

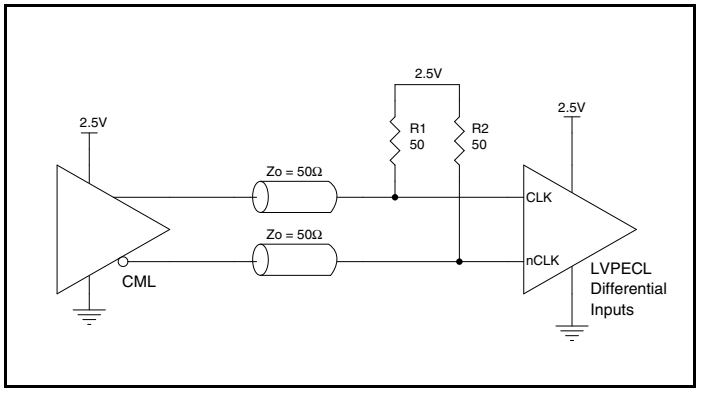


Figure 2A. CLK/nCLK Input Driven by a CML Driver

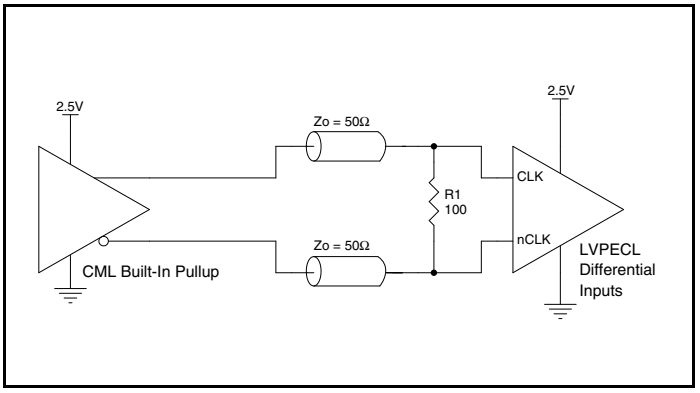


Figure 2D. CLK/nCLK Input Driven by a Built-In Pullup CML Driver

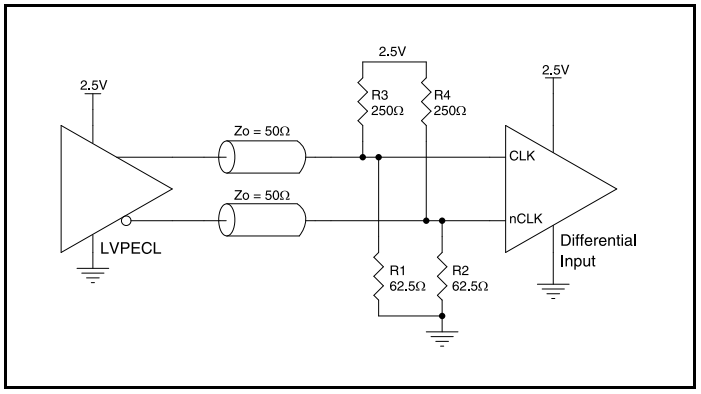


Figure 2B. CLK/nCLK Input Driven by a 2.5V LVPECL Driver

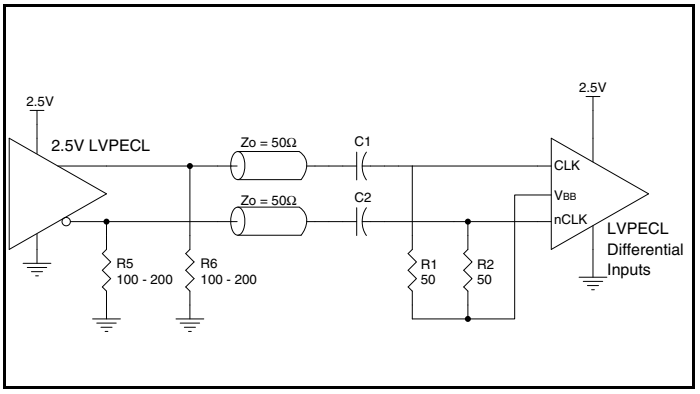


Figure 2E. CLK/nCLK Input Driven by a 2.5V LVPECL Driver with AC Couple

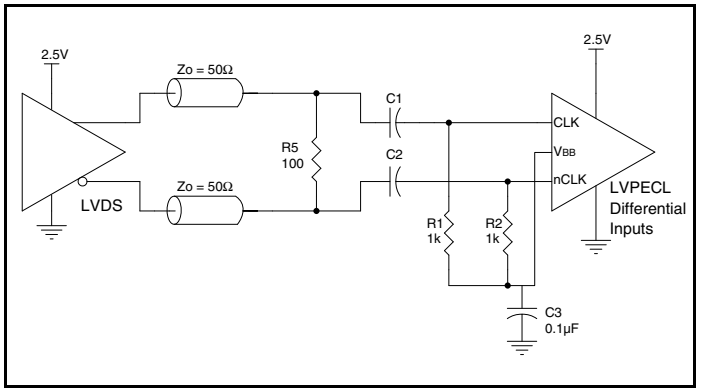


Figure 2C. CLK/nCLK Input Driven by a 2.5V LVDS Driver

Wiring the Differential Input to Accept Single-ended LVPECL Levels

Figure 3 shows an example of the differential input that can be wired to accept single-ended LVPECL levels. The reference voltage level V_{BB} generated from the device is connected to the negative input. The C1 capacitor should be located as close as possible to the input pin.

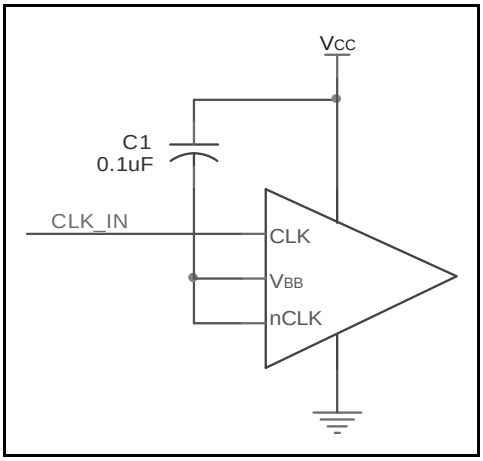


Figure 3. Single-Ended LVPECL Signal Driving Differential Input

Recommendations for Unused Input and Output Pins

Inputs:

LVCMOS Control Pins

All control pins have internal pull-ups; additional resistance is not required but can be added for additional protection. A 1kΩ resistor can be used.

Outputs:

LVPECL Outputs

The unused LVPECL output pair can be left floating. We recommend that there is no trace attached. Both sides of the differential output pair should either be left floating or terminated.

LVCMOS Outputs

The unused LVCMOS output can be left floating. There should be no trace attached.

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VFQFPN EPAD Thermal Release Path

In order to maximize both the removal of heat from the package and the electrical performance, a land pattern must be incorporated on the Printed Circuit Board (PCB) within the footprint of the package corresponding to the exposed metal pad or exposed heat slug on the package, as shown in *Figure 4.* The solderable area on the PCB, as defined by the solder mask, should be at least the same size/shape as the exposed pad/slug area on the package to maximize the thermal/electrical performance. Sufficient clearance should be designed on the PCB between the outer edges of the land pattern and the inner edges of pad pattern for the leads to avoid any shorts.

While the land pattern on the PCB provides a means of heat transfer and electrical grounding from the package to the board through a solder joint, thermal vias are necessary to effectively conduct from the surface of the PCB to the ground plane(s). The land pattern must be connected to ground through these vias. The vias act as “heat pipes”. The number of vias (i.e. “heat pipes”) are application specific and dependent upon the package power dissipation as well as electrical conductivity requirements. Thus, thermal and electrical analysis and/or testing are recommended to determine the minimum number needed. Maximum thermal and electrical performance is achieved when an array of vias is incorporated in the land pattern. It is recommended to use as many vias connected to ground as possible. It is also recommended that the via diameter should be 12 to 13mils (0.30 to 0.33mm) with 1oz copper via barrel plating. This is desirable to avoid any solder wicking inside the via during the soldering process which may result in voids in solder between the exposed pad/slug and the thermal land. Precautions should be taken to eliminate any solder voids between the exposed heat slug and the land pattern. Note: These recommendations are to be used as a guideline only. For further information, please refer to the Application Note on the Surface Mount Assembly of Amkor’s Thermally/ Electrically Enhance Lead frame Base Package, Amkor Technology.

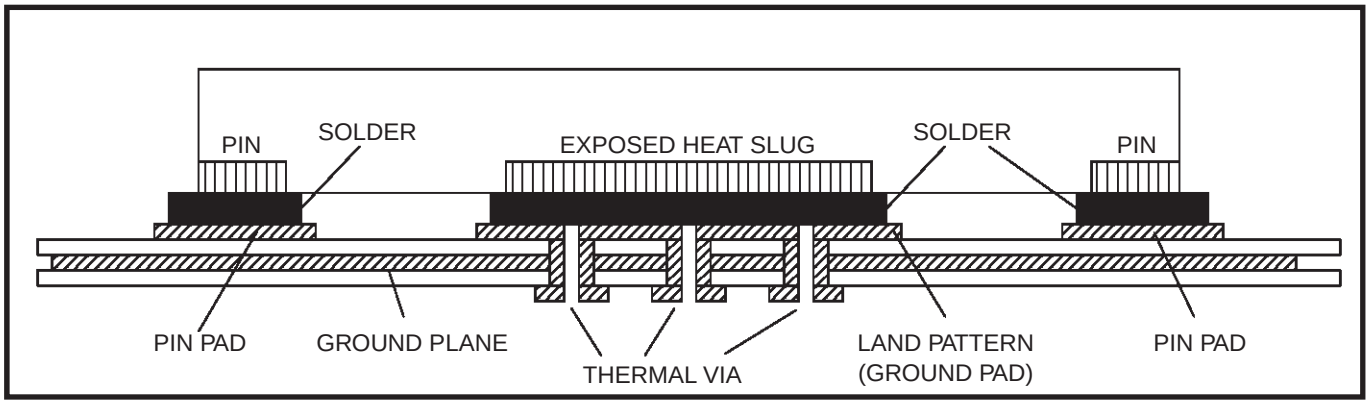


Figure 4. P.C. Assembly for Exposed Pad Thermal Release Path – Side View (drawing not to scale)

Termination for 3.3V LVPECL Outputs

The clock layout topology shown below is a typical termination for LVPECL outputs. The two different layouts mentioned are recommended only as guidelines.

The differential outputs are low impedance follower outputs that generate ECL/LVPECL compatible outputs. Therefore, terminating resistors (DC current path to ground) or current sources must be used for functionality. These outputs are designed to drive 50Ω transmission lines. Matched impedance techniques should be used to maximize operating frequency and minimize signal distortion. *Figure 5A and* Figure 5B show two different layouts which are recommended only as guidelines. Other suitable clock layouts may exist and it would be recommended that the board designers simulate to guarantee compatibility across all printed circuit and clock component process variations.

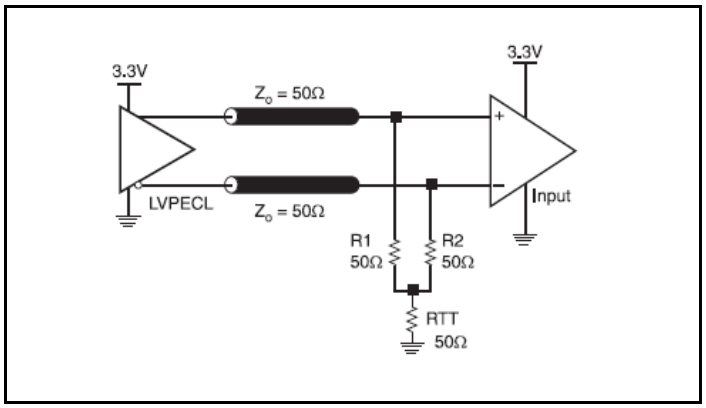


Figure 5A. 3.3V LVPECL Output Termination

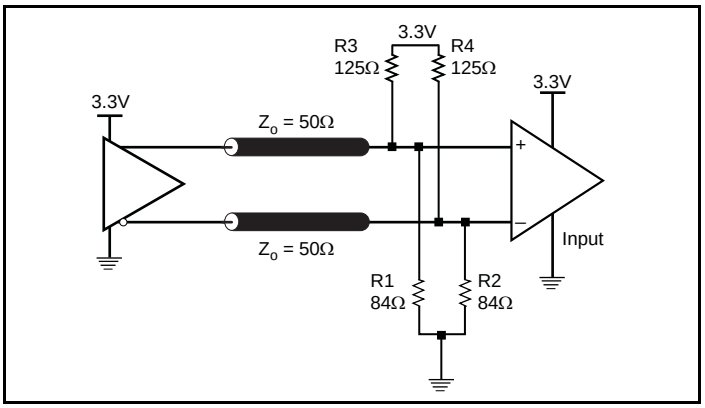


Figure 5B. 3.3V LVPECL Output Termination

Termination for 2.5V LVPECL Outputs

Figure 6A and Figure 6B show examples of termination for 2.5V LVPECL driver. These terminations are equivalent to terminating 50Ω to V_{CCO} – 2V. For V_{CCO} = 2.5V, the V_{CCO} – 2V is very close to ground level. The R3 in Figure 6B can be eliminated and the termination is shown in *Figure 6C*.

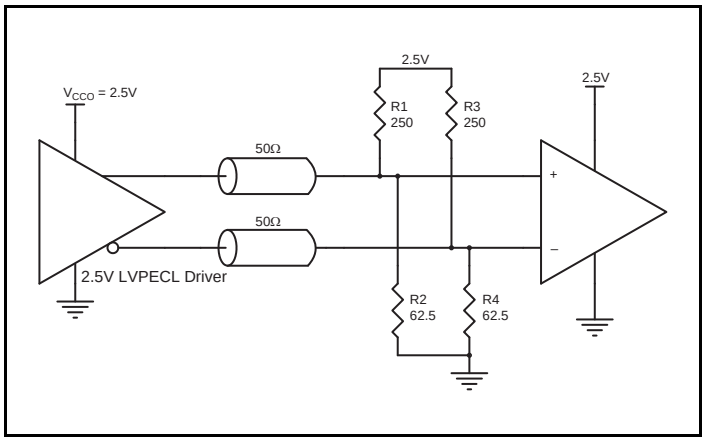


Figure 6A. 2.5V LVPECL Driver Termination Example

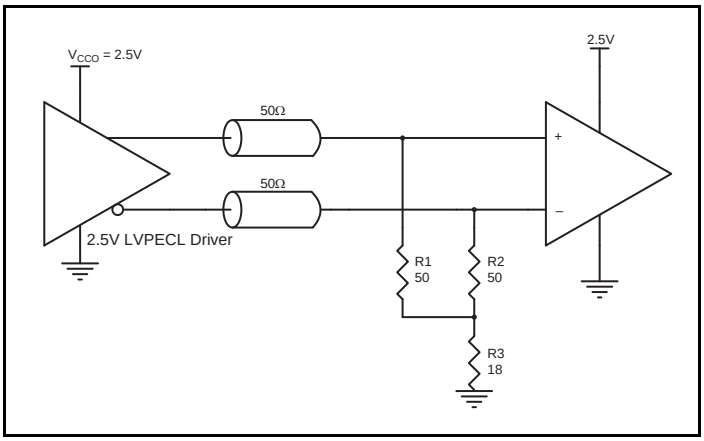


Figure 6C. 2.5V LVPECL Driver Termination Example

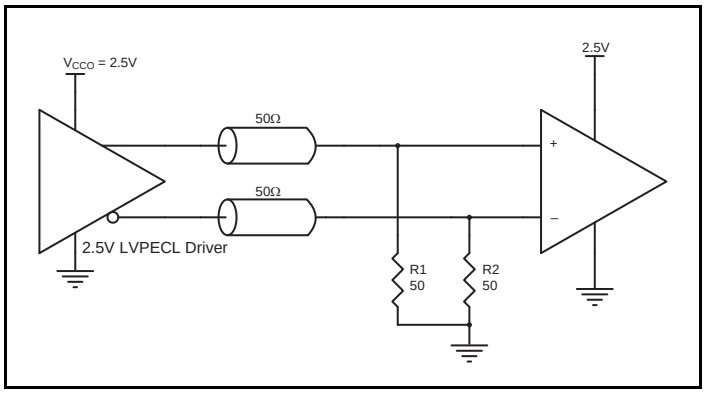


Figure 6B. 2.5V LVPECL Driver Termination Example

Power Considerations

This section provides information on power dissipation and junction temperature for the 8T73S1802.
Equations and example calculations are also provided.

1. Power Dissipation.

The total power dissipation for the 8T73S1802 is the sum of the core power plus the power dissipated due to the load.

Output Load:
LVPECL output load is 50Ω to (V_{CCO_QA} – 2V)
LVCMOS output load is 10pF

Frequency:
LVPECL is 800MHz
LVCMOS is 200MHz

The following is the power dissipation for V_{CC} = 3.3V + 5% = 3.465V, which gives worst case results.

The maximum current at 85°C is as follows:

I_{EE_MAX} = 109mA

- Power$_{_MAX}$ = V_{CCx_MAX} * I_{EE_MAX} = 3.465V * 109mA = **377.685mW**

2. Junction Temperature.

Junction temperature, Tj, is the temperature at the junction of the bond wire and bond pad, and directly affects the reliability of the device. The maximum recommended junction temperature is 125°C. Limiting the internal transistor junction temperature, Tj, to 125°C ensures that the bond wire and bond pad temperature remains below 125°C.

The equation for Tj is as follows: Tj = θ_{JA} * Pd_total + T_A

Tj = Junction Temperature

θ_{JA} = Junction-to-Ambient Thermal Resistance

Pd_total = Total Device Power Dissipation (example calculation is in section 1 above)

T_A = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance θ_{JA} must be used. Assuming no air flow and a multi-layer board, the appropriate value is 74.7°C/W per Table 6 below.

Therefore, Tj for an ambient temperature of 85°C with all outputs switching is:

85°C + 0.378W * 74.7°C/W = 113.2°C. This is below the limit of 125°C.

This calculation is only an example. Tj will obviously vary depending on the number of loaded outputs, supply voltage, air flow and the type of board (multi-layer).

Table 6. Thermal Resistance θ_{JA} for 16-Lead VFQFPN, Forced Convection

θ_{JA} vs. Air Flow			
Meters per Second	**0**	**1**	**2.5**
Multi-Layer PCB, JEDEC Standard Test Boards	74.7°C/W	65.3°C/W	58.5°C/W

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Reliability Information

Table 7. θ_{JA} vs. Air Flow Table for a 16-Lead VFQFPN

θ_{JA} vs. Air Flow			
Meters per Second	**0**	**1**	**2.5**
Multi-Layer PCB, JEDEC Standard Test Boards	74.7°C/W	65.3°C/W	58.5°C/W

Transistor Count

The transistor count for 8T73S1802 is: 1,255

Package Outline Drawings

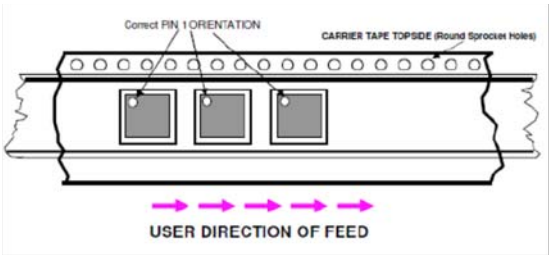
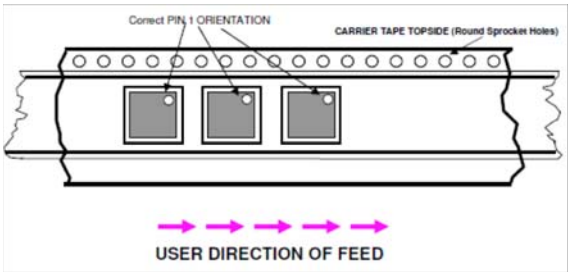
The package outline drawings are located at the end of this document. The package information is the most current data available and is subject to change without notice or revision of this document.

Order Information

Table 8. Ordering Information

Part/Order Number	Marking	Package	Shipping Packaging	Temperature
8T73S1802NLGI	1802I	RoHS 6/6 16 VFQFPN	Tube	-40°C to +85°C
8T73S1802NLGI8	1802I	RoHS 6/6 16 VFQFPN Quadrant 1 (EIA-481-C)	Tape & Reel, Pin 1 Orientation: EIA-481-C	-40°C to +85°C
8T73S1802NLGI/W	1802I	RoHS 6/6 16 VFQFPN Quadrant 2 (EIA-481-D)	Tape & Reel, Pin 1 Orientation: EIA-481-D	-40°C to +85°C

Table 9. Pin 1 Orientation in Tape and Reel Packaging

Part Number Suffix	Pin 1 Orientation	Illustration
8	Quadrant 1 (EIA-481-C)	
/W	Quadrant 2 (EIA-481-D)	

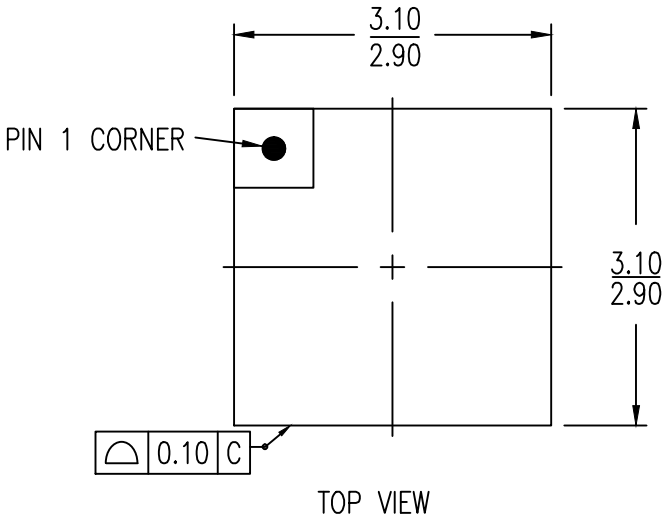
Revision History

Revision Date	Description of Change
January 21, 2018	▪ Updated the package outline drawings; however, no technical changes. ▪ Replaced the package term VFQFN with VFQFPN.
February 7, 2017	▪ Page 24, Table 8 Ordering Information table- corrected first row/ Shipping Packaging column from Tray to Tube.

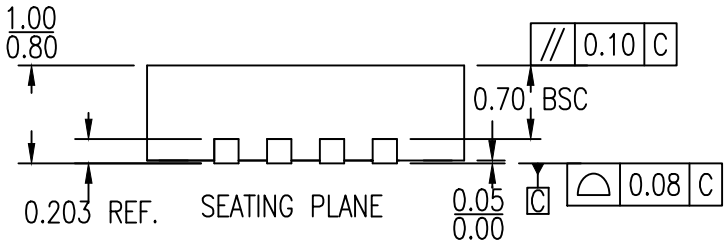
16-VFQFPN Package Outline Drawing

3.0 x 3.0 x 0.9 mm, 0.5mm Pitch, 1.70 x 1.70 mm Epad

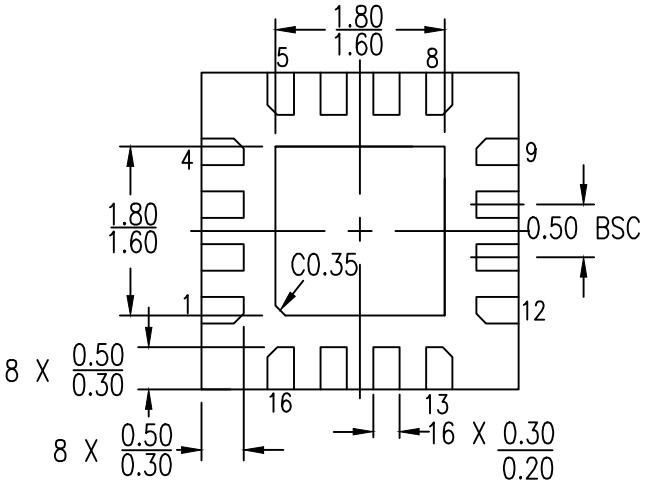
NL/NLG16P2, PSC-4169-02, Rev 05, Page 1



TOP VIEW



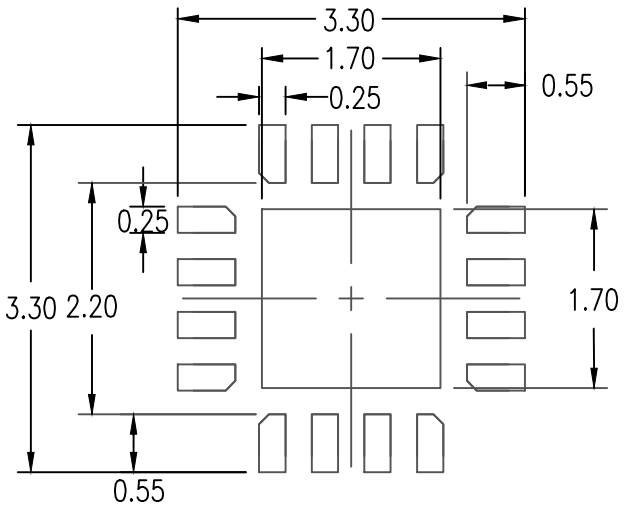
SIDE VIEW



BOTTOM VIEW

NOTES:
1. ALL DIMENSIONS ARE IN mm. ANGLES IN DEGREES

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RECOMMENDED LAND PATTERN DIMENSION

NOTES:
1. ALL DIMENSIONS ARE IN mm. ANGLES IN DEGREES
2. TOP DOWN VIEW–AS VIEWED ON PCB
3. LAND PATTERN RECOMMENDATION IS PER IPC–7351B GENERIC REQUIREMENT FOR SURFACE MOUNT DESIGN AND LAND PATTERN

Package Revision History		
Date Created	Rev No.	Description
Oct 25, 2017	Rev 04	Remove Bookmak at Pdf Format & Update Thickness Tolerance
Jan 18, 2018	Rev 05	Change QFN to VFQFPN

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