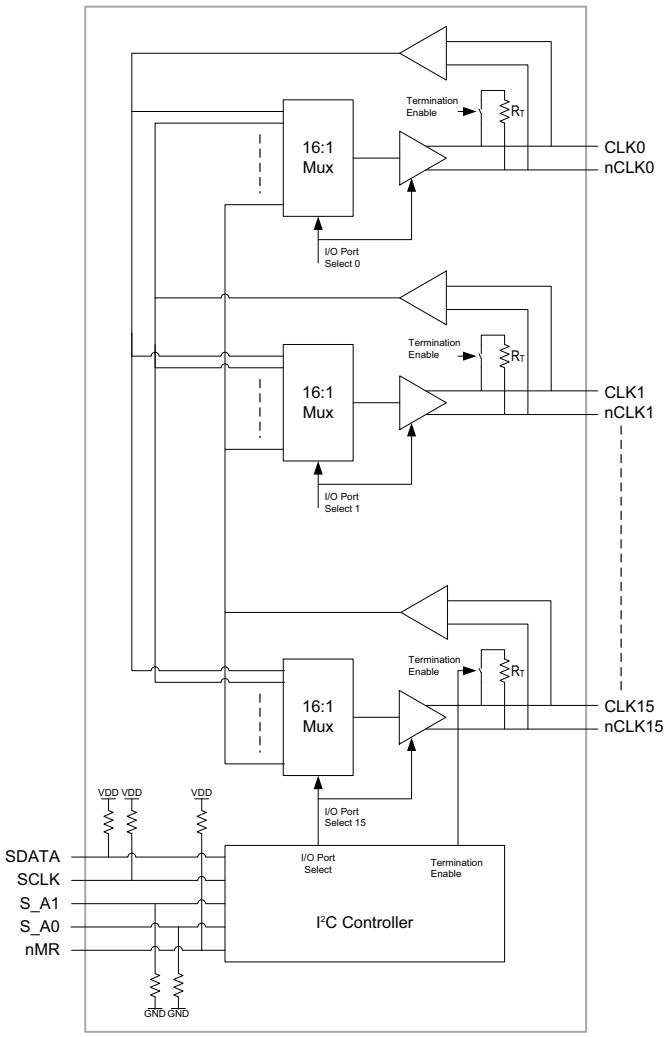
Description

The 8V54816A is a 16-port, bi-directional cross-point clock switch designed for clock distribution in MicroTCA.4 systems. It features 16 bi-directional M-LVDS ports. Each port can be individually set as input or output. Each output port can be connected to any port defined as input. Each port features switchable termination (ON: 100Ω, OFF: High impedance). Output ports can drive up to 19-inch PCB tracks with M-LVDS levels. The device is optimized for very low additive phase noise. Configuration of the device is achieved by I^2C. At startup, a default configuration is set where all ports are in High-Impedance mode with outputs disabled.

Features

- Sixteen bi-directional M-LVDS ports
- Operating frequency: up to 350MHz (maximum)
- Switchable termination resistors
- I^2C support with read-back capabilities up to 400kHz
- PCI Express (2.5Gb/S), Gen 2 (5Gb/s) and Gen 3 (8Gb/s) jitter compliant
- Architecturally compliant with MicroTCA.4 specification
- Output polarity inversion
- Support for 1PPS signals
- Full 3.3V supply voltage
- 12 × 12 mm, 100-lead VFQFN
- Epad size: 6.9 × 6.9 mm
- 0 to +70°C ambient operating temperature
- Lead-free (RoHS 6) packaging

Block Diagram



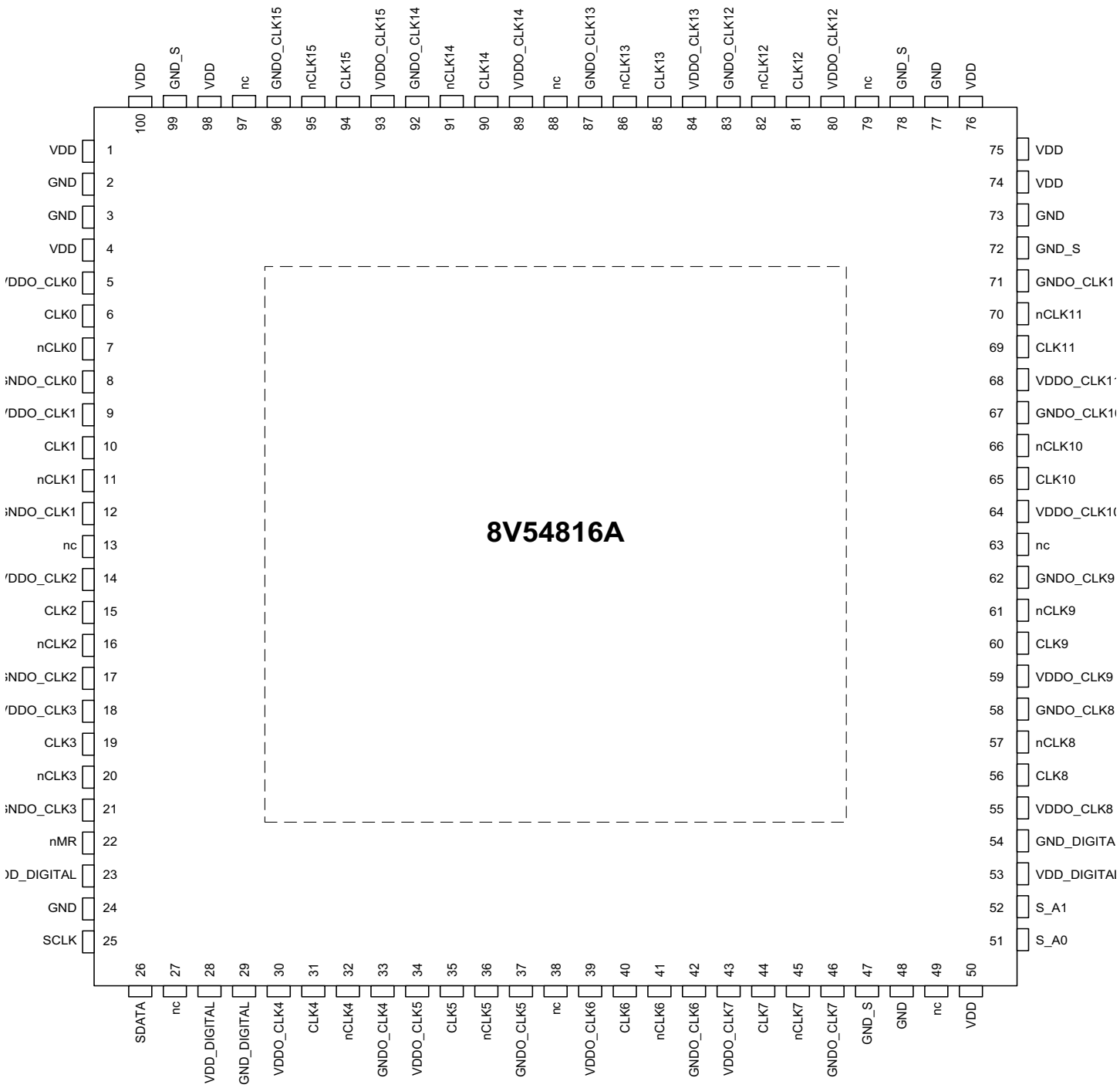
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Pin Assignment

Figure 1. Pin Assignment for 12 × 12 mm, 100-Pin VFQFN Package (Top View)



Pin Descriptions and Characteristics

Table 1. Pin Description Table[a]

Number	Name	Type		Description
1, 4, 50, 74, 75, 76, 98, 100	V_{DD}	Power		Power supply pins.
2, 3, 24, 48, 73, 77	GND	Power		Power supply ground.
5	V_{DDO_CLK0}	Power		Port 0 output power supply.
6, 7	CLK0, nCLK0	I/O		Bi-directional clock port 0.
8	GNDO_CLK0	Power		Port 0 power supply ground.
9	V_{DDO_CLK1}	Power		Port 1 output power supply.
10, 11	CLK1, nCLK1	I/O		Bi-directional clock port 1.
12	GNDO_CLK1	Power		Port 1 power supply ground.
13, 27, 38, 49, 63, 79, 88, 97	nc	Unused		Do not connect.
14	V_{DDO_CLK2}	Power		Port 2 output power supply.
15, 16	CLK2, nCLK2	I/O		Bi-directional clock port 2.
17	GNDO_CLK2	Power		Port 2 power supply ground.
18	V_{DDO_CLK3}	Power		Port 3 output power supply.
19, 20	CLK3, nCLK3	I/O		Bi-directional clock port 3.
21	GNDO_CLK3	Power		Port 3 power supply ground.
22	nMR	Input	Pull-up	Master reset. Active Low. LVCMOS/LVTTL interface levels.
23, 28, 53	$V_{DD_DIGITAL}$	Power		Digital power supply pins.
25	SCLK	Input	Pull-up	I^2C compatible SCLK. This pin has an internal pull-up resistor. LVCMOS/LVTTL interface levels.
26	SDATA	I/O	Pull-up	I^2C compatible SDATA. This pin has an internal pull-up resistor. LVCMOS/LVTTL interface levels.
29, 54	GND_DIGITAL	Power		Digital power supply ground.
30	V_{DDO_CLK4}	Power		Port 4 output power supply.
31, 32	CLK4, nCLK4	I/O		Bi-directional clock port 4.
33	GNDO_CLK4	Power		Port 4 power supply ground.
34	V_{DDO_CLK5}	Power		Port 5 output power supply.
35, 36	CLK5, nCLK5	I/O		Bi-directional clock port 5.
37	GNDO_CLK5	Power		Port 5 power supply ground.
39	V_{DDO_CLK6}	Power		Port 6 output power supply.
40, 41	CLK6, nCLK6	I/O		Bi-directional clock port 6.
42	GNDO_CLK6	Power		Port 6 power supply ground.
43	V_{DDO_CLK7}	Power		Port 7 output power supply.
44, 45	CLK7, nCLK7	I/O		Bi-directional clock port 7.
46	GNDO_CLK7	Power		Port 7 power supply ground.
47, 72, 78, 99	GND_S	Power		Power supply ground.

Table 1. Pin Description Table[a]

Number	Name	Type		Description
51	S_A0	Input	Pull-down	I^2C address bit 0. LVCMOS/LVTTL interface levels.
52	S_A1	Input	Pull-down	I^2C address bit 1. LVCMOS/LVTTL interface levels.
55	V_{DDO_CLK8}	Power		Port 8 output power supply.
56, 57	CLK8, nCLK8	I/O		Bi-directional clock port 8.
58	GNDO_CLK8	Power		Port 8 power supply ground.
59	V_{DDO_CLK9}	Power		Port 9 output power supply.
60, 61	CLK9, nCLK9	I/O		Bi-directional clock port 9.
62	GNDO_CLK9	Power		Port 9 power supply ground.
64	V_{DDO_CLK10}	Power		Port 10 output power supply.
65, 66	CLK10, nCLK10	I/O		Bi-directional clock port 10.
67	GNDO_CLK10	Power		Port 10 power supply ground.
68	V_{DDO_CLK11}	Power		Port 11 output power supply.
69, 70	CLK11, nCLK11	I/O		Bi-directional clock port 11.
71	GNDO_CLK11	Power		Port 11 power supply ground.
80	V_{DDO_CLK12}	Power		Port 12 output power supply.
81, 82	CLK12, nCLK12	I/O		Bi-directional clock port 12.
83	GNDO_CLK12	Power		Port 12 power supply ground.
84	V_{DDO_CLK13}	Power		Port 13 output power supply.
85, 86	CLK13, nCLK13	I/O		Bi-directional clock port 13.
87	GNDO_CLK13	Power		Port 13 power supply ground.
89	V_{DDO_CLK14}	Power		Port 14 output power supply.
90, 91	CLK14, nCLK14	I/O		Bi-directional clock port 14.
92	GNDO_CLK14	Power		Port 14 power supply ground.
93	V_{DDO_CLK15}	Power		Port 15 output power supply.
94, 95	CLK15, nCLK15	I/O		Bi-directional clock port 15.
96	GNDO_CLK15	Power		Port 15 power supply ground.

[a] *Pull-up, Pull-down* refers to internal input resistors. See Table 2, *Pin Characteristics,* for typical values.

Table 2. Pin Characteristics Table

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
C_{IN}	Input Capacitance			4		pF
R_{PULLUP}	Input Pull-up Resistor			51		kΩ
$R_{PULLDOWN}$	Input Pull-down Resistor			51		kΩ
R_T	Output Termination			100		Ω

Serial Interface Configuration Description

The 8V54816A has an I^{2}C-compatible configuration interface to access any of the internal registers (Table 2) for frequency and PLL parameter programming. The 8V54816A acts as a slave device on the I^{2}C bus and has the address 0b**10110**xx, where xx is set by the values on the S_A0 & S_A1 pins (see Table 2 for details). Data bytes (registers) are accessed in sequential order from the lowest to the highest byte (most significant bit first). Only read and write full block transfers are supported. The I2C sequence should consist only of the Device Address and 16 Data bytes. It is recommended to terminate I^{2}C read or write transfer after accessing byte #15.

For full electrical I^{2}C compliance, it is recommended to use external pull-up resistors for SDATA and SCLK. The internal pull-up resistors have a size of 51kΩ typical.

Table 3. I²C Address

1	0	1	1	0	S_A1	S_A0	R/W

Table 4. I²C Register Map

Register	Binary Register Address	Function
0	0x00	Port 0 configuration
1	0x01	Port 1 configuration
2	0x02	Port 2 configuration
3	0x03	Port 3 configuration
4	0x04	Port 4 configuration
5	0x05	Port 5 configuration
6	0x06	Port 6 configuration
7	0x07	Port 7 configuration
8	0x08	Port 8 configuration
9	0x09	Port 9 configuration
10	0x0A	Port 10 configuration
11	0x0B	Port 11 configuration
12	0x0C	Port 12 configuration
13	0x0D	Port 13 configuration
14	0x0E	Port 14 configuration
15	0x0F	Port 15 configuration

Table 5. Port Configuration Bit Allocation Table

Bit	Description	Default	Function
7	Port I/O	0	0 = Port is input 1 = Port is output
6	Termination On/Off	0	0 = Internal termination is off (high-impedance) 1 = Internal termination is on (100Ω)
5	Polarity	0	0 = Inverted 1 = Non-inverted
4	Reserved	0	Reserved
[3:0]	Output Port Signal Source [3:0]	0000	If port is an output (Port I/O = 1): Bit[3:0] specifies the input port that is used as a signal source for this output If port is an input (Port I/O = 0): Bit[3:0] has no meaning

Absolute Maximum Ratings

NOTE: Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics or AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Table 6. Absolute Maximum Ratings Table

Item	Rating
Supply Voltage, V_{DD}	3.63V
Inputs, V_I	-0.5V to V_{DD} + 0.5V
Outputs, I_O Continuous Current Surge Current	 10mA 15mA
Junction Temperature, T_J	125°C
Storage Temperature, T_{STG}	-65°C to 150°C

DC Electrical Characteristics

Table 7. Power Supply DC Characteristics, V_{DD} = $V_{DD_DIGITAL}$ = V_{DDO_X}[a] = 3.3V ± 5%, T_A = 0°C to 70°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{DD}	Power Supply Voltage		3.135	3.3	3.465	V
$V_{DD_DIGITAL}$	Digital Supply Voltage		3.135	3.3	3.465	V
V_{DDO_X}	Output Supply Voltage		3.135	3.3	3.465	V
I_{DD}	Power Supply Current			258	295	mA
$I_{DD_DIGITAL}$	Digital Supply Current			6	7	mA
I_{DDO}[b]	Total Output Supply Current	0 Ports Configured as Outputs		63		mA
		15 Ports Configured as Outputs		258	295	mA
I_{DDO_inc}[b, c]	Output Current Contribution, per output port			13		mA

[a] V_{DDO_X} denotes $V_{DDO_[0:15]}$.

[b] Output ports are terminated internally and externally with 100Ω across CLK and nCLK.

[c] This is the increase in I_{DDO} when the number of output ports is increased by one.

Table 8. LVCMOS/LVTTL DC Characteristics, V_{DD} = $V_{DD_DIGITAL}$ = V_{DDO_X}[a] = 3.3V ± 5%, T_A = 0°C to 70°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
V_{IH}	Input High Voltage	SDATA, SCLK, S_A0, S_A1, nMR		2.2		V_{DD} + 0.3	V
V_{IL}	Input Low Voltage	SDATA, SCLK, S_A0, S_A1, nMR		-0.3		0.8	V
I_{IH}	Input High Current	S_A0, S_A1	V_{DD} = V_{IN} = 3.465V			150	µA
		nMR, SCLK, SDATA	V_{DD} = V_{IN} = 3.465V			5	µA
I_{IL}	Input Low Current	S_A0, S_A1	V_{DD} = 3.465V, V_{IN} = 0V	-5			µA
		nMR, SCLK, SDATA	V_{DD} = 3.465V, V_{IN} = 0V	-150			µA

[a] V_{DDO_X} denotes $V_{DDO_[0:15]}$.

Table 9. Differential Input DC Characteristics, $V_{DD} = V_{DD_DIGITAL} = V_{DDO_X}$[a] = 3.3V ± 5%, T_A = 0°C to 70°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{PP}	Peak-to-Peak Voltage[b]		0.15		1.3	V
V_{CMR}	Common Mode Range[b, c]		0.5		V_{DD} – 1	V

[a] V_{DDO_X} denotes $V_{DDO_[0:15]}$.

[b] Common mode input is defined at the differential crosspoint.

[c] V_{IL} must not be less than -0.3V. V_{IH} must be less than V_{DD}.

Table 10. M-LVDS DC Characteristics, $V_{DD} = V_{DD_DIGITAL} = V_{DDO_X}$[a] = 3.3V ± 5%, T_A = 0°C to 70°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{OD}	Differential Output Voltage		400		850	mV
ΔV_{OD}	V_{OD} Magnitude Change				50	mV
V_{OS}	Offset Voltage		0.3		2.1	V
ΔV_{OS}	V_{OS} Magnitude Change				50	mV

[a] V_{DDO_X} denotes $V_{DDO_[0:15]}$.

AC Electrical Characteristics

Table 11. AC Characteristics, $V_{DD} = V_{DD_DIGITAL} = V_{DDO_X}$[a] = 3.3V ± 5%, T_A = 0°C to 70°C[b]

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
f_{OUT}	Output Frequency				350	MHz
t_{PD}	Propagation Delay[c]		2	3.8	6	ns
*t*sl(o)	Output Slew Rate	Measured at the Differential Waveform, ±200mV from the Center	0.9	2.4	4	V/ns
V_{AC}	AC Swing		400	674	850	mV
*t*jit	Buffer Additive Phase Jitter, RMS[d]	f_{OUT} = 125MHz, Integration Range 12kHz – 20MHz		0.32	0.5	ps
*t*jit(T_J)	Total Time Domain Jitter[e], [f]	f_{OUT} = 100MHz		60	94	ps
odc	Output Duty Cycle[g]	$f_{IN} \leq$ 200MHz	45	50	55	%
t_R / t_F	Output Rise/Fall Time	20% to 80%		380	741	ps

[a] V_{DDO_X} denotes $V_{DDO_[0:15]}$.

[b] Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfpm. The device will meet specifications after thermal equilibrium has been reached under these conditions.

[c] Measured from the differential input crosspoint to the differential output crosspoint.

[d] SMA-100 as the signal source. With CLK6 as the input port and CLK4 as the output port for measurement (internal termination enabled.)

[e] Total Jitter (Peak-to-Peak) = [RMS Multiplier * Random Jitter (R^J)] + Deterministic Jitter (D^J), RMS Multiplier = 14.26 (BER = 1E-12).

[f] Device configured for 15 inputs and 1 output. Input source is a Renesas clock generator 8714008D driven by an SRS CG635 signal generator.

[g] Input Duty Cycle must be 50%.

Table 12. Serial Rapid IO Switch Jitter Specification, V_{DD} = $V_{DD_DIGITAL}$ = V_{DDO_X}[a] = 3.3V ± 5%, T_A = 0°C to 70°C[b]

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
J_{CLK_REF}	Total Phase Jitter, RMS[c], [d], [e], [f]	f_{OUT} = 156.25MHz		0.247	0.5	ps

[a] V_{DDO_X} denotes $V_{DDO_[0:15]}$.

[b] Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfpm. The device will meet specifications after thermal equilibrium has been reached under these conditions.

[c] Evaluation band with sRIO mask applied: 10Hz - 40MHz.

[d] Total phase jitter includes random and deterministic jitter.

[e] Jitter data is measured using a Rohde & Schwarz SMA 100 input source and an Agilent E5052 phase noise analyzer.

[f] CLK0 is the input port. All other CLKs are programmed as output ports.

Table 13. PCI Express Jitter Specifications, V_{DD} = $V_{DD_DIGITAL}$ = V_{DDO_X}[a] = 3.3V ± 5%, T_A = 0°C to 70°C[b]

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	PCIe Industry Specification	Units
t_j (PCIe Gen 1)	Phase Jitter, Peak-to-Peak[c], [d], [e], [f]	f = 100MHz, Evaluation Band: 0Hz - Nyquist (clock frequency/2)		11.2	20	86	ps
$t_{REFCLK_HF_RMS}$ (PCIe Gen 2)	Phase Jitter, RMS[c, d, f, [g]	f = 100MHz, High Band: 1.5MHz - Nyquist (clock frequency/2)		1	2	3.1	ps
$t_{REFCLK_LF_RMS}$ (PCIe Gen 2)	Phase Jitter, RMS[c, d, f, g	f = 100MHz Low Band: 10kHz - 1.5MHz		0.06	0.5	3.0	ps
t_{REFCLK_RMS} (PCIe Gen 3)	Phase Jitter, RMS[c, d, f, [h]	f = 100MHz Evaluation Band: 0Hz - Nyquist (clock frequency/2)		0.15	0.5	0.8	ps

[a] V_{DDO_X} denotes $V_{DDO_[0:15]}$.

[b] Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfpm. The device will meet specifications after thermal equilibrium has been reached under these conditions. For additional information, refer to the PCI Express Application Note *section* in the datasheet.

[c] This parameter is guaranteed by characterization. Not tested in production.

[d] Parameter measured with an SRS CG635 as the input source.

[e] Peak-to-Peak jitter after applying system transfer function for the Common Clock Architecture. Maximum limit for PCI Express Gen 1 is 86ps peak-to-peak for a sample size of 10^6 clock periods.

[f] CLK0 is the input port. All other CLKs are programmed as output ports. CLK4 and CLK12 are output ports for measurement.

[g] RMS jitter after applying the two evaluation bands to the two transfer functions defined in the Common Clock Architecture and reporting the worst case results for each evaluation band. Maximum limit for PCI Express Generation 2 is 3.1ps RMS for $t_{REFCLK_HF_RMS}$ (High Band) and 3.0ps RMS for $t_{REFCLK_LF_RMS}$ (Low Band).

[h] RMS jitter after applying system transfer function for the common clock architecture. This specification is based on the *PCI Express Base Specification Revision 0.7, October 2009* and is subject to change pending the final release version of the specification.

Parameter Measurement Information

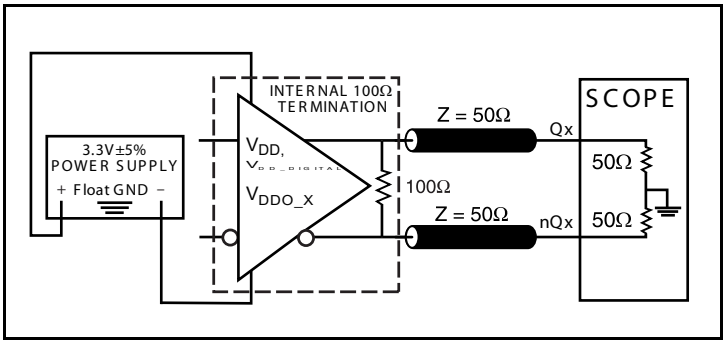


Figure 2. 3.3V M-LVDS Output Load AC Test Circuit

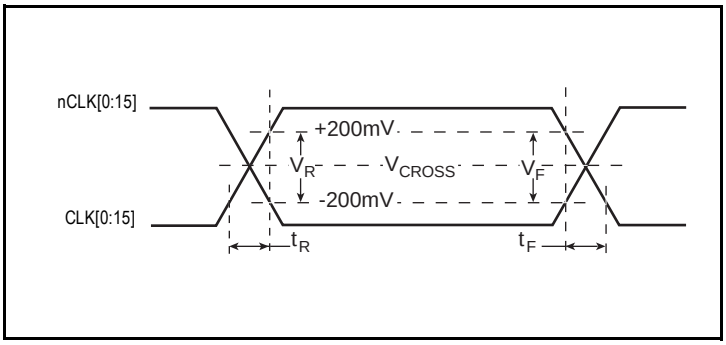


Figure 3. Output Slew Rate

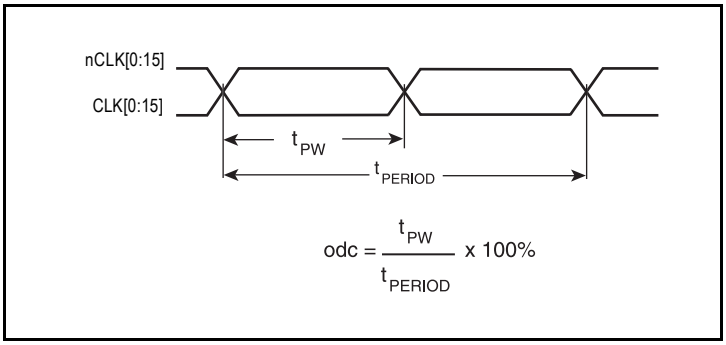


Figure 4. Output Duty Cycle/Pulse Width/tPeriod

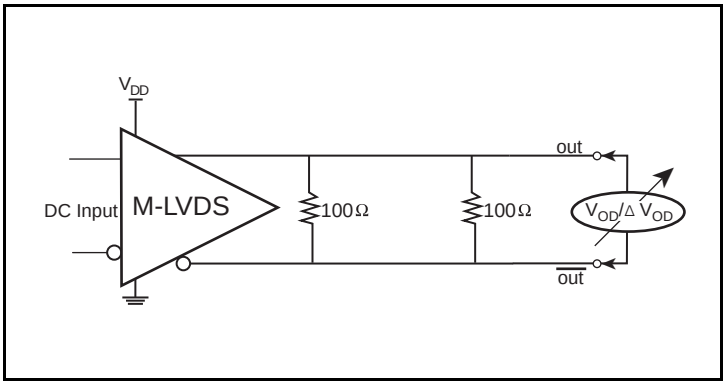


Figure 5. M-LVDS Differential Output Voltage Setup

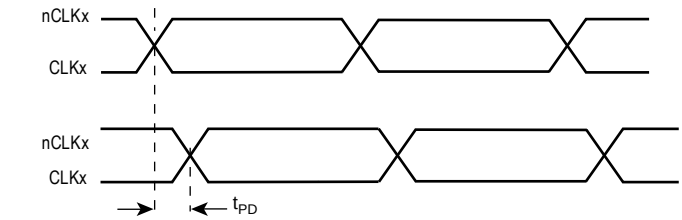


Figure 6. Propagation Delay

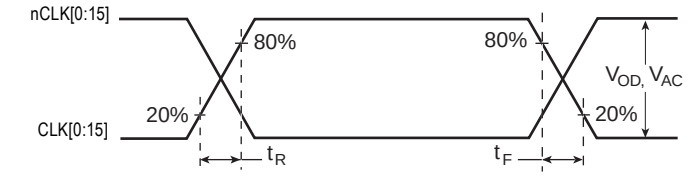


Figure 7. Output Rise/Fall Time, V_{OD}, V_{AC}

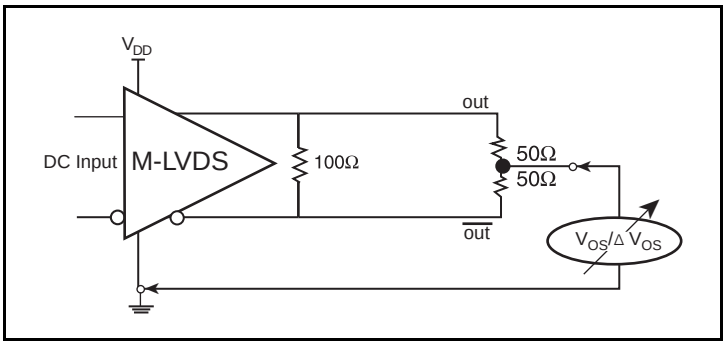


Figure 8. M-LVDS Offset Voltage Setup

Applications Information

The 8V54816A is a clock crosspoint switch designed to distribute clocks in MicroTCA.4 systems. The 8V54816A distributes clock coming from an AMC Timing card to other AMC cards.

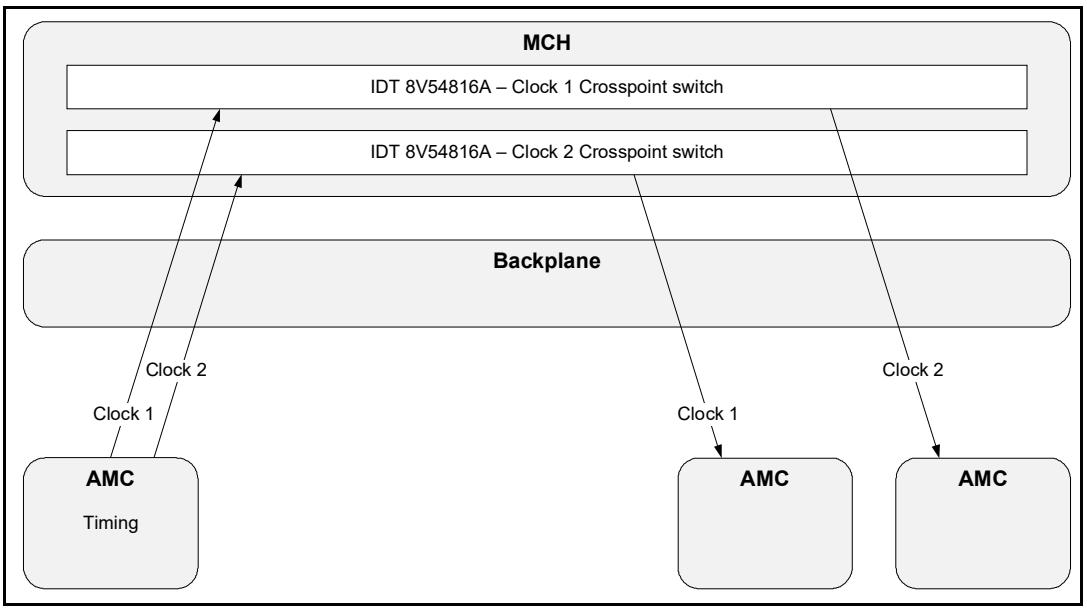


Figure 9. 8V54816A Application Drawing

Port Termination

All 16 bi-directional clock ports (CLKx, nCLKx) feature a switchable, 100Ω termination. External 100Ω termination may be used. In that case the internal termination shall be turned off.

Internal termination is turned on by setting Bit 6 of the configuration register corresponding to the considered I/O port to 1.

Case 1: Terminations present on the backplane

In case 100Ω terminations are present on the backplane, terminations of the corresponding ports of the 8V54816A shall be turned off. No termination shall be present on AMC cards. *See Figure 10.*

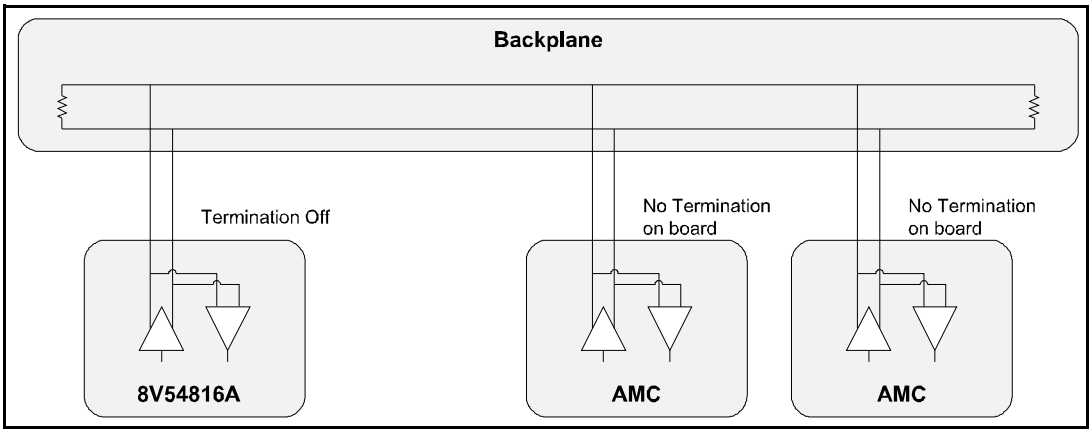


Figure 10. Termination on Blackplane

Case 2: No terminations present on the backplane

When no terminations are present on the backplane, two terminations shall be turned on in order to realize a multi-point M-LVDS configuration. See Figure 11.

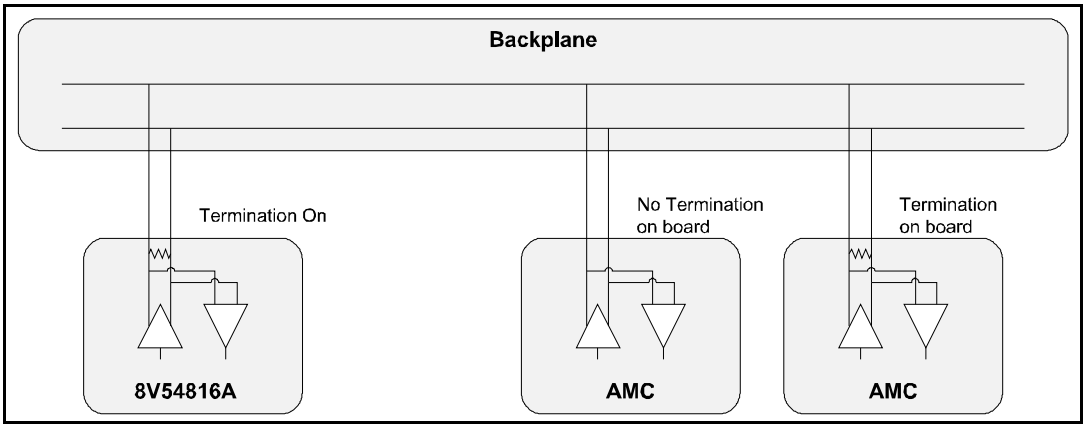


Figure 11. No Termination on Backplane

Polarity Inversion

Polarity inversion of each port can be used in order to facilitate board layout. Polarity inversion is enabled by setting Bit 5 of the register corresponding to the considered port to 1. If polarity inversion is enabled,

- CLKx becomes the negative input or output of port x
- nCLKx becomes the positive input or output of port x

Port Configuration Example

Any CLKx, nCLKx port of the 8V54816A can be configured as either input or output. Let's consider the following examples:

- 100MHz clock source routed to port 2
- 100MHz clock to be distributed to ports 3, 5, 8 and 9
- 25MHz clock source routed to port 6
- 25MHz clock to be distributed to ports 1, 11 and 12
- Ports 13, 14 and 15 are not used

Table 14. Port Configuration Table

I^2C Register	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Bit Description	**Port I/O**	**Termination On/Off**	**Polarity**	**Reserved**	**Output Port Select [3]**	**Output Port Select[2]**	**Output Port Select [1]**	**Output Port Select [0]**
0	n/a	According to Backplane		Reserved	n/a			
1	1				0	1	1	0
2	0				X	X	X	X
3	1				0	0	1	0
4	n/a				n/a			
5	1				0	0	1	0
6	0				X	X	X	X
7	n/a				n/a			
8	1				0	0	1	0
9	1				0	0	1	0
10	n/a				n/a			
11	1				0	1	1	0
12	1				0	1	1	0
13	0	0	X		X	X	X	X
14	0	0	X		X	X	X	X
15	0	0	X		X	X	X	X

Recommendations for Unused Input Pins

Inputs:

LVCMOS Control Pins

All control pins have internal pull-up or pull-down resistors; additional resistance is not required but can be added for additional protection. A 1kΩ resistor can be used.

Bi-directional CLK/nCLK Ports

The bi-directional input/output ports do not feature pull-up or pull-down resistors. Ports configured as inputs and left floating might toggle due to noise. This noise can propagate into the device's core and increase the noise of the valid clocks due to internal crosstalk.

Therefore, it is recommended to connect external biasing resistors to unused ports:

- Resistor to GND on the CLKx pin (e.g. 1 kΩ to GND)
- Resistor network to GND and V_{DD} on the nCLKx pin (e.g. 1.2kΩ to GND and 2.7 kΩ to V_{DD}) and configure the port as an input. The internal termination can be disabled or enabled.

If using external biasing resistors to unused ports cannot be realized, the recommended operation of an unused port is to:

- leave the port unconnected
- configure the port as an output
- disable the internal termination (to save power)
- select a valid clock input as clock source for this port.

Differential Clock Input Interface

The CLKx /nCLKx accepts LVDS and other differential signals. Both differential signals must meet the V_{PP} and V_{CMR} input requirements. *Figure 12* shows an interface example for the CLKx/nCLKx input driven by the most common driver types. The input interfaces suggested here are examples only. Please consult with the vendor of the driver component to confirm the driver termination requirements. If the driver is from another vendor, use their termination recommendation.

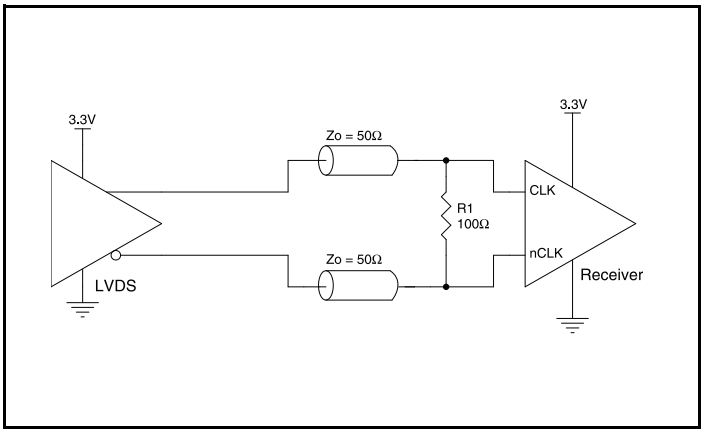


Figure 12. CLK/nCLK Input Driven by a 3.3V LVDS Driver

3.3V M-LVDS Driver Termination

A general M-LVDS interface is shown in Figure 13 In a 100Ω differential transmission line environment, M-LVDS drivers require a matched load termination of 100Ω across near the receiver input. For a multiple M-LVDS outputs buffer, if only partial outputs are used, it is recommended to terminate the unused outputs.

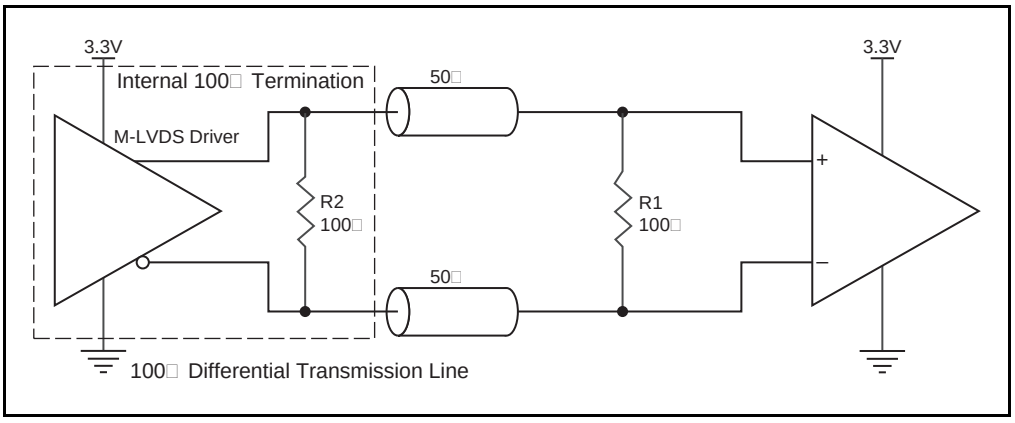


Figure 13. Typical M-LVDS Driver Termination

VFQFN EPAD Thermal Release Path

In order to maximize both the removal of heat from the package and the electrical performance, a land pattern must be incorporated on the Printed Circuit Board (PCB) within the footprint of the package corresponding to the exposed metal pad or exposed heat slug on the package, as shown in *Figure 14*. The solderable area on the PCB, as defined by the solder mask, should be at least the same size/shape as the exposed pad/slug area on the package to maximize the thermal/electrical performance. Sufficient clearance should be designed on the PCB between the outer edges of the land pattern and the inner edges of pad pattern for the leads to avoid any shorts.

While the land pattern on the PCB provides a means of heat transfer and electrical grounding from the package to the board through a solder joint, thermal vias are necessary to effectively conduct from the surface of the PCB to the ground plane(s). The land pattern must be connected to ground through these vias. The vias act as “heat pipes”. The number of vias (i.e. “heat pipes”) are application specific and dependent upon the package power dissipation as well as electrical conductivity requirements. Thus, thermal and electrical analysis and/or testing are recommended to determine the minimum number needed. Maximum thermal and electrical performance is achieved when an array of vias is incorporated in the land pattern. It is recommended to use as many vias connected to ground as possible. It is also recommended that the via diameter should be 12 to 13mils (0.30 to 0.33mm) with 1oz copper via barrel plating. This is desirable to avoid any solder wicking inside the via during the soldering process which may result in voids in solder between the exposed pad/slug and the thermal land. Precautions should be taken to eliminate any solder voids between the exposed heat slug and the land pattern. Note: These recommendations are to be used as a guideline only. For further information, please refer to the Application Note on the Surface Mount Assembly of Amkor’s Thermally/ Electrically Enhance Leadframe Base Package, Amkor Technology.

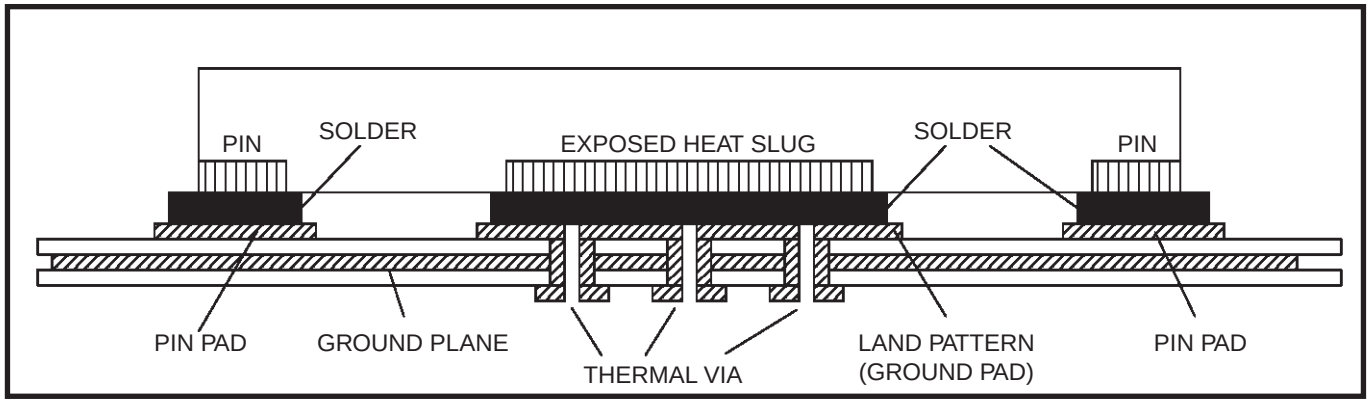


Figure 14. P.C. Assembly for Exposed Pad Thermal Release Path – Side View (drawing not to scale)

PCI Express Application Note

PCI Express jitter analysis methodology models the system response to reference clock jitter. The block diagram below shows the most frequently used *Common Clock Architecture* in which a copy of the reference clock is provided to both ends of the PCI Express Link.

In the jitter analysis, the transmit (Tx) and receive (Rx) serdes PLLs are modeled as well as the phase interpolator in the receiver. These transfer functions are called H1, H2, and H3 respectively. The overall system transfer function at the receiver is:

$$Ht(s) = H3(s) \times [H1(s) - H2(s)]$$

The jitter spectrum seen by the receiver is the result of applying this system transfer function to the clock spectrum X(s) and is:

$$Y(s) = X(s) \times H3(s) \times [H1(s) - H2(s)]$$

In order to generate time domain jitter numbers, an inverse Fourier Transform is performed on X(s)*H3(s) * [H1(s) - H2(s)].

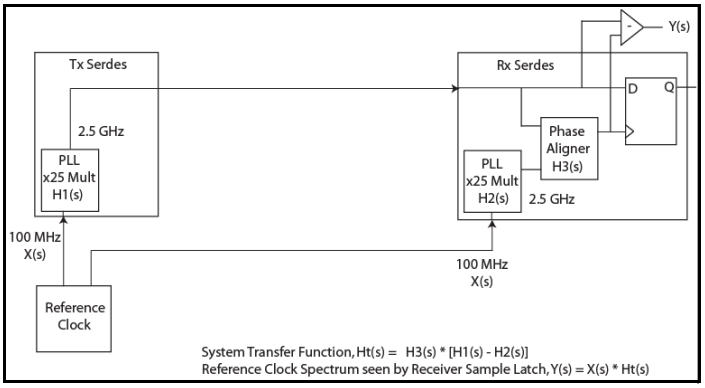


Figure 15. PCI Express Common Clock Architecture

For **PCI Express Gen 1**, one transfer function is defined and the evaluation is performed over the entire spectrum: DC to Nyquist (e.g for a 100MHz reference clock: 0Hz – 50MHz) and the jitter result is reported in peak-peak.

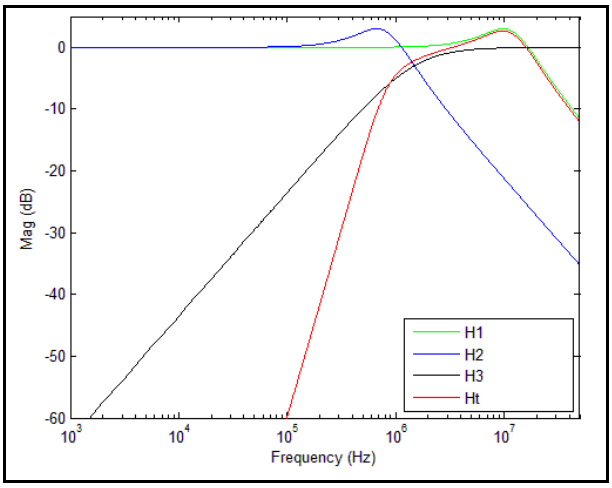


Figure 16. PCIe Gen 1 Magnitude of Transfer Function

For **PCI Express Gen 2**, two transfer functions are defined with 2 evaluation ranges and the final jitter number is reported in rms. The two evaluation ranges for PCI Express Gen 2 are 10kHz – 1.5MHz (Low Band) and 1.5MHz – Nyquist (High Band). The plots show the individual transfer functions as well as the overall transfer function Ht.

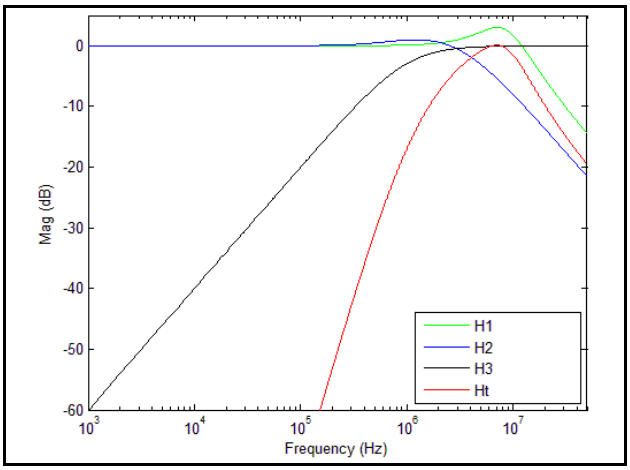


Figure 17. PCIe Gen 2A Magnitude of Transfer Function

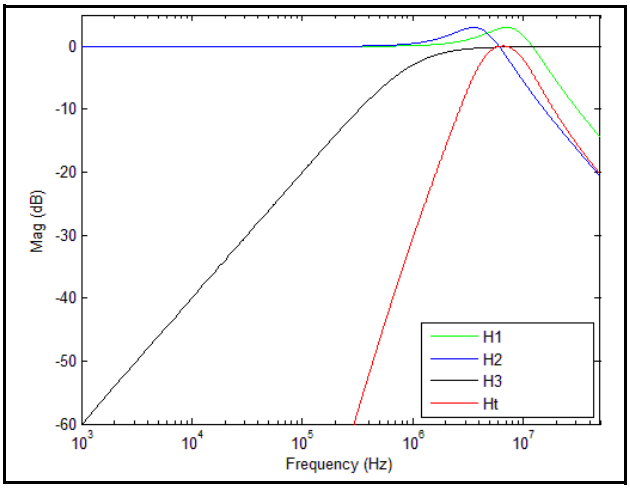


Figure 18. PCIe Gen 2B Magnitude of Transfer Function

For **PCI Express Gen 3**, one transfer function is defined and the evaluation is performed over the entire spectrum. The transfer function parameters are different from Gen 1 and the jitter result is reported in RMS.

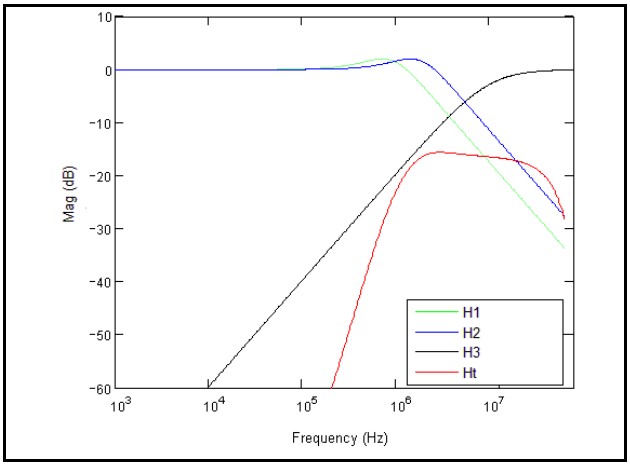


Figure 19. PCIe Gen 3 Magnitude of Transfer Function

For a more thorough overview of PCI Express jitter analysis methodology, please refer to Renesas Application Note *PCI Express Reference Clock Requirements.*

Power Considerations

This section provides information on power dissipation and junction temperature for the 8V54816A.
Equations and example calculations are also provided.

The following calculation is for maximum current at 70°C.

1. Power Dissipation.

The total power dissipation for the 8V54816A is the sum of the core power plus the power dissipated due to into the load.
The following is the power dissipation for V_{DD}= 3.3V + 5% = 3.465V, which gives worst case results.

The maximum current at 70°C is as below:
I_{DD_MAX} = 293mA
$I_{DD_DIGITAL_MAX}$ = 7mA

I_{DDO_MAX} = 295mA

- Power $(core)_{MAX} = V_{DD_MAX} * (I_{DD_MAX} + I_{DD_DIGITAL_MAX})$= 3.465V * (293mA + 7mA) = **1040mW**
- Power $(outputs)_{MAX} = V_{DDO_MAX} * I_{DDO_MAX}$ = 3.465V * 295mA = **1022.2mW**

Total Power$_{MAX}$ = 1040mW + 1022.2mW = **2062.2mW**

2. Junction Temperature.

Junction temperature, Tj, is the temperature at the junction of the bond wire and bond pad directly affects the reliability of the device. The maximum recommended junction temperature is 125°C. Limiting the internal transistor junction temperature, Tj, to 125°C ensures that the bond wire and bond pad temperature remains below 125°C.

The equation for Tj is as follows: $Tj = \theta_{JA} * Pd_total + T_A$

Tj = Junction Temperature

θ_{JA} = Junction-to-Ambient Thermal Resistance

Pd_total = Total Device Power Dissipation (example calculation is in section 1 above)

T_A = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance θ_{JA} must be used. Assuming no air flow and a multi-layer board, the appropriate value is 22.9°C/W per Table 15 below.

Therefore, Tj for an ambient temperature of 70°C with all outputs switching is:

70°C + 2.06W * 22.9°C/W = 117.2°C. This is below the limit of 125°C.

This calculation is only an example. Tj will obviously vary depending on the number of loaded outputs, supply voltage, air flow and the type of board (multi-layer).

Table 15. Thermal Resistance θ_{JA} for 100-Lead VFQFN, Forced Convection

θ_{JA} by Velocity			
Meters per Second	**0**	**1**	**2.5**
Multi-Layer PCB, JEDEC Standard	22.9°C/W	18.0°C/W	16.0°C/W

Reliability Information

Table 16. θ_{JA} vs. Air Flow Table for a 100-Lead VFQFN Package

θ_{JA} vs. Air Flow			
Meters per Second	**0**	**1**	**2.5**
Multi-Layer PCB, JEDEC Standard Test Boards	22.9°C/W	18.0°C/W	16.0°C/W

Transistor Count

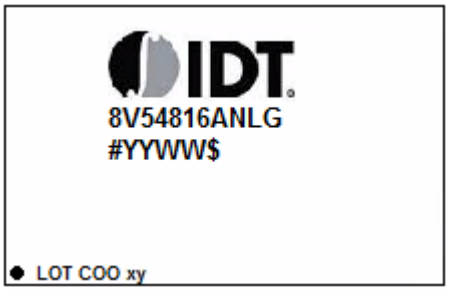
The transistor count for 8V54816A is: 195,306

Package Outline Drawings

The package outline drawings are appended at the end of this document and are accessible from the link below. The package information is the most current data available.

www.idt.com/us/en/document/psc/nlnlg100p1-package-outline-120-x-120-mm-body-sawn-epad-690-x-690-mm-qfn

Marking Diagram



- Line 2: part number.
- Line 3 indicates the following:
  - "#" denotes stepping.
  - "YY" is the last two digits of the year; "WW" is the work week number when the part was assembled.
  - "$" denotes the mark code.
- "LOT" denotes the lot number
- "COO" denotes country of origin.

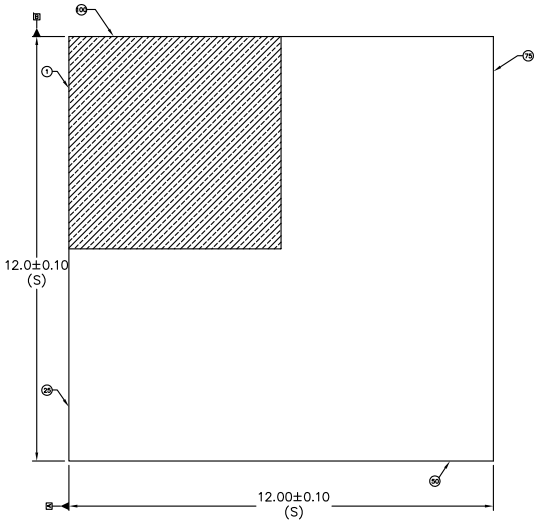
Ordering Information

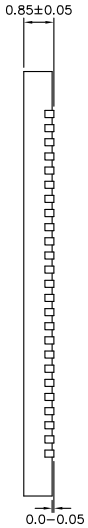
Part/Order Number	Package	Shipping Packaging	Temperature
8V54816ANLG	100-lead VFQFN, Lead-Free	Tray	0°C to 70°C
8V54816ANLG8	100-lead VFQFN, Lead-Free	Tape and Reel	0°C to 70°C

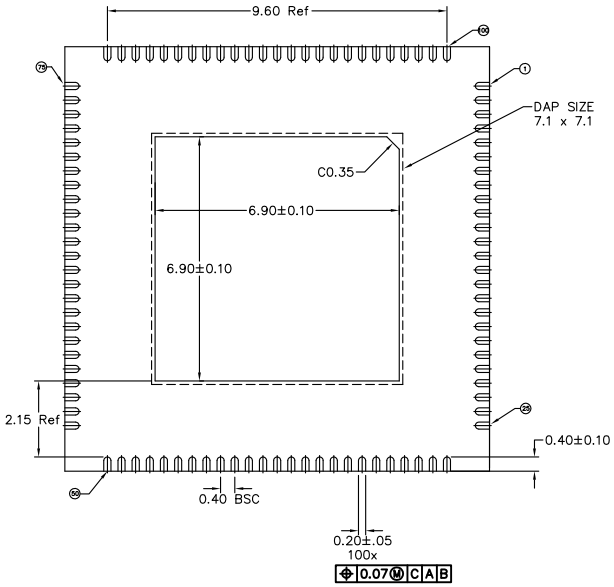
Revision History

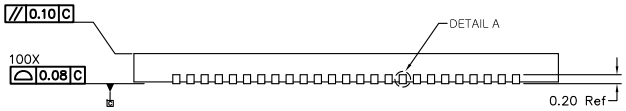
Revision Date	Description of Change
October 27, 2020	▪ Updated the text in section Serial Interface Configuration Description. ▪ Updated Package Outline Drawings section. ▪ Reformatted document to Renesas.
December 18, 2015	Initial release.

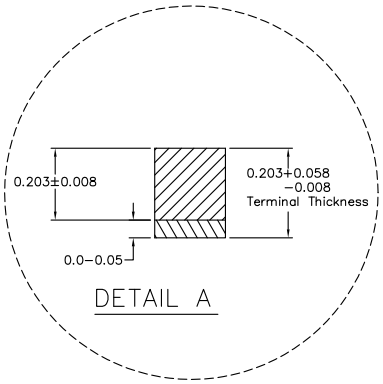
REVISIONS			
REV	DESCRIPTION	DATE	APPROVED
00	INITIAL RELEASE	01/11/16	JH











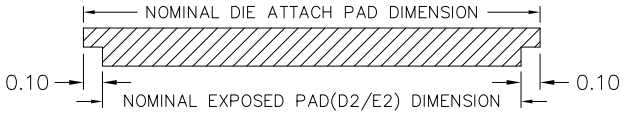
1. ALL DIMENSION ARE IN mm. ANGLES IN DEGREES.
2. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS. COPLANARITY SHALL NOT EXCEED 0.08 mm.
3. WARPAGE SHALL NOT EXCEED 0.10 mm.
4. PACKAGE LENGTH/ PACKAGE WIDTH ARE CONSIDERED AS SPECIAL CHARACTERISTIC. (S)
5. REFER TO JEDEC MO-220.

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APPROVALS	DATE	TITLE	NL/NLG100 PACKAGE OUTLINE 12.0 x 12.0 mm BODY, SAWN EPAD 6.90 x 6.90 mm QFN
DRAWN PSC	01/11/16		
CHECKED			
		SIZE: C	DRAWING No.: PSC–4286–01 REV: 00
		DO NOT SCALE DRAWING	SHEET 1 OF 4

REVISIONS			
REV	DESCRIPTION	DATE	APPROVED
00	INITIAL RELEASE	01/11/16	JH

SYMBOL	DIMENSIONS			NOTE
	MIN.	NOM.	MAX.	
A	0.80	0.85	0.90	
A1	0.00	0.01	0.05	10
A2	0.60	0.65	0.70	
A3		0.20 REF.		
D		12.00 BSC		
E		12.00 BSC		
e		0.40 BSC		
N		100		3
Nd		25		3
Ne		25		3
L	0.30	0.40	0.50	
b	0.15	0.20	0.25	4,12
D2	6.80	6.90	7.00	
E2	6.80	6.90	7.00	

GENERAL ; NOMINAL EXPOSED PAD(D2/E2) DIMENSION = NOMINAL DIE ATTACH PAD DIMENSION−0.20



<DIE ATTACH PAD X−SECTION VIEW>

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EPAD 6.90 x 6.90 mm QFN

SIZE	DRAWING No.	REV
C	PSC−4286−01	00

DO NOT SCALE DRAWING

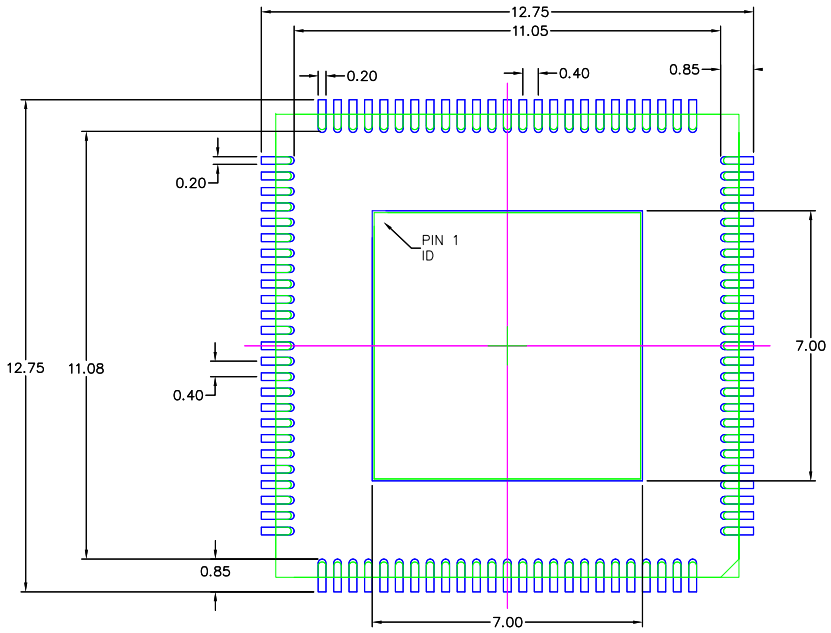
REVISIONS			
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NOTES:

1. DIE THICKNESS ALLOWABLE IS 0.305mm MAXIMUM(.012 INCHES MAXIMUM)
2. DIMENSIONING & TOLERANCES CONFORM TO ASME Y14.5M. – 1994.
3. N IS THE NUMBER OF TERMINALS.
   Nd IS THE NUMBER OF TERMINALS IN X–DIRECTION &
   Ne IS THE NUMBER OF TERMINALS IN Y–DIRECTION.
4. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30mm FROM TERMINAL TIP.
5. THE PIN #1 IDENTIFIER MUST BE EXISTED ON THE TOP SURFACE OF THE PACKAGE BY USING INDENTATION MARK OR OTHER FEATURE OF PACKAGE BODY.
6. EXACT SHAPE AND SIZE OF THIS FEATURE IS OPTIONAL.
7. ALL DIMENSIONS ARE IN MILLIMETERS.
8. THE SHAPE SHOWN ON FOUR CORNERS ARE NOT ACTUAL I/O.
9. BILATERAL COPLANARITY ZONE APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.
10. APPLIED ONLY FOR TERMINALS.
11. Q AND R APPLIES ONLY FOR STRAGHT TIEBAR SHAPES.
12. FOR 0.40mm LEAD PITCH, THE LEAD POSITION TOLERANCE MUST BE 0.07mm AT THE ACTUAL MEAN VALUE OF BODY SIZE.
13. MOLD FLASH OR PLATING COVERAGE ON THE RING PAD AREA SHALL BE ALLOWABLE

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		SIZE C	DRAWING No. PSC–4286–01 REV 00
		DO NOT SCALE DRAWING	SHEET 3 OF 4

REVISIONS			
REV	DESCRIPTION	DATE	APPROVED
00	INITIAL RELEASE	01/11/16	JH



RECOMMENDED LAND PATTERN DIMENSION

NOTES:
1. ALL DIMENSIONS ARE IN mm. ANGLES IN DEGREES.
2. TOP DOWN VIEW. AS VIEWED ON PCB.
3. COMPONENT OUTLINE SHOWS FOR REFERENCE IN GREEN.
4. LAND PATTERN IN BLUE. NSMD PATTERN ASSUMED.
5. LAND PATTERN RECOMMENDATION PER IPC-7351B GENERIC REQUIREMENT FOR SURFACE MOUNT DESIGN AND LAND PATTERN.

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APPROVALS DATE DRAWN RAC 01/11/16 CHECKED	TITLE NL/NLG100 PACKAGE OUTLINE 12.0 x 12.0 mm BODY, SAWN EPAD 6.90 x 6.90 mm QFN
	SIZE C | DRAWING No. PSC-4286-01 | REV 00
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(Rev.1.0 Mar 2020)

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