# PCIe Gen 2 main Clock for Intel-based Servers

### Recommended Application:

PCIe Gen 2 & FBD compliant CK410B/CK410B+ clock for Intel-based servers

### Output Features:

- 5 - 0.7V current-mode differential CPU pairs
- 4 - 0.7V current-mode differential SRC pair
- 4 - PCI (33MHz)
- 3 - PCICLK_F, (33MHz) free-running
- 1 - 48MHz
- 2 - REF, 14.318MHz

### Key Specifications:

- CPU cycle-cycle jitter: < 50ps
- SRC cycle-cycle jitter: < 125ps
- PCI cycle-cycle jitter: < 500ps
- CPU output skew: < 100ps
- SRC output skew: < 250ps
- ± 300ppm frequency accuracy on all outputs except 48MHz
- ± 100ppm frequency accuracy on 48MHz

### Features/Benefits:

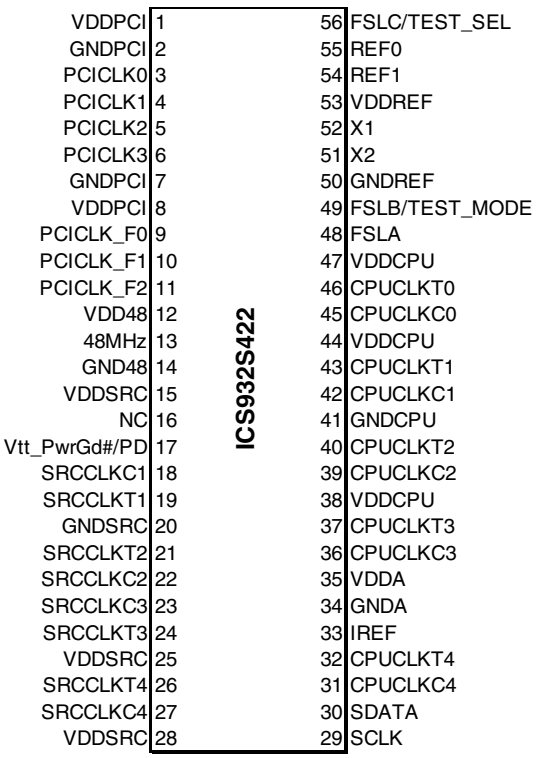
- Supports spread spectrum modulation, 0 to -0.5% down spread
- Uses external 14.318MHz crystal and external load capacitors for low ppm synthesis error
- CPU clocks independent of SRC/PCI clocks
- D2/D3 SMBus address
- Compliant with PCIe Gen II phase noise specifications

### Functionality

| FSLC[1] | FSLB[1] | FSLA[2] | CPU MHz | SRC MHz | PCI MHz | REF MHz | USB MHz |
|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 266.67 | 100.00 | 33.33 | 14.318 | 48.000 |
| 0 | 0 | 1 | 133.33 | 100.00 | 33.33 | 14.318 | 48.000 |
| 0 | 1 | 0 | 200.00 | 100.00 | 33.33 | 14.318 | 48.000 |
| 0 | 1 | 1 | 166.67 | 100.00 | 33.33 | 14.318 | 48.000 |
| 1 | 0 | 0 | 333.33 | 100.00 | 33.33 | 14.318 | 48.000 |
| 1 | 0 | 1 | 100.00 | 100.00 | 33.33 | 14.318 | 48.000 |
| 1 | 1 | 0 | 400.00 | 100.00 | 33.33 | 14.318 | 48.000 |
| 1 | 1 | 1 | Reserved | | | | |

1. FSLB and FSLC are three-level inputs. Please see VIL_FS and VIH_FS specifications in the Input/Supply/Common Output Parameters Table for correct values. Also refer to the Test Clarification Table.
2.FSLA is a low-threshold input. Please see the VIL_FS and VIH_FS specifications in the Input/Supply/Common Output Parameters Table for correct values.

### Pin Configuration




**56-pin SSOP & TSSOP**

1412A—12/10/07

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## Pin Description

| Pin # | PIN NAME | PIN TYPE | DESCRIPTION |
|---|---|---|---|
| 1 | VDDPCI | PWR | Power supply for PCI clocks, nominal 3.3V |
| 2 | GNDPCI | PWR | Ground pin for the PCI outputs |
| 3 | PCICLK0 | OUT | PCI clock output. |
| 4 | PCICLK1 | OUT | PCI clock output. |
| 5 | PCICLK2 | OUT | PCI clock output. |
| 6 | PCICLK3 | OUT | PCI clock output. |
| 7 | GNDPCI | PWR | Ground pin for the PCI outputs |
| 8 | VDDPCI | PWR | Power supply for PCI clocks, nominal 3.3V |
| 9 | PCICLK_F0 | OUT | Free running PCI clock not affected by PCI_STOP# . |
| 10 | PCICLK_F1 | OUT | Free running PCI clock not affected by PCI_STOP# . |
| 11 | PCICLK_F2 | OUT | Free running PCI clock not affected by PCI_STOP# . |
| 12 | VDD48 | PWR | Power pin for the 48MHz output.3.3V |
| 13 | 48MHz | OUT | 48MHz clock output. |
| 14 | GND48 | PWR | Ground pin for the 48MHz outputs |
| 15 | VDDSRC | PWR | Supply for SRC clocks, 3.3V nominal |
| 16 | NC | N/A | No Connection. |
| 17 | Vtt_PwrGd#/PD | IN | Vtt_PwrGd# is an active low input used to determine when latched inputs are ready to be sampled. PD is an asynchronous active high input pin used to put the device into a low power state. The internal clocks, PLLs and the crystal oscillator are stopped. |
| 18 | SRCCLKC1 | OUT | Complement clock of differential push-pull SRC clock pair. |
| 19 | SRCCLKT1 | OUT | True clock of differential SRC clock pair. |
| 20 | GNDSRC | PWR | Ground pin for the SRC outputs |
| 21 | SRCCLKT2 | OUT | True clock of differential SRC clock pair. |
| 22 | SRCCLKC2 | OUT | Complement clock of differential SRC clock pair. |
| 23 | SRCCLKC3 | OUT | Complement clock of differential SRC clock pair. |
| 24 | SRCCLKT3 | OUT | True clock of differential SRC clock pair. |
| 25 | VDDSRC | PWR | Supply for SRC clocks, 3.3V nominal |
| 26 | SRCCLKT4 | OUT | True clock of differential SRC clock pair. |
| 27 | SRCCLKC4 | OUT | Complement clock of differential SRC clock pair. |
| 28 | VDDSRC | PWR | Supply for SRC clocks, 3.3V nominal |



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## Pin Description (Continued)

| Pin # | PIN NAME | Type | Pin Description |
|---|---|---|---|
| 29 | SCLK | IN | Clock pin of SMBus circuitry, 5V tolerant. |
| 30 | SDATA | I/O | Data pin for SMBus circuitry, 3.3V tolerant. |
| 31 | CPUCLKC4 | OUT | Complementary clock of differential pair CPU outputs. These are current mode outputs. External resistors are required for voltage bias. |
| 32 | CPUCLKT4 | OUT | True clock of differential pair CPU outputs. These are current mode outputs. External resistors are required for voltage bias. |
| 33 | IREF | OUT | This pin establishes the reference current for the differential current-mode output pairs. This pin requires a fixed precision resistor tied to ground in order to establish the appropriate current. 475 ohms is the standard value. |
| 34 | GNDA | PWR | Ground pin for the PLL core. |
| 35 | VDDA | PWR | 3.3V power for the PLL core. |
| 36 | CPUCLKC3 | OUT | Complementary clock of differential pair CPU outputs. These are current mode outputs. External resistors are required for voltage bias. |
| 37 | CPUCLKT3 | OUT | True clock of differential pair CPU outputs. These are current mode outputs. External resistors are required for voltage bias. |
| 38 | VDDCPU | PWR | Supply for CPU clocks, 3.3V nominal |
| 39 | CPUCLKC2 | OUT | Complementary clock of differential pair CPU outputs. These are current mode outputs. External resistors are required for voltage bias. |
| 40 | CPUCLKT2 | OUT | True clock of differential pair CPU outputs. These are current mode outputs. External resistors are required for voltage bias. |
| 41 | GNDCPU | PWR | Ground pin for the CPU outputs |
| 42 | CPUCLKC1 | OUT | Complementary clock of differential pair CPU outputs. These are current mode outputs. External resistors are required for voltage bias. |
| 43 | CPUCLKT1 | OUT | True clock of differential pair CPU outputs. These are current mode outputs. External resistors are required for voltage bias. |
| 44 | VDDCPU | PWR | Supply for CPU clocks, 3.3V nominal |
| 45 | CPUCLKC0 | OUT | Complementary clock of differential pair CPU outputs. These are current mode outputs. External resistors are required for voltage bias. |
| 46 | CPUCLKT0 | OUT | True clock of differential pair CPU outputs. These are current mode outputs. External resistors are required for voltage bias. |
| 47 | VDDCPU | PWR | Supply for CPU clocks, 3.3V nominal |
| 48 | FSLA | IN | 3.3V tolerant input for CPU frequency selection. Refer to input electrical characteristics for Vil_FS and Vih_FS values. |
| 49 | FSLB/TEST_MODE | IN | 3.3V tolerant input for CPU frequency selection. Refer to input electrical characteristics for Vil_FS and Vih_FS values. TEST_MODE is a real time input to select between Hi-Z and REF/N divider mode while in test mode. Refer to Test Clarification Table. |
| 50 | GNDREF | PWR | Ground pin for the REF outputs. |
| 51 | X2 | OUT | Crystal output, Nominally 14.318MHz |
| 52 | X1 | IN | Crystal input, Nominally 14.318MHz. |
| 53 | VDDREF | PWR | Ref, XTAL power supply, nominal 3.3V |
| 54 | REF1 | OUT | 14.318 MHz reference clock. |
| 55 | REF0 | OUT | 14.318 MHz reference clock. |
| 56 | FSLC/TEST_SEL | IN | 3.3V tolerant input for CPU frequency selection. Low voltage threshold inputs, see input electrical characteristics for Vil_FS and Vih_FS values. TEST_Sel: 3-level latched input to enable test mode. Refer to Test Clarification Table |

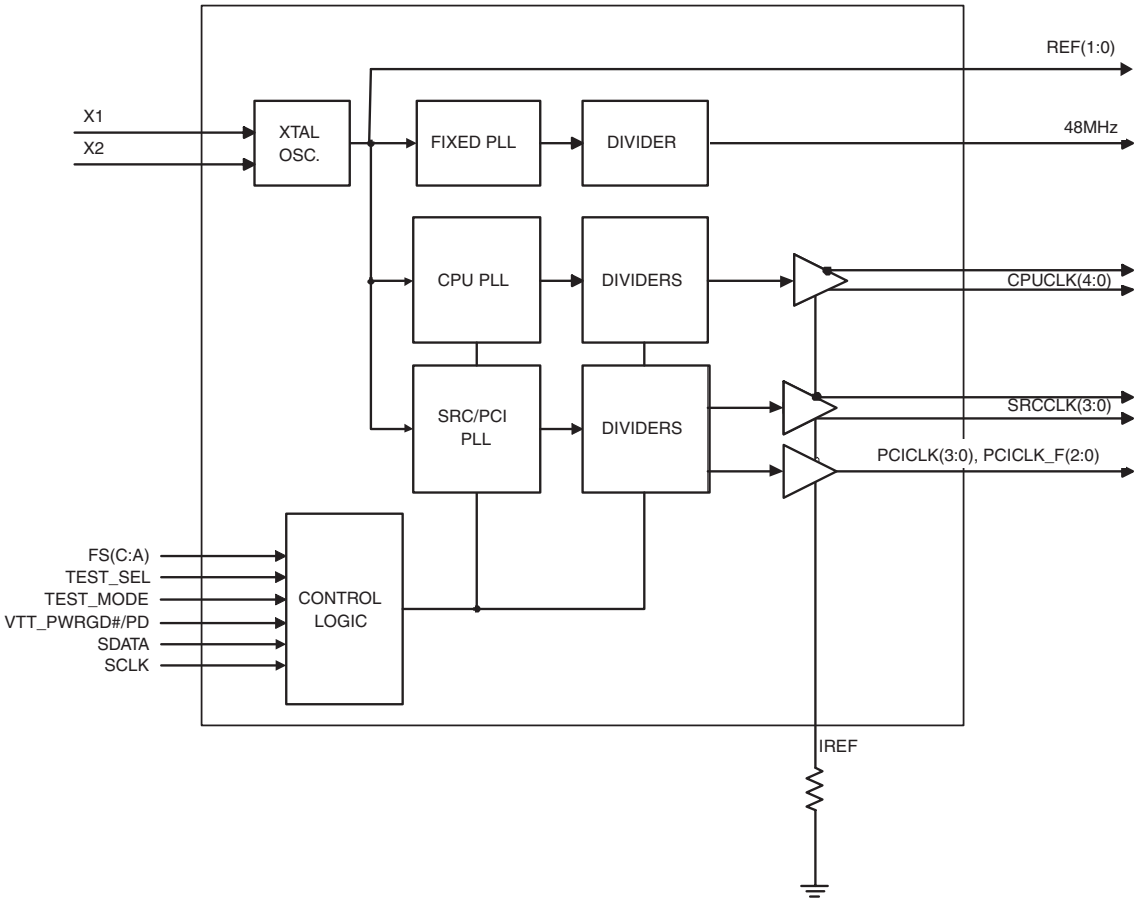


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## General Description

The **ICS932S422C** is a main clock synthesizer for CK410-generation Intel server platforms. The **ICS932S422C** is driven with a 14.318MHz crystal. It generates 5 CPU output pairs up to 400MHz and PCI-Express clocks at 100 or 200 MHz. The 48 MHz USB clock is an exact 48.000 MHz clock.

## Block Diagram



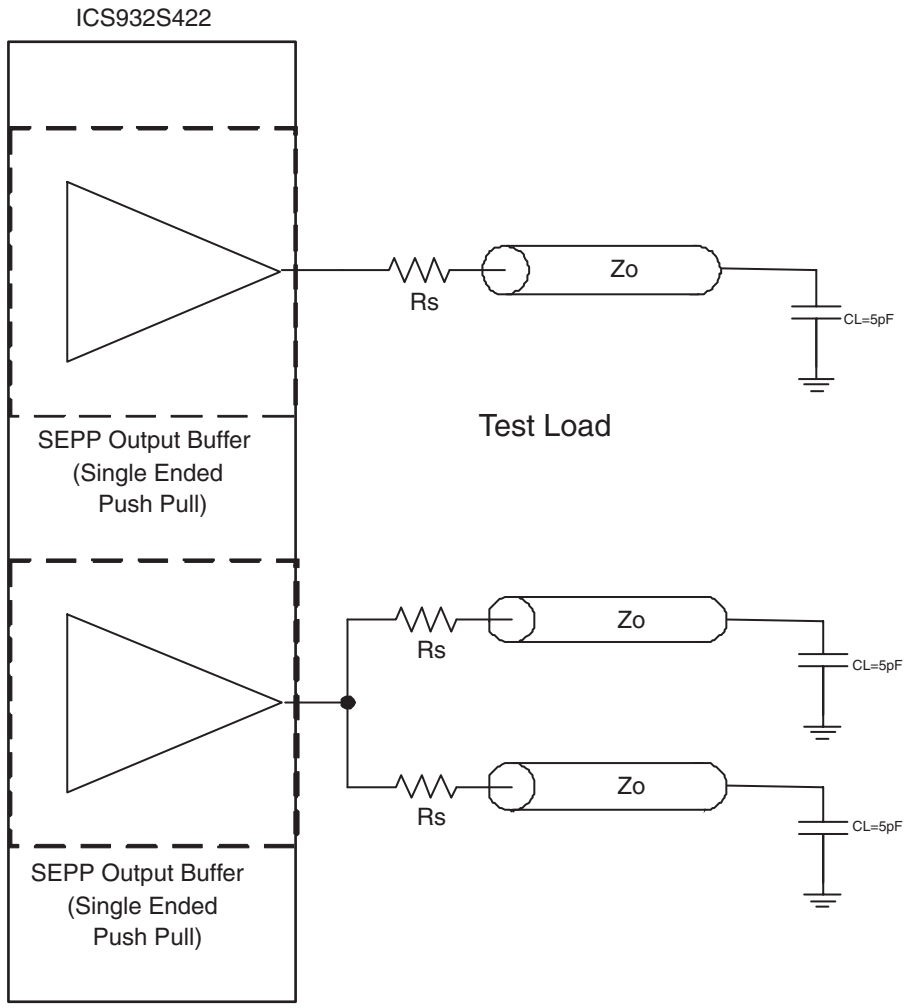

## Power Groups

| Pin Number | | Description |
|---|---|---|
| VDD | GND | |
| 53 | 50 | Xtal, Ref |
| 1,8 | 2,7 | PCICLK outputs |
| 15,25,28 | 20 | SRCCLK outputs |
| 35 | 34 | Master clock, CPU Analog |
| 12 | 14 | 48MHz, PLL_48 |
| 47,44,38 | 41 | CPUCLK clocks |



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## Single-ended Output Terminations




The singled-ended outputs of the ICS 932S422 default to a drive strength of 2 loads. The REF clocks can be turned down to 1-load strength via the SMBus. Suggested termination resistors are as follows for transmission lines with Zo = 50 ohms:

| | |
|---|---|
| Single-ended outputs at 2-load strength (Power up default for all single-ended outputs) | Driving 1 load, Rs = 33 ohms |
| | Driving 2 loads, Rs = 7.5 ohms |
| Single-ended outputs at 1-load strength (REF clock only) | Driving 1 load, Rs = 22 ohms |



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## Absolute Maximum Rating

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS | Notes |
|---|---|---|---|---|---|---|---|
| 3.3V Core Supply Voltage | VDD_A | - | | | $V_{DD}$ + 0.5V | V | 1 |
| 3.3V Logic Input Supply Voltage | VDD_In | - | GND - 0.5 | | $V_{DD}$ + 0.5V | V | 1 |
| Storage Temperature | Ts | - | -65 | | 150 | ˚C | 1 |
| Ambient Operating Temp | Tambient | - | 0 | | 70 | °C | 1 |
| Case Temperature | Tcase | - | | | 115 | °C | 1 |
| Input ESD protection HBM | ESD prot | - | 2000 | | | V | 1 |

[1]Guaranteed by design and characterization, not 100% tested in production.

## Electrical Characteristics - Input/Supply/Common Output Parameters

| PARAMETER | SYMBOL | CONDITIONS* | MIN | TYP | MAX | UNITS | Notes |
|---|---|---|---|---|---|---|---|
| Input High Voltage | $V_{IH}$ | 3.3 V +/-5% | 2 | | $V_{DD}$ + 0.3 | V | 1 |
| Input Low Voltage | $V_{IL}$ | 3.3 V +/-5% | $V_{SS}$ - 0.3 | | 0.8 | V | 1 |
| Input High Current | $I_{IH}$ | $V_{IN} = V_{DD}$ | -5 | | 5 | uA | 1 |
| Input Low Current | $I_{IL1}$ | $V_{IN}$ = 0 V; Inputs with no pull-up resistors | -5 | | | uA | 1 |
| | $I_{IL2}$ | $V_{IN}$ = 0 V; Inputs with pull-up resistors | -200 | | | uA | 1 |
| Low Threshold Input-High Voltage | $V_{IH_FS}$ | 3.3 V +/-5% | 0.7 | | $V_{DD}$ + 0.3 | V | 1 |
| Low Threshold Input-Low Voltage | $V_{IL_FS}$ | 3.3 V +/-5% | $V_{SS}$ - 0.3 | | 0.35 | V | 1 |
| Operating Supply Current | $I_{DD3.3OP}$ | Full Active, $C_L$ = Full load; | | | 350 | mA | 1 |
| Operating Current | $I_{DD3.3OP}$ | all outputs driven | | | 400 | mA | 1 |
| Powerdown Current | $I_{DD3.3PD}$ | all diff pairs driven | | | 70 | mA | 1 |
| | | all differential pairs tri-stated | | | 12 | mA | 1 |
| Input Frequency | $F_i$ | $V_{DD}$ = 3.3 V | | 14.31818 | | MHz | 2 |
| Pin Inductance | $L_{pin}$ | | | | 7 | nH | 1 |
| Input Capacitance | $C_{IN}$ | Logic Inputs | | | 5 | pF | 1 |
| | $C_{OUT}$ | Output pin capacitance | | | 6 | pF | 1 |
| | $C_{INX}$ | X1 & X2 pins | | | 5 | pF | 1 |
| Clk Stabilization | $T_{STAB}$ | From VDD Power-Up or de-assertion of PD to 1st clock | | | 1.8 | ms | 1 |
| Modulation Frequency | | Triangular Modulation | 30 | | 33 | kHz | 1 |
| Tdrive_PD | | CPU output enable after PD de-assertion | | | 300 | us | 1 |
| Tfall_PD | | PD fall time of | | | 5 | ns | 1 |
| Trise_PD | | PD rise time of | | | 5 | ns | 1 |
| SMBus Voltage | $V_{DD}$ | | 2.7 | | 5.5 | V | 1 |
| Low-level Output Voltage | $V_{OL}$ | @ $I_{PULLUP}$ | | | 0.4 | V | 1 |
| Current sinking at $V_{OL}$ = 0.4 V | $I_{PULLUP}$ | | 4 | | | mA | 1 |
| SCLK/SDATA Clock/Data Rise Time | $T_{RI2C}$ | (Max VIL - 0.15) to (Min VIH + 0.15) | | | 1000 | ns | 1 |
| SCLK/SDATA Clock/Data Fall Time | $T_{FI2C}$ | (Min VIH + 0.15) to (Max VIL - 0.15) | | | 300 | ns | 1 |

*TA = 0 - 70°C; Supply Voltage VDD = 3.3 V +/-5%

[1]Guaranteed by design and characterization, not 100% tested in production.

[2] Input frequency should be measured at the REF pin and tuned to ideal 14.31818MHz to meet ppm frequency accuracy on PLL outputs.



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## Electrical Characteristics - CPU 0.7V Current Mode Differential Pair

| PARAMETER | SYMBOL | CONDITIONS* | MIN | TYP | MAX | UNITS | NOTES |
|---|---|---|---|---|---|---|---|
| Current Source Output Impedance | Zo | $V_O = V_x$ | 3000 | | | Ω | 1 |
| Voltage High | VHigh | Statistical measurement on single ended signal | 660 | | 850 | mV | 1,3 |
| Voltage Low | VLow | | -150 | | 150 | mV | 1,3 |
| Max Voltage | Vovs | Measurement on single ended signal using absolute value. | | | 1150 | mV | 1 |
| Min Voltage | Vuds | | -300 | | | mV | 1 |
| Crossing Voltage (abs) | Vx(abs) | | 250 | | 550 | mV | 1 |
| Crossing Voltage (var) | d-Vx | Variation of crossing over all edges | | | 140 | mV | 1 |
| Long Accuracy | ppm | see Tperiod min-max values | -300 | | 300 | ppm | 1,2 |
| Average period | Tperiod | 400MHz nominal | 2.4993 | | 2.5008 | ns | 2 |
| | | 400MHz spread | 2.4993 | | 2.5133 | ns | 2 |
| | | 333.33MHz nominal | 2.9991 | | 3.0009 | ns | 2 |
| | | 333.33MHz spread | 2.9991 | | 3.016 | ns | 2 |
| | | 266.66MHz nominal | 3.7489 | | 3.7511 | ns | 2 |
| | | 266.66MHz spread | 3.7489 | | 3.77 | ns | 2 |
| | | 200MHz nominal | 4.9985 | | 5.0015 | ns | 2 |
| | | 200MHz spread | 4.9985 | | 5.0266 | ns | 2 |
| | | 166.66MHz nominal | 5.9982 | | 6.0018 | ns | 2 |
| | | 166.66MHz spread | 5.9982 | | 6.0320 | ns | 2 |
| | | 133.33MHz nominal | 7.4978 | | 7.5023 | ns | 2 |
| | | 133.33MHz spread | 7.4978 | | 7.5400 | ns | 2 |
| | | 100.00MHz nominal | 9.9970 | | 10.0030 | ns | 2 |
| | | 100.00MHz spread | 9.9970 | | 10.0533 | ns | 2 |
| Absolute min period | $T_{absmin}$ | 400MHz nominal/spread | 2.4143 | | | ns | 1,2 |
| | | 333.33MHz nominal/spread | 2.9141 | | | ns | 1,2 |
| | | 266.66MHz nominal/spread | 3.6639 | | | ns | 1,2 |
| | | 200MHz nominal/spread | 4.8735 | | | ns | 1,2 |
| | | 166.66MHz nominal/spread | 5.8732 | | | ns | 1,2 |
| | | 133.33MHz nominal/spread | 7.3728 | | | ns | 1,2 |
| | | 100.00MHz nominal/spread | 9.8720 | | | ns | 1,2 |
| Rise Time | $t_r$ | $V_{OL}$ = 0.175V, $V_{OH}$ = 0.525V | 175 | | 525 | ps | 1 |
| Fall Time | $t_f$ | $V_{OH}$ = 0.525V $V_{OL}$ = 0.175V | 175 | | 525 | ps | 1 |
| Rise Time Variation | d-$t_r$ | $V_{OL}$ = 0.175V, $V_{OH}$ = 0.525V | | | 125 | ps | 1 |
| Fall Time Variation | d-$t_f$ | $V_{OH}$ = 0.525V $V_{OL}$ = 0.175V | | | 125 | ps | 1 |
| Duty Cycle | $d_{t3}$ | Measurement from differential wavefrom | 45 | | 55 | % | 1 |
| Skew | $t_{sk3}$ | CPU(4:0), $V_T$ = 50% | | | 100 | ps | 1 |
| Jitter, Cycle to cycle | $t_{jcyc-cyc}$ | Measurement from differential wavefrom, (CPU(4:0)) | | | 50 | ps | 1 |

*$T_A$ = 0 - 70°C; $V_{DD}$ = 3.3 V +/-5%; $C_L$ =2pF, $R_S$=33.2Ω, $R_P$=49.9Ω, $I_{REF}$ = 475Ω

[1]Guaranteed by design and characterization, not 100% tested in production.

[2] All Long Term Accuracy and Clock Period specifications are guaranteed assuming that REF is at 14.31818MHz

[3]$I_{REF} = V_{DD}/(3xR_R)$. For $R_R$ = 475Ω (1%), $I_{REF}$ = 2.32mA. $I_{OH}$ = 6 x $I_{REF}$ and $V_{OH}$ = 0.7V @ $Z_O$=50Ω.



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## Electrical Characteristics - SRC/SATA 0.7V Current Mode Differential Pair

| PARAMETER | SYMBOL | CONDITIONS* | MIN | TYP | MAX | UNITS | Notes |
|---|---|---|---|---|---|---|---|
| Current Source Output Impedance | Zo | $V_O = V_x$ | 3000 | | | Ω | 1 |
| Voltage High | VHigh | Statistical measurement on single ended signal | 660 | | 850 | mV | 1,3 |
| Voltage Low | VLow | | -150 | | 150 | mV | 1,3 |
| Max Voltage | Vovs | Measurement on single ended signal using absolute value. | | | 1150 | mV | 1 |
| Min Voltage | Vuds | | -300 | | | mV | 1 |
| Crossing Voltage (abs) | Vx(abs) | | 250 | | 550 | mV | 1 |
| Crossing Voltage (var) | d-Vx | Variation of crossing over all edges | | | 140 | mV | 1 |
| Long Accuracy | ppm | see Tperiod min-max values | -300 | | 300 | ppm | 1,2 |
| Average period | Tperiod | 100.00MHz nominal | 9.9970 | | 10.0030 | ns | 2 |
| | | 100.00MHz spread | 9.9970 | | 10.0533 | ns | 2 |
| Absolute min period | Tabsmin | 100.00MHz nominal/spread | 9.8720 | | | ns | 1,2 |
| Rise Time | $t_r$ | $V_{OL}$ = 0.175V, $V_{OH}$ = 0.525V | 175 | | 525 | ps | 1 |
| Fall Time | $t_f$ | $V_{OH}$ = 0.525V $V_{OL}$ = 0.175V | 175 | | 525 | ps | 1 |
| Rise Time Variation | d-$t_r$ | $V_{OL}$ = 0.175V, $V_{OH}$ = 0.525V | | | 125 | ps | 1 |
| Fall Time Variation | d-$t_f$ | $V_{OH}$ = 0.525V $V_{OL}$ = 0.175V | | | 125 | ps | 1 |
| Duty Cycle | $d_{t3}$ | Measurement from differential wavefrom | 45 | | 55 | % | 1 |
| Skew | $t_{sk3}$ | $V_T$ = 50% | | | 250 | ps | 1 |
| Jitter, Cycle to cycle | $t_{jcyc-cyc}$ | Measurement from differential wavefrom | | | 125 | ps | 1 |

*$T_A$ = 0 - 70°C; $V_{DD}$ = 3.3 V +/-5%; $C_L$ =2pF, $R_S$=33.2Ω, $R_P$=49.9Ω, $I_{REF}$ = 475Ω

[1]Guaranteed by design and characterization, not 100% tested in production.

[2] All Long Term Accuracy and Clock Period specifications are guaranteed assuming that REF is at 14.31818MHz

[3]$I_{REF} = V_{DD}/(3xR_R)$. For $R_R$ = 475Ω (1%), $I_{REF}$ = 2.32mA. $I_{OH}$ = 6 x $I_{REF}$ and $V_{OH}$ = 0.7V @ $Z_O$=50Ω.

## Electrical Characteristics - PCICLK/PCICLK_F

| PARAMETER | SYMBOL | CONDITIONS* | MIN | TYP | MAX | UNITS | NOTES |
|---|---|---|---|---|---|---|---|
| Output Impedance | $R_{DSP}$ | $V_O = V_{DD}$*(0.5) | 12 | | 55 | Ω | 1 |
| Output High Voltage | $V_{OH}$ | $I_{OH}$ = -1 mA | 2.4 | | | V | 1 |
| Output Low Voltage | $V_{OL}$ | $I_{OL}$ = 1 mA | | | 0.55 | V | 1 |
| Output High Current | $I_{OH}$ | $V_{OH}$ @MIN = 1.0 V | -33 | | | mA | 1 |
| | | $V_{OH}$@MAX = 3.135 V | | | -33 | mA | 1 |
| Output Low Current | $I_{OL}$ | $V_{OL}$ @ MIN = 1.95 V | 30 | | | mA | 1 |
| | | $V_{OL}$ @ MAX = 0.4 V | | | 38 | mA | 1 |
| Rise Time | $t_r$ | $V_{OL}$ = 0.4 V, $V_{OH}$ = 2.4 V | 0.5 | | 2 | ns | 1 |
| Fall Time | $t_f$ | $V_{OH}$ = 2.4 V, $V_{OL}$ = 0.4 V | 0.5 | | 2 | ns | 1 |
| Duty Cycle | $d_{t1}$ | $V_T$ = 1.5 V | 45 | | 55 | % | 1 |
| Group Skew | $t_{skew}$ | $V_T$ = 1.5 V | | | 250 | ps | 1 |
| Jitter, Cycle to cycle | $t_{jcyc-cyc}$ | $V_T$ = 1.5 V | | | 500 | ps | 1 |

*TA = 0 - 70°C; Supply Voltage VDD = 3.3 V +/-5%, CL = 5 pF with Rs = 22Ω (unless otherwise specified)

[1]Guaranteed by design and characterization, not 100% tested in production.

[3] Spread Spectrum is off



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## Electrical Characteristics - USB48MHz

| PARAMETER | SYMBOL | CONDITIONS* | MIN | TYP | MAX | UNITS | NOTES |
|---|---|---|---|---|---|---|---|
| Long Accuracy | ppm | see Tperiod min-max values | -100 | | 100 | ppm | 1,2 |
| Clock period | $T_{period}$ | 48.00MHz output nominal | 20.8313 | | 20.8354 | ns | 2 |
| Output Impedance | $R_{DSP}$ | $V_O = V_{DD}*(0.5)$ | 12 | | 55 | Ω | 1 |
| Output High Voltage | $V_{OH}$ | $I_{OH}$ = -1 mA | 2.4 | | | V | 1 |
| Output Low Voltage | $V_{OL}$ | $I_{OL}$ = 1 mA | | | 0.55 | V | 1 |
| Output High Current | $I_{OH}$ | $V_{OH}$ @MIN = 1.0 V | -29 | | | mA | 1 |
| | | $V_{OH}$@MAX = 3.135 V | | | -33 | mA | 1 |
| Output Low Current | $I_{OL}$ | $V_{OL}$ @ MIN = 1.95 V | 29 | | | mA | 1 |
| | | $V_{OL}$ @ MAX = 0.4 V | | | 27 | mA | 1 |
| Rise Time | $t_{r_USB}$ | $V_{OL}$ = 0.4 V, $V_{OH}$ = 2.4 V | 1 | | 2 | ns | 1 |
| Fall Time | $t_{f_USB}$ | $V_{OH}$ = 2.4 V, $V_{OL}$ = 0.4 V | 1 | | 2 | ns | 1 |
| Duty Cycle | $d_{t1}$ | $V_T$ = 1.5 V | 45 | | 55 | % | 1 |
| Group Skew | $t_{skew}$ | $V_T$ = 1.5 V | | | 250 | ps | 1 |
| Jitter, Cycle to cycle | $t_{jcyc-cyc}$ | $V_T$ = 1.5 V | | | 500 | ps | 1 |

*TA = 0 - 70°C; Supply Voltage VDD = 3.3 V +/-5%, CL = 5 pF with Rs = 22Ω

[1]Guaranteed by design and characterization, not 100% tested in production.

## Electrical Characteristics - REF-14.318MHz

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS | Notes |
|---|---|---|---|---|---|---|---|
| Long Accuracy | ppm | see Tperiod min-max values | -300 | | 300 | ppm | 1,2 |
| Clock period | $T_{period}$ | 14.318MHz output nominal | 69.8270 | | 69.8550 | ns | 2 |
| Output High Voltage | $V_{OH}$ | $I_{OH}$ = -1 mA | 2.4 | | | V | 1 |
| Output Low Voltage | $V_{OL}$ | $I_{OL}$ = 1 mA | | | 0.4 | V | 1 |
| Output High Current | $I_{OH}$ | $V_{OH}$ @MIN = 1.0 V | -33 | | | mA | 1 |
| | | $V_{OH}$@MAX = 3.135 V | | | -33 | mA | 1 |
| Output Low Current | $I_{OL}$ | $V_{OL}$ @ MIN = 1.95 V | 30 | | | mA | 1 |
| | | $V_{OL}$ @ MAX = 0.4 V | | | 38 | mA | 1 |
| Rise Time | $t_{r1}$ | $V_{OL}$ = 0.4 V, $V_{OH}$ = 2.4 V | 0.5 | | 2 | ns | 1 |
| Fall Time | $t_{f1}$ | $V_{OH}$ = 2.4 V, $V_{OL}$ = 0.4 V | 0.5 | | 2 | ns | 1 |
| Skew | $t_{sk1}$ | $V_T$ = 1.5 V | | | 500 | ps | 1 |
| Duty Cycle | $d_{t1}$ | $V_T$ = 1.5 V | 45 | | 55 | % | 1 |
| Jitter | $t_{jcyc-cyc}$ | $V_T$ = 1.5 V | | | 1000 | ps | 1 |

*TA = 0 - 70°C; Supply Voltage VDD = 3.3 V +/-5%, CL = 5 pF with Rs = 22Ω (Rs is used in USB48MHz test only)

[1]Guaranteed by design and characterization, not 100% tested in production.

[2] All Long Term Accuracy and Clock Period specifications are guaranteed assuming that REF is at 14.31818MHz

## Electrical Characteristics - Differential Jitter Parameters

| PARAMETER | Symbol | Conditions | Min | TYP | Max | Units | Notes |
|---|---|---|---|---|---|---|---|
| Jitter, Phase | $t_{jphasePLL}$ | PCIe Gen 1 | | | 86 | ps (p-p) | 1,2 |
| | $t_{jphaseLo}$ | PCIe Gen 2<br>10kHz < f < 1.5MHz | | | 3 | ps (RMS) | 1,2 |
| | $t_{jphaseHigh}$ | PCIe Gen 2<br>1.5MHz < f < Nyquist (50MHz) | | | 3.1 | ps (RMS) | 1,2 |
| | $t_{jphFBD1_3.2G}$ | FBD1 3.2/4G<br>11MHz to 33MHz | | | 3 | ps (RMS) | 1,2 |
| | $t_{jphFBD1_4.0G}$ | FBD1 4.8G<br>11MHz to 33MHz | | | 2.5 | ps (RMS) | 1,2 |

*TA = 0 - 70°C; Supply Voltage VDD = 3.3 V +/-5%

[1]Guaranteed by design and characterization, not 100% tested in production.

[2]See http://www.pcisig.com for compelte specs

1412A—12/10/07

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# General SMBus serial interface information for the ICS932S422C

## How to Write:

- Controller (host) sends a start bit.
- Controller (host) sends the write address D2 (H)
- ICS clock will ***acknowledge***
- Controller (host) sends the begining byte location = N
- ICS clock will ***acknowledge***
- Controller (host) sends the data byte count = X
- ICS clock will ***acknowledge***
- Controller (host) starts sending ***Byte N through Byte N + X -1***
  (see Note 2)
- ICS clock will ***acknowledge*** each byte ***one at a time***
- Controller (host) sends a Stop bit

## How to Read:

- Controller (host) will send start bit.
- Controller (host) sends the write address D2 (H)
- ICS clock will ***acknowledge***
- Controller (host) sends the begining byte location = N
- ICS clock will ***acknowledge***
- Controller (host) will send a separate start bit.
- Controller (host) sends the read address D3 (H)
- ICS clock will ***acknowledge***
- ICS clock will send the data byte count = X
- ICS clock sends ***Byte N + X -1***
- ICS clock sends ***Byte 0 through byte X (if X(H) was written to byte 8)***.
- Controller (host) will need to acknowledge each byte
- Controllor (host) will send a not acknowledge bit
- Controller (host) will send a stop bit

**Index Block Write Operation**

| Controller (Host) | | | ICS (Slave/Receiver) |
|---|---|---|---|
| T | starT bit | | |
| Slave Address D2(H) | | | |
| WR | WRite | | |
| | | | ACK |
| Beginning Byte = N | | | |
| | | | ACK |
| Data Byte Count = X | | | |
| | | | ACK |
| Beginning Byte N | | X Byte | |
| | | | ACK |
| ◇ | | | |
| ◇ | | | ◇ |
| ◇ | | | ◇ |
| | | | ◇ |
| Byte N + X - 1 | | | |
| | | | ACK |
| P | stoP bit | | |

**Index Block Read Operation**

| Controller (Host) | | ICS (Slave/Receiver) | |
|---|---|---|---|
| T | starT bit | | |
| Slave Address D2(H) | | | |
| WR | WRite | | |
| | | ACK | |
| Beginning Byte = N | | | |
| | | ACK | |
| RT | Repeat starT | | |
| Slave Address D3(H) | | | |
| RD | ReaD | | |
| | | ACK | |
| | | | |
| | | Data Byte Count = X | |
| ACK | | | |
| | | X Byte | Beginning Byte N |
| ACK | | | |
| | | | ◇ |
| ◇ | | | ◇ |
| ◇ | | | ◇ |
| ◇ | | | |
| | | | Byte N + X - 1 |
| N | Not acknowledge | | |
| P | stoP bit | | |



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**SMBus Table: SRC Output Enable Register**

| Byte 0 | Pin # | Name | Control Function | Type | 0 | 1 | PWD |
|---|---|---|---|---|---|---|---|
| Bit 7 | NA | SRCCLK7 Enable | Output Enable | RW | Disable-Hi-Z | Enable | 1 |
| Bit 6 | NA | SRCCLK6 Enable | Output Enable | RW | Disable-Hi-Z | Enable | 1 |
| Bit 5 | NA | SRCCLK5 Enable | Output Enable | RW | Disable-Hi-Z | Enable | 1 |
| Bit 4 | 26,27 | SRCCLK4 Enable | Output Enable | RW | Disable-Hi-Z | Enable | 1 |
| Bit 3 | 23,24 | SRCCLK3 Enable | Output Enable | RW | Disable-Hi-Z | Enable | 1 |
| Bit 2 | 21,22 | SRCCLK2 Enable | Output Enable | RW | Disable-Hi-Z | Enable | 1 |
| Bit 1 | 18,19 | SRCCLK1 Enable | Output Enable | RW | Disable-Hi-Z | Enable | 1 |
| Bit 0 | 32,31 | CPUCLK4 | Output Enable | RW | Disable-Hi-Z | Enable | 1 |

**SMBus Table: CPU, REF and 48 MHz Output Enable Register**

| Byte 1 | Pin # | Name | Control Function | Type | 0 | 1 | PWD |
|---|---|---|---|---|---|---|---|
| Bit 7 | 54 | REF1 Enable | Output Enable | RW | Disable-Low | Enable | 1 |
| Bit 6 | 55 | REF0 Enable | Output Enable | RW | Disable-Low | Enable | 1 |
| Bit 5 | 36,37 | CPUCLK3 | Output Enable | RW | Disable-Hi-Z | Enable | 1 |
| Bit 4 | 39,40 | CPUCLK2 | Output Enable | RW | Disable-Hi-Z | Enable | 1 |
| Bit 3 | - | RESERVED | | | | | 0 |
| Bit 2 | 42,43 | CPUCLK1 | Output Enable | RW | Disable-Hi-Z | Enable | 1 |
| Bit 1 | 45,46 | CPUCLK0 | Output Enable | RW | Disable-Hi-Z | Enable | 1 |
| Bit 0 | CPU, SRC, PCI | Spread Spectrum Enable | Spread Off/On | RW | Spread Off | Spread On | 0 |

**SMBus Table: PCI and PCICLK_F Output Enable Register**

| Byte 2 | Pin # | Name | Control Function | Type | 0 | 1 | PWD |
|---|---|---|---|---|---|---|---|
| Bit 7 | 6 | PCICLK3 | Output Enable | RW | Disable-Low | Enable | 1 |
| Bit 6 | 5 | PCICLK2 | Output Enable | RW | Disable-Low | Enable | 1 |
| Bit 5 | 4 | PCICLK1 | Output Enable | RW | Disable-Low | Enable | 1 |
| Bit 4 | 3 | PCICLK0 | Output Enable | RW | Disable-Low | Enable | 1 |
| Bit 3 | 11 | PCICLK_F2 Enable | Output Enable | RW | Disable-Low | Enable | 1 |
| Bit 2 | 10 | PCICLK_F1 Enable | Output Enable | RW | Disable-Low | Enable | 1 |
| Bit 1 | 9 | PCICLK_F0 Enable | Output Enable | RW | Disable-Low | Enable | 1 |
| Bit 0 | 13 | 48MHz Enable | Output Enable | RW | Disable-Low | Enable | 1 |

**SMBus Table: PCICLK_F and SRC Stop Control Register**

| Byte 3 | Pin # | Name | Control Function | Type | 0 | 1 | PWD |
|---|---|---|---|---|---|---|---|
| Bit 7 | 11 | PCICLK_F2 Stop En | Free-Running Control, Default: not affected by PCI/SRC_STOP (Byte 4, bit 5) | RW | Free-Running | Stoppable | 1 |
| Bit 6 | 10 | PCICLK_F1 Stop En | | RW | Free-Running | Stoppable | 1 |
| Bit 5 | 9 | PCICLK_F0 Stop En | | RW | Free-Running | Stoppable | 1 |
| Bit 4 | 26,27 | SRCCLK4 Stop En | | RW | Free-Running | Stoppable | 1 |
| Bit 3 | 23,24 | SRCCLK3 Stop En | | RW | Free-Running | Stoppable | 1 |
| Bit 2 | 21,22 | SRCCLK2 Stop En | | RW | Free-Running | Stoppable | 1 |
| Bit 1 | 18,19 | SRCCLK1 Stop En | | RW | Free-Running | Stoppable | 1 |
| Bit 0 | - | RESERVED | | | | | 0 |



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**SMBus Table: CPU and SRC Stop and Power Down Mode Drive Control Register**

| Byte 4 | Pin # | Name | Control Function | Type | 0 | 1 | PWD |
|---|---|---|---|---|---|---|---|
| Bit 7 | 36,37 | CPUCLK3 PD Drive | Drive Mode in PD | RW | Driven | Hi-Z | 0 |
| Bit 6 | 39,40 | CPUCLK2 PD Drive | Drive Mode in PD | RW | Driven | Hi-Z | 0 |
| Bit 5 | 42,43 | CPUCLK1 PD Drive | Drive mode in PD | RW | Driven | Hi-Z | 0 |
| Bit 4 | 45,46 | CPUCLK0 PD Drive | Drive mode in PD | RW | Driven | Hi-Z | 0 |
| Bit 3 | - | RESERVED | | | | | 0 |
| Bit 2 | - | RESERVED | | | | | 0 |
| Bit 1 | - | RESERVED | | | | | 0 |
| Bit 0 | - | RESERVED | | | | | 0 |

**SMBus Table: Output and Spread Spectrum Control Register**

| Byte 5 | Pin # | Name | Control Function | Type | 0 | 1 | PWD |
|---|---|---|---|---|---|---|---|
| Bit 7 | 32,31 | CPUCLK4 PD Drive | Drive Mode in PD | RW | Driven | Hi-Z | 0 |
| Bit 6 | SRC | SRC Stop Drive Mode | Driven in STOP | RW | Driven | Hi-Z | 0 |
| Bit 5 | SRC | SRC PD Drive Mode | Driven in PD | RW | Driven | Hi-Z | 0 |
| Bit 4 | - | RESERVED | | | | | 0 |
| Bit 3 | - | RESERVED | | | | | 0 |
| Bit 2 | - | RESERVED | | | | | 0 |
| Bit 1 | - | RESERVED | | | | | 0 |
| Bit 0 | - | RESERVED | | | | | 0 |

**SMBus Table: Device ID Register**

| Byte 6 | Pin # | Name | Control Function | Type | 0 | 1 | PWD |
|---|---|---|---|---|---|---|---|
| Bit 7 | - | Test Mode Selection | Test Mode Selection | RW | Hi-Z | REF/N | 0 |
| Bit 6 | - | Test Clock Mode Entry | Test Mode | RW | Disable | Enable | 0 |
| Bit 5 | - | RESERVED | | | | | 0 |
| Bit 4 | 54,55 | REF Drive Strength | 1X or 2X | RW | 1X | 2X | 1 |
| Bit 3 | PCI, SRC | PCI_STOP Control | Stop non-free running PC and SRC clocks. | RW | Stop | Run | 1 |
| Bit 2 | - | FS_C | FS_C readback | R | See 932S422 Functionality Table | | Latch |
| Bit 1 | - | FS_B | FS_B readback | R | | | Latch |
| Bit 0 | - | FS_A | FS_A readback | R | | | Latch |

**SMBus Table: Vendor & Revision ID Register**

| Byte 7 | Pin # | Name | Control Function | Type | 0 | 1 | PWD |
|---|---|---|---|---|---|---|---|
| Bit 7 | - | RID3 | REVISION ID | R | - | - | 0 |
| Bit 6 | - | RID2 | | R | - | - | 0 |
| Bit 5 | - | RID1 | | R | - | - | 1 |
| Bit 4 | - | RID0 | | R | - | - | 0 |
| Bit 3 | - | VID3 | VENDOR ID | R | - | - | 0 |
| Bit 2 | - | VID2 | | R | - | - | 0 |
| Bit 1 | - | VID1 | | R | - | - | 0 |
| Bit 0 | - | VID0 | | R | - | - | 1 |



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**SMBus Table: Byte Count Register**

| Byte 8 | Pin # | Name | Control Function | Type | 0 | 1 | PWD |
|---|---|---|---|---|---|---|---|
| Bit 7 | - | BC7 | Byte Count Programming b(7:0) | RW | Writing to this register will configure how many bytes will be read back, default is 8 bytes. (0 to 7) | | 0 |
| Bit 6 | - | BC6 | | RW | | | 0 |
| Bit 5 | - | BC5 | | RW | | | 0 |
| Bit 4 | - | BC4 | | RW | | | 0 |
| Bit 3 | - | BC3 | | RW | | | 1 |
| Bit 2 | - | BC2 | | RW | | | 0 |
| Bit 1 | - | BC1 | | RW | | | 0 |
| Bit 0 | - | BC0 | | RW | | | 0 |

**SMBus Table: Device ID Register**

| Byte 9 | Pin # | Name | Control Function | Type | 0 | 1 | PWD |
|---|---|---|---|---|---|---|---|
| Bit 7 | | DID7 | Device ID (0C hex) | R | - | - | 0 |
| Bit 6 | | DID6 | | R | - | - | 0 |
| Bit 5 | | DID5 | | R | - | - | 0 |
| Bit 4 | | DID4 | | R | - | - | 0 |
| Bit 3 | | DID3 | | R | - | - | 1 |
| Bit 2 | | DID2 | | R | - | - | 1 |
| Bit 1 | | DID1 | | R | - | - | 0 |
| Bit 0 | | DID0 | | R | - | - | 0 |

**SMBus Table: M/N Programming & Control Register**

| Byte 10 | Pin # | Name | Control Function | Type | 0 | 1 | PWD |
|---|---|---|---|---|---|---|---|
| Bit 7 | - | M/N_EN | CPU and SRC M/N Programming | RW | Disable | Enable | 0 |
| Bit 6 | - | RESERVED | | | | | 0 |
| Bit 5 | CPU | Spread Spectrum Enable | Spread Off/On | RW | Spread Off | Spread On | 0 |
| Bit 4 | SRC | Spread Spectrum Enable | Spread Off/On | RW | Spread Off | Spread On | 0 |
| Bit 3 | SRC, PCI | SRC Alternate Frequency (96% of Nominal) | Set SRC = 96 MHz and PCI = 32 MHz Only active if Byte 10, bit 2 = 1 | RW | Normal | Alternate Frequency | 0 |
| Bit 2 | CPU | CPU Alternate Frequency (96% of Nominal) Only active if latched frequency is 166 MHz or 333 MHz. | Set alternate CPU frequency: 166 MHz to 160 MHz 333 MHz to 320 MHz | RW | Normal | Alternate Frequency | 0 |
| Bit 1 | 54 | REF1 Drive Strength | 1X or 2X | RW | See REF Drive Strength Functionality Table | | 1 |
| Bit 0 | 55 | REF0 Drive Strength | 1X or 2X | RW | | | 1 |



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**SMBus Table: CPU Frequency Control Register**

| Byte 11 | Pin # | Name | Control Function | Type | 0 | 1 | PWD |
|---|---|---|---|---|---|---|---|
| Bit 7 | - | CPU N Div8 | N Divider Prog bit 8 | RW | The decimal representation of M and N Divider in Byte 11 and 12 will configure the CPU VCO frequency. Default at power up = latch-in or Byte 0 Rom table. VCO Frequency = 14.318 x [NDiv(9:0)+8] / [MDiv(5:0)+2] | | X |
| Bit 6 | - | CPU N Div9 | N Divider Prog bit 9 | RW | | | X |
| Bit 5 | - | CPU M Div5 | M Divider Programming bit (5:0) | RW | | | X |
| Bit 4 | - | CPU M Div4 | | RW | | | X |
| Bit 3 | - | CPU M Div3 | | RW | | | X |
| Bit 2 | - | CPU M Div2 | | RW | | | X |
| Bit 1 | - | CPU M Div1 | | RW | | | X |
| Bit 0 | - | CPU M Div0 | | RW | | | X |

**SMBus Table: CPU Frequency Control Register**

| Byte 12 | Pin # | Name | Control Function | Type | 0 | 1 | PWD |
|---|---|---|---|---|---|---|---|
| Bit 7 | - | CPU N Div7 | N Divider Programming Byte12 bit(7:0) and Byte11 bit(7:6) | RW | The decimal representation of M and N Divider in Byte 11 and 12 will configure the CPU VCO frequency. Default at power up = latch-in or Byte 0 Rom table. VCO Frequency = 14.318 x [NDiv(9:0)+8] / [MDiv(5:0)+2] | | X |
| Bit 6 | - | CPU N Div6 | | RW | | | X |
| Bit 5 | - | CPU N Div5 | | RW | | | X |
| Bit 4 | - | CPU N Div4 | | RW | | | X |
| Bit 3 | - | CPU N Div3 | | RW | | | X |
| Bit 2 | - | CPU N Div2 | | RW | | | X |
| Bit 1 | - | CPU N Div1 | | RW | | | X |
| Bit 0 | - | CPU N Div0 | | RW | | | X |

**SMBus Table: CPU Spread Spectrum Control Register**

| Byte 13 | Pin # | Name | Control Function | Type | 0 | 1 | PWD |
|---|---|---|---|---|---|---|---|
| Bit 7 | - | CPU SSP7 | Spread Spectrum Programming bit(7:0) | RW | These Spread Spectrum bits in Byte 13 and 14 will program the spread pecentage of CPU | | X |
| Bit 6 | - | CPU SSP6 | | RW | | | X |
| Bit 5 | - | CPU SSP5 | | RW | | | X |
| Bit 4 | - | CPU SSP4 | | RW | | | X |
| Bit 3 | - | CPU SSP3 | | RW | | | X |
| Bit 2 | - | CPU SSP2 | | RW | | | X |
| Bit 1 | - | CPU SSP1 | | RW | | | X |
| Bit 0 | - | CPU SSP0 | | RW | | | X |

**SMBus Table: CPU Spread Spectrum Control Register**

| Byte 14 | Pin # | Name | Control Function | Type | 0 | 1 | PWD |
|---|---|---|---|---|---|---|---|
| Bit 7 | - | Reserved | | | | | 0 |
| Bit 6 | - | CPU SSP14 | Spread Spectrum Programming bit(14:8) | RW | These Spread Spectrum bits in Byte 13 and 14 will program the spread pecentage of CPU | | X |
| Bit 5 | - | CPU SSP13 | | RW | | | X |
| Bit 4 | - | CPU SSP12 | | RW | | | X |
| Bit 3 | - | CPU SSP11 | | RW | | | X |
| Bit 2 | - | CPU SSP10 | | RW | | | X |
| Bit 1 | - | CPU SSP9 | | RW | | | X |
| Bit 0 | - | CPU SSP8 | | RW | | | X |



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**SMBus Table: SRC Frequency Control Register**

| Byte 15 | Pin # | Name | Control Function | Type | 0 | 1 | PWD |
|---|---|---|---|---|---|---|---|
| Bit 7 | - | SRC N Div8 | N Divider Prog bit 8 | RW | The decimal representation of M and N Divider in Byte 15 and 16 will configure the SRC VCO frequency. Default at power up = latch-in or Byte 0 Rom table. VCO Frequency = 14.318 x [NDiv(9:0)+8] / [MDiv(5:0)+2] | | X |
| Bit 6 | - | SRC N Div9 | N Divider Prog bit 9 | RW | | | X |
| Bit 5 | - | SRC M Div5 | M Divider Programming bits | RW | | | X |
| Bit 4 | - | SRC M Div4 | | RW | | | X |
| Bit 3 | - | SRC M Div3 | | RW | | | X |
| Bit 2 | - | SRC M Div2 | | RW | | | X |
| Bit 1 | - | SRC M Div1 | | RW | | | X |
| Bit 0 | - | SRC M Div0 | | RW | | | X |

**SMBus Table: SRC Frequency Control Register**

| Byte 16 | Pin # | Name | Control Function | Type | 0 | 1 | PWD |
|---|---|---|---|---|---|---|---|
| Bit 7 | - | SRC N Div7 | N Divider Programming b(7:0) | RW | The decimal representation of M and N Divider in Byte 15 and 16 will configure the SRC VCO frequency. Default at power up = latch-in or Byte 0 Rom table. VCO Frequency = 14.318 x [NDiv(9:0)+8] / [MDiv(5:0)+2] | | X |
| Bit 6 | - | SRC N Div6 | | RW | | | X |
| Bit 5 | - | SRC N Div5 | | RW | | | X |
| Bit 4 | - | SRC N Div4 | | RW | | | X |
| Bit 3 | - | SRC N Div3 | | RW | | | X |
| Bit 2 | - | SRC N Div2 | | RW | | | X |
| Bit 1 | - | SRC N Div1 | | RW | | | X |
| Bit 0 | - | SRC N Div0 | | RW | | | X |

**SMBus Table: SRC Spread Spectrum Control Register**

| Byte 17 | Pin # | Name | Control Function | Type | 0 | 1 | PWD |
|---|---|---|---|---|---|---|---|
| Bit 7 | - | SRC SSP7 | Spread Spectrum Programming b(7:0) | RW | These Spread Spectrum bits in Byte 17 and 18 will program the spread pecentage of SRC | | X |
| Bit 6 | - | SRC SSP6 | | RW | | | X |
| Bit 5 | - | SRC SSP5 | | RW | | | X |
| Bit 4 | - | SRC SSP4 | | RW | | | X |
| Bit 3 | - | SRC SSP3 | | RW | | | X |
| Bit 2 | - | SRC SSP2 | | RW | | | X |
| Bit 1 | - | SRC SSP1 | | RW | | | X |
| Bit 0 | - | SRC SSP0 | | RW | | | X |

**SMBus Table: SRC Spread Spectrum Control Register**

| Byte 18 | Pin # | Name | Control Function | Type | 0 | 1 | PWD |
|---|---|---|---|---|---|---|---|
| Bit 7 | - | Reserved | Reserved | R | - | - | 0 |
| Bit 6 | - | SRC SSP14 | Spread Spectrum Programming b(14:8) | RW | These Spread Spectrum bits in Byte 17 and 18 will program the spread pecentage of SRC | | X |
| Bit 5 | - | SRC SSP13 | | RW | | | X |
| Bit 4 | - | SRC SSP12 | | RW | | | X |
| Bit 3 | - | SRC SSP11 | | RW | | | X |
| Bit 2 | - | SRC SSP10 | | RW | | | X |
| Bit 1 | - | SRC SSP9 | | RW | | | X |
| Bit 0 | - | SRC SSP8 | | RW | | | X |



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**SMBus Table: CPU Programmable Output Divider Register**

| Byte 19 | Pin # | Name | Control Function | Type | 0 | 1 | PWD |
|---|---|---|---|---|---|---|---|
| Bit 7 | - | CPUDiv3 | CPU Divider Ratio Programming Bits | RW | See CPU, SRC and PCI Divider Ratios Table | | X |
| Bit 6 | - | CPUDiv2 | | RW | | | X |
| Bit 5 | - | CPUDiv1 | | RW | | | X |
| Bit 4 | - | CPUDiv0 | | RW | | | X |
| Bit 3 | | RESERVED | | | | | X |
| Bit 2 | | RESERVED | | | | | X |
| Bit 1 | | RESERVED | | | | | X |
| Bit 0 | | RESERVED | | | | | X |

**SMBus Table: SRC and PCI Programmable Output Divider Register**

| Byte 20 | Pin # | Name | Control Function | Type | 0 | 1 | PWD |
|---|---|---|---|---|---|---|---|
| Bit 7 | - | PCIDiv3 | PCI Divider Ratio Programming Bits | RW | See CPU, SRC and PCI Divider Ratios Table | | X |
| Bit 6 | - | PCIDiv2 | | RW | | | X |
| Bit 5 | - | PCIDiv1 | | RW | | | X |
| Bit 4 | - | PCIDiv0 | | RW | | | X |
| Bit 3 | - | SRC_Div3 | SRC_ Divider Ratio Programming Bits | RW | See CPU, SRC and PCI Divider Ratios Table | | X |
| Bit 2 | - | SRC_Div2 | | RW | | | X |
| Bit 1 | - | SRC_Div1 | | RW | | | X |
| Bit 0 | - | SRC_Div0 | | RW | | | X |

**SMBusTable: Test Byte Register**

| Byte 21 | Test | Test Function | Type | Test Result | PWD |
|---|---|---|---|---|---|
| Bit 7 | - | ICS ONLY TEST | RW | Reserved | 0 |
| Bit 6 | - | ICS ONLY TEST | RW | Reserved | 0 |
| Bit 5 | - | ICS ONLY TEST | RW | Reserved | 0 |
| Bit 4 | - | ICS ONLY TEST | RW | Reserved | 0 |
| Bit 3 | - | ICS ONLY TEST | RW | Reserved | 0 |
| Bit 2 | - | ICS ONLY TEST | RW | Reserved | 0 |
| Bit 1 | - | ICS ONLY TEST | RW | Reserved | 0 |
| Bit 0 | - | ICS ONLY TEST | RW | Reserved | 0 |

**Note: Do NOT write to Bit 21. Erratic device operation will result!**



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## PD, Power Down

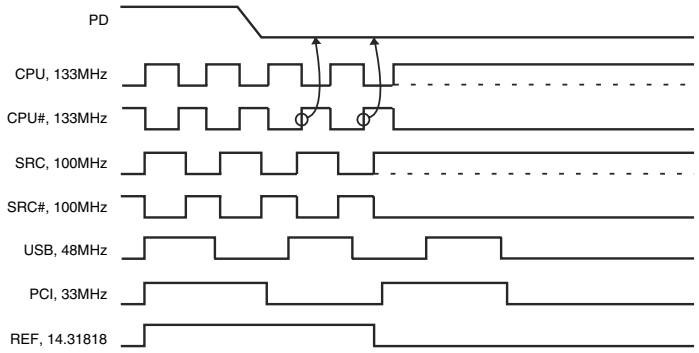
PD is an asynchronous active high input used to shut off all clocks cleanly prior to system power down.
When PD is asserted, all clocks will be driven low before turning off the VCO. All clocks will start without glitches when PD is

| PD | CPU | CPU # | SRC | SRC# | PCIF/PCI | USB | REF | Note |
|---|---|---|---|---|---|---|---|---|
| 1 | Normal | Normal | Normal | Normal | 33MHz | 48MHz | 14.318MHz | 1 |
| 0 | Iref * 2 or Float | Float | Iref * 2 or Float | Float | Low | Low | Low | 1 |

Notes:
1. Refer to SMBus Byte 4 for additional information.

## PD Assertion

PD should be sampled low by 2 consecutive CPU# rising edges before stopping clocks. All single ended clocks will be held low on their next high to low transition.
All differential clocks will be held high on the next high to low transition of the complimentary clock. If the control register determining to drive mode is set to 'tri-state', the differential pair will be stopped in tri-state mode, undriven.
When the drive mode corresponding to the CPU or SRC clock of interest is set to '0' the true clock will be driven high at 2 x Iref and the complementary clock will be tristated. If the control register is programmed to '1' both clocks will be tristated.
See SMBus Byte 4 for additional information.




**CPU, SRC and PCI Divider Ratios**

| | Div(3:0) | Divider |
|---|---|---|
| 0 | 0000 | 2 |
| 1 | 0001 | 3 |
| 2 | 0010 | 5 |
| 3 | 0011 | 15 |
| 4 | 0100 | 4 |
| 5 | 0101 | 6 |
| 6 | 0110 | 10 |
| 7 | 0111 | 30 |
| 8 | 1000 | 8 |
| 9 | 1001 | 12 |
| 10 | 1010 | 20 |
| 11 | 1011 | 60 |
| 12 | 1100 | 16 |
| 13 | 1101 | 24 |
| 14 | 1110 | 40 |
| 15 | 1111 | 120 |

**REF Drive Strength Functionality**

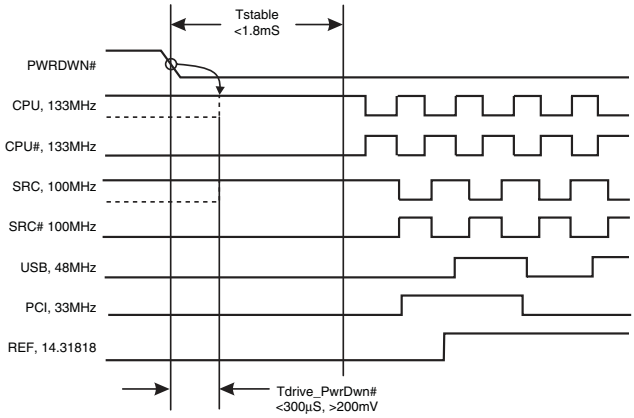
| Byte6, bit 4 | Byte 10, bit 1 | Byte 10, bit 0 | REF1 | REF0 |
|---|---|---|---|---|
| 0 | X | X | 1x | 1x |
| 1 | 0 | 0 | 1x | 1x |
| 1 | 0 | 1 | 1x | 2x |
| 1 | 1 | 0 | 2x | 1x |
| **1** | **1** | **1** | **2x** | **2x** |



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## PD De-assertion

The time from the de-assertion of PD or until power supply ramps to get stable clocks will be less than 1.8ms. If the drive mode control bit for PD tristate is programmed to '1' the stopped differential pair must first be driven high to a minimum of 200mV in less than 300µs of PD deassertion.

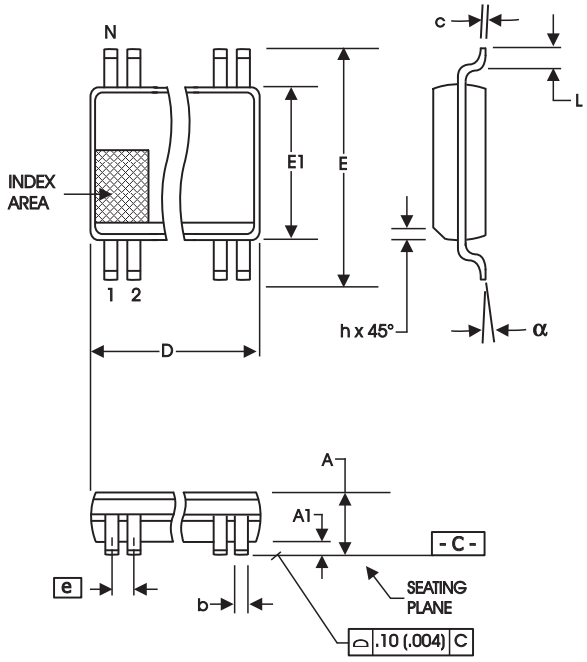



## Test Clarification Table

| Comments | HW | | SW | | |
|---|---|---|---|---|---|
| | FSLC/TEST_SEL HW PIN | FSLB/TEST_MODE HW PIN | TEST ENTRY BIT B6b6 | REF/N or HI-Z B6b7 | OUTPUT |
| | 0 | X | 0 | X | NORMAL |
| Power-up w/ TEST_SEL = 1 to enter test mode<br>Cycle power to disable test mode<br>FSLC./TEST_SEL -->3-level latched input<br>If power-up w/ V>2.0V (-0.3V) then use TEST_SEL<br>If power-up w/ V<2.0V (-0.3V) then use FSLC<br>FSLB/TEST_MODE -->low Vth input<br>TEST_MODE is a real time input. | 1 | 0 | X | 0 | HI-Z |
| | 1 | 0 | X | 1 | REF/N |
| | 1 | 1 | X | 0 | REF/N |
| | 1 | 1 | X | 1 | REF/N |
| If TEST_SEL HW pin is 0 during power-up,<br>test mode can be invoked through B6b6.<br>If test mode is invoked by B6b6, only B6b7<br>is used to select HI-Z or REF/N<br>FSLB/TEST_Mode pin is not used.<br>Cycle power to disable test mode, one shot control | 0 | X | 1 | 0 | HI-Z |
| | 0 | X | 1 | 1 | REF/N |
| B6b6: 1= ENTER TEST MODE, Default = 0 (NORMAL OPERATION) | | | | | |
| B6b7: 1= REF/N, Default = 0 (HI-Z) | | | | | |



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**56-Lead, 300 mil Body, 25 mil, SSOP**

| SYMBOL | In Millimeters COMMON DIMENSIONS | | In Inches COMMON DIMENSIONS | |
|---|---|---|---|---|
| | MIN | MAX | MIN | MAX |
| A | 2.41 | 2.80 | .095 | .110 |
| A1 | 0.20 | 0.40 | .008 | .016 |
| b | 0.20 | 0.34 | .008 | .0135 |
| c | 0.13 | 0.25 | .005 | .010 |
| D | SEE VARIATIONS | | SEE VARIATIONS | |
| E | 10.03 | 10.68 | .395 | .420 |
| E1 | 7.40 | 7.60 | .291 | .299 |
| e | 0.635 BASIC | | 0.025 BASIC | |
| h | 0.38 | 0.64 | .015 | .025 |
| L | 0.50 | 1.02 | .020 | .040 |
| N | SEE VARIATIONS | | SEE VARIATIONS | |
| a | 0° | 8° | 0° | 8° |

VARIATIONS

| N | D mm. | | D (inch) | |
|---|---|---|---|---|
| | MIN | MAX | MIN | MAX |
| 56 | 18.31 | 18.55 | .720 | .730 |

Reference Doc.: JEDEC Publication 95, MO-118

10-0034

# Ordering Information

**ICS932S422CFLF-T**

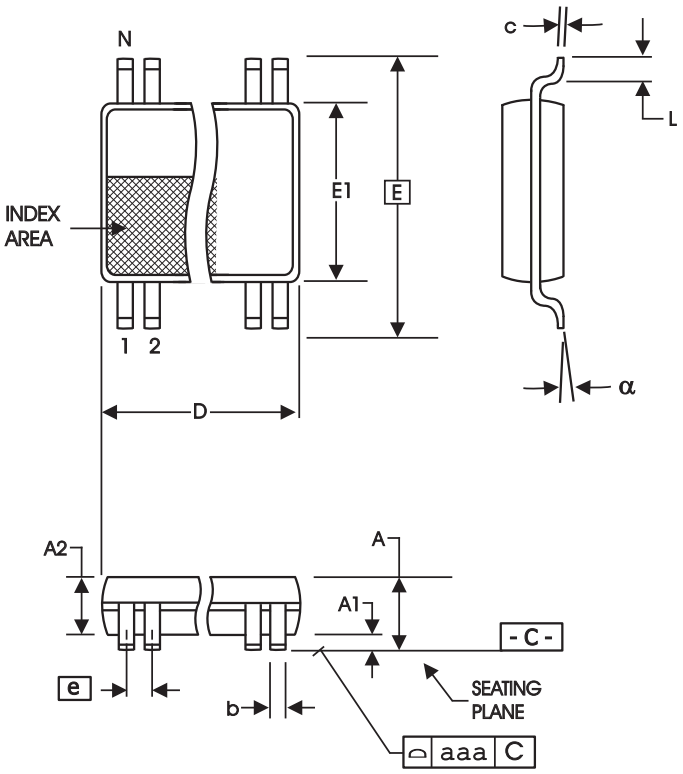
Example:

**ICS XXXX C F LF- T**

- **Designation for tape and reel packaging**
- **Annealed Lead Free (optional)**
- **Package Type**
  F = SSOP
- **Revision Designator** (will not correlate with datasheet revision)
- **Device Type**
- **Prefix**
  ICS = Standard Device

1412A—12/10/07

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**56-Lead 6.10 mm. Body, 0.50 mm. Pitch TSSOP**
**(240 mil) (20 mil)**

| SYMBOL | In Millimeters COMMON DIMENSIONS | | In Inches COMMON DIMENSIONS | |
|---|---|---|---|---|
| | MIN | MAX | MIN | MAX |
| A | -- | 1.20 | -- | .047 |
| A1 | 0.05 | 0.15 | .002 | .006 |
| A2 | 0.80 | 1.05 | .032 | .041 |
| b | 0.17 | 0.27 | .007 | .011 |
| c | 0.09 | 0.20 | .0035 | .008 |
| D | SEE VARIATIONS | | SEE VARIATIONS | |
| E | 8.10 BASIC | | 0.319 BASIC | |
| E1 | 6.00 | 6.20 | .236 | .244 |
| e | 0.50 BASIC | | 0.020 BASIC | |
| L | 0.45 | 0.75 | .018 | .030 |
| N | SEE VARIATIONS | | SEE VARIATIONS | |
| a | 0° | 8° | 0° | 8° |
| aaa | -- | 0.10 | -- | .004 |

VARIATIONS

| N | D mm. | | D (inch) | |
|---|---|---|---|---|
| | MIN | MAX | MIN | MAX |
| 56 | 13.90 | 14.10 | .547 | .555 |

Reference Doc.: JEDEC Publication 95, MO-153

10-0039

# Ordering Information

**ICS932S422CGLF-T**

Example:

**ICS XXXX C G LF- T**

- **Designation for tape and reel packaging**
- **Annealed Lead Free (optional)**
- **Package Type**
  G = TSSOP
- **Revision Designator** (will not correlate with datasheet revision)
- **Device Type**
- **Prefix**
  ICS = Standard Device

1412A—12/10/07

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## Revision History

| Rev. | Issue Date | Description | Page # |
|---|---|---|---|
| A | 12/10/07 | Initial Release | - |
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