Low Power Clock Chip for Serverworks HT2400 Servers

Recommended Application:

Serverworks HT2400-based systems using AMD Opteron processors

Output Features:

- 7 - Pairs of AMD Low Power K8 Greyhound compliant clocks
- 7 - Pair of SRC/PCI Express* Gen 2 clocks
- 3 - 14.318 MHz REF clocks including 1 free-running
- 2 - 48MHz clocks
- 2 - PCI 33 MHz clocks
- 2 - 25MHz clocks

Features:

- Spread Spectrum for EMI reduction
- Outputs may be disabled via SMBus
- M/N programming via SMBus
- PCIe clocks meet PCIe Gen 2.
- Low Power differential outputs

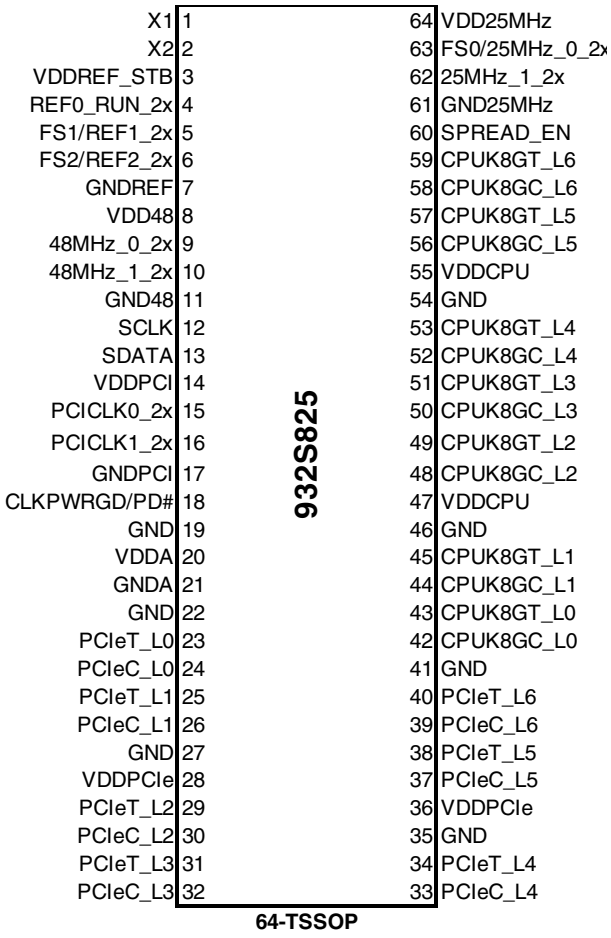
Functionality

FS2	FS1	FS0	CPU (MHz)
0	0	0	Hi-Z
0	0	1	X/6
0	1	0	180.00
0	1	1	220.00
1	0	0	100.00
1	0	1	133.33
1	1	0	Reserved
1	1	1	200.00

Power Groups

Pin Number		Description
VDD	GND	
8	11	48MHz Clocks
64	61	25MHz Clocks
14	17	33 MHz PCI Clocks
20	21	Analog Core
36, 28	35, 27	PCIe clocks
55, 47	54, 46	K8G CPU Clocks
3	7	REF Clocks, Xtal Osc.

Pin Configuration



64-TSSOP

*Other names and brands may be claimed as the property of others.

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Pin Description

PIN #	PIN NAME	TYPE	DESCRIPTION
1	X1	IN	Crystal input, Nominally 14.318MHz.
2	X2	OUT	Crystal output, Nominally 14.318MHz
3	VDDREF_STB	PWR	Ref, XTAL power supply, nominal 3.3V standby power
4	REF0_RUN_2x	OUT	14.318MHz Free Running XTAL Output. This output runs as long as standby VDD is applied to the part. Default drive is 2 loads.
5	FS1/REF1_2x	I/O	Frequency select latch input pin / 14.318 MHz reference clock. Default 2 load drive.
6	FS2/REF2_2x	I/O	Frequency select latch input pin / 14.318 MHz reference clock. Default 2 load drive.
7	GNDREF	PWR	Ground pin for the REF outputs.
8	VDD48	PWR	Power pin for the 48MHz output.3.3V
9	48MHz_0_2x	OUT	48MHz clock output. Default 2 load drive strength
10	48MHz_1_2x	OUT	48MHz clock output. Default 2 load drive strength
11	GND48	PWR	Ground pin for the 48MHz outputs
12	SCLK	IN	Clock pin of SMBus circuitry, 5V tolerant.
13	SDATA	I/O	Data pin for SMBus circuitry, 3.3V tolerant.
14	VDDPCI	PWR	Power supply for PCI clocks, nominal 3.3V
15	PCICLK0_2x	OUT	3.3V PCI clock output. Default 2 load drive strength.
16	PCICLK1_2x	OUT	3.3V PCI clock output. Default 2 load drive strength.
17	GNDPCI	PWR	Ground pin for the PCI outputs
18	CLKPWRGD/PD#	IN	This 3.3V LVTTL input is a level sensitive strobe used to determine when latch inputs are valid and are ready to be sampled. This is an active high input. / Asynchronous active low input pin used to power down the device into a low power state.
19	GND	PWR	Ground pin.
20	VDDA	PWR	3.3V power for the PLL core.
21	GNDA	PWR	Ground pin for the PLL core.
22	GND	PWR	Ground pin.
23	PCIeT_L0	OUT	True clock of 0.8V differential push-pull PCI_Express pair (no 50ohm resistor to GND needed)
24	PCIeC_L0	OUT	Complement clock of 0.8V differential push-pull PCI_Express pair. (no 50ohm resistor to GND needed)
25	PCIeT_L1	OUT	True clock of 0.8V differential push-pull PCI_Express pair (no 50ohm resistor to GND needed)
26	PCIeC_L1	OUT	Complement clock of 0.8V differential push-pull PCI_Express pair. (no 50ohm resistor to GND needed)
27	GND	PWR	Ground pin.
28	VDDPCIe	PWR	Power supply for PCI Express clocks, nominal 3.3V
29	PCIeT_L2	OUT	True clock of 0.8V differential push-pull PCI_Express pair (no 50ohm resistor to GND needed)
30	PCIeC_L2	OUT	Complement clock of 0.8V differential push-pull PCI_Express pair. (no 50ohm resistor to GND needed)
31	PCIeT_L3	OUT	True clock of 0.8V differential push-pull PCI_Express pair (no 50ohm resistor to GND needed)
32	PCIeC_L3	OUT	Complement clock of 0.8V differential push-pull PCI_Express pair. (no 50ohm resistor to GND needed)

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Pin Description (continued)

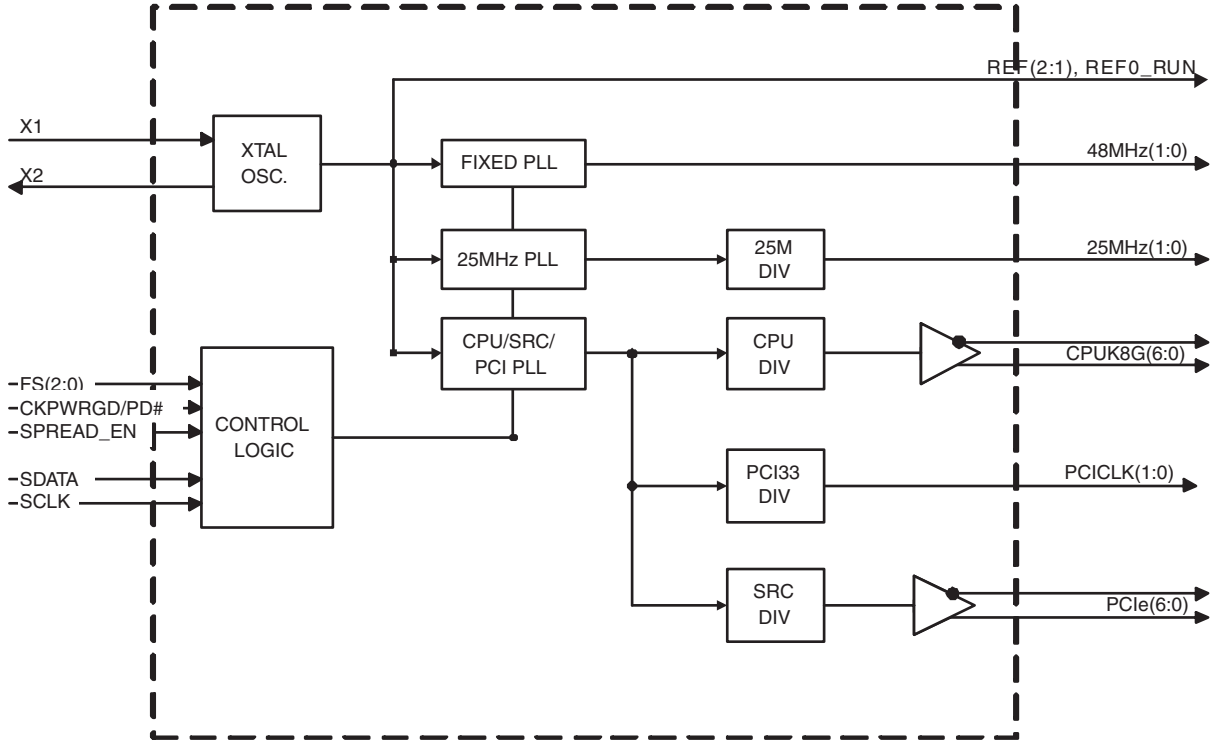
PIN #	PIN NAME	TYPE	DESCRIPTION
33	PCIeC_L4	OUT	Complement clock of 0.8V differential push-pull PCI_Express pair. (no 50ohm resistor to GND needed)
34	PCIeT_L4	OUT	True clock of 0.8V differential push-pull PCI_Express pair (no 50ohm resistor to GND needed)
35	GND	PWR	Ground pin.
36	VDDPCIe	PWR	Power supply for PCI Express clocks, nominal 3.3V
37	PCIeC_L5	OUT	Complement clock of 0.8V differential push-pull PCI_Express pair. (no 50ohm resistor to GND needed)
38	PCIeT_L5	OUT	True clock of 0.8V differential push-pull PCI_Express pair (no 50ohm resistor to GND needed)
39	PCIeC_L6	OUT	Complement clock of 0.8V differential push-pull PCI_Express pair. (no 50ohm resistor to GND needed)
40	PCIeT_L6	OUT	True clock of 0.8V differential push-pull PCI_Express pair (no 50ohm resistor to GND needed)
41	GND	PWR	Ground pin.
42	CPUK8GC_L0	OUT	Complementary signal of low-power differential push-pull AMD K8 "Greyhound" clock
43	CPUK8GT_L0	OUT	True signal of low-power differential push-pull AMD K8 "Greyhound" clock
44	CPUK8GC_L1	OUT	Complementary signal of low-power differential push-pull AMD K8 "Greyhound" clock
45	CPUK8GT_L1	OUT	True signal of low-power differential push-pull AMD K8 "Greyhound" clock
46	GND	PWR	Ground pin.
47	VDDCPU	PWR	Supply for CPU clocks, 3.3V nominal
48	CPUK8GC_L2	OUT	Complementary signal of low-power differential push-pull AMD K8 "Greyhound" clock
49	CPUK8GT_L2	OUT	True signal of low-power differential push-pull AMD K8 "Greyhound" clock
50	CPUK8GC_L3	OUT	Complementary signal of low-power differential push-pull AMD K8 "Greyhound" clock
51	CPUK8GT_L3	OUT	True signal of low-power differential push-pull AMD K8 "Greyhound" clock
52	CPUK8GC_L4	OUT	Complementary signal of low-power differential push-pull AMD K8 "Greyhound" clock
53	CPUK8GT_L4	OUT	True signal of low-power differential push-pull AMD K8 "Greyhound" clock
54	GND	PWR	Ground pin.
55	VDDCPU	PWR	Supply for CPU clocks, 3.3V nominal
56	CPUK8GC_L5	OUT	Complementary signal of low-power differential push-pull AMD K8 "Greyhound" clock
57	CPUK8GT_L5	OUT	True signal of low-power differential push-pull AMD K8 "Greyhound" clock
58	CPUK8GC_L6	OUT	Complementary signal of low-power differential push-pull AMD K8 "Greyhound" clock
59	CPUK8GT_L6	OUT	True signal of low-power differential push-pull AMD K8 "Greyhound" clock
60	SPREAD_EN	IN	Asynchronous, active high input to enable spread spectrum functionality.
61	GND25MHz	PWR	Ground pin for the 25Mhz outputs
62	25MHz_1_2x	OUT	25MHz clock output, 3.3V. Default 2 load drive
63	FS0/25MHz_0_2x	I/O	Frequency select latch input pin / Fixed 25MHz 3.3V clock output. Default 2 load drive
64	VDD25MHz	PWR	Power supply for 25MHz clocks, 3.3V nominal.

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General Description

The **ICS932S825** is a main clock synthesizer chip that all clocks required by Serverworks HT2400-based servers. An SMBus interface allows full control of the device.

Block Diagram



Single-ended Terminations (All Single-Ended Outputs)

Single-ended Output Strength	Number of Loads on Board	Series Resistor for Proper Termination Zo = 50 ohms
1 Load	1	33
2 Load (Default)	1	39
	2	22

Differential Terminations

Differential Output	Number of Loads on Board	Series Resistor for Proper Termination Zo = 50 ohms
CPUK8Gx	1	33
PCIe_Lx	1	33

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Frequency Selection Table

Byte 0									
Bit 4 SS_EN	**Bit 3 FS3**	**Bit2 FS2**	**Bit1 FS1**	**Bit0 FS0**	**CPU (MHz)**	**SRC (MHz)**	**PCI (MHz)**	**Spread %**	**OverClock Amount**
0	0	0	0	0	Hi-Z	Hi-Z	Hi-Z	N/A	N/A
0	0	0	0	1	X/4	X/8	x/24	N/A	N/A
0	0	0	1	0	180.00	90.00	30.00	0	0.90
0	0	0	1	1	220.00	110.00	36.67	0	1.10
0	0	1	0	0	100.00	100.00	33.33	0	1.00
0	0	1	0	1	133.33	100.00	33.33	0	1.00
0	0	1	1	0	Reserved				
0	0	1	1	1	200.00	100.00	33.33	0	1.00
0	1	0	0	0	184.00	92.00	30.67	0	0.92
0	1	0	0	1	188.00	94.00	31.33	0	0.94
0	1	0	1	0	192.00	96.00	32.00	0	0.96
0	1	0	1	1	196.00	98.00	32.67	0	0.98
0	1	1	0	0	204.00	102.00	34.00	0	1.02
0	1	1	0	1	208.00	104.00	34.67	0	1.04
0	1	1	1	0	212.00	106.00	35.33	0	1.06
0	1	1	1	1	216.00	108.00	36.00	0	1.08
1	0	0	0	0	Hi-Z	Hi-Z	Hi-Z	N/A	N/A
1	0	0	0	1	X/4	X/8	x/24	N/A	N/A
1	0	0	1	0	180.00	90.00	30.00	-0.5%	1.00
1	0	0	1	1	220.00	110.00	36.67	-0.5%	1.00
1	0	1	0	0	100.00	100.00	33.33	-0.5%	1.00
1	0	1	0	1	133.33	100.00	33.33	-0.5%	1.00
1	0	1	1	0	Reserved				
1	0	1	1	1	200.00	100.00	33.33	-0.5%	1.00
1	1	0	0	0	184.00	92.00	30.67	-0.5%	0.92
1	1	0	0	1	188.00	94.00	31.33	-0.5%	0.94
1	1	0	1	0	192.00	96.00	32.00	-0.5%	0.96
1	1	0	1	1	196.00	98.00	32.67	-0.5%	0.98
1	1	1	0	0	204.00	102.00	34.00	-0.5%	1.02
1	1	1	0	1	208.00	104.00	34.67	-0.5%	1.04
1	1	1	1	0	212.00	106.00	35.33	-0.5%	1.06
1	1	1	1	1	216.00	108.00	36.00	-0.5%	1.08

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CPU Divider Ratios

	Divider (3:2)								
Divider (1:0)	**Bit**	**00**		**01**		**10**		**11**	**MSB**
	00	0000	**2**	0100	**4**	1000	**8**	1100	**16**
	01	0001	**3**	0101	**6**	1001	**12**	1101	**24**
	10	0010	**5**	0110	**10**	1010	**20**	1110	**40**
	11	0011	**15**	0111	**30**	1011	**60**	1111	**120**
	LSB	Address	Div	Address	Div	Address	Div	Address	Div

PCI Divider Ratios

	Divider (3:2)								
Divider (1:0)	**Bit**	**00**		**01**		**10**		**11**	**MSB**
	00	0000	**4**	0100	**8**	1000	**16**	1100	**32**
	01	0001	**3**	0101	**6**	1001	**12**	1101	**24**
	10	0010	**5**	0110	**10**	1010	**20**	1110	**40**
	11	0011	**15**	0111	**30**	1011	**60**	1111	**120**
	LSB	Address	Div	Address	Div	Address	Div	Address	Div

SRC Divider Ratios

	Divider (3:2)								
Divider (1:0)	**Bit**	**00**		**01**		**10**		**11**	**MSB**
	00	0000	**2**	0100	**4**	1000	**8**	1100	**16**
	01	0001	**3**	0101	**6**	1001	**12**	1101	**24**
	10	0010	**5**	0110	**10**	1010	**20**	1110	**40**
	11	0011	**7**	0111	**14**	1011	**28**	1111	**56**
	LSB	Address	Div	Address	Div	Address	Div	Address	Div

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Absolute Maximum Ratings

Parameter	Symbol	Min	Max	Units	Notes
3.3V Core Supply Voltage	VDDA		GND + 4.5V	V	1
3.3V Logic Input Supply Voltage	VDD		GND +4.5V	V	1
Storage Temperature	Ts	-50	150	°C	
Ambient Operating Temp	Tambient	0	70	°C	
Input ESD protection human body model	ESD prot	2000		V	1

[1]Operation at these extremes is neither implied nor guaranteed

Electrical Characteristics - Input/Supply/Common Output Parameters

T_A = 0 - 70°C; Supply Voltage V_{DD} = 3.3 V +/-5%

PARAMETER	SYMBOL	Conditions	MIN	TYP	MAX	UNITS	NOTES
Input High Voltage	V_{IH}		2		V_{DD} + 0.3	V	1
Input Low Voltage	V_{IL}		V_{SS} - 0.3		0.8	V	1
Input High Current	I_{IH}	V_{IN} = V_{DD}	-5		5	uA	1
Input Low Current	I_{IL1}	V_{IN} = 0 V; Inputs with no pull-up resistors	-5			uA	1
	I_{IL2}	V_{IN} = 0 V; Inputs with pull-up resistors	-200			uA	1
Operating Current	$I_{DD3.3OP}$	all outputs driven			250	mA	
Powerdown Current	$I_{DD3.3PD}$	all diff pairs Low/Low			15	mA	
Input Frequency[3]	F_i	V_{DD} = 3.3 V		14.318		MHz	3
Pin Inductance[1]	L_{pin}				7	nH	1
Input Capacitance[1]	C_{IN}	Logic Inputs			5	pF	1
	C_{OUT}	Output pin capacitance			6	pF	1
	C_{INX}	X1 & X2 pins			5	pF	1
Clk Stabilization[1,2]	T_{STAB}	From V_{DD} Power-Up or de-assertion of PD# to 1st clock			3	ms	1,2
Modulation Frequency		Triangular Modulation	30		33	kHz	1
SMBus Voltage	V_{DD}		2.7		5.5	V	1
Low-level Output Voltage	V_{OL}	@ I_{PULLUP}			0.4	V	1
Current sinking at V_{OL} = 0.4 V	I_{PULLUP}		4			mA	1
SCLK/SDATA Clock/Data Rise Time[3]	T_{RI2C}	(Max VIL - 0.15) to (Min VIH + 0.15)			1000	ns	1
SCLK/SDATA Clock/Data Fall Time[3]	T_{FI2C}	(Min VIH + 0.15) to (Max VIL - 0.15)			300	ns	1

[1]Guaranteed by design and characterization, not 100% tested in production.

[2]See timing diagrams for timing requirements.

[3] Input frequency should be measured at the REFOUT pin and tuned to ideal 14.31818MHz to meet ppm frequency accuracy on PLL outputs.

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AC Electrical Characteristics - Low Power Differential PCIe Outputs

T_A = 0 - 70°C; V_{DD} = 3.3 V +/-5%; C_L =2pF, R_S=33.2Ω

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	NOTES
Rising Edge Slew Rate	t_{SLR}	Differential Measurement	0.5		2	V/ns	1,2
Falling Edge Slew Rate	t_{FLR}	Differential Measurement	0.5		2	V/ns	1,2
Slew Rate Variation	t_{SLVAR}	Single-ended Measurement			20	%	1
Maximum Output Voltage	V_{HIGH}	Includes overshoot			1150	mV	1
Minimum Output Voltage	V_{LOW}	Includes undershoot	-300			mV	1
Differential Voltage Swing	V_{SWING}	Differential Measurement	400			mV	1
Crossing Point Voltage	V_{XABS}	Single-ended Measurement	300		550	mV	1,3,4
Crossing Point Variation	$V_{XABSVAR}$	Single-ended Measurement			140	mV	1,3,5
Duty Cycle	D_{CYC}	Differential Measurement	45		55	%	1
PCIe Jitter - Cycle to Cycle	$PCIeJ_{C2C}$	Differential Measurement			125	ps	1
PCIe[6:0] Skew	$PCIe_{SKEW}$	Differential Measurement			250	ps	1

Notes on Electrical Characteristics:

[1]Guaranteed by design and characterization, not 100% tested in production.

[2] Slew rate measured through Vswing centered around differential zero

[3] Vxabs is defined as the voltage where CLK = CLK#

[4] Only applies to the differential rising edge (CLK rising and CLK# falling)

[5] Defined as the total variation of all crossing voltages of CLK rising and CLK# falling.

[6] All Long Term Accuracy and Clock Period specifications are guaranteed assuming that REFOUT is at 14.31818MHz

PCIe Phase Jitter Impact

Parameter		Conditions	Min	Typical	Max	Units	Notes
Output phase jitter impact – PCIe* Gen1	θ_{PCIe1}	(including PLL BW 1.5-22 MHz, z = 0.54, Td=10 ns, Ftrk=1.5 MHz)	0		108	ps	1,2,3,4
Output phase jitter impact - PCIe Gen2	θ_{PCIe2}	(including PLL BW5-16 MHz, 8 – 16 MHz, z = 0.54, Td=10 ns)	0		3.1	ps RMS	1,2,3,4

NOTES:

1. Post processed evaluation through Intel supplied Matlab scripts.
2. PCIe* Gen2 filter characteristics are subject to final ratification by PC ISIG. Please check the PCI* SIG for the latest specification.
3. These jitter numbers are defined for a BER of 1E-12. Measured numbers at a smaller sample size have to be extrapolated to this BER target.
4. Guaranteed by design and characterization, not 100% tested in production.

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AC Electrical Characteristics - Low Power Differential CPU Outputs

T_A = 0 - 70°C; V_{DD} = 3.3 V +/-5%; C_L =AMD64 Processor Test Load

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	NOTES
Crossing Point Variation	ΔV_{CROSS}	Single-ended Measurement			140	mV	1
Frequency	f		198.8		200	MHz	2
Long Term Accuracy	ppm		-300		300	ppm	3
Rising Edge Slew Rate	t_{SLR}	Differential Measurement	0.5		10	V/ns	4,5
Falling Edge Slew Rate	t_{FLR}	Differential Measurement	0.5		10	V/ns	4,5
CPU Jitter - Cycle to Cycle	$CPUJ_{C2C}$	Differential Measurement			150	ps	6
CPU Jitter - Accumulated	$CPUJ_{ACC}$	Over a 10 uS period	-1		1	ns	7
Maximum Output Voltage	V_{HIGH}	Includes overshoot, single-ended measurement			1150	mV	1
Minimum Output Voltage	V_{LOW}	Includes undershoot, single-ended measurement	-300			mV	1
Differential Voltage Swing Peak-to-Peak	V_{DPK-PK}	Differential Measurement	400		2400	mV	8
Differential Voltage	V_D	Differential Measurement	200		1200	mV	9
Change in V_D DC cycle-to-cycle	ΔV_D	Single-ended Measurement	-75		75	mV	10
Duty Cycle	D_{CYC}	Differential Measurement	45		55	%	11
CPU[6:0] Skew	CPU_{SKEW10}	Differential Measurement			250	ps	

Notes on Electrical Characteristics (Guaranteed by design and characterization, not 100% tested in production):

[1]Single-ended measurement at crossing point. Value is max-min over all time. DC value of common mode is not important due to the blocking cap.

[2] Minimum frequency results from 0.5% down spread.

[3] Measured with spread spectrum off.

[4] This parameter is intended to give guidance for simulation.

[5] Differential measurement through the range of +/-100mV

[6] Between any two adjacent cycles.

[7] Accumulated over a 10 uS time periode, measured with JIT2 TIE at 50ps interval.

[8] V_{DPK-PK} is the overall magnitude of the differential signal.

[9] V_{DMIN} is the amplitude of the ring-back differential measurement, guaranteed by design, that ring-back will not cross 0V V_D. V_{DMAX} is the largest amplitude allowed.

[10] The difference in magnitude of two adjacent V_{DDC} measurements. V_{DDC} is the stable post overshoot and ring-back part

[11] Defined as tHIGH/tCYCLE

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Electrical Characteristics - 33 MHz PCICLK, 25MHz Outputs

T_A = 0 - 70°C; VDD=3.3V +/-5%; C_L = 5 pF (unless otherwise specified)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	Notes
PCI Long Accuracy	ppm	see Tperiod min-max values	-300		300	ppm	1,2
PCI Clock period	T_{period}	33.33MHz output nominal	29.9910		30.0090	ns	2
		33.33MHz output spread	29.9910		30.1598	ns	2
25MHz Long Accuracy	ppm	see Tperiod min-max values	-50		50	ns	2
25MHz Clock period	T_{period}	25MHz output nominal		40		ns	2
Output High Voltage	V_{OH}	I_{OH} = -1 mA	2.4			V	1
Output Low Voltage	V_{OL}	I_{OL} = 1 mA			0.55	V	1
Output High Current	I_{OH}	V_{OH} @MIN = 1.0 V	-33			mA	1
		V_{OH}@ MAX = 3.135 V			-33	mA	1
Output Low Current	I_{OL}	V_{OL} @ MIN = 1.95 V	30			mA	1
		V_{OL} @ MAX = 0.4 V			38	mA	1
Edge Rate	δV/δt	Rising edge rate	1		4	V/ns	1
Edge Rate	δV/δt	Falling edge rate	1		4	V/ns	1
Duty Cycle	d_{t1}	V_T = 1.5 V	45		55	%	1
PCI Skew	t_{sk1}	V_T = 1.5 V			250	ps	1
25MHz Skew	t_{sk1}	V_T = 1.5 V			250	ps	1
Jitter, Cycle to cycle	$t_{jcyc-cyc}$	V_T = 1.5 V			250	ps	1

[1]Guaranteed by design and characterization, not 100% tested in production.

[2] All Long Term Accuracy and Clock Period specifications are guaranteed assuming that REF is at 14.31818MHz

Electrical Characteristics - 48MHz

T_A = 0 - 70°C; V_{DD} = 3.3 V +/-5%; C_L = 5 pF (unless otherwise specified)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	Notes
Long Accuracy	ppm	see Tperiod min-max values	-100		100	ppm	1,2
Clock period	T_{period}	48.00MHz output nominal	20.8257		20.8340	ns	2
Output High Voltage	V_{OH}	I_{OH} = -1 mA	2.4			V	1
Output Low Voltage	V_{OL}	I_{OL} = 1 mA			0.55	V	1
Output High Current	I_{OH}	V_{OH} @ MIN = 1.0 V	-33			mA	1
		V_{OH}@ MAX = 3.135 V			-33	mA	1
Output Low Current	I_{OL}	V_{OL} @MIN = 1.95 V	30			mA	1
		V_{OL} @ MAX = 0.4 V			38	mA	1
Edge Rate	δV/δt	Rising edge rate	1		2	V/ns	1
Edge Rate	δV/δt	Falling edge rate	1		2	V/ns	1
Duty Cycle	d_{t1}	V_T = 1.5 V	45		55	%	1
Group Skew	t_{sk1}	V_T = 1.5 V			250	ps	1
Jitter, Cycle to cycle	$t_{jcyc-cyc}$	V_T = 1.5 V			250	ps	1

[1]Guaranteed by design and characterization, not 100% tested in production.

[2] All Long Term Accuracy and Clock Period specifications are guaranteed assuming that REF is at 14.31818MHz

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Electrical Characteristics - REF-14.318MHz

T_A = 0 - 70°C; V_{DD} = 3.3 V +/-5%; C_L = 5 pF (unless otherwise specified)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	Notes
Long Accuracy	ppm	see Tperiod min-max values	-300		300	ppm	1
Clock period	T_{period}	14.318MHz output nominal	69.8270		69.8550	ns	2
Output High Voltage	V_{OH}	I_{OH} = -1 mA	2.4			V	1
Output Low Voltage	V_{OL}	I_{OL} = 1 mA			0.4	V	1
Output High Current	I_{OH}	V_{OH}@MIN = 1.0 V, V_{OH}@MAX = 3.135 V	-29		-23	mA	1
Output Low Current	I_{OL}	V_{OL}@MIN = 1.95 V, V_{OL}@MAX = 0.4 V	29		27	mA	1
Edge Rate	δV/δt	Rising edge rate	1		2	V/ns	1
Edge Rate	δV/δt	Falling edge rate	1		2	V/ns	1
Skew	t_{sk1}	V_T = 1.5 V			500	ps	1
Duty Cycle	d_{t1}	V_T = 1.5 V	45		55	%	1
Jitter, Cycle to cycle	$t_{jcyc-cyc}$	V_T = 1.5 V			1000	ps	1

[1]Guaranteed by design and characterization, not 100% tested in production.

[2] All Long Term Accuracy and Clock Period specifications are guaranteed assuming that REF is at 14.31818MHz

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General SMBus serial interface information

How to Write:

- Controller (host) sends a start bit.
- Controller (host) sends the write address D2 (h)
- ICS clock will ***acknowledge***
- Controller (host) sends the begining byte location = N
- ICS clock will ***acknowledge***
- Controller (host) sends the data byte count = X
- ICS clock will ***acknowledge***
- Controller (host) starts sending ***Byte N through Byte N + X -1***
- ICS clock will ***acknowledge*** each byte ***one at a time***
- Controller (host) sends a Stop bit

How to Read:

- Controller (host) will send start bit.
- Controller (host) sends the write address D2 (h)
- ICS clock will ***acknowledge***
- Controller (host) sends the begining byte location = N
- ICS clock will ***acknowledge***
- Controller (host) will send a separate start bit.
- Controller (host) sends the read address D3 (h)
- ICS clock will ***acknowledge***
- ICS clock will send the data byte count = X
- ICS clock sends ***Byte N + X -1***
- ICS clock sends ***Byte 0 through byte X (if X (h) was written to byte 8)***.
- Controller (host) will need to acknowledge each byte
- Controllor (host) will send a not acknowledge bit
- Controller (host) will send a stop bit

Index Block Write Operation

Controller (Host)			ICS (Slave/Receiver)
T	starT bit		
Slave Address D2(h)			
WR	WRite		
			ACK
Beginning Byte = N			
			ACK
Data Byte Count = X			
			ACK
Beginning Byte N		X Byte	
			ACK
○			
○			○
○			○
			○
Byte N + X - 1			
			ACK
P	stoP bit		

Index Block Read Operation

Controller (Host)			ICS (Slave/Receiver)
T	starT bit		
Slave Address D2(h)			
WR	WRite		
			ACK
Beginning Byte = N			
			ACK
RT	Repeat starT		
Slave Address D3(h)			
RD	ReaD		
			ACK
			Data Byte Count = X
ACK			
		X Byte	Beginning Byte N
ACK			
			○
○			○
○			○
○			
			Byte N + X - 1
N	Not acknowledge		
P	stoP bit		

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SMBus Table: Frequency Select and Spread Control Register

Byte 0	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	-	Reserved	Reserved	RW	Reserved	Reserved	0
Bit 6	-	Reserved	Reserved	RW	Reserved	Reserved	0
Bit 5	-	Reserved	Reserved	RW	Reserved	Reserved	0
Bit 4	-	SS_EN	Spread Spectrum Enable	RW	See CPU Frequency Select Table		Latched
Bit 3	-	FS3	Freq Select Bit 3	RW			0
Bit 2	-	FS2	Freq Select Bit 2	RW			Latched
Bit 1	-	FS1	Freq Select Bit 1	RW			Latched
Bit 0	-	FS0	Freq Select Bit 0	RW			Latched

SMBus Table: Output Control Register

Byte 1	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	6	REF2	Output Enable	RW	Hi-Z	Enable	1
Bit 6	5	REF1	Output Enable	RW	Hi-Z	Enable	1
Bit 5	4	REF0_RUN	Output Enable	RW	Disable (Low)	Enable	1
Bit 4	17	PCICLK1	Output Enable	RW	Disable (Low)	Enable	1
Bit 3	16	PCICLK0	Output Enable	RW	Disable (Low)	Enable	1
Bit 2	-	Reserved	Reserved	RW	Reserved	Reserved	1
Bit 1	10	48MHz_1	Output Enable	RW	Disable (Low)	Enable	1
Bit 0	9	48MHz_0	Output Enable	RW	Disable (Low)	Enable	1

SMBus Table: Output Control Register

Byte 2	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	-	Reserved	Reserved	RW	Reserved	Reserved	0
Bit 6	59/58	CPUK8G_L(6)	Output Enable When Disabled CPUK8GT_L = 0 CPUK8GC_L = 0	RW	Disable	Enable	1
Bit 5	57/56	CPUK8G_L(5)		RW	Disable	Enable	1
Bit 4	53/52	CPUK8G_L(4)		RW	Disable	Enable	1
Bit 3	51/50	CPUK8G_L(3)		RW	Disable	Enable	1
Bit 2	47/46	CPUK8G_L(2)		RW	Disable	Enable	1
Bit 1	45/44	CPUK8G_L(1)		RW	Disable	Enable	1
Bit 0	43/42	CPUK8G_L(0)		RW	Disable	Enable	1

SMBus Table: Output Control Register

Byte 3	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	-	Reserved	Reserved	RW	Reserved	Reserved	0
Bit 6	40/39	PCIe_L6	Output Enable When Disabled PCIeT_L = 0 PCIeC_L = 0	RW	Disable	Enable	1
Bit 5	38/37	PCIe_L5		RW	Disable	Enable	1
Bit 4	33/34	PCIe_L4		RW	Disable	Enable	1
Bit 3	31/32	PCIe_L3		RW	Disable	Enable	1
Bit 2	29/30	PCIe_L2		RW	Disable	Enable	1
Bit 1	25/26	PCIe_L1		RW	Disable	Enable	1
Bit 0	23/24	PCIe_L0		RW	Disable	Enable	1

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SMBus Table: Drive Strength Control Register

Byte 4	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	6	REF2	Drive Strength Select	RW	1 Load	2 Loads	1
Bit 6	5	REF1	Drive Strength Select	RW	1 Load	2 Loads	1
Bit 5	4	REF0_RUN	Drive Strength Select	RW	1 Load	2 Loads	1
Bit 4	17	PCICLK1	Drive Strength Select	RW	1 Load	2 Loads	1
Bit 3	16	PCICLK0	Drive Strength Select	RW	1 Load	2 Loads	1
Bit 2	11	48MHz_2	Drive Strength Select	RW	1 Load	2 Loads	1
Bit 1	10	48MHz_1	Drive Strength Select	RW	1 Load	2 Loads	1
Bit 0	9	48MHz_0	Drive Strength Select	RW	1 Load	2 Loads	1

SMBus Table: Drive Strength Control Register

Byte 5	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	62	25MHz_1	Output Enable	RW	Low	Enable	1
Bit 6	63	25MHz_0	Output Enable	RW	Hi-Z	Enable	1
Bit 5	62	25MHz_1	Drive Strength Select	RW	1 Load	2 Loads	1
Bit 4	63	25MHz_0	Drive Strength Select	RW	1 Load	2 Loads	1
Bit 3	-	Reserved	Reserved	RW	Reserved	Reserved	0
Bit 2	-	VDIFF2	VDIFF MSB	RW	See VDIFF Select Table		1
Bit 1	-	VDIFF1	VDIFF Select Bit 0	RW			0
Bit 0	-	VDIFF0	VDIFF LSB	RW			1

SMBus Table: Device ID Register

Byte 6	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	-	DevID 7	Device ID MSB	R	-	-	0
Bit 6	-	DevID 6	Device ID 6	R	-	-	0
Bit 5	-	DevID 5	Device ID 5	R	-	-	1
Bit 4	-	DevID 4	Device ID4	R	-	-	0
Bit 3	-	DevID 3	Device ID3	R	-	-	0
Bit 2	-	DevID 2	Device ID2	R	-	-	1
Bit 1	-	DevID 1	Device ID1	R	-	-	0
Bit 0	-	DevID 0	Device ID LSB	R	-	-	1

SMBus Table: Vendor ID Register

Byte 7	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	-	RID3	Revision ID	R	-	-	0
Bit 6	-	RID2		R	-	-	0
Bit 5	-	RID1		R	-	-	0
Bit 4	-	RID0		R	-	-	1
Bit 3	-	VID3	VENDOR ID (0001 = ICS)	R	-	-	0
Bit 2	-	VID2		R	-	-	0
Bit 1	-	VID1		R	-	-	0
Bit 0	-	VID0		R	-	-	1

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SMBus Table: Byte Count Register

Byte 8	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	-	BC7	Byte Count Programming b(7:0)	RW	Writing to this register will configure how many bytes will be read back, default is 9 bytes.		0
Bit 6	-	BC6		RW			0
Bit 5	-	BC5		RW			0
Bit 4	-	BC4		RW			0
Bit 3	-	BC3		RW			1
Bit 2	-	BC2		RW			0
Bit 1	-	BC1		RW			0
Bit 0	-	BC0		RW			1

SMBus Table: Reserved Register

Byte 9	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	-	Reserved	Reserved	RW	Reserved	Reserved	0
Bit 6	-	Reserved	Reserved	RW	Reserved	Reserved	0
Bit 5	-	Reserved	Reserved	RW	Reserved	Reserved	0
Bit 4	-	Reserved	Reserved	RW	Reserved	Reserved	0
Bit 3	-	Reserved	Reserved	RW	Reserved	Reserved	0
Bit 2	-	Reserved	Reserved	RW	Reserved	Reserved	0
Bit 1	-	Reserved	Reserved	RW	Reserved	Reserved	0
Bit 0	-	Reserved	Reserved	RW	Reserved	Reserved	0

SMBus Table: M/N Programming Enable

Byte 10	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	-	M/N_EN	CPU PLL M/N Programming Enable	RW	Disable	Enable	0
Bit 6	-	Reserved	Reserved	RW	-	-	0
Bit 5	-	Reserved	Reserved	RW	-	-	0
Bit 4	-	Reserved	Reserved	RW	-	-	0
Bit 3	-	Reserved	Reserved	RW	-	-	0
Bit 2	-	Reserved	Reserved	RW	-	-	0
Bit 1	-	Reserved	Reserved	RW	-	-	0
Bit 0	-	Reserved	Reserved	RW	-	-	0

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Bytes 11:14 are Reserved Registers

SMBus Table: CPU Frequency Control Register

Byte 15	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	-	N Div8	N Divider Prog bit 8	RW	The decimal representation of M and N Divier in Byte 11 and 12 will configure the CPU VCO frequency. Default at power up = latch-in or Byte 0 Rom table. VCO Frequency = 14.318 x [NDiv(9:0)+8] / [MDiv(5:0)+2]		X
Bit 6	-	N Div9	N Divider Prog bit 9	RW			X
Bit 5	-	M Div5	M Divider Programming bit (5:0)	RW			X
Bit 4	-	M Div4		RW			X
Bit 3	-	M Div3		RW			X
Bit 2	-	M Div2		RW			X
Bit 1	-	M Div1		RW			X
Bit 0	-	M Div0		RW			X

SMBus Table: CPU Frequency Control Register

Byte 16	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	-	N Div7	N Divider Programming Byte12 bit(7:0) and Byte11 bit(7:6)	RW	The decimal representation of M and N Divier in Byte 11 and 12 will configure the CPU VCO frequency. Default at power up = latch-in or Byte 0 Rom table. VCO Frequency = 14.318 x [NDiv(9:0)+8] / [MDiv(5:0)+2]		X
Bit 6	-	N Div6		RW			X
Bit 5	-	N Div5		RW			X
Bit 4	-	N Div4		RW			X
Bit 3	-	N Div3		RW			X
Bit 2	-	N Div2		RW			X
Bit 1	-	N Div1		RW			X
Bit 0	-	N Div0		RW			X

SMBus Table: CPU Spread Spectrum Control Register

Byte 17	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	-	SSP7	Spread Spectrum Programming bit(7:0)	RW	These Spread Spectrum bits in Byte 13 and 14 will program the spread pecentage of CPU		X
Bit 6	-	SSP6		RW			X
Bit 5	-	SSP5		RW			X
Bit 4	-	SSP4		RW			X
Bit 3	-	SSP3		RW			X
Bit 2	-	SSP2		RW			X
Bit 1	-	SSP1		RW			X
Bit 0	-	SSP0		RW			X

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SMBus Table: CPU Spread Spectrum Control Register

Byte 18	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	-	Reserved	Reserved	R	-	-	0
Bit 6	-	SSP14	Spread Spectrum Programming bit(14:8)	RW	These Spread Spectrum bits in Byte 13 and 14 will program the spread pecentage of CPU		X
Bit 5	-	SSP13		RW			X
Bit 4	-	SSP12		RW			X
Bit 3	-	SSP11		RW			X
Bit 2	-	SSP10		RW			X
Bit 1	-	SSP9		RW			X
Bit 0	-	SSP8		RW			X

SMBus Table: Programmable Output Divider Register

Byte 19	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	-	CPUDiv3	CPU Divider Ratio Programming Bits	RW	See CPU Divider Ratios Table		X
Bit 6	-	CPUDiv2		RW			X
Bit 5	-	CPUDiv1		RW			X
Bit 4	-	CPUDiv0		RW			X
Bit 3	-	Reserved	Reserved	R	-	-	0
Bit 2	-	Reserved	Reserved	R	-	-	0
Bit 1	-	Reserved	Reserved	R	-	-	0
Bit 0	-	Reserved	Reserved	R	-	-	0

SMBus Table: Programmable Output Divider Register

Byte 20	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	-	33MHzDiv3	33MHz Divider Ratio Programming Bits	RW	33MHz Divider Ratio Table		X
Bit 6	-	33MHzDiv2		RW			X
Bit 5	-	33MHzDiv1		RW			X
Bit 4	-	33MHzDiv0		RW			X
Bit 3	-	SRC_Div3	SRC_ Divider Ratio Programming Bits	RW	SRC Divider Ratio Table		X
Bit 2	-	SRC_Div2		RW			X
Bit 1	-	SRC_Div1		RW			X
Bit 0	-	SRC_Div0		RW			X

SMBusTable: Reserved Regsiter

Byte 21 is reserved do not write this register!

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Shared Pin Operation - Input/Output Pins

The I/O pins designated by (input/output) on the **ICS932S825** serve as dual signal functions to the device. During initial power-up, they act as input pins. The logic level (voltage) that is present on these pins at this time is read and stored into a 5-bit internal data latch. At the end of Power-On reset, (see AC characteristics for timing values), the device changes the mode of operations for these pins to an output function. In this mode the pins produce the specified buffered clocks to external loads.

To program (load) the internal configuration register for these pins, a resistor is connected to either the VDD (logic 1) power supply or the GND (logic 0) voltage potential. A 10 Kilohm (10K) resistor is used to provide both the solid CMOS programming voltage needed during the power-up programming period and to provide an insignificant load on the output clock during the subsequent operating period.

Figure 1 shows a means of implementing this function when a switch or 2 pin header is used. With no jumper is installed the pin will be pulled high. With the jumper in place the pin will be pulled low. If programmability is not necessary, than only a single resistor is necessary. The programming resistors should be located close to the series termination resistor to minimize the current loop area. It is more important to locate the series termination resistor close to the driver than the programming resistor.

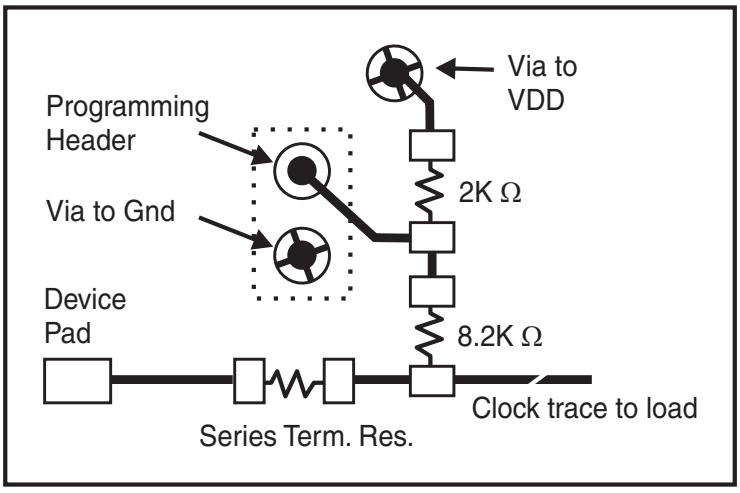
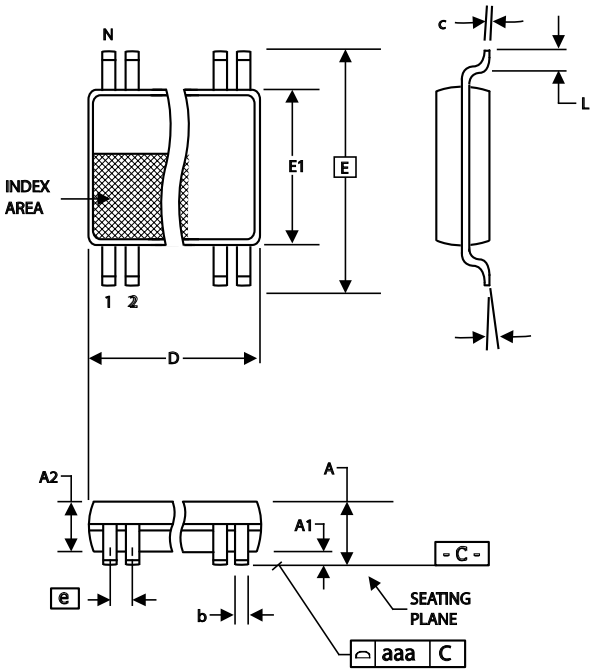


Fig. 1

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6.10 mm. Body, 0.50 mm. Pitch TSSOP
(240 mil) (20 mil)

SYMBOL	In Millimeters COMMON DIMENSIONS		In Inches COMMON DIMENSIONS	
	MIN	MAX	MIN	MAX
A	--	1.20	--	.047
A1	0.05	0.15	.002	.006
A2	0.80	1.05	.032	.041
b	0.17	0.27	.007	.011
c	0.09	0.20	.0035	.008
D	SEE VARIATIONS		SEE VARIATIONS	
E	8.10 BASIC		0.319 BASIC	
E1	6.00	6.20	.236	.244
e	0.50 BASIC		0.020 BASIC	
L	0.45	0.75	.018	.030
N	SEE VARIATIONS		SEE VARIATIONS	
α	0°	8°	0°	8°
aaa	--	0.10	--	.004

VARIATIONS

N	D mm.		D (inch)	
	MIN	MAX	MIN	MAX
64	16.90	17.10	.665	.673

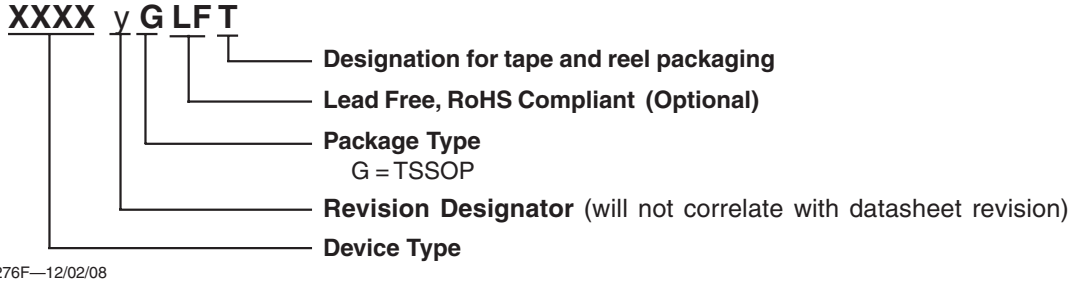
Reference Doc.: JEDEC Publication 95, MO-153

10-0039

Ordering Information

932S825yGLFT

Example:



1276F—12/02/08

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Revision History

Rev.	Issue Date	Description	Page #
A	2/28/2007	1. Updated Electrical Characteristics. 2. Going to Preliminary. 3. Updated Idd to reflect low power outputs	Various
B	9/11/2007	1. Updated pin description	2, 3
C	9/12/2007	1. Updated quantity of PCIEX outputs listed under "Output Features"	1
D	10/25/2007	1. Corrected CPU/SRC/PCI PLL control bytes to B(15:18) from B(11:14) 2. Changed pin names to indicate default drive strength. NO silicon changes. 3. Corrected Byte 0 SS_EN and FS3 reference in FS table. 4. Simplified the Terminations Table.. 5. Release to Final	1, 2, 3, 4, 5, 16,17
E	12/14/2007	Updated SMBus serial Interface Information	12
F	12/2/2008	Removed ICS prefix from ordering information.	19

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