CK420BQ DERIVATIVE SUPPORTING SRNS PCIE CLOCKING

932SQ426

General Description

The 932SQ426 is a CK420BQ derivative supporting Separate Reference no Spread (SRnS) PCIe clocking architectures. It uses a 25MHz crystal for maximum performance and has 100MHz outputs tuned for non-spreading applications to provide the most open eye diagram on PCIe links.

Recommended Application

CK420BQ for SRnS applications

Output Features

- 11 - HCSL 100MHz outputs for SRnS
- 4 - NS_SAS/SRC outputs
- 4 - CPU outputs
- 3 - SRC outputs
- 1 - HCSL DOT96 output
- 1 - 3.3V 48M output
- 5 - 3.3V PCI outputs
- 1 - 3.3V 14.318M output

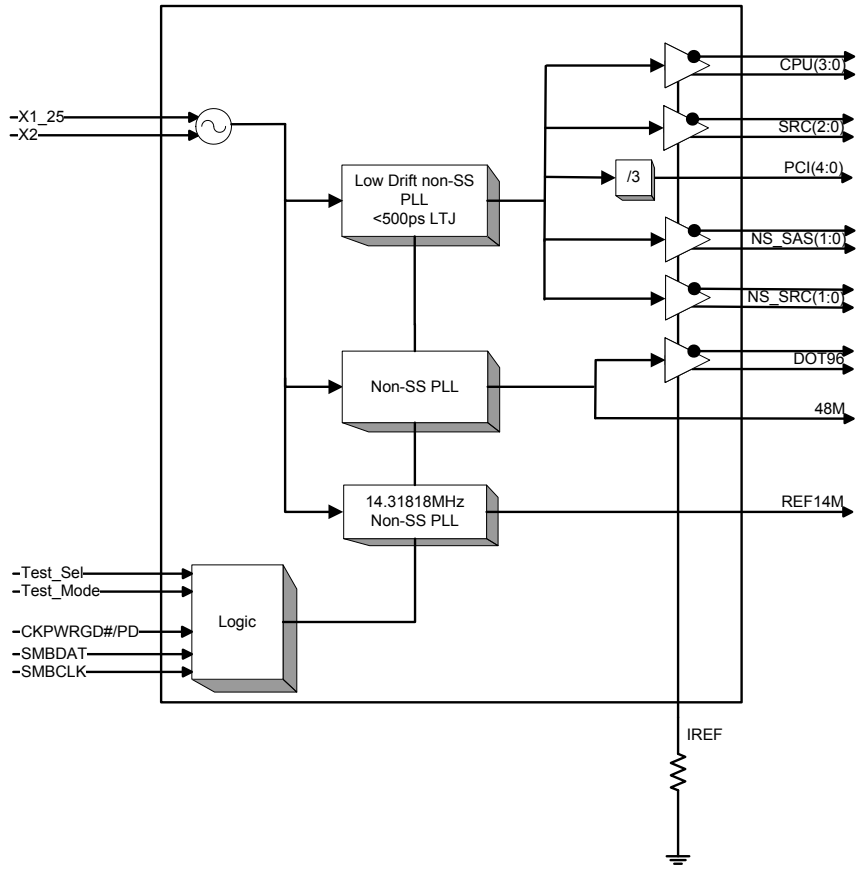
Features/Benefits

- Non-spread 100MHz outputs/ Supports SRnS PCIe architectures
- 64-pin TSSOP and VFQFPN packages; maximum space savings

Key Specifications

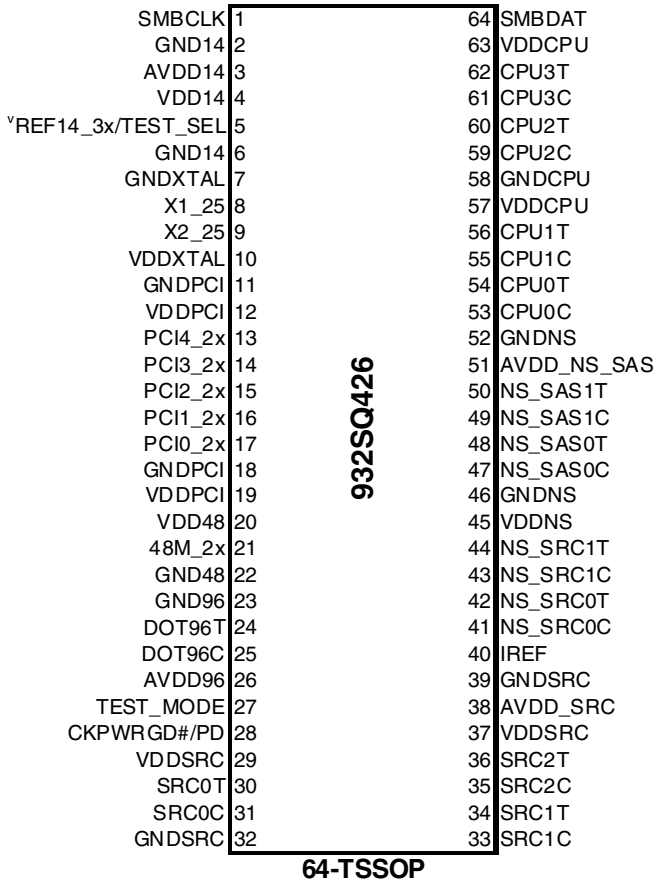
- Cycle to cycle jitter: CPU/SRC/NS_SRC/NS_SAS < 50ps
- Phase jitter: PCIe Gen2 <3ps rms
- Phase jitter: PCIe Gen3 <1ps rms
- Phase jitter: QPI 9.6GB/s <0.2ps rms
- Phase jitter: NS-SAS <0.4ps rms using raw phase data
- Phase jitter: NS-SAS <1.3ps rms using Clk Jit Tool 1.6.4

Block Diagram



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Pin Configuration (TSSOP)



64-TSSOP

Note: Pins with ^ prefix have internal 120K pullup
Pins with v prefix have internal 120K pulldown

932SQ426 Functionality

CPU, SRC, NS_SAS, NS_SRC	PCI	REF	DOT96	USB	
100	33.33	14.318	96.00	48.00	MHz

Power Group Pin Numbers

QFN		TSSOP		Description
VDD	GND	VDD	GND	
57	56	3	2	14MHz PLL Analog
58	60	4	6	REF14M Output and Logic
64	61	10	7	25MHz XTAL
2,9	1,8	12, 19	11,18	PCI Outputs and Logic
10	12	20	22	48MHz Output and Logic
16	13	26	23	96MHz PLL Analog, Output and Logic
19,27,28	22	29,37,38	32,39	SRC Outputs and Logic
35	36	45	46	Non-Spreading Differential Outputs & Logic
41	42	51	52	NS-SAS/SRC PLL Analog
47,53	48	57,63	58	CPU Outputs and Logic

932SQ426 Power Down Functionality

CKPWRGD#/PD	Differential Outputs	Single-ended Outputs	Single ended Outputs w/Latch
1	HI-Z[1]	Low	Low[2]
0	Running		

1. Hi-Z on the differential outputs will result in both True and Complement being low due to the termination
2. These outputs are Hi-Z after VDD is applied and before the first assertion of CKPWRGD#.

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Pin Descriptions (TSSOP)

PIN #	PIN NAME	TYPE	DESCRIPTION
1	SMBCLK	IN	Clock pin of SMBUS circuitry, 5V tolerant
2	GND14	PWR	Ground pin for 14MHz output and logic.
3	AVDD14	PWR	Analog power pin for 14MHz PLL
4	VDD14	PWR	Power pin for 14MHz output and logic
5	vREF14_3x/TEST_SEL	I/O	14.318 MHz reference clock. 3X drive strength as default / TEST_SEL latched input to enable test mode. Refer to Test Clarification Table. This pin has a weak (~120Kohm) internal pull down.
6	GND14	PWR	Ground pin for 14MHz output and logic.
7	GNDXTAL	PWR	Ground pin for Crystal Oscillator.
8	X1_25	IN	Crystal input, Nominally 25.00MHz.
9	X2_25	OUT	Crystal output, Nominally 25.00MHz.
10	VDDXTAL	PWR	3.3V power for the crystal oscillator.
11	GNDPCI	PWR	Ground pin for PCI outputs and logic.
12	VDDPCI	PWR	3.3V power for the PCI outputs and logic
13	PCI4_2x	OUT	3.3V PCI clock output
14	PCI3_2x	OUT	3.3V PCI clock output
15	PCI2_2x	OUT	3.3V PCI clock output
16	PCI1_2x	OUT	3.3V PCI clock output
17	PCI0_2x	OUT	3.3V PCI clock output
18	GNDPCI	PWR	Ground pin for PCI outputs and logic.
19	VDDPCI	PWR	3.3V power for the PCI outputs and logic
20	VDD48	PWR	3.3V power for the 48MHz output and logic
21	48M_2x	OUT	3.3V 48MHz output
22	GND48	PWR	Ground pin for 48MHz output and logic.
23	GND96	PWR	Ground pin for DOT96 output and logic.
24	DOT96T	OUT	True clock of differential 96MHz output. These are current mode outputs and external series resistors and shunt resistors are required for termination. See Test Loads and Recommended Terminations for specific values.
25	DOT96C	OUT	Complementary clock of differential 96MHz output. These are current mode outputs and external series resistors and shunt resistors are required for termination. See Test Loads and Recommended Terminations for specific values.
26	AVDD96	PWR	3.3V power for the 48/96MHz PLL and the 96MHz output and logic
27	TEST_MODE	IN	TEST_MODE is a real time input to select between Hi-Z and REF/N divider mode while in test mode. Refer to Test Clarification Table.
28	CKPWRGD#/PD	IN	CKPWRGD# is an active low input used to sample latched inputs and allow the device to Power Up. PD is an asynchronous active high input pin used to put the device into a low power state. The internal clocks and PLLs are stopped.
29	VDDSRC	PWR	3.3V power for the SRC outputs and logic
30	SRC0T	OUT	True clock of differential SRC output. These are current mode outputs and external series resistors and shunt resistors are required for termination. See Test Loads and Recommended Terminations for specific values.
31	SRC0C	OUT	Complementary clock of differential SRC output. These are current mode outputs and external series resistors and shunt resistors are required for termination. See Test Loads and Recommended Terminations for specific values.
32	GNDSRC	PWR	Ground pin for SRC outputs and logic.
33	SRC1C	OUT	Complementary clock of differential SRC output. These are current mode outputs and external series resistors and shunt resistors are required for termination. See Test Loads and Recommended Terminations for specific values.
34	SRC1T	OUT	True clock of differential SRC output. These are current mode outputs and external series resistors and shunt resistors are required for termination. See Test Loads and Recommended Terminations for specific values.
35	SRC2C	OUT	Complementary clock of differential SRC output. These are current mode outputs and external series resistors and shunt resistors are required for termination. See Test Loads and Recommended Terminations for specific values.
36	SRC2T	OUT	True clock of differential SRC output. These are current mode outputs and external series resistors and shunt resistors are required for termination. See Test Loads and Recommended Terminations for specific values.
37	VDDSRC	PWR	3.3V power for the SRC outputs and logic
38	AVDD_SRC	PWR	3.3V power for the SRC PLL analog circuits
39	GNDSRC	PWR	Ground pin for SRC outputs and logic.
40	IREF	OUT	This pin establishes the reference current for the differential current-mode output pairs. This pin requires a fixed precision resistor tied to ground in order to establish the appropriate current. 475 ohms is the standard value.

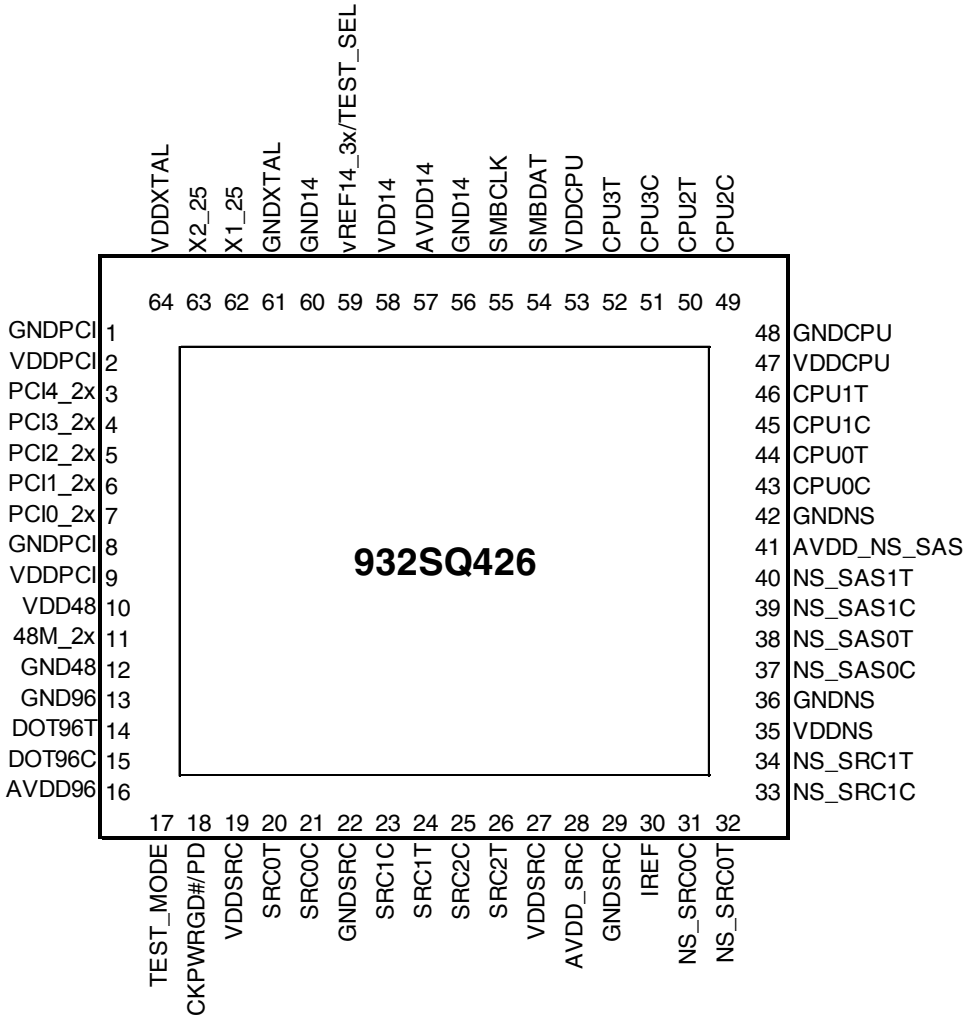
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Pin Descriptions (TSSOP, cont.)

PIN #	PIN NAME	TYPE	DESCRIPTION
41	NS_SRC0C	OUT	Complementary clock of differential non-spreading SRC output. These are current mode outputs and external series resistors and shunt resistors are required for termination. See Test Loads and Recommended Terminations for specific values.
42	NS_SRC0T	OUT	True clock of differential non-spreading SRC output. These are current mode outputs and external series resistors and shunt resistors are required for termination. See Test Loads and Recommended Terminations for specific values.
43	NS_SRC1C	OUT	Complementary clock of differential non-spreading SRC output. These are current mode outputs and external series resistors and shunt resistors are required for termination. See Test Loads and Recommended Terminations for specific values.
44	NS_SRC1T	OUT	True clock of differential non-spreading SRC output. These are current mode outputs and external series resistors and shunt resistors are required for termination. See Test Loads and Recommended Terminations for specific values.
45	VDDNS	PWR	3.3V power for the Non-Spreading differential outputs outputs and logic
46	GNDNS	PWR	Ground pin for non-spreading differential outputs and logic.
47	NS_SAS0C	OUT	Complementary clock of differentia non-spreading SAS output. These are current mode outputs and external series resistors and shunt resistors are required for termination. See Test Loads and Recommended Terminations for specific values.
48	NS_SAS0T	OUT	True clock of differential non-spreading SAS output. These are current mode outputs and external series resistors and shunt resistors are required for termination. See Test Loads and Recommended Terminations for specific values.
49	NS_SAS1C	OUT	Complementary clock of differentia non-spreading SAS output. These are current mode outputs and external series resistors and shunt resistors are required for termination. See Test Loads and Recommended Terminations for specific values.
50	NS_SAS1T	OUT	True clock of differential non-spreading SAS output. These are current mode outputs and external series resistors and shunt resistors are required for termination. See Test Loads and Recommended Terminations for specific values.
51	AVDD_NS_SAS	PWR	3.3V power for the non-spreading SAS/SRC PLL analog circuits.
52	GNDNS	PWR	Ground pin for non-spreading differential outputs and logic.
53	CPU0C	OUT	Complementary clock of differential CPU output. These are current mode outputs and external series resistors and shunt resistors are required for termination. See Test Loads and Recommended Terminations for specific values.
54	CPU0T	OUT	True clock of differential CPU output. These are current mode outputs and external series resistors and shunt resistors are required for termination. See Test Loads and Recommended Terminations for specific values.
55	CPU1C	OUT	Complementary clock of differential CPU output. These are current mode outputs and external series resistors and shunt resistors are required for termination. See Test Loads and Recommended Terminations for specific values.
56	CPU1T	OUT	True clock of differential CPU output. These are current mode outputs and external series resistors and shunt resistors are required for termination. See Test Loads and Recommended Terminations for specific values.
57	VDDCPU	PWR	3.3V power for the CPU outputs and logic
58	GNDCPU	PWR	Ground pin for CPU outputs and logic.
59	CPU2C	OUT	Complementary clock of differential CPU output. These are current mode outputs and external series resistors and shunt resistors are required for termination. See Test Loads and Recommended Terminations for specific values.
60	CPU2T	OUT	True clock of differential CPU output. These are current mode outputs and external series resistors and shunt resistors are required for termination. See Test Loads and Recommended Terminations for specific values.
61	CPU3C	OUT	Complementary clock of differential CPU output. These are current mode outputs and external series resistors and shunt resistors are required for termination. See Test Loads and Recommended Terminations for specific values.
62	CPU3T	OUT	True clock of differential CPU output. These are current mode outputs and external series resistors and shunt resistors are required for termination. See Test Loads and Recommended Terminations for specific values.
63	VDDCPU	PWR	3.3V power for the CPU outputs and logic
64	SMBDAT	I/O	Data pin of SMBUS circuitry, 5V tolerant

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Pin Configuration (VFQFPN)



64-pin VFQFPN

Note: Pins with ^ prefix have internal 120K pullup
Pins with v prefix have internal 120K pulldowm

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Pin Descriptions (VFQFPN)

PIN #	PIN NAME	TYPE	DESCRIPTION
1	GNDPCI	932SQ426	Ground pin for PCI outputs and logic.
2	VDDPCI	PWR	
3	PCI4_2x	OUT	3.3V PCI clock output
4	PCI3_2x	OUT	3.3V PCI clock output
5	PCI2_2x	OUT	3.3V PCI clock output
6	PCI1_2x	OUT	3.3V PCI clock output
7	PCI0_2x	OUT	3.3V PCI clock output
8	GNDPCI	PWR	Ground pin for PCI outputs and logic.
9	VDDPCI	PWR	3.3V power for the PCI outputs and logic
10	VDD48	PWR	3.3V power for the 48MHz output and logic
11	48M_2x	OUT	3.3V 48MHz output
12	GND48	PWR	Ground pin for 48MHz output and logic.
13	GND96	PWR	Ground pin for DOT96 output and logic.
14	DOT96T	OUT	True clock of differential 96MHz output. These are current mode outputs and external series resistors and shunt resistors are required for termination. See Test Loads and Recommended Terminations for specific values.
15	DOT96C	OUT	Complementary clock of differential 96MHz output. These are current mode outputs and external series resistors and shunt resistors are required for termination. See Test Loads and Recommended Terminations for specific values.
16	AVDD96	PWR	3.3V power for the 48/96MHz PLL and the 96MHz output and logic
17	TEST_MODE	IN	TEST_MODE is a real time input to select between Hi-Z and REF/N divider mode while in test mode. Refer to Test Clarification Table.
18	CKPWRGD#/PD	IN	CKPWRGD# is an active low input used to sample latched inputs and allow the device to Power Up. PD is an asynchronous active high input pin used to put the device into a low power state. The internal clocks and PLLs are stopped.
19	VDDSRC	PWR	3.3V power for the SRC outputs and logic
20	SRC0T	OUT	True clock of differential SRC output. These are current mode outputs and external series resistors and shunt resistors are required for termination. See Test Loads and Recommended Terminations for specific values.
21	SRC0C	OUT	Complementary clock of differential SRC output. These are current mode outputs and external series resistors and shunt resistors are required for termination. See Test Loads and Recommended Terminations for specific values.
22	GNDSRC	PWR	Ground pin for SRC outputs and logic.
23	SRC1C	OUT	Complementary clock of differential SRC output. These are current mode outputs and external series resistors and shunt resistors are required for termination. See Test Loads and Recommended Terminations for specific values.
24	SRC1T	OUT	True clock of differential SRC output. These are current mode outputs and external series resistors and shunt resistors are required for termination. See Test Loads and Recommended Terminations for specific values.
25	SRC2C	OUT	Complementary clock of differential SRC output. These are current mode outputs and external series resistors and shunt resistors are required for termination. See Test Loads and Recommended Terminations for specific values.
26	SRC2T	OUT	True clock of differential SRC output. These are current mode outputs and external series resistors and shunt resistors are required for termination. See Test Loads and Recommended Terminations for specific values.
27	VDDSRC	PWR	3.3V power for the SRC outputs and logic
28	AVDD_SRC	PWR	3.3V power for the SRC PLL analog circuits
29	GNDSRC	PWR	Ground pin for SRC outputs and logic.
30	IREF	OUT	This pin establishes the reference current for the differential current-mode output pairs. This pin requires a fixed precision resistor tied to ground in order to establish the appropriate current. 475 ohms is the standard value.
31	NS_SRC0C	OUT	Complementary clock of differential non-spreading SRC output. These are current mode outputs and external series resistors and shunt resistors are required for termination. See Test Loads and Recommended Terminations for specific values.
32	NS_SRC0T	OUT	True clock of differential non-spreading SRC output. These are current mode outputs and external series resistors and shunt resistors are required for termination. See Test Loads and Recommended Terminations for specific values.

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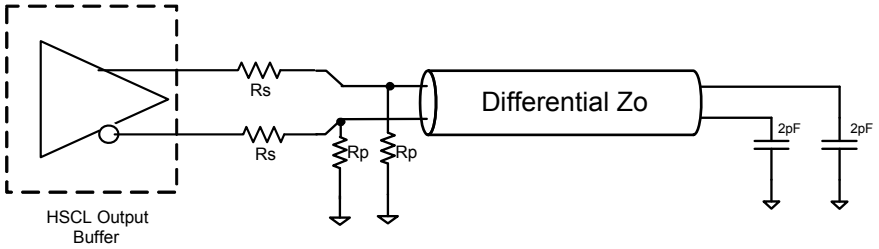
Pin Descriptions (VFQFPN, cont.)

PIN #	PIN NAME	TYPE	DESCRIPTION
33	NS_SRC1C	OUT	Complementary clock of differential non-spreading SRC output. These are current mode outputs and external series resistors and shunt resistors are required for termination. See Test Loads and Recommended Terminations for specific values.
34	NS_SRC1T	OUT	True clock of differential non-spreading SRC output. These are current mode outputs and external series resistors and shunt resistors are required for termination. See Test Loads and Recommended Terminations for specific values.
35	VDDNS	PWR	3.3V power for the Non-Spreading differential outputs outputs and logic
36	GNDNS	PWR	Ground pin for non-spreading differential outputs and logic.
37	NS_SAS0C	OUT	Complementary clock of differentia non-spreading SAS output. These are current mode outputs and external series resistors and shunt resistors are required for termination. See Test Loads and Recommended Terminations for specific values.
38	NS_SAS0T	OUT	True clock of differential non-spreading SAS output. These are current mode outputs and external series resistors and shunt resistors are required for termination. See Test Loads and Recommended Terminations for specific values.
39	NS_SAS1C	OUT	Complementary clock of differentia non-spreading SAS output. These are current mode outputs and external series resistors and shunt resistors are required for termination. See Test Loads and Recommended Terminations for specific values.
40	NS_SAS1T	OUT	True clock of differential non-spreading SAS output. These are current mode outputs and external series resistors and shunt resistors are required for termination. See Test Loads and Recommended Terminations for specific values.
41	AVDD_NS_SAS	PWR	3.3V power for the non-spreading SAS/SRC PLL analog circuits.
42	GNDNS	PWR	Ground pin for non-spreading differential outputs and logic.
43	CPU0C	OUT	Complementary clock of differential CPU output. These are current mode outputs and external series resistors and shunt resistors are required for termination. See Test Loads and Recommended Terminations for specific values.
44	CPU0T	OUT	True clock of differential CPU output. These are current mode outputs and external series resistors and shunt resistors are required for termination. See Test Loads and Recommended Terminations for specific values.
45	CPU1C	OUT	Complementary clock of differential CPU output. These are current mode outputs and external series resistors and shunt resistors are required for termination. See Test Loads and Recommended Terminations for specific values.
46	CPU1T	OUT	True clock of differential CPU output. These are current mode outputs and external series resistors and shunt resistors are required for termination. See Test Loads and Recommended Terminations for specific values.
47	VDDCPU	PWR	3.3V power for the CPU outputs and logic
48	GNDCPU	PWR	Ground pin for CPU outputs and logic.
49	CPU2C	OUT	Complementary clock of differential CPU output. These are current mode outputs and external series resistors and shunt resistors are required for termination. See Test Loads and Recommended Terminations for specific values.
50	CPU2T	OUT	True clock of differential CPU output. These are current mode outputs and external series resistors and shunt resistors are required for termination. See Test Loads and Recommended Terminations for specific values.
51	CPU3C	OUT	Complementary clock of differential CPU output. These are current mode outputs and external series resistors and shunt resistors are required for termination. See Test Loads and Recommended Terminations for specific values.
52	CPU3T	OUT	True clock of differential CPU output. These are current mode outputs and external series resistors and shunt resistors are required for termination. See Test Loads and Recommended Terminations for specific values.
53	VDDCPU	PWR	3.3V power for the CPU outputs and logic
54	SMBDAT	I/O	Data pin of SMBUS circuitry, 5V tolerant
55	SMBCLK	IN	Clock pin of SMBUS circuitry, 5V tolerant
56	GND14	PWR	Ground pin for 14MHz output and logic.
57	AVDD14	PWR	Analog power pin for 14MHz PLL
58	VDD14	PWR	Power pin for 14MHz output and logic
59	vREF14_3x/TEST_SEL	I/O	14.318 MHz reference clock. 3X drive strength as default / TEST_SEL latched input to enable test mode. Refer to Test Clarification Table. This pin has a weak (~120Kohm) internal pull down.
60	GND14	PWR	Ground pin for 14MHz output and logic.
61	GNDXTAL	PWR	Ground pin for Crystal Oscillator.
62	X1_25	IN	Crystal input, Nominally 25.00MHz.
63	X2_25	OUT	Crystal output, Nominally 25.00MHz.
64	VDDXTAL	PWR	3.3V power for the crystal oscillator.

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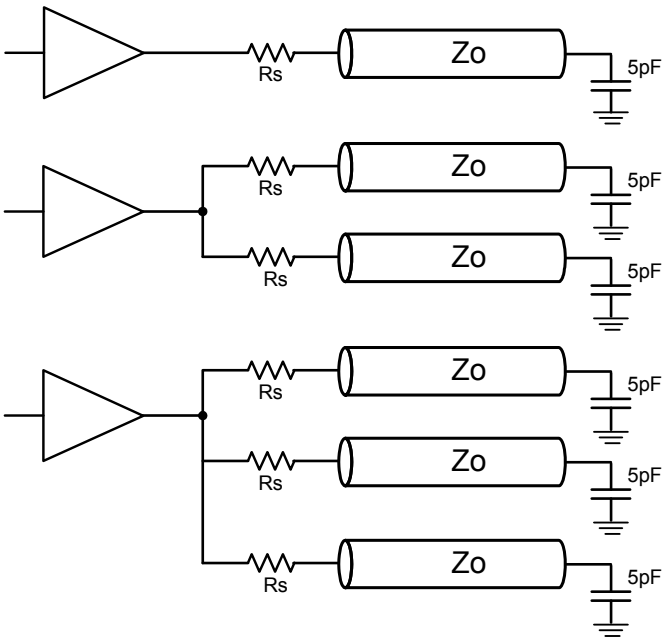
Test Loads and Recommended Terminations

932SQ426 Differential Test Loads



Differential Output Termination Table

DIF Zo (Ω)	Iref (Ω)	Rs (Ω)	Rp (Ω)
100	475	33	50
85	412	27	43.2



Single-ended Output Termination Table

		Rs Value (for each load)	
Output	Loads	Zo = 50Ω	Zo =60Ω
PCI/USB	1	36	43
PCI/USB	2	22	33
REF	1	39	47
REF	2	27	36
REF	3	10	20

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Electrical Characteristics - Absolute Maximum Ratings

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	NOTES
.3V Core Supply Voltag	VDDA	932SQ426AKLF			4.6	V	1,2
3V Logic Supply Voltag	VDD				4.6	V	1,2
Input Low Voltage	V_{IL}		GND-0.5			V	1
Input High Voltage	V_{IH}	Except for SMBus interface			V_{DD}+0.5V	V	1
Input High Voltage	V_{IHSMB}	SMBus clock and data pins			5.5V	V	1
Storage Temperature	Ts		-65		150	°C	1
Junction Temperature	Tj				125	°C	1
Input ESD protection	ESD prot	Human Body Model	2000			V	1

[1]Guaranteed by design and characterization, not 100% tested in production.

[2] Operation under these conditions is neither implied nor guaranteed.

Electrical Characteristics - Current Consumption

TA = $T_{COM;}$ Supply Voltage VDD = 3.3 V +/-5%

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	NOTES
Operating Supply Current	$I_{DD3.3OP}$	All outputs active @100MHz, C_L = Full load;		370	400	mA	
Powerdown Current	$I_{DD3.3PDZ}$	All differential pairs tri-stated		17	20	mA	

[1]Guaranteed by design and characterization, not 100% tested in production.

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DC Electrical Characteristics - Differential Current Mode Outputs

$T_A = T_{COM;}$ Supply Voltage VDD = 3.3 V +/-5%

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	NOTES
Slew rate	dV/dt	Scope averaging on	1	2.3	4	V/ns	1, 2, 3
Slew rate matching	ΔdV/dt	Slew rate matching, Scope averaging on		10	20	%	1, 2, 4
Rise/Fall Time Matching	ΔTrf	Rise/fall matching, Scope averaging off		17	125	ps	1, 8, 9
Voltage High	VHigh	Statistical measurement on single-ended signal using oscilloscope math function. (Scope averaging on)	660	716	850	mV	
Voltage Low	VLow		-150	20	150		
Max Voltage	Vmax	Measurement on single ended signal using absolute value. (Scope averaging off)		757	1150	mV	1, 7
Min Voltage	Vmin		-300	-9			1, 7
Vswing	Vswing	Scope averaging off	300	1393		mV	1, 2
Crossing Voltage (abs)	Vcross_abs	Scope averaging off	250	338	550	mV	1, 5
Crossing Voltage (var)	Δ-Vcross	Scope averaging off		32	140	mV	1, 6

[1]Guaranteed by design and characterization, not 100% tested in production. IREF = VDD/(3xR_R). For R_R =412Ω (1%), I_{REF} = 2.67mA. I_{OH} = 6 x I_{REF} and V_{OH} = 0.7V @ Z_O= 85Ω differential impedance.

[2] Measured from differential waveform

[3] Slew rate is measured through the Vswing voltage range centered around differential 0V. This results in a +/-150mV window around differential 0V.

[4] Matching applies to rising edge rate for Clock and falling edge rate for Clock#. It is measured using a +/-75mV window centered on the average cross point where Clock rising meets Clock# falling. The median cross point is used to calculate the voltage thresholds the oscilloscope is to use for the edge rate calculations.

[5] Vcross is defined as voltage where Clock = Clock# measured on a component test board and only applies to the differential rising edge (i.e. Clock rising and Clock# falling).

[6] The total variation of all Vcross measurements in any particular system. Note that this is a subset of V_cross_min/max (V_cross absolute) allowed. The intent is to limit Vcross induced modulation by setting V_cross_delta to be smaller than V_cross absolute.

[7] Includes overshoot and undershoot.

[8] Measured from single-ended waveform

[9] Measured with scope averaging off, using statistics function. Variation is difference between min and max.

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Electrical Characteristics - Input/Supply/Common Parameters

TA = $T_{COM;}$ Supply Voltage VDD = 3.3 V +/-5%

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	NOTES
Ambient Operating Temperature	T_{COM}	Commmercial range	0	25	70	°C	1
Input High Voltage	V_{IH}	Single-ended inputs, except SMBus, low threshold and tri-level inputs	2.2	2.4	V_{DD} + 0.3	V	
Input Low Voltage	V_{IL}	Single-ended inputs, except SMBus, low threshold and tri-level inputs	GND - 0.3	0.4	0.8	V	
Input Current	I_{IN}	Single-ended inputs, V_{IN} = GND, V_{IN} = VDD	-5		5	uA	
	I_{INP}	Single-ended inputs. V_{IN} = 0 V; Inputs with internal pull-up resistors V_{IN} = VDD; Inputs with internal pull-down resistors	-200		200	uA	
Low Threshold Input-High Voltage	V_{IH_FS}	3.3 V +/-5%	0.7		V_{DD} + 0.3	V	
Low Threshold Input-Low Voltage	V_{IL_FS}	3.3 V +/-5%	V_{SS} - 0.3		0.35	V	
Input Frequency	F_i			25.00		MHz	2
Pin Inductance	L_{pin}				7	nH	1
Capacitance	C_{IN}	Logic Inputs			5	pF	1
	C_{OUT}	Output pin capacitance			5	pF	1
	C_{INX}	X1 & X2 pins			5	pF	1
Clk Stabilization	T_{STAB}	From V_{DD} Power-Up and after input clock stabilization or de-assertion of PD# to 1st clock		1.3	1.8	ms	2
Tdrive_PD#	t_{DRVPD}	Differential output enable after PD# de-assertion		200	300	us	1,3
Tfall	t_F	Fall time of control inputs			5	ns	1,2
Trise	t_R	Rise time of control inputs			5	ns	1,2
SMBus Input Low Voltage	V_{ILSMB}				0.8	V	
SMBus Input High Voltage	V_{IHSMB}		2.1		V_{DDSMB}	V	1
SMBus Output Low Voltage	V_{OLSMB}	@ I_{PULLUP}			0.4	V	
SMBus Sink Current	I_{PULLUP}	@ V_{OL}	4			mA	
Nominal Bus Voltage	V_{DDSMB}	3V to 5V +/- 10%	2.7		5.5	V	
SCLK/SDATA Rise Time	t_{RSMB}	(Max VIL - 0.15) to (Min VIH + 0.15)			1000	ns	1
SCLK/SDATA Fall Time	t_{FSMB}	(Min VIH + 0.15) to (Max VIL - 0.15)			300	ns	1
SMBus Operating Frequency	f_{MAXSMB}	Maximum SMBus operating frequency			100	kHz	

[1]Guaranteed by design and characterization, not 100% tested in production.

[2]Control input must be monotonic from 20% to 80% of input swing.

[3]Time from deassertion until outputs are >200 mV

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AC Electrical Characteristics - Differential Current Mode Outputs

TA = $T_{COM;}$ Supply Voltage VDD = 3.3 V +/-5%

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	NOTES
Duty Cycle	t_{DC}	Measured differentially, PLL Mode	45	52	55	%	1
Skew, Output to Output	t_{sk3SRC}	Across all SRC, NS-SAS outputs, V_T = 50%		12	50	ps	1
Skew, Output to Output	t_{sk3CPU}	Across all CPU outputs, V_T = 50%		35	50	ps	1
Jitter, Cycle to cycle	$t_{jcyc-cyc}$	CPU, SRC, NS_SAS outputs @100M		34	50	ps	1,3
		DOT96 output		75	250	ps	1,3

[1]Guaranteed by design and characterization, not 100% tested in production.

[2] I_{REF} = VDD/(3xRR). For RR =412Ω (1%), IREF = 2.67mA. IOH = 6 x IREF and VOH = 0.7V @ ZO= 85Ω differential impedance.

[3] Measured from differential waveform

Electrical Characteristics - Phase Jitter Parameters

T_A = 0 - 70°C; Supply Voltage V_{DD}/V_{DDA} = 3.3 V +/-5%,

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	Notes
Phase Jitter	$t_{jphPCIeG1}$	PCIe Gen 1		16	86	ps (p-p)	1,2,3,6
	$t_{jphPCIeG2}$	PCIe Gen 2 Lo Band 10kHz < f < 1.5MHz		0.37	3	ps (rms)	1,2,6
		PCIe Gen 2 High Band 1.5MHz < f < Nyquist (50MHz)		1.45	3.1	ps (rms)	1,2,6
	$t_{jphPCIeG3}$	PCIe Gen 3 (PLL BW of 2-4MHz, CDR = 10MHz)		0.35	1	ps (rms)	1,2,4,6
	t_{jphQPI_SMI}	QPI & SMI (100MHz or 133MHz, 4.8Gb/s, 6.4Gb/s 12UI)		0.29	0.5	ps (rms)	1,5,6
		QPI & SMI (100MHz, 8.0Gb/s, 12UI)		0.15	0.3	ps (rms)	1,5,6
		QPI & SMI (100MHz, 9.6Gb/s, 12UI)		0.13	0.2	ps (rms)	1,5,6
	$t_{jphSAS12G}$	SAS12G (Filtered REFCLK Jitter 20KHz to 20MHz.)		0.30	0.4	ps (rms)	1,7,8
	$t_{jphSAS12G}$	SAS 12G		0.54	1.3	ps (rms)	1,5,8

[1] Guaranteed by design and characterization, not 100% tested in production.

[2] See http://www.pcisig.com for complete specs

[3] Sample size of at least 100K cycles. This figures extrapolates to 108ps pk-pk @ 1M cycles for a BER of 1-12.

[4] Subject to final radification by PCI SIG.

[5] Calculated from Intel-supplied Clock Jitter Tool v 1.6.4

[6] Applies to CPU, SRC and NS_SAS outputs

[7] Intel calculation from raw phase noise data

[8] Applies to NS_SAS and NS_SRC outputs only.

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Electrical Characteristics - PCI

T_A = 0 - 70°C; Supply Voltage V_{DD}/V_{DDA} = 3.3 V +/-5%,

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	NOTES
Output Impedance	R_{DSP}	$V_O = V_{DD}*(0.5)$	12		55	Ω	1
Output High Voltage	V_{OH}	I_{OH} = -1 mA	2.4			V	
Output Low Voltage	V_{OL}	I_{OL} = 1 mA			0.55	V	
Clock High Time	T_{HIGH}	1.5V	12			ns	1
Clock Low Time	T_{LOW}	1.5V	12			ns	1
Edge Rate	$t_{slewr/f}$	Rising/Falling edge rate	1	1.7	4	V/ns	1,2
Duty Cycle	d_{t1}	V_T = 1.5 V	45	51.3	55	%	1
Group Skew	t_{skew}	V_T = 1.5 V		279	500	ps	1
Jitter, Cycle to cycle	$t_{jcyc-cyc}$	V_T = 1.5 V		96	500	ps	1

See "Single-ended Test Loads Page" for termination circuits

[1]Guaranteed by design and characterization, not 100% tested in production.

[2] Measured between 0.8V and 2.0V

Electrical Characteristics - 48MHz

T_A = 0 - 70°C; Supply Voltage V_{DD}/V_{DDA} = 3.3 V +/-5%,

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	NOTES
Output Impedance	R_{DSP}	$V_O = V_{DD}*(0.5)$	20		60	Ω	1
Output High Voltage	V_{OH}	I_{OH} = -1 mA	2.4			V	
Output Low Voltage	V_{OL}	I_{OL} = 1 mA			0.55	V	
Clock High Time	T_{HIGH}	1.5V	8.094		10.036	ns	1
Clock Low Time	T_{LOW}	1.5V	7.694		9.836	ns	1
Edge Rate	t_{slewr/f_USB}	Rising/Falling edge rate	1	1.8	2	V/ns	1,2
Duty Cycle	d_{t1}	V_T = 1.5 V	45	51	55	%	1
Jitter, Cycle to cycle	$t_{jcyc-cyc}$	V_T = 1.5 V		122	350	ps	1

See "Single-ended Test Loads Page" for termination circuits

[1]Guaranteed by design and characterization, not 100% tested in production.

[2] Measured between 0.8V and 2.0V

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Electrical Characteristics - REF

T_A = 0 - 70°C; Supply Voltage V_{DD}/V_{DDA} = 3.3 V +/-5%,

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	Notes
Output Impedance	R_{DSP}	$V_O = V_{DD}*(0.5)$	12		55	Ω	1
Output High Voltage	V_{OH}	I_{OH} = -1 mA	2.4			V	
Output Low Voltage	V_{OL}	I_{OL} = 1 mA			0.55	V	
Clock High Time	T_{HIGH}	1.5V	27.5			ns	1
Clock Low Time	T_{LOW}	1.5V	27.5			ns	1
Edge Rate	$t_{slewr/f}$	Rising/Falling edge rate	1	1.5	4	V/ns	1,2
Duty Cycle	d_{t1}	V_T = 1.5 V	45	50.5	55	%	1
Jitter, Cycle to cycle	$t_{jcyc-cyc}$	V_T = 1.5 V		89	1000	ps	1

See "Single-ended Test Loads Page" for termination circuits

[1]Guaranteed by design and characterization, not 100% tested in production.

[2] Measured between 0.8V and 2.0V

Clock AC Tolerances

	CPU	SRC, NS_SAS, NS_SRC	PCI	DOT96	48MHz	REF	
PPM tolerance	100	100	100	100	100	100	**ppm**
Cycle to Cycle Jitter	50	50	500	250	350	1000	**ps**

Clock Periods – Outputs without Spread Spectrum

SSC ON	Center Freq. MHz	Measurement Window							Units	Notes
		1 Clock	1us	0.1s	0.1s	0.1s	1us	1 Clock		
		-c2c jitter AbsPer Min	-SSC Short-Term Average Min	- ppm Long-Term Average Min	0 ppm Period Nominal	+ ppm Long-Term Average Max	+SSC Short-Term Average Max	+c2c jitter AbsPer Max		
CPU	100.00000	9.94900		9.99900	10.00000	10.00100		10.05100	ns	1,2
SRC, NS_SAS, NS_SRC	100.00000	9.94900		9.99900	10.00000	10.00100		10.05100	ns	1,2
PCI	33.33333	29.49700		29.99700	30.00000	30.00300		30.50300	ns	1,2
DOT96	96.00000	10.16563		10.41563	10.41667	10.41771		10.66771	ns	1,2
48MHz	48.00000	20.48125		20.83125	20.83333	20.83542		21.18542	ns	1,2
REF	14.31818	69.78429		69.83429	69.84128	69.84826		69.89826	ns	1,2

[1]Guaranteed by design and characterization, not 100% tested in production.

[2] All Long Term Accuracy specifications are guaranteed with the assumption that the REF output is tuned to exactly 14.31818MHz.

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General SMBus Serial Interface Information

How to Write

- Controller (host) sends a start bit
- Controller (host) sends the write address
- IDT clock will **acknowledge**
- Controller (host) sends the beginning byte location = N
- IDT clock will **acknowledge**
- Controller (host) sends the byte count = X
- IDT clock will **acknowledge**
- Controller (host) starts sending Byte **N through Byte N+X-1**
- IDT clock will **acknowledg**e each byte **one at a time**
- Controller (host) sends a Stop bit

Index Block Write Operation			
Controller (Host)			**IDT (Slave/Receiver)**
T	starT bit		
Slave Address			
WR	WRite		
			ACK
Beginning Byte = N			
			ACK
Data Byte Count = X			
			ACK
Beginning Byte N		X Byte	
			ACK
O			
O			O
O			O
			O
Byte N + X - 1			
			ACK
P	stoP bit		

SMBus write address = D2 hex

SMBus read address = D3 hex

How to Read

- Controller (host) will send a start bit
- Controller (host) sends the write address
- IDT clock will **acknowledge**
- Controller (host) sends the beginning byte location = N
- IDT clock will **acknowledge**
- Controller (host) will send a separate start bit
- Controller (host) sends the read address
- IDT clock will **acknowledge**
- IDT clock will send the data byte count = X
- IDT clock sends Byte **N+X-1**
- IDT clock sends **Byte 0 through Byte X (if $X_{(H)}$ was written to Byte 8)**
- Controller (host) will need to acknowledge each byte
- Controller (host) will send a not acknowledge bit
- Controller (host) will send a stop bit

Index Block Read Operation			
Controller (Host)			**IDT (Slave/Receiver)**
T	starT bit		
Slave Address			
WR	WRite		
			ACK
Beginning Byte = N			
			ACK
RT	Repeat starT		
Slave Address			
RD	ReaD		
			ACK
			Data Byte Count=X
ACK			
		X Byte	Beginning Byte N
ACK			
			O
O			O
O			O
O			
			Byte N + X - 1
N	Not acknowledge		
P	stoP bit		

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SMBus Table: Output Enable Register

Byte 0	Pin #	Name	Control Function	Type	0	1	Default
Bit 7	24/25	DOT96 Enable	Output Enable	RW	Disable-Hi-Z	Enable	1
Bit 6	50/49	NS_SAS1 Enable	Output Enable	RW	Disable-Hi-Z	Enable	1
Bit 5	48/47	NS_SAS0 Enable	Output Enable	RW	Disable-Hi-Z	Enable	1
Bit 4	44/43	NS_SRC1 Enable	Output Enable	RW	Disable-Hi-Z	Enable	1
Bit 3	42/41	NS_SRC0 Enable	Output Enable	RW	Disable-Hi-Z	Enable	1
Bit 2	36/35	SRC2 Enable	Output Enable	RW	Disable-Hi-Z	Enable	1
Bit 1	34/33	SRC1 Enable	Output Enable	RW	Disable-Hi-Z	Enable	1
Bit 0	30/31	SRC0 Enable	Output Enable	RW	Disable-Hi-Z	Enable	1

SMBus Table: Output Enable Register

Byte 1	Pin #	Name	Control Function	Type	0	1	Default
Bit 7	5	REF14_3x Enable	Output Enable	RW	Disable-Low	Enable	1
Bit 6		RESERVED					0
Bit 5		RESERVED					0
Bit 4	62/61	CPU3	Output Enable	RW	Disable-Hi-Z	Enable	1
Bit 3	60/59	CPU2	Output Enable	RW	Disable-Hi-Z	Enable	1
Bit 2	56/55	CPU1	Output Enable	RW	Disable-Hi-Z	Enable	1
Bit 1	54/53	CPU0	Output Enable	RW	Disable-Hi-Z	Enable	1
Bit 0		RESERVED					0

SMBus Table: Output Enable Register

Byte 2	Pin #	Name	Control Function	Type	0	1	Default
Bit 7		RESERVED					0
Bit 6		RESERVED					0
Bit 5	13	PCI4 Enable	Output Enable	RW	Disable-Low	Enable	1
Bit 4	14	PCI3 Enable	Output Enable	RW	Disable-Low	Enable	1
Bit 3	15	PCI2 Enable	Output Enable	RW	Disable-Low	Enable	1
Bit 2	16	PCI1 Enable	Output Enable	RW	Disable-Low	Enable	1
Bit 1	17	PCI0 Enable	Output Enable	RW	Disable-Low	Enable	1
Bit 0	21	48MHz Enable	Output Enable	RW	Disable-Low	Enable	1

SMBus Table: Reserved Register

Byte 3	Pin #	Name	Control Function	Type	0	1	Default
Bit 7		RESERVED					0
Bit 6		RESERVED					0
Bit 5		RESERVED					0
Bit 4		RESERVED					0
Bit 3		RESERVED					0
Bit 2		RESERVED					0
Bit 1		RESERVED					0
Bit 0		RESERVED					0

SMBus Table: Reserved Register

Byte 4	Pin #	Name	Control Function	Type	0	1	Default
Bit 7		RESERVED					0
Bit 6		RESERVED					0
Bit 5		RESERVED					0
Bit 4		RESERVED					0
Bit 3		RESERVED					0
Bit 2		RESERVED					0
Bit 1		RESERVED					0
Bit 0		RESERVED					0

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SMBus Table: Reserved Register

Byte 5	Pin #	Name	Control Function	Type	0	1	Default
Bit 7		RESERVED					0
Bit 6		RESERVED					0
Bit 5		RESERVED					0
Bit 4		RESERVED					0
Bit 3		RESERVED					1
Bit 2		RESERVED					1
Bit 1		RESERVED					1
Bit 0		RESERVED					1

SMBus Table: Test Mode Register

Byte 6	Pin #	Name	Control Function	Type	0	1	Default
Bit 7	-	Test Mode	Test Mode Type	RW	Hi-Z	REF/N	0
Bit 6	-	Test Select	Select Test Mode	RW	Disable	Enable	0
Bit 5	-	RESERVED					0
Bit 4	-	RESERVED					1
Bit 3	-	RESERVED					1
Bit 2	-	RESERVED					0
Bit 1	-	RESERVED					0
Bit 0	-	RESERVED					0

SMBus Table: Vendor & Revision ID Register

Byte 7	Pin #	Name	Control Function	Type	0	1	Default
Bit 7	-	RID3	REVISION ID	R	0000 for A rev		0
Bit 6	-	RID2		R			0
Bit 5	-	RID1		R			0
Bit 4	-	RID0		R			0
Bit 3	-	VID3	VENDOR ID	R	0001 for ICS/IDT		0
Bit 2	-	VID2		R			0
Bit 1	-	VID1		R			0
Bit 0	-	VID0		R			1

SMBus Table: Byte Count Register

Byte 8	Pin #	Name	Control Function	Type	0	1	Default
Bit 7	-	BC7	Byte Count Programming b(7:0)	RW	Writing to this register will configure how many bytes will be read back, default is A bytes. (0 to 9		0
Bit 6	-	BC6		RW			0
Bit 5	-	BC5		RW			0
Bit 4	-	BC4		RW			0
Bit 3	-	BC3		RW			1
Bit 2	-	BC2		RW			0
Bit 1	-	BC1		RW			1
Bit 0	-	BC0		RW			0

SMBus Table: Device ID Register

Byte 9	Pin #	Name	Control Function	Type	0	1	Default
Bit 7		DID7	Device ID (1A hex)	R	-	-	0
Bit 6		DID6		R	-	-	0
Bit 5		DID5		R	-	-	0
Bit 4		DID4		R	-	-	1
Bit 3		DID3		R	-	-	1
Bit 2		DID2		R	-	-	0
Bit 1		DID1		R	-	-	1
Bit 0		DID0		R	-	-	0

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DIF Reference Clock			
Common Recommendations for Differential Routing	Dimension or Value	Unit	Figure
L1 length, route as non-coupled 50ohm trace	0.5 max	inch	1
L2 length, route as non-coupled 50ohm trace	0.2 max	inch	1
L3 length, route as non-coupled 50ohm trace	0.2 max	inch	1
Rs	33	ohm	1
Rt	49.9	ohm	1

Down Device Differential Routing			
L4 length, route as coupled microstrip 100ohm differential trace	2 min to 16 max	inch	1
L4 length, route as coupled stripline 100ohm differential trace	1.8 min to 14.4 max	inch	1

Differential Routing to PCI Express Connector			
L4 length, route as coupled microstrip 100ohm differential trace	0.25 to 14 max	inch	2
L4 length, route as coupled stripline 100ohm differential trace	0.225 min to 12.6 max	inch	2

Figure 1: Down Device Routing

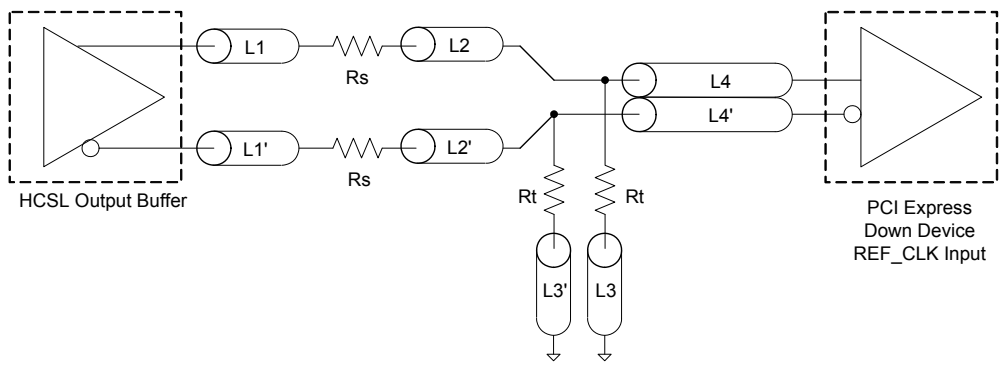
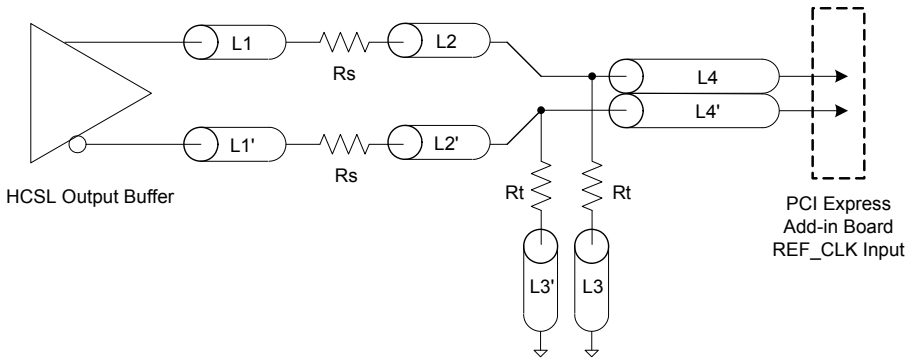


Figure 2: PCI Express Connector Routing

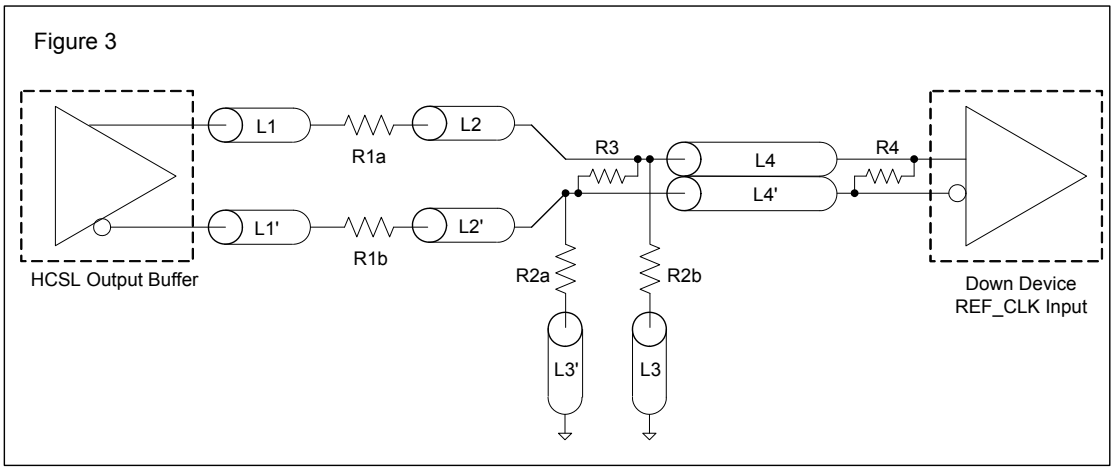


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Alternative Termination for LVDS and other Common Differential Signals (figure 3)							
Vdiff	Vp-p	Vcm	R1	R2	R3	R4	Note
0.45v	0.22v	1.08	33	150	100	100	
0.58	0.28	0.6	33	78.7	137	100	
0.80	0.40	0.6	33	78.7	none	100	ICS874003i-02 input compatible
0.60	0.3	1.2	33	174	140	100	Standard LVDS

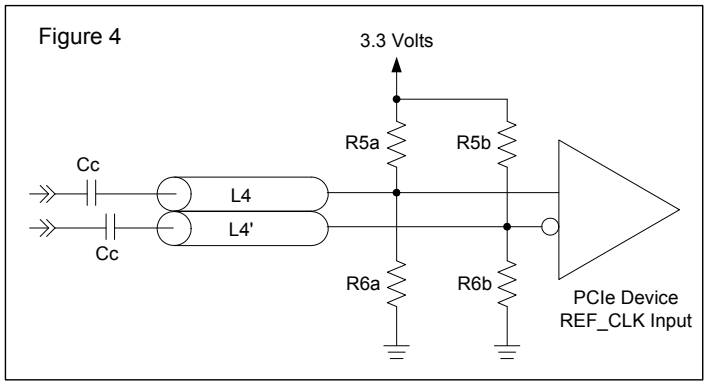
R1a = R1b = R1
R2a = R2b = R2

Figure 3



Cable Connected AC Coupled Application (figure 4)		
Component	Value	Note
R5a, R5b	8.2K 5%	
R6a, R6b	1K 5%	
Cc	0.1 µF	
Vcm	0.350 volts	

Figure 4



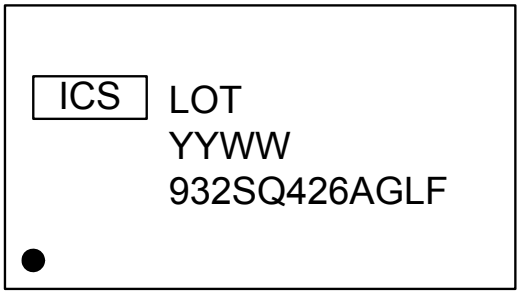
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Test Clarification Table

Comments	HW		SW		
	TEST_SEL HW PIN	932SQ426A KLF	ENTRY BIT B6b6	HI-Z B6b7	OUTPUT
	0	X	0	X	NORMAL
Power-up w/ TEST_SEL = 1 (>2.0V) to enter test mode. Cycle power to disable test mode.	1	0	X	0	HI-Z
	1	0	X	1	REF/N
	1	1	X	0	REF/N
	1	1	X	1	REF/N
If TEST_SEL HW pin is 0 during power-up, test mode can be selected through B6b6. If test mode is selected by B6b6, then B6b7 is used to select HI-Z or REF/N. TEST_Mode pin is not used. Cycle power to disable test mode.	0	X	1	0	HI-Z
	0	X	1	1	REF/N

B6b6: 1= ENTER TEST MODE, Default = 0 (NORMAL OPERATION)
B6b7: 1= REF/N, Default = 0 (HI-Z)

Marking Diagrams

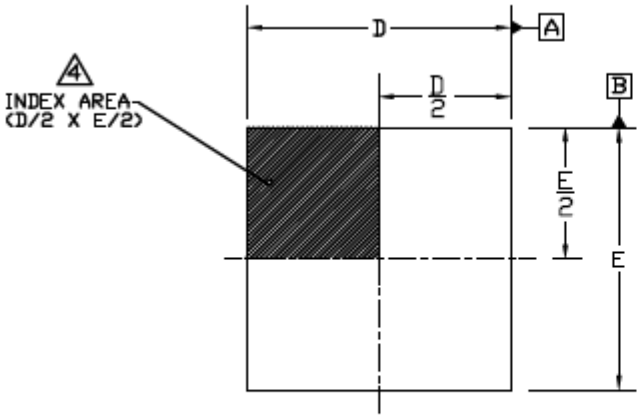


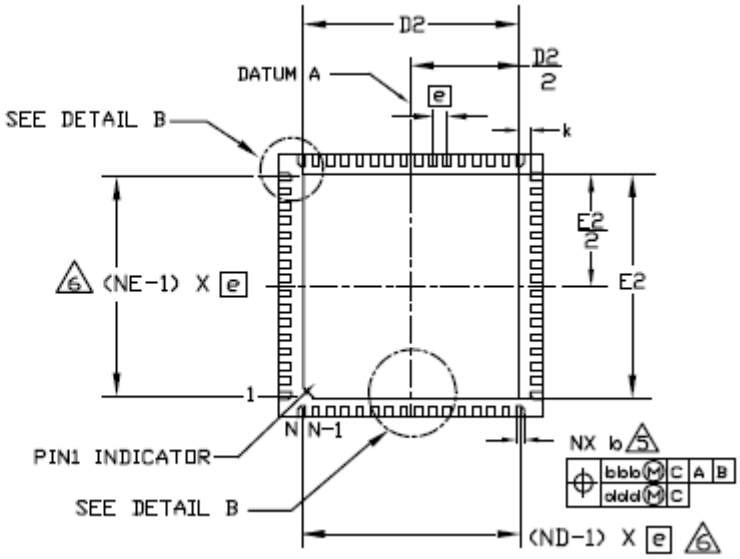


Notes:
1. “LOT” denotes lot number.
2. “YYWW” is the date code.
3. “COO” denotes country of origin.
4. “L” or “LF” denotes RoHS compliant package.

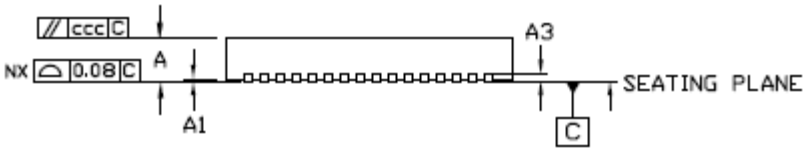
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Package Outline and Package Dimensions (NLG64)

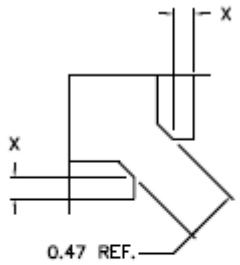




TOP VIEW



SIDE VIEW

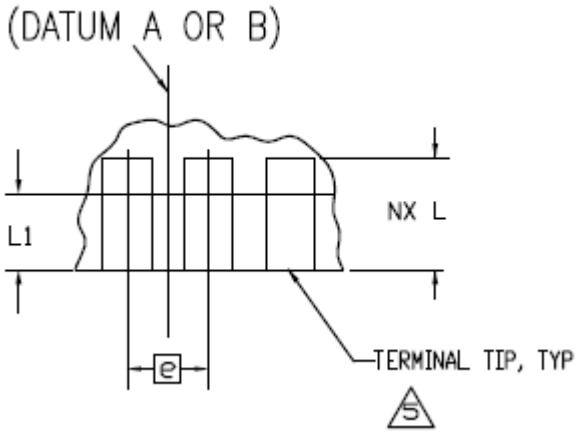


DETAIL B

CORNER LEAD
CHAMFER DETAILS
8

NOTES:

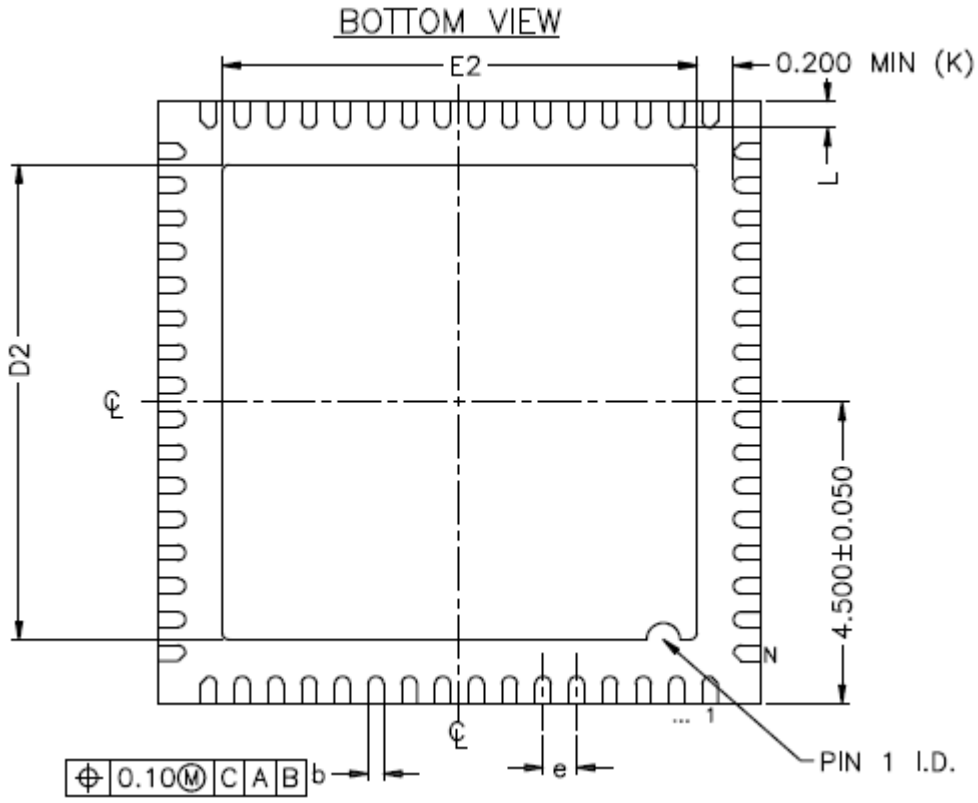
1. DIMENSIONING & TOLERANCING CONFORM TO ASME Y14.5M–1994.
2. ALL DIMENSIONS ARE IN MILLIMETERS. ANGLES ARE IN DEGREES.
3. N IS THE TOTAL NUMBER OF TERMINALS.
4. THE TERMINAL #1 IDENTIFIER AND TERMINAL NUMBERING CONVENTION SHALL CONFORM TO JEDEC PUBLICATION 95 SPP–002. DETAILS OF TERMINAL #1 IDENTIFIER ARE OPTIONAL, BUT MUST BE LOCATED WITHIN THE ZONE INDICATED. THE TERMINAL #1 IDENTIFIER MAY BE EITHER A MOLD OR MARKED FEATURE.
5. DIMENSION b APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.25mm AND 0.30mm FROM TERMINAL TIP.
6. ND AND NE REFER TO THE NUMBER OF TERMINALS ON EACH D AND E SIDE RESPECTIVELY.
7. DEPOPULATION IS POSSIBLE IN A SYMMETRICAL FASHION.
8. CORNER LEAD CHAMFERS ARE APPLIED TO MAINTAIN MINIMUM CORNER LEAD SPACING (8 PLACES).



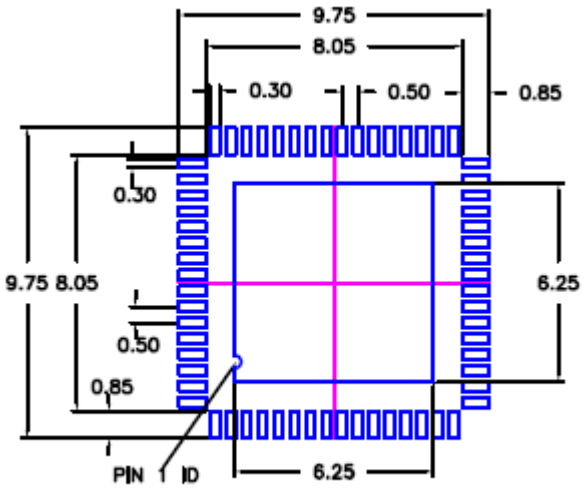
DETAIL B

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Package Outline and Package Dimensions, cont. (NLG64)



DIMENSIONS			
PACKAGE	64L 9.0x9.0 – 0.50		
REF.	MIN.	NOM.	MAX.
A	0.80	0.90	1.00
b	0.18	0.25	0.30
D		9.00 BSC	
D2	6.0	6.15	6.25
E		9.00 BSC	
E2	6.0	6.15	6.25
e		0.50 BSC.	
L	0.30	0.40	0.50
N		64	
ND		16	
NE		16	
k	0.20		



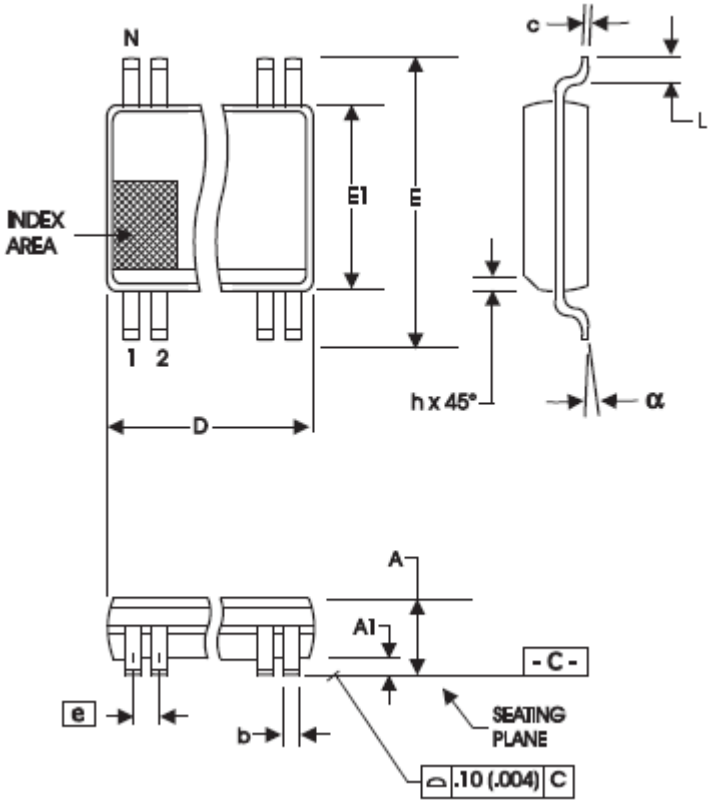
EPAD 6.15

SYMBOL	COMMON DIMENSIONS			NOTE
	MIN.	NOM.	MAX.	
A1	0	0.02	0.05	
A3	–	0.20 REF.	–	
X	b/2	–	–	
TOLERANCES OF FORM AND POSITION				
bbb	0.10			
ccc	0.10			
ddd	0.05			

NOTES:
1. ALL DIMENSION ARE IN mm. ANGLES IN DEGREES.
2. TOP DOWN VIEW. AS VIEWED ON PCB.
3. LAND PATTERN IN BLUE. NSMD PATTERN ASSUMED.
4. LAND PATTERN RECOMMENDATION PER IPC-7351B LP CALCULATOR.

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Package Outline and Package Dimensions (64-pin TSSOP)



6.10 mm. Body, 0.50 mm. Pitch TSSOP
(240 mil) (20 mil)

SYMBOL	In Millimeters COMMON DIMENSIONS		In Inches COMMON DIMENSIONS	
	MIN	MAX	MIN	MAX
A	--	1.20	--	.047
A1	0.05	0.15	.002	.006
A2	0.80	1.05	.032	.041
b	0.17	0.27	.007	.011
c	0.09	0.20	.0035	.008
D	SEE VARIATIONS		SEE VARIATIONS	
E	8.10 BASIC		0.319 BASIC	
E1	6.00	6.20	.236	.244
e	0.50 BASIC		0.020 BASIC	
L	0.45	0.75	.018	.030
N	SEE VARIATIONS		SEE VARIATIONS	
α	0°	8°	0°	8°
aaa	--	0.10	--	.004

VARIATIONS

N	D mm.		D (inch)	
	MIN	MAX	MIN	MAX
64	16.90	17.10	.665	.673

Reference Doc.: JEDEC Publication 95, MO-153

10-0039

Ordering Information

Part / Order Number	Shipping Pacakging	Package	Temperature
932SQ426AGLF	Tubes	64-pin TSSOP	0 to +70° C
932SQ426AGLFT	Tape and Reel	64-pin TSSOP	0 to +70° C
932SQ426AKLF	Tray	64-pin VFQFPN	0 to +70° C
932SQ426AKLFT	Tape and Reel	64-pin VFQFPN	0 to +70° C

"LF" suffix to the part number are the Pb-Free configuration, RoHS compliant.

"A" is the device revision designator (will not correlate with the datasheet revision).

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Revision History

Rev.	Issue Date	Who	Description	Page #
A	10/14/2011	RDW	1. Updated Electrical Tables with typical values 2. Updated Pin Descriptions on Differential outputs to refer to "Test Loads and Recommended Termiations" table for Rs and Rp values. 3. Updated Byte 5 to Reserved 4. Updated Byte 6 Default value to 18hex from 00hex 5. Removed Non-Spread Output Margining Table on page 15 6. Add Mark Spec 7. Move to Final	Various
B	7/8/2015	RDW	1.Updated front page text 2. Added 64-QFN power groupings to power grouping table. 3. Added 64-QFN pin out, pin description 4. Updated marking info for 64-QFN 5. Added 64-QFN ordering info	1-5,17,18
C	2/26/2016	RDW	1.Minor grammatical corrections to electrical tables	9-14

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