Low-Power CK420BQ Derivative for PCIe Common Clock Architectures

932SQL450

DATASHEET

General Description

The 932SQL450 is a low power version of the CK420BQ synthesizer for Intel-based server platforms. It has 85-ohm LP-HCSL outputs allowing for direct connection to 85-ohm transmission lines. The 932SQL450 is driven with a 25MHz crystal for maximum performance. It generates CPU outputs of 100MHz. This device has a “low-drift” non-spread SAS/SRC PLL for use in systems that need to communicate across PCIe domains.

Recommended Application

Low Power CK420BQ w/Zout=85ohms or PCIe Common Clocked Systems (CC)

Key Specifications

- CPU, SRC, NS_SRC and NS_SAS cycle-cycle jitter <50ps
- Output to output skew <50ps
- Phase jitter: PCIe Gen2 <2.5ps rms
- Phase jitter: PCIe Gen3 <0.6ps rms
- Phase jitter: QPI <0.3ps rms
- Phase jitter: NS-SAS <1.3ps rms using long period phase jitter method

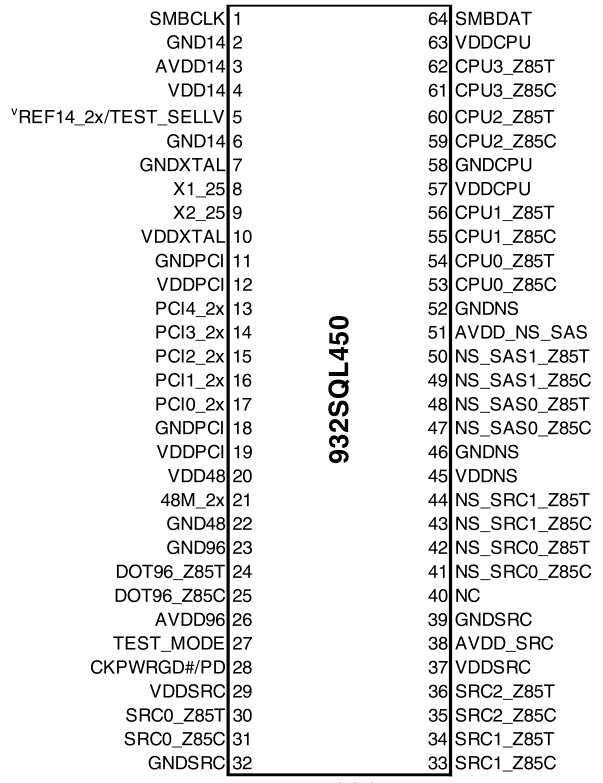
Features/Benefits

- Integrated 85 ohm differential terminations; saves 48 resistors and 82mm^2 area
- LP-HCSL output drivers; 40% typical power savings over 932SQ420
- 0.5% down spread capable on CPU, SRC and PCI outputs; reduce EMI
- Additional down spread amounts selectable via SMBus; maximal system flexibility
- 64-pin TSSOP and VFQFPN packages; smallest board footprint

Output Features

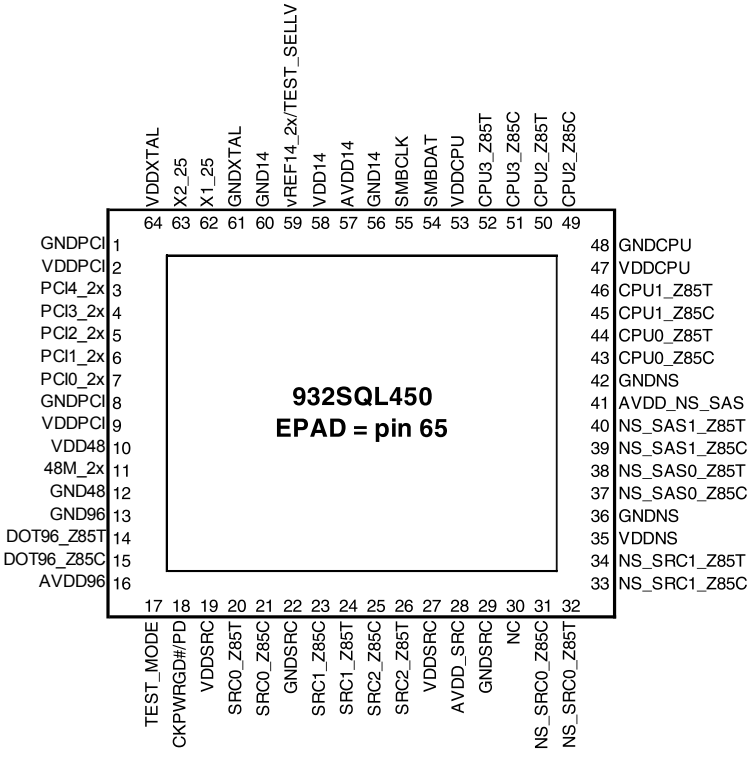
- 4 - Low-Power HCSL-compatible (LP-HCSL) CPU outputs
- 2 - LP-HCSL NS_SAS outputs
- 2 - LP-HCSL NS_SRC outputs
- 3 - LP-HCSL SRC outputs
- 1 - LP-HCSL DOT96 output
- 1 - 3.3V 48M output
- 5 - 3.3V PCI outputs
- 1 - 3.3V 14.318M output

Pin Configurations



64-TSSOP

Note: Pins with ^ prefix have internal 120K pullup
Pins with v prefix have internal 120K pulldown



64-Pin VFQFPN

Note: Pins with ^ prefix have internal 120K pullup
Pins with v prefix have internal 120K pulldown

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64TSSOP Pin Descriptions

PIN #	PIN NAME	TYPE	DESCRIPTION
1	SMBCLK	IN	Clock pin of SMBUS circuitry, 5V tolerant
2	GND14	PWR	Ground pin for 14MHz output and logic.
3	AVDD14	PWR	Analog power pin for 14MHz PLL
4	VDD14	PWR	Power pin for 14MHz output and logic
5	vREF14_2x/TEST_SELLV	I/O	14.318 MHz reference clock capable of driving 2 loads/ TEST_SEL latched input to enable test mode. The TEST_SEL input is a low threshold input. See the Electrical Tables and the Test Clarification Table. This pin has a weak (~120Kohm) internal pull down.
6	GND14	PWR	Ground pin for 14MHz output and logic.
7	GNDXTAL	PWR	Ground pin for Crystal Oscillator.
8	X1_25	IN	Crystal input, Nominally 25.00MHz.
9	X2_25	OUT	Crystal output, Nominally 25.00MHz.
10	VDDXTAL	PWR	3.3V power for the crystal oscillator.
11	GNDPCI	PWR	Ground pin for PCI outputs and logic.
12	VDDPCI	PWR	3.3V power for the PCI outputs and logic
13	PCI4_2x	OUT	3.3V PCI clock output capable of driving two loads.
14	PCI3_2x	OUT	3.3V PCI clock output capable of driving two loads.
15	PCI2_2x	OUT	3.3V PCI clock output capable of driving two loads.
16	PCI1_2x	OUT	3.3V PCI clock output capable of driving two loads.
17	PCI0_2x	OUT	3.3V PCI clock output capable of driving two loads.
18	GNDPCI	PWR	Ground pin for PCI outputs and logic.
19	VDDPCI	PWR	3.3V power for the PCI outputs and logic
20	VDD48	PWR	3.3V power for the 48MHz output and logic
21	48M_2x	OUT	3.3V 48MHz output capable of driving 2 loads.
22	GND48	PWR	Ground pin for 48MHz output and logic.
23	GND96	PWR	Ground pin for DOT96 output and logic.
24	DOT96_Z85T	OUT	True clock of low-power push-pull differential 96MHz output. Internally terminated to drive 85ohm transmission lines with no external components.
25	DOT96_Z85C	OUT	Complementary clock of low-power push-pull differential 96MHz output. Internally terminated to drive 85ohm transmission lines with no external components.
26	AVDD96	PWR	3.3V power for the 48/96MHz PLL and the 96MHz output and logic
27	TEST_MODE	IN	TEST_MODE is a real time input to select between Hi-Z and REF/N divider mode while in test mode. Refer to Test Clarification Table.
28	CKPWRGD#/PD	IN	CKPWRGD# is an active low input used to sample latched inputs and allow the device to Power Up. PD is an asynchronous active high input pin used to put the device into a low power state. The internal clocks and PLLs are stopped.
29	VDDSRC	PWR	3.3V power for the SRC outputs and logic
30	SRC0_Z85T	OUT	True clock of low-power push-pull differential SRC output. Internally terminated to drive 85ohm transmission lines with no external components.
31	SRC0_Z85C	OUT	Complementary clock of low-power push-pull differential SRC output. Internally terminated to drive 85ohm transmission lines with no external components.
32	GNDSRC	PWR	Ground pin for SRC outputs and logic.
33	SRC1_Z85C	OUT	Complementary clock of low-power push-pull differential SRC output. Internally terminated to drive 85ohm transmission lines with no external components.
34	SRC1_Z85T	OUT	True clock of low-power push-pull differential SRC output. Internally terminated to drive 85ohm transmission lines with no external components.
35	SRC2_Z85C	OUT	Complementary clock of low-power push-pull differential SRC output. Internally terminated to drive 85ohm transmission lines with no external components.
36	SRC2_Z85T	OUT	True clock of low-power push-pull differential SRC output. Internally terminated to drive 85ohm transmission lines with no external components.
37	VDDSRC	PWR	3.3V power for the SRC outputs and logic
38	AVDD_SRC	PWR	3.3V power for the SRC PLL analog circuits
39	GNDSRC	PWR	Ground pin for SRC outputs and logic.
40	NC	N/A	No Connection.

64TSSOP Pin Descriptions (cont.)

PIN #	PIN NAME	TYPE	DESCRIPTION
41	NS_SRC0_Z85C	OUT	Complementary clock of low-power push-pull differential non-spreading SRC output. Internally terminated to drive 85ohm transmission lines with no external components.
42	NS_SRC0_Z85T	OUT	True clock of low-power push-pull differential non-spreading SRC output. Internally terminated to drive 85ohm transmission lines with no external components.
43	NS_SRC1_Z85C	OUT	Complementary clock of low-power push-pull differential non-spreading SRC output. Internally terminated to drive 85ohm transmission lines with no external components.
44	NS_SRC1_Z85T	OUT	True clock of low-power push-pull differential non-spreading SRC output. Internally terminated to drive 85ohm transmission lines with no external components.
45	VDDNS	PWR	3.3V power for the Non-Spreading differential outputs outputs and logic
46	GNDNS	PWR	Ground pin for non-spreading differential outputs and logic.
47	NS_SAS0_Z85C	OUT	Complementary clock of low-power push-pull differential non-spreading SAS output. Internally terminated to drive 85ohm transmission lines with no external components.
48	NS_SAS0_Z85T	OUT	True clock of low-power push-pull differential non-spreading SAS output. Internally terminated to drive 85ohm transmission lines with no external components.
49	NS_SAS1_Z85C	OUT	Complementary clock of low-power push-pull differential non-spreading SAS output. Internally terminated to drive 85ohm transmission lines with no external components.
50	NS_SAS1_Z85T	OUT	True clock of low-power push-pull differential non-spreading SAS output. Internally terminated to drive 85ohm transmission lines with no external components.
51	AVDD_NS_SAS	PWR	3.3V power for the non-spreading SAS/SRC PLL analog circuits.
52	GNDNS	PWR	Ground pin for non-spreading differential outputs and logic.
53	CPU0_Z85C	OUT	Complementary clock of low-power push-pull differential CPU output. Internally terminated to drive 85ohm transmission lines with no external components.
54	CPU0_Z85T	OUT	True clock of low-power push-pull differential CPU output. Internally terminated to drive 85ohm transmission lines with no external components.
55	CPU1_Z85C	OUT	Complementary clock of low-power push-pull differential CPU output. Internally terminated to drive 85ohm transmission lines with no external components.
56	CPU1_Z85T	OUT	True clock of low-power push-pull differential CPU output. Internally terminated to drive 85ohm transmission lines with no external components.
57	VDDCPU	PWR	3.3V power for the CPU outputs and logic
58	GNDCPU	PWR	Ground pin for CPU outputs and logic.
59	CPU2_Z85C	OUT	Complementary clock of low-power push-pull differential CPU output. Internally terminated to drive 85ohm transmission lines with no external components.
60	CPU2_Z85T	OUT	True clock of low-power push-pull differential CPU output. Internally terminated to drive 85ohm transmission lines with no external components.
61	CPU3_Z85C	OUT	Complementary clock of low-power push-pull differential CPU output. Internally terminated to drive 85ohm transmission lines with no external components.
62	CPU3_Z85T	OUT	True clock of low-power push-pull differential CPU output. Internally terminated to drive 85ohm transmission lines with no external components.
63	VDDCPU	PWR	3.3V power for the CPU outputs and logic
64	SMBDAT	I/O	Data pin of SMBUS circuitry, 5V tolerant

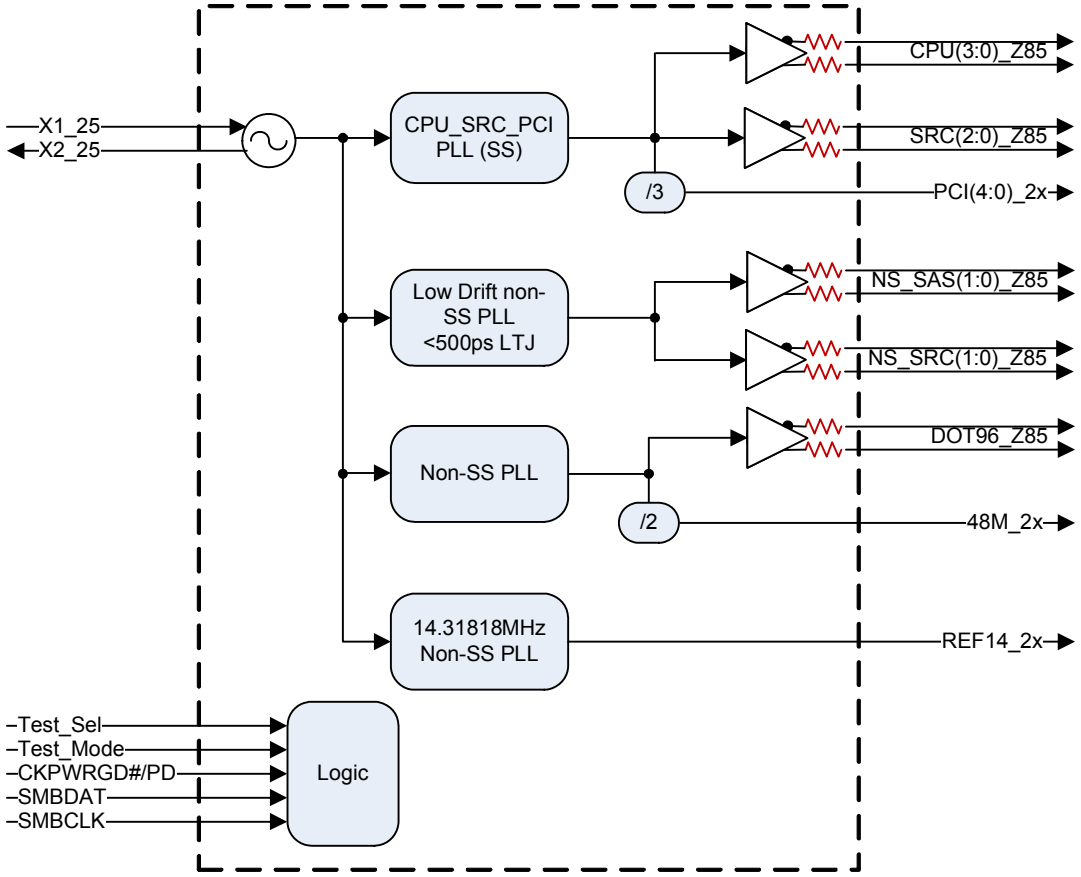
64VFQFPN Pin Descriptions

PIN #	PIN NAME	TYPE	DESCRIPTION
1	GNDPCI	PWR	Ground pin for PCI outputs and logic.
2	VDDPCI	PWR	3.3V power for the PCI outputs and logic
3	PCI4_2x	OUT	3.3V PCI clock output capable of driving two loads.
4	PCI3_2x	OUT	3.3V PCI clock output capable of driving two loads.
5	PCI2_2x	OUT	3.3V PCI clock output capable of driving two loads.
6	PCI1_2x	OUT	3.3V PCI clock output capable of driving two loads.
7	PCI0_2x	OUT	3.3V PCI clock output capable of driving two loads.
8	GNDPCI	PWR	Ground pin for PCI outputs and logic.
9	VDDPCI	PWR	3.3V power for the PCI outputs and logic
10	VDD48	PWR	3.3V power for the 48MHz output and logic
11	48M_2x	OUT	3.3V 48MHz output capable of driving 2 loads.
12	GND48	PWR	Ground pin for 48MHz output and logic.
13	GND96	PWR	Ground pin for DOT96 output and logic.
14	DOT96_Z85T	OUT	True clock of low-power push-pull differential 96MHz output. Internally terminated to drive 85ohm transmission lines with no external components.
15	DOT96_Z85C	OUT	Complementary clock of low-power push-pull differential 96MHz output. Internally terminated to drive 85ohm transmission lines with no external components.
16	AVDD96	PWR	3.3V power for the 48/96MHz PLL and the 96MHz output and logic
17	TEST_MODE	IN	TEST_MODE is a real time input to select between Hi-Z and REF/N divider mode while in test mode. Refer to Test Clarification Table.
18	CKPWRGD#/PD	IN	CKPWRGD# is an active low input used to sample latched inputs and allow the device to Power Up. PD is an asynchronous active high input pin used to put the device into a low power state. The internal clocks and PLLs are stopped.
19	VDDSRC	PWR	3.3V power for the SRC outputs and logic
20	SRC0_Z85T	OUT	True clock of low-power push-pull differential SRC output. Internally terminated to drive 85ohm transmission lines with no external components.
21	SRC0_Z85C	OUT	Complementary clock of low-power push-pull differential SRC output. Internally terminated to drive 85ohm transmission lines with no external components.
22	GNDSRC	PWR	Ground pin for SRC outputs and logic.
23	SRC1_Z85C	OUT	Complementary clock of low-power push-pull differential SRC output. Internally terminated to drive 85ohm transmission lines with no external components.
24	SRC1_Z85T	OUT	True clock of low-power push-pull differential SRC output. Internally terminated to drive 85ohm transmission lines with no external components.
25	SRC2_Z85C	OUT	Complementary clock of low-power push-pull differential SRC output. Internally terminated to drive 85ohm transmission lines with no external components.
26	SRC2_Z85T	OUT	True clock of low-power push-pull differential SRC output. Internally terminated to drive 85ohm transmission lines with no external components.
27	VDDSRC	PWR	3.3V power for the SRC outputs and logic
28	AVDD_SRC	PWR	3.3V power for the SRC PLL analog circuits
29	GNDSRC	PWR	Ground pin for SRC outputs and logic.
30	NC	N/A	No Connection.
31	NS_SRC0_Z85C	OUT	Complementary clock of low-power push-pull differential non-spreading SRC output. Internally terminated to drive 85ohm transmission lines with no external components.
32	NS_SRC0_Z85T	OUT	True clock of low-power push-pull differential non-spreading SRC output. Internally terminated to drive 85ohm transmission lines with no external components.
33	NS_SRC1_Z85C	OUT	Complementary clock of low-power push-pull differential non-spreading SRC output. Internally terminated to drive 85ohm transmission lines with no external components.
34	NS_SRC1_Z85T	OUT	True clock of low-power push-pull differential non-spreading SRC output. Internally terminated to drive 85ohm transmission lines with no external components.
35	VDDNS	PWR	3.3V power for the Non-Spreading differential outputs outputs and logic
36	GNDNS	PWR	Ground pin for non-spreading differential outputs and logic.
38	NS_SAS0_Z85T	OUT	True clock of low-power push-pull differential non-spreading SAS output. Internally terminated to drive 85ohm transmission lines with no external components.

64VFQFPN Pin Descriptions (cont.)

PIN #	PIN NAME	TYPE	DESCRIPTION
39	NS_SAS1_Z85C	OUT	Complementary clock of low-power push-pull differential non-spreading SAS output. Internally terminated to drive 85ohm transmission lines with no external components.
40	NS_SAS1_Z85T	OUT	True clock of low-power push-pull differential non-spreading SAS output. Internally terminated to drive 85ohm transmission lines with no external components.
41	AVDD_NS_SAS	PWR	3.3V power for the non-spreading SAS/SRC PLL analog circuits.
42	GNDNS	PWR	Ground pin for non-spreading differential outputs and logic.
43	CPU0_Z85C	OUT	Complementary clock of low-power push-pull differential CPU output. Internally terminated to drive 85ohm transmission lines with no external components.
44	CPU0_Z85T	OUT	True clock of low-power push-pull differential CPU output. Internally terminated to drive 85ohm transmission lines with no external components.
45	CPU1_Z85C	OUT	Complementary clock of low-power push-pull differential CPU output. Internally terminated to drive 85ohm transmission lines with no external components.
46	CPU1_Z85T	OUT	True clock of low-power push-pull differential CPU output. Internally terminated to drive 85ohm transmission lines with no external components.
47	VDDCPU	PWR	3.3V power for the CPU outputs and logic
48	GNDCPU	PWR	Ground pin for CPU outputs and logic.
49	CPU2_Z85C	OUT	Complementary clock of low-power push-pull differential CPU output. Internally terminated to drive 85ohm transmission lines with no external components.
50	CPU2_Z85T	OUT	True clock of low-power push-pull differential CPU output. Internally terminated to drive 85ohm transmission lines with no external components.
51	CPU3_Z85C	OUT	Complementary clock of low-power push-pull differential CPU output. Internally terminated to drive 85ohm transmission lines with no external components.
52	CPU3_Z85T	OUT	True clock of low-power push-pull differential CPU output. Internally terminated to drive 85ohm transmission lines with no external components.
53	VDDCPU	PWR	3.3V power for the CPU outputs and logic
54	SMBDAT	I/O	Data pin of SMBUS circuitry, 5V tolerant
55	SMBCLK	IN	Clock pin of SMBUS circuitry, 5V tolerant
56	GND14	PWR	Ground pin for 14MHz output and logic.
57	AVDD14	PWR	Analog power pin for 14MHz PLL
58	VDD14	PWR	Power pin for 14MHz output and logic
59	vREF14_2x/TEST_SELLV	I/O	14.318 MHz reference clock capable of driving 2 loads/ TEST_SEL latched input to enable test mode. The TEST_SEL input is a low threshold input. See the Electrical Tables and the Test Clarification Table. This pin has a weak (~120Kohm) internal pull down.
60	GND14	PWR	Ground pin for 14MHz output and logic.
61	GNDXTAL	PWR	Ground pin for Crystal Oscillator.
62	X1_25	IN	Crystal input, Nominally 25.00MHz.
63	X2_25	OUT	Crystal output, Nominally 25.00MHz.
64	VDDXTAL	PWR	3.3V power for the crystal oscillator.
65	EPAD	GND	Epad should be connected to ground.

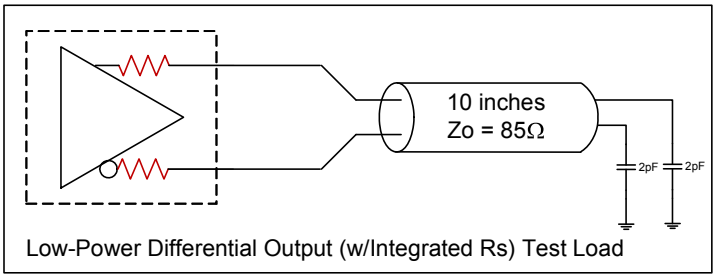
Block Diagram



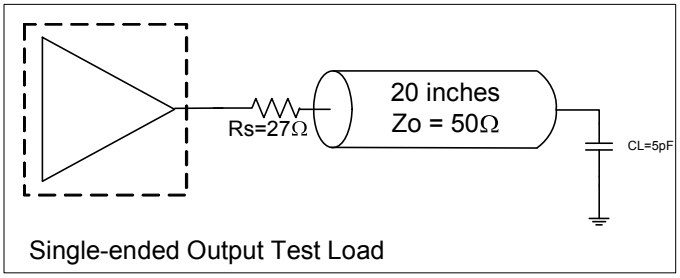
Power Supply and Test Loads

Power Group Pin Numbers

VFQFPN		TSSOP		Description
VDD	GND	VDD	GND	
57	56	3	2	14MHz PLL Analog
58	60	4	6	REF14M Output and Logic
64	61	10	7	25MHz XTAL
2, 9	1, 8	12, 19	11, 18	PCI Outputs and Logic
10	12	20	22	48MHz Output and Logic
16	13	26	23	96MHz PLL Analog, Output and Logic
19, 27	22	29, 37	32	SRC Outputs and Logic
28	29	38	39	SRC PLL Analog
35	36	45	46	Non-Spreading Differential Outputs & Logic
41	42	51	52	NS-SAS/SRC PLL Analog
47, 53	48	57,63	58	CPU Outputs and Logic

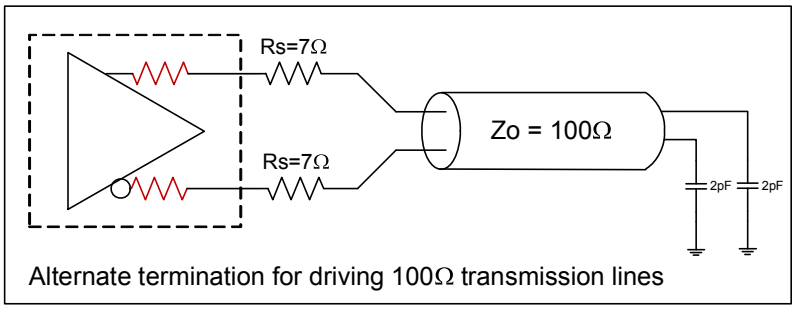


Low-Power Differential Output (w/Integrated Rs) Test Load

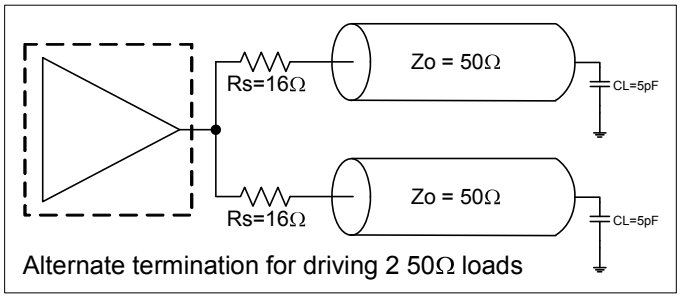


Single-ended Output Test Load

Alternate Terminations



Alternate termination for driving 100Ω transmission lines



Alternate termination for driving 2 50Ω loads

Functionality and CPU SAS Frequency Tables

932SQL450 Functionality

CPU	SRC	PCI	REF	NS_SAS NS_SRC	DOT96	USB	
100	100	33.33	14.318	100.00	96.00	48.00	MHz

Spread Spectrum Control Functionality

SS_Enable (B1b0)	CPU, SRC & PCI
0	OFF
1	-0.50%

932SQL450 Power Down Functionality

CKPWRGD#/PD	Differential Outputs	Single-ended Outputs	Single-ended Outputs w/Latch
1	Low/Low	Low	Low[1]
0	Running		

1. Single-ended outputs with a Latch will be Hi-Z until the first application of CKPWRGD#.

CPU/SRC/PCI Margining Table

Line	Byte6 Bit2 FS2	Byte6 Bit1 FS1	Byte6 Bit0 FS0	CPU Speed (MHz)	SRC (MHz)	PCI (MHz)	
0	0	0	0	97.00	97.00	32.33	
1	0	0	1	98.00	98.00	32.67	
2	0	1	0	99.00	99.00	33.00	
3	0	1	1	100.00	100.00	33.33	**Default for 100MHz**
4	1	0	0	101.00	101.00	33.67	
5	1	0	1	102.00	102.00	34.00	
6	1	1	0	103.00	103.00	34.33	
7	1	1	1	104.00	104.00	34.67	

NS_SAS Margining Table

Line	Byte5 Bit3 FS3	Byte5 Bit2 FS2	Byte5 Bit1 FS1	Byte5 Bit0 FS0	NS_xxx (MHz)
0	0	0	0	0	82.5
1	0	0	0	1	85.0
2	0	0	1	0	87.5
3	0	0	1	1	90.0
4	0	1	0	0	92.5
5	0	1	0	1	95.0
6	0	1	1	0	97.5
7	**0**	**1**	**1**	**1**	100.0
8	1	0	0	0	102.5
9	1	0	0	1	105.0
10	1	0	1	0	107.5
11	1	0	1	1	110.0
12	1	1	0	0	112.5
13	1	1	0	1	115.0
14	1	1	1	0	117.5
15	1	1	1	1	120.0

NOTE: Operation at other than the default entry is not guaranteed. These values are for margining purposes only.

Clock AC Tolerances

	CPU, SRC	NS_SAS, NS_SRC	PCI	DOT96	48MHz	REF	
PPM tolerance	100	100	100	100	100	100	**ppm**
Cycle to Cycle Jitter	50	50	500	250	350	1000	**ps**
Spread	-0.50%	0.00%	-0.50%	0	0.00%	0.00%	%

Clock Periods–Outputs with Spread Spectrum Disabled

SSC OFF	Center Freq. MHz	Measurement Window							Units	Notes
		1 Clock	1us	0.1s	0.1s	0.1s	1us	1 Clock		
		-c2c jitter AbsPer Min	-SSC Short-Term Average Min	- ppm Long-Term Average Min	0 ppm Period Nominal	+ ppm Long-Term Average Max	+SSC Short-Term Average Max	+c2c jitter AbsPer Max		
CPU	100.000	9.94900		9.99900	10.00000	10.00100		10.05100	ns	1,2
SRC, NS_SAS, NS_SRC	100.000	9.94900		9.99900	10.00000	10.00100		10.05100	ns	1,2
PCI	33.333	29.49700		29.99700	30.00000	30.00300		30.50300	ns	1,2
DOT96	96.000	10.16563		10.41563	10.41667	10.41771		10.66771	ns	1,2
48MHz	48.000	20.48125		20.83125	20.83333	20.83542		21.18542	ns	1,2
REF	14.318	69.78429		69.83429	69.84128	69.84826		69.89826	ns	1,2

Clock Periods–Outputs with Spread Spectrum Enabled

SSC ON	Center Freq. MHz	Measurement Window							Units	Notes
		1 Clock	1us	0.1s	0.1s	0.1s	1us	1 Clock		
		-c2c jitter AbsPer Min	-SSC Short-Term Average Min	- ppm Long-Term Average Min	0 ppm Period Nominal	+ ppm Long-Term Average Max	+SSC Short-Term Average Max	+c2c jitter AbsPer Max		
CPU	99.75	9.94906	9.99906	10.02406	10.02506	10.02607	10.05107	10.10107	ns	1,2
PCI	33.25	29.49718	29.99718	30.07218	30.07519	30.07820	30.15320	30.65320	ns	1,2
SRC	99.75	9.94906	9.99906	10.02406	10.02506	10.02607	10.05107	10.10107	ns	1,2

[1]Guaranteed by design and characterization, not 100% tested in production.

[2] All Long Term Accuracy specifications are guaranteed with the assumption that the REF output is tuned to exactly 14.31818MHz.

General SMBus Serial Interface Information for 932SQL450

How to Write

- Controller (host) sends a start bit
- Controller (host) sends the write address
- IDT clock will **acknowledge**
- Controller (host) sends the beginning byte location = N
- IDT clock will **acknowledge**
- Controller (host) sends the byte count = X
- IDT clock will **acknowledge**
- Controller (host) starts sending Byte **N through Byte N+X-1**
- IDT clock will **acknowledg**e each byte **one at a time**
- Controller (host) sends a Stop bit

How to Read

- Controller (host) will send a start bit
- Controller (host) sends the write address
- IDT clock will **acknowledge**
- Controller (host) sends the beginning byte location = N
- IDT clock will **acknowledge**
- Controller (host) will send a separate start bit
- Controller (host) sends the read address
- IDT clock will **acknowledge**
- IDT clock will send the data byte count = X
- IDT clock sends Byte **N+X-1**
- IDT clock sends **Byte 0 through Byte X (if $X_{(H)}$ was written to Byte 8)**
- Controller (host) will need to acknowledge each byte
- Controller (host) will send a not acknowledge bit
- Controller (host) will send a stop bit

Index Block Write Operation			
Controller (Host)			IDT (Slave/Receiver)
T	starT bit		
Slave Address $D2_{(H)}$			
WR	WRite		
			ACK
Beginning Byte = N			
			ACK
Data Byte Count = X			
			ACK
Beginning Byte N		X Byte	
			ACK
O			
O			O
O			O
			O
Byte N + X - 1			
			ACK
P	stoP bit		

Index Block Read Operation			
Controller (Host)			IDT (Slave/Receiver)
T	starT bit		
Slave Address $D2_{(H)}$			
WR	WRite		
			ACK
Beginning Byte = N			
			ACK
RT	Repeat starT		
Slave Address $D3_{(H)}$			
RD	ReaD		
			ACK
			Data Byte Count=X
ACK			
		X Byte	Beginning Byte N
ACK			
			O
O			O
O			O
O			
			Byte N + X - 1
N	Not acknowledge		
P	stoP bit		

Read Address	Write Address
$D3_{(H)}$	$D2_{(H)}$

NOTE: Pin numbers refer to TSSOP

SMBus Table: Output Enable Register

Byte 0	Pin #	Name	Control Function	Type	0	1	Default
Bit 7	24/25	DOT96 Enable	Output Enable	RW	Disable-Low/Low	Enable	1
Bit 6	50/49	NS_SAS1 Enable	Output Enable	RW	Disable-Low/Low	Enable	1
Bit 5	48/47	NS_SAS0 Enable	Output Enable	RW	Disable-Low/Low	Enable	1
Bit 4	44/43	NS_SRC1 Enable	Output Enable	RW	Disable-Low/Low	Enable	1
Bit 3	42/41	NS_SRC0 Enable	Output Enable	RW	Disable-Low/Low	Enable	1
Bit 2	36/35	SRC2 Enable	Output Enable	RW	Disable-Low/Low	Enable	1
Bit 1	34/33	SRC1 Enable	Output Enable	RW	Disable-Low/Low	Enable	1
Bit 0	30/31	SRC0 Enable	Output Enable	RW	Disable-Low/Low	Enable	1

SMBus Table: Output Enable Register

Byte 1	Pin #	Name	Control Function	Type	0	1	Default
Bit 7	5	REF14_3x Enable	Output Enable	RW	Disable-Low	Enable	1
Bit 6		RESERVED					0
Bit 5		RESERVED					0
Bit 4	62/61	CPU3	Output Enable	RW	Disable-Low/Low	Enable	1
Bit 3	60/59	CPU2	Output Enable	RW	Disable-Low/Low	Enable	1
Bit 2	56/55	CPU1	Output Enable	RW	Disable-Low/Low	Enable	1
Bit 1	54/53	CPU0	Output Enable	RW	Disable-Low/Low	Enable	1
Bit 0	CPU/SRC/ PCI	Spread Spectrum Enable	Spread Off/On	RW	Spread Off	Spread On	0

SMBus Table: Output Enable Register

Byte 2	Pin #	Name	Control Function	Type	0	1	Default
Bit 7		RESERVED					0
Bit 6		RESERVED					0
Bit 5	13	PCI4 Enable	Output Enable	RW	Disable-Low	Enable	1
Bit 4	14	PCI3 Enable	Output Enable	RW	Disable-Low	Enable	1
Bit 3	15	PCI2 Enable	Output Enable	RW	Disable-Low	Enable	1
Bit 2	16	PCI1 Enable	Output Enable	RW	Disable-Low	Enable	1
Bit 1	17	PCI0 Enable	Output Enable	RW	Disable-Low	Enable	1
Bit 0	21	48MHz Enable	Output Enable	RW	Disable-Low	Enable	1

SMBus Table: Differential Amplitude Control

Byte 3	Pin #	Name	Control Function	Type	0	1	Default
Bit 7		CPU AMPLITUDE 1	CPU Vhigh	RW	00 = 700mV	01 = 800mV	0
Bit 6		CPU AMPLITUDE 0		RW	10 = 900mV	11 = 1000mV	1
Bit 5		SRC AMPLITUDE 1	SRC Vhigh	RW	00 = 700mV	01 = 800mV	0
Bit 4		SRC AMPLITUDE 0		RW	10 = 900mV	11 = 1000mV	1
Bit 3		DOT96 AMPLITUDE 1	DOT96 Vhigh	RW	00 = 700mV	01 = 800mV	0
Bit 2		DOT96 AMPLITUDE 0		RW	10 = 900mV	11 = 1000mV	1
Bit 1		NS-SAS/SRC AMPLITUDE 1	NS-SAS/SRC Vhigh	RW	00 = 700mV	01 = 800mV	0
Bit 0		NS-SAS/SRC AMPLITUDE 0		RW	10 = 900mV	11 = 1000mV	1

SMBus Table: Spread Amount Register

Byte 4	Pin #	Name	Control Function	Type	0	1	Default
Bit 7		RESERVED					0
Bit 6		RESERVED					0
Bit 5		RESERVED					0
Bit 4		RESERVED					0
Bit 3		RESERVED					0
Bit 2		RESERVED					0
Bit 1		SS AMOUNT[1]	Spread Amount (note	RW	00= -0.2%	10= -0.4%	1
Bit 0		SS AMOUNT[0]	B1b0 must be set to '1')	RW	01= -0.3%	11= -0.5%	1

SMBus Table: NS_SAS/NS_SRC Frequency Margining Table

Byte 5	Pin #	Name	Control Function	Type	0	1	Default
Bit 7		RESERVED					0
Bit 6		RESERVED					0
Bit 5		RESERVED					0
Bit 4		RESERVED					0
Bit 3	-	FS3	Freq. Sel 3	RW	See NS_SAS/NS_SRC Frequency Table.		0
Bit 2	-	FS2	Freq. Sel 2	RW			1
Bit 1	-	FS1	Freq. Sel 1	RW			1
Bit 0	-	FS0	Freq. Sel 0	RW			1

SMBus Table: Test Mode and CPU/SRC/PCI Frequency Select Register

Byte 6	Pin #	Name	Control Function	Type	0	1	Default
Bit 7	-	Test Mode	Test Mode Type	RW	Hi-Z	REF/N	0
Bit 6	-	Test Select	Select Test Mode	RW	Disable	Enable	0
Bit 5	-	RESERVED					0
Bit 4	-	RESERVED					1
Bit 3	-	RESERVED					0
Bit 2	-	FS2	Freq. Sel 2	RW	See CPU/SRC/PCI Frequency Select Table		0
Bit 1	-	FS1	Freq. Sel 1	RW			1
Bit 0	-	FS0	Freq. Sel 0	RW			1

Note: Internal Pull up on 100M_133M# pin will result in default CPU frequency of 100 MHz.

SMBus Table: Vendor & Revision ID Register

Byte 7	Pin #	Name	Control Function	Type	0	1	Default
Bit 7	-	RID3	REVISION ID (1h forB rev)	R	1 for B rev		0
Bit 6	-	RID2		R			0
Bit 5	-	RID1		R			0
Bit 4	-	RID0		R			1
Bit 3	-	VID3	VENDOR ID	R	0001 for ICS/IDT		0
Bit 2	-	VID2		R			0
Bit 1	-	VID1		R			0
Bit 0	-	VID0		R			1

SMBus Table: Byte Count Register

Byte 8	Pin #	Name	Control Function	Type	0	1	Default
Bit 7	-	BC7	Byte Count Programming b(7:0)	RW	Writing to this register will configure how many bytes will be read back, default is A bytes. (0 to 9		0
Bit 6	-	BC6		RW			0
Bit 5	-	BC5		RW			0
Bit 4	-	BC4		RW			0
Bit 3	-	BC3		RW			0
Bit 2	-	BC2		RW			0
Bit 1	-	BC1		RW			0
Bit 0	-	BC0		RW			1

SMBus Table: Device ID Register

Byte 9	Pin #	Name	Control Function	Type	0	1	Default
Bit 7		DID7	Device ID (45 hex)	R	-	-	0
Bit 6		DID6		R	-	-	1
Bit 5		DID5		R	-	-	0
Bit 4		DID4		R	-	-	0
Bit 3		DID3		R	-	-	0
Bit 2		DID2		R	-	-	1
Bit 1		DID1		R	-	-	0
Bit 0		DID0		R	-	-	1

Absolute Maximum Ratings

Stresses above the ratings listed below can cause permanent damage to the 932SQL450. These ratings, which are standard values for IDT commercially rated parts, are stress ratings only. Functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods can affect product reliability. Electrical parameters are guaranteed only over the recommended operating temperature range.

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	NOTES
3.3V Core Supply Voltage	VDDA				4.6	V	1,2
3.3V Logic Supply Voltage	VDD				4.6	V	1,2
Input Low Voltage	V_{IL}		GND-0.5			V	1
Input High Voltage	V_{IH}	Except for SMBus interface			V_{DD}+0.5V	V	1
Input High Voltage	V_{IHSMB}	SMBus clock and data pins			5.5V	V	1
Storage Temperature	Ts		-65		150	°C	1
Junction Temperature	Tj				125	°C	1
Case Temperature	Tc				110	°C	1
Input ESD protection	ESD prot	Human Body Model	2000			V	1

[1]Guaranteed by design and characterization, not 100% tested in production.

[2] Operation under these conditions is neither implied nor guaranteed.

Electrical Characteristics–Current Consumption

TA = $T_{COM;}$ Supply Voltage VDD = 3.3 V +/-5%

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	NOTES
Operating Supply Current	$I_{DD3.3OP}$	All outputs active CPU@100MHz, See Test Loads.		233	265	mA	
Powerdown Current	$I_{DD3.3PDZ}$			6	10	mA	

AC Electrical Characteristics–Differential LP-HCSL Outputs (CPU, SRC, NS_SAS, NS_SRC, DOT96)

TA = $T_{COM;}$ Supply Voltage VDD = 3.3 V +/-5%

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	NOTES
Duty Cycle	t_{DC}	Measured differentially, PLL Mode	45	49.9	55	%	1
Skew, Output to Output	t_{sk3SRC}	Across all SRC outputs, V_T = 50%		40	50	ps	1
Skew, Output to Output	t_{sk3CPU}	Across all CPU outputs, V_T = 50%		19	50	ps	1
Jitter, Cycle to cycle	$t_{jcyc-cyc}$	CPU, SRC, NS_SAS outputs		15	50	ps	1,3
		DOT96 output		16	250	ps	1,3

[1]Guaranteed by design and characterization, not 100% tested in production.

[2] Zo=85Ω (differential impedance).

[3] Measured from differential waveform

Electrical Characteristics–Input/Supply/Common Parameters

TA = $T_{COM;}$ Supply Voltage VDD = 3.3 V +/-5%

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	NOTES
Ambient Operating Temperature	T_{COM}	Commmercial range	0		70	°C	
Input High Voltage	V_{IH}	Single-ended inputs, except SMBus, low threshold and tri-level inputs	2		V_{DD} + 0.3	V	
Input Low Voltage	V_{IL}	Single-ended inputs, except SMBus, low threshold and tri-level inputs	GND - 0.3		0.8	V	
Low Threshold Input-High Voltage	V_{IH_FS}	3.3 V +/-5%	0.7		V_{DD} + 0.3	V	
Low Threshold Input-Low Voltage	V_{IL_FS}	3.3 V +/-5%	V_{SS} - 0.3		0.35	V	
Input Current	I_{IN}	Single-ended inputs, V_{IN} = GND, V_{IN} = VDD	-5		5	uA	
	I_{INP}	Single-ended inputs. V_{IN} = 0 V; Inputs with internal pull-up resistors V_{IN} = VDD; Inputs with internal pull-down resistors	-200		200	uA	
Input Frequency	F_i			25.00		MHz	2
Pin Inductance	L_{pin}				7	nH	1
Capacitance	C_{IN}	Logic Inputs			5	pF	1
	C_{OUT}	Output pin capacitance			5	pF	1
	C_{INX}	X1 & X2 pins			5	pF	1
Clk Stabilization	T_{STAB}	From V_{DD} Power-Up and after input clock stabilization or de-assertion of PD# to 1st clock		0.4	1.8	ms	1,2
SS Modulation Frequency	f_{MODIN}	Allowable Frequency (Triangular Modulation)	30	31.5	33	kHz	1
Tdrive_PD#	t_{DRVPD}	Differential output enable after PD# de-assertion		98	300	us	1,3
Tfall	t_F	Fall time of control inputs			5	ns	1,2
Trise	t_R	Rise time of control inputs			5	ns	1,2
SMBus Input Low Voltage	V_{ILSMB}				0.8	V	
SMBus Input High Voltage	V_{IHSMB}		2.1		V_{DDSMB}	V	
SMBus Output Low Voltage	V_{OLSMB}	@ I_{PULLUP}			0.4	V	
SMBus Sink Current	I_{PULLUP}	@ V_{OL}	4			mA	
Nominal Bus Voltage	V_{DDSMB}	3V to 5V +/- 10%	2.7		5.5	V	
SCLK/SDATA Rise Time	t_{RSMB}	(Max VIL - 0.15) to (Min VIH + 0.15)			1000	ns	1
SCLK/SDATA Fall Time	t_{FSMB}	(Min VIH + 0.15) to (Max VIL - 0.15)			300	ns	1
SMBus Operating Frequency	f_{MAXSMB}	Maximum SMBus operating frequency			100	kHz	

[1]Guaranteed by design and characterization, not 100% tested in production.

[2]Control input must be monotonic from 20% to 80% of input swing.

[3]Time from deassertion until outputs are >200 mV

DC Electrical Characteristics–Differential LP-HCSL Outputs (CPU, SRC, NS_SAS, NS_SRC, DOT96)

$T_A = T_{COM;}$ Supply Voltage VDD = 3.3 V +/-5%

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	NOTES
Slew rate	dV/dt	Scope averaging on	1.5	2.9	4	V/ns	1,2,3
Slew rate matching	ΔdV/dt	Slew rate matching, Scope averaging on		5	20	%	1,2,4
Voltage High	VHigh	Statistical measurement on single-ended signal using oscilloscope math function. (Scope averaging on)	660	774	850	mV	
Voltage Low	VLow		-150	83	150		
Max Voltage	Vmax	Measurement on single ended signal using absolute value. (Scope		918	1150	mV	7
Min Voltage	Vmin		-300	-3			7
Vswing	Vswing	Scope averaging off	300	1359		mV	1,2
Crossing Voltage (abs)	Vcross_abs	Scope averaging off	250	432	550	mV	1,5
Crossing Voltage (var)	Δ-Vcross	Scope averaging off		14	140	mV	1,6

[1]Guaranteed by design and characterization, not 100% tested in production. Z_O=85Ω (differential impedance).

[2] Measured from differential waveform

[3] Slew rate is measured through the Vswing voltage range centered around differential 0V. This results in a +/-150mV window around differential 0V.

[4] Matching applies to rising edge rate for Clock and falling edge rate for Clock#. It is measured using a +/-75mV window centered on the average cross point where Clock rising meets Clock# falling. The median cross point is used to calculate the voltage thresholds the oscilloscope is to use for the edge rate calculations.

[5] Vcross is defined as voltage where Clock = Clock# measured on a component test board and only applies to the differential rising edge (i.e. Clock rising and Clock# falling).

[6] The total variation of all Vcross measurements in any particular system. Note that this is a subset of V_cross_min/max (V_cross absolute) allowed. The intent is to limit Vcross induced modulation by setting V_cross_delta to be smaller than

[7] Includes overshoot and undershoot.

[8] Measured from single-ended waveform

[9] Measured with scope averaging off, using statistics function. Variation is difference between min and max.

Electrical Characteristics–48MHz

T_A = 0 - 70°C; Supply Voltage V_{DD}/V_{DDA} = 3.3 V +/-5%,

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	NOTES
Output Impedance	R_{DSP}	$V_O = V_{DD}*(0.5)$	12	21.7	55	Ω	1
Output High Voltage	V_{OH}	I_{OH} = -1 mA	2.4			V	
Output Low Voltage	V_{OL}	I_{OL} = 1 mA			0.55	V	
Clock High Time	T_{HIGH}	1.5V	8.094		10.036	ns	1
Clock Low Time	T_{LOW}	1.5V	7.694		9.836	ns	1
Edge Rate	t_{slewr/f_USB}	Rising/Falling edge rate	1		2.3	V/ns	1,2
Duty Cycle	d_{t1}	V_T = 1.5 V	45	50.4	55	%	1
Jitter, Cycle to cycle	$t_{jcyc-cyc}$	V_T = 1.5 V			350	ps	1

See "Power Supply and Test Loads" page for termination circuits

[1]Guaranteed by design and characterization, not 100% tested in production.

[2] Measured between 0.8V and 2.0V

Electrical Characteristics–Phase Jitter Parameters

T_A = 0 - 70°C; Supply Voltage V_{DD}/V_{DDA} = 3.3 V +/-5%,

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	INDUST. LIMIT	UNITS	Notes
Phase Jitter	$t_{jphPCIeG1}$	PCIe Gen 1		35	39	86	ps (p-p)	1,2,3, 6
	$t_{jphPCIeG2}$	PCIe Gen 2 Lo Band 10kHz < f < 1.5MHz		1.52	1.84	3	ps (rms)	1,2,6
		PCIe Gen 2 High Band 1.5MHz < f < Nyquist (50MHz)		2.19	2.42	3.1	ps (rms)	1,2,6
	$t_{jphPCIeG3}$	PCIe Gen 3 (PLL BW of 2-4MHz, CDR = 10MHz)		0.51	0.59	1	ps (rms)	1,2,4, 6
	t_{jphQPI_SMI}	QPI & SMI (100MHz, 4.8Gb/s, 6.4Gb/s 12UI)		0.25	0.37	0.5	ps (rms)	1,5,7
		QPI & SMI (100MHz, 8.0Gb/s, 12UI)		0.18	0.23	0.3	ps (rms)	1,5,7
		QPI & SMI (100MHz, 9.6Gb/s, 12UI)		0.15	0.19	0.2	ps (rms)	1,5,7
	$t_{jphSAS12G}$	SAS 12G		1.15	1.27	1.3	ps (rms)	1,5,8

[1] Guaranteed by design and characterization, not 100% tested in production.

[2] See http://www.pcisig.com for complete specs

[3] Sample size of at least 100K cycles. This figures extrapolates to 108ps pk-pk @ 1M cycles for a BER of 1-12.

[4] Subject to final radification by PCI SIG.

[5] Calculated from Intel-supplied Clock Jitter Tool v 1.6.6

[6] Applied to SRC outputs

[7] Applies to CPU outputs

[8] Applies to NS_SAS, NS_SRC outputs, Spread Off

Electrical Characteristics–PCI

T_A = 0 - 70°C; Supply Voltage V_{DD}/V_{DDA} = 3.3 V +/-5%,

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	NOTES
Output Impedance	R_{DSP}	$V_O = V_{DD}*(0.5)$	12	22	55	Ω	1
Output High Voltage	V_{OH}	I_{OH} = -1 mA	2.4			V	
Output Low Voltage	V_{OL}	I_{OL} = 1 mA			0.55	V	
Clock High Time	T_{HIGH}	1.5V	12			ns	1
Clock Low Time	T_{LOW}	1.5V	12			ns	1
Edge Rate	$t_{slewr/f}$	Rising/Falling edge rate	1	1.7	4	V/ns	1,2
Duty Cycle	d_{t1}	V_T = 1.5 V	45	50.4	55	%	1
Group Skew	t_{skew}	V_T = 1.5 V		197	500	ps	1
Jitter, Cycle to cycle	$t_{jcyc-cyc}$	V_T = 1.5 V		45.52	500	ps	1

See "Power Supply and Test Loads" page for termination circuits

[1]Guaranteed by design and characterization, not 100% tested in production.

[2] Measured between 0.8V and 2.0V

Electrical Characteristics–REF14M

T_A = 0 - 70°C; Supply Voltage V_{DD}/V_{DDA} = 3.3 V +/-5%,

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	Notes
Output Impedance	R_{DSP}	$V_O = V_{DD}*(0.5)$	12	21.7	55	Ω	1
Output High Voltage	V_{OH}	I_{OH} = -1 mA	2.4			V	
Output Low Voltage	V_{OL}	I_{OL} = 1 mA			0.55	V	
Clock High Time	T_{HIGH}	1.5V	27.5			ns	1
Clock Low Time	T_{LOW}	1.5V	27.5			ns	1
Edge Rate	$t_{slewr/f}$	Rising/Falling edge rate	1	1.9	4	V/ns	1,2
Duty Cycle	d_{t1}	V_T = 1.5 V	45	50.1	55	%	1
Jitter, Cycle to cycle	$t_{jcyc-cyc}$	V_T = 1.5 V		42	1000	ps	1

See "Power Supply and Test Loads" page for termination circuits

[1]Guaranteed by design and characterization, not 100% tested in production.

[2] Measured between 0.8V and 2.0V

Test Clarification Table

Comments	HW		SW		
	TEST_SEL HW PIN	TEST_MODE HW PIN	TEST ENTRY BIT B6b6	REF/N or HI-Z B6b7	OUTPUT
	0	X	0	X	NORMAL
Power-up w/ TEST_SEL = 1 (>0.7V) to enter test mode. Cycle power to disable test mode.	1	0	X	0	HI-Z
	1	0	X	1	REF/N
	1	1	X	0	REF/N
	1	1	X	1	REF/N
If TEST_SEL HW pin is 0 during power-up, test mode can be selected through B6b6. If test mode is selected by B6b6, then B6b7 is used to select HI-Z or REF/N FS_B/TEST_Mode pin is not used. Cycle power to disable test mode.	0	X	1	0	HI-Z
	0	X	1	1	REF/N

B6b6: 1= ENTER TEST MODE, Default = 0 (NORMAL OPERATION)

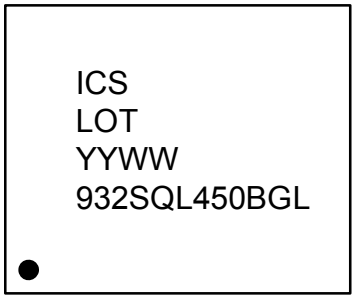
B6b7: 1= REF/N, Default = 0 (HI-Z)

Recommended Crystal Characteristics (3225 package)

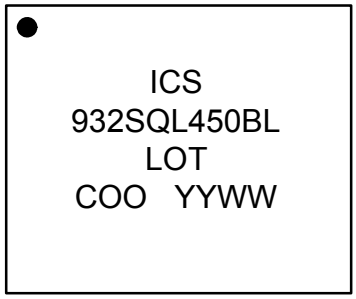
PARAMETER	VALUE	UNITS	NOTES
Frequency	25	MHz	1
Resonance Mode	Fundamental	-	1
Frequency Tolerance @ 25°C	±20	PPM Max	1
Frequency Stability, ref @ 25°C Over Operating Temperature Range	±20	PPM Max	1
Temperature Range (commerical)	0~70	°C	1
Temperature Range (industrial)	-40~85	°C	2
Equivalent Series Resistance (ESR)	50	Ω Max	1
Shunt Capacitance (C_O)	7	pF Max	1
Load Capacitance (C_L)	8	pF Max	1
Drive Level	0.3	mW Max	1
Aging per year	±5	PPM Max	1

Notes:
1. Fox Electronics 603-25-150 or equivalent
2. For I-temp, contact Fox Electronics at Foxonline.com

Marking Diagrams



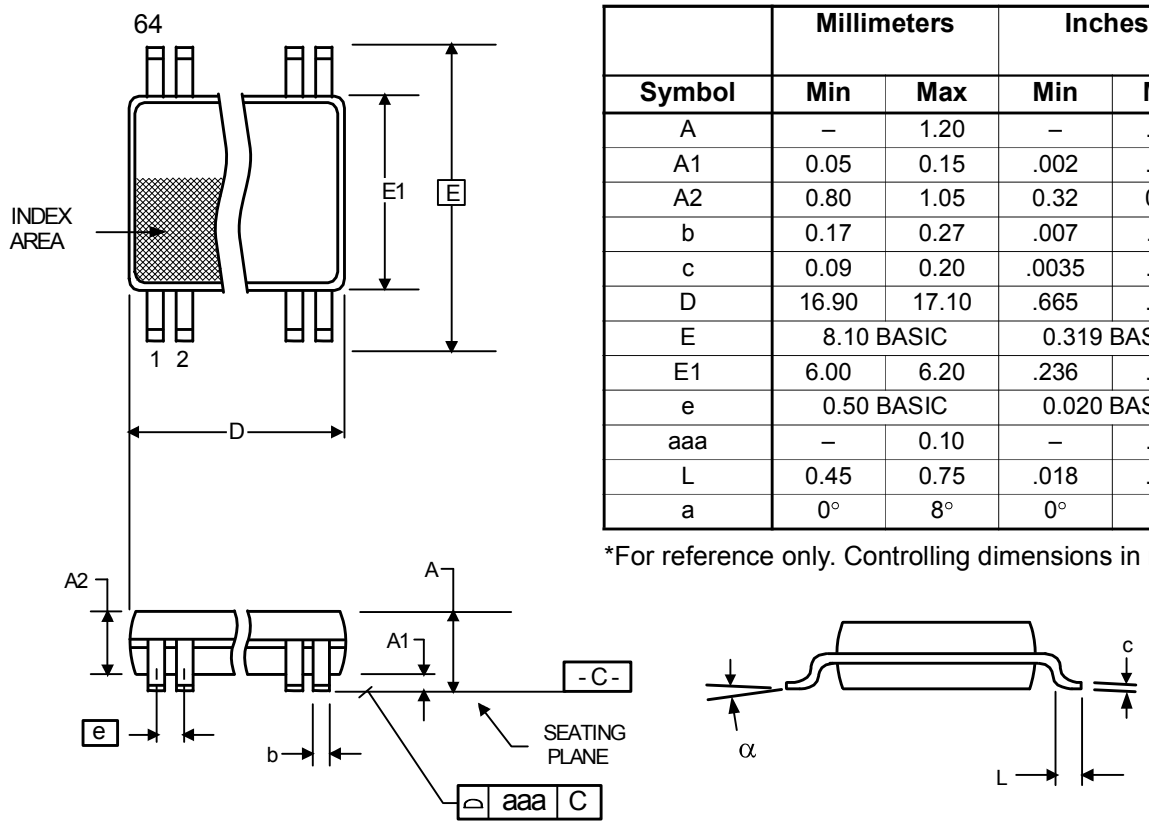
64TSSOP



64VFQFPN

Notes:
1. “L” denotes Pb-free, RoHS compliant.
2. “LOT” denotes the lot number.
3. “YYWW” denotes the last two digits and week the part was assembled.
4. “COO” denotes the country of origin.
5. “B” denotes the device revision designator.
6. Bottom marking (TSSOP only): country of origin.

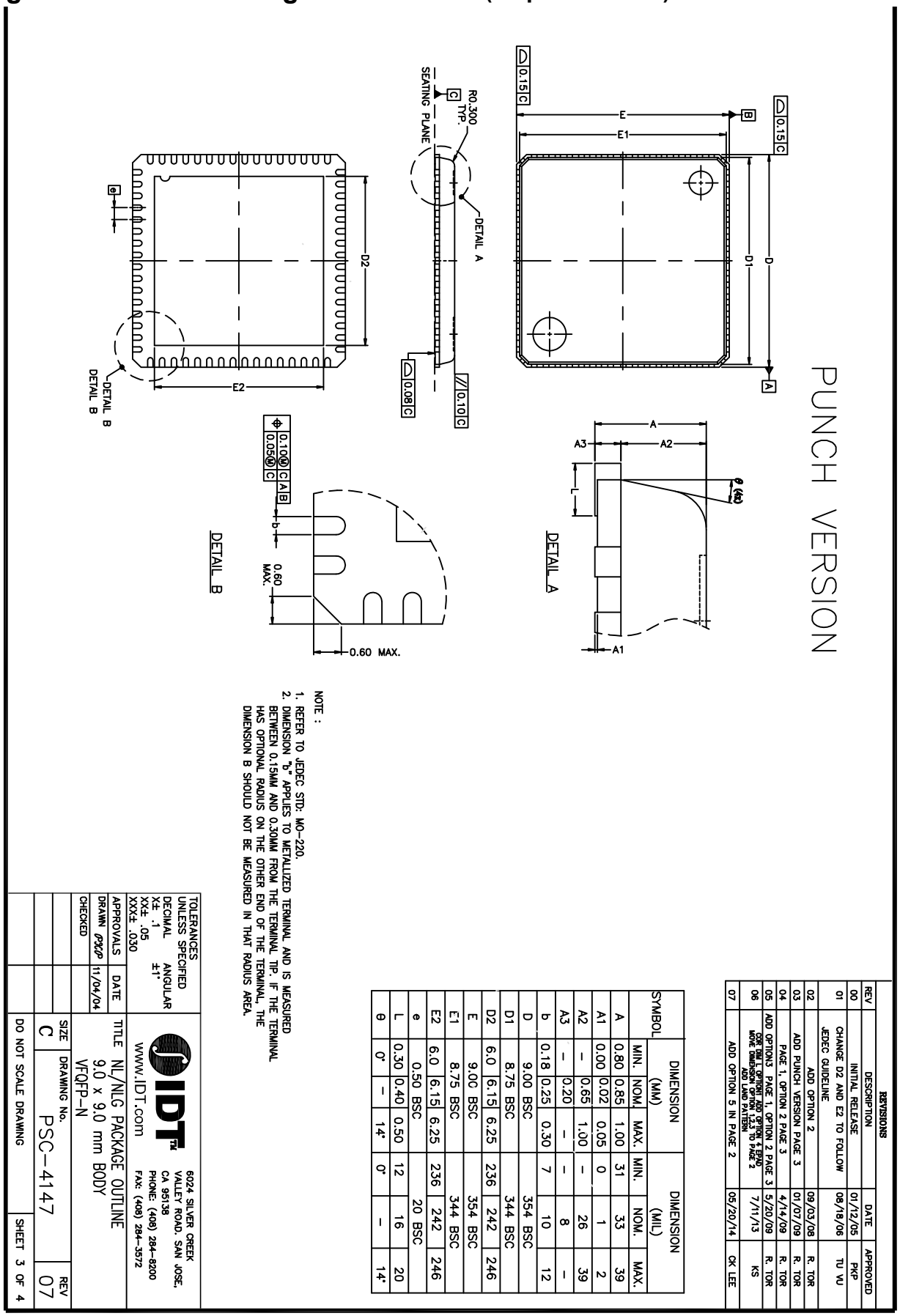
Package Outline and Package Dimensions (64-pin TSSOP)



	Millimeters		Inches*	
Symbol	**Min**	**Max**	**Min**	**Max**
A	–	1.20	–	.047
A1	0.05	0.15	.002	.006
A2	0.80	1.05	0.32	0.41
b	0.17	0.27	.007	.011
c	0.09	0.20	.0035	.008
D	16.90	17.10	.665	.673
E	8.10 BASIC		0.319 BASIC	
E1	6.00	6.20	.236	.244
e	0.50 BASIC		0.020 BASIC	
aaa	–	0.10	–	.004
L	0.45	0.75	.018	.030
a	0°	8°	0°	8°

*For reference only. Controlling dimensions in mm.

Package Outline and Package Dimensions (64-pin VFQFPN)



NOTE :

1. REFER TO JEDEC STD: MO-220.
2. DIMENSION "b" APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.15MM AND 0.30MM FROM THE TERMINAL TIP. IF THE TERMINAL HAS OPTIONAL RADIUS ON THE OTHER END OF THE TERMINAL, THE DIMENSION B SHOULD NOT BE MEASURED IN THAT RADIUS AREA.

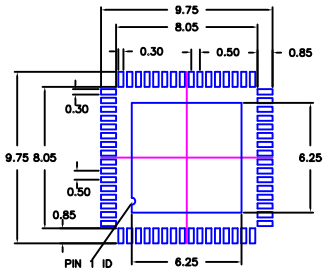
SYMBOL	DIMENSION (MM)			DIMENSION (MIL)		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.80	0.85	1.00	31	33	39
A1	0.00	0.02	0.05	0	1	2
A2	–	0.65	1.00	–	26	39
A3	–	0.20	–	–	8	–
b	0.18	0.25	0.30	7	10	12
D	9.00 BSC			354 BSC		
D1	8.75 BSC			344 BSC		
D2	6.0	6.15	6.25	236	242	246
E	9.00 BSC			354 BSC		
E1	8.75 BSC			344 BSC		
E2	6.0	6.15	6.25	236	242	246
e	0.50 BSC			20 BSC		
L	0.30	0.40	0.50	12	16	20
θ	0°	–	14°	0°	–	14°

REV	DESCRIPTION	DATE	APPROVED
00	INITIAL RELEASE	01/12/05	PKP
01	CHANGE D2 AND E2 TO FOLLOW JEDEC GUIDELINE	08/18/06	TU VU
02	ADD OPTION 2 ADD PUNCH VERSION PAGE 3	09/03/08	R. TOR
03	PAGE 1, OPTION 2 PAGE 3	01/07/09	R. TOR
04	ADD OPTION3 PAGE 1, OPTION 2 PAGE 3	4/14/09	R. TOR
05	CORRECT OPTION, ADD OPTION 4 EPAD MOVE DIMENSION OPTION 1,2,3 TO PAGE 2 ADD LAND PATTERN	5/20/09	R. TOR
06		7/11/13	KS
07	ADD OPTION 5 IN PAGE 2	05/20/14	CK LEE

TOLERANCES UNLESS SPECIFIED DECIMAL ANGULAR X± .1 ±1° XX± .05 XXX± .030	IDT™ www.IDT.com	6024 SILVER CREEK VALLEY ROAD. SAN JOSE. CA 95138 PHONE: (408) 284-8200 FAX: (408) 284-3572	
APPROVALS DATE	TITLE NL/NLG PACKAGE OUTLINE 9.0 x 9.0 mm BODY VFQFP-N		
DRAWN PKP 11/04/04			
CHECKED	SIZE C	DRAWING No. PSC-4147	REV 07
DO NOT SCALE DRAWING			SHEET 3 OF 4

Package Outline and Package Dimensions (64-pin VFQFPN), cont.

REVISIONS			
REV	DESCRIPTION	DATE	APPROVED
00	INITIAL RELEASE	01/12/05	PKP
01	CHANGE D2 AND E2 TO FOLLOW JEDEC GUIDELINE	08/18/06	TU VU
02	ADD OPTION 2	09/03/08	R. TOR
03	ADD PUNCH VERSION PAGE 3	01/07/09	R. TOR
04	PAGE 1, OPTION 2 PAGE 3	4/14/09	R. TOR
05	ADD OPTION3 PAGE 1, OPTION 2 PAGE 3	5/20/09	R. TOR
06	COR DIM L OPTION1 ADD OPTION 4 EPAD MOVE DIMENSION OPTION 1,2,3 TO PAGE 2 ADD LAND PATTERN	7/11/13	KS
07	ADD OPTION 5 IN PAGE 2	05/20/14	CK LEE



NOTES:
1. ALL DIMENSION ARE IN mm. ANGLES IN DEGREES.
2. TOP DOWN VIEW. AS VIEWED ON PCB.
3. LAND PATTERN IN BLUE. NSMD PATTERN ASSUMED.
4. LAND PATTERN RECOMMENDATION PER IPC-7351B LP CALCULATOR.

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APPROVALS	DATE	TITLE	NL/NLG PACKAGE OUTLINE 9.0 x 9.0 mm BODY VFQFP-N
DRAWN PKP	11/04/04		
CHECKED		SIZE C	DRAWING No. PSC-4147 REV 07
		DO NOT SCALE DRAWING	SHEET 4 OF 4

Ordering Information

Part / Order Number	Shipping Packaging	Package	Temperature
932SQL450BGLF	Tubes	64-pin TSSOP	0 to +70° C
932SQL450BGLFT	Tape and Reel	64-pin TSSOP	0 to +70° C
932SQL450BKLF	Tray	64-pin VFQFPN	0 to +70° C
932SQL450BKLFT	Tape and Reel	64-pin VFQFPN	0 to +70° C

"LF" suffix to the part number are the Pb-Free configuration and are RoHS compliant.

“B” is the device revision designator (will not correlate with the datasheet revision).

Revision History

Rev.	Issue Date	Who	Description	Page #
A	3/5/2014	RDW	1. Updated electrical table format and data to final. 2. Updated TEST_SEL pin description and TEST CLARIFICATION TABLE to indicate that this input is a low threshold input. 3. Updated TEST LOADS and added ALTERNATE TERMINATIONS diagrams. 4. Updated block diagram to latest format and updated pin names to match the pinout. 5. Updated front page text to latest format 6. Move to Final.	Various
B	3/6/2015	RDW	1. Corrected typo in Powerdown Current max limit. Max limit changed from 9mA to 10mA.	13

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(Rev.1.0 Mar 2020)

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