Frequency Generator with 200MHz Differential CPU Clocks

Recommended Application:

CK-408 clock for BANIAS processor/ ODEM and MONTARA-G chipsets.

Output Features:

- 3 0.7V Differential CPU Clock Pairs
- 7 PCI (3.3V) @ 33.3MHz
- 3 PCI_F (3.3V) @ 33.3MHz
- 1 USB (3.3V) @ 48MHz
- 1 DOT (3.3V) @ 48MHz
- 1 REF (3.3V) @ 14.318MHz
- 5 3V66 (3.3V) @ 66.6MHz
- 1 VCH/3V66 (3.3V) @ 48MHz or 66.6MHz

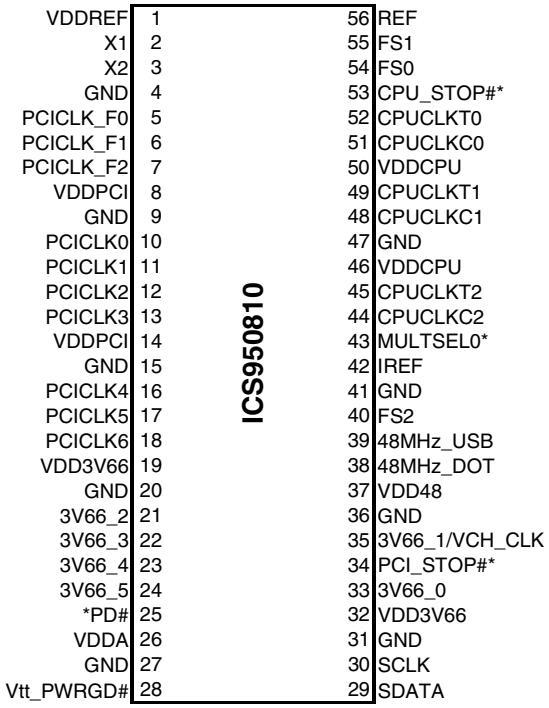
Features:

- Supports spread spectrum modulation, down spread 0 to -0.5%. (CPU, 3V66, PCI)
- Efficient power management scheme through PD#, CPU_STOP# and PCI_STOP#.

Key Specifications:

- CPU Output Jitter <150ps
- 3V66 Output Jitter <250ps
- CPU Output Skew <100ps

Pin Configuration

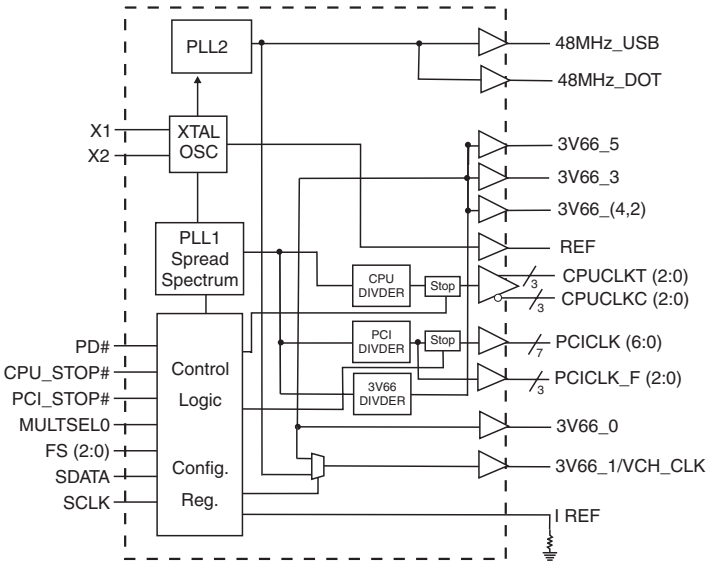


56-Pin 300mil SSOP

6.10 mm. Body, 0.50 mm. pitch TSSOP

* These inputs have 150K internal pull-up resistor to VDD.

Block Diagram



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Functionality

FS2	FS1	FS0	CPU (MHz)	3V66(5:0) (MHz)	PCI_F PCI (MHz)
X	0	0	166.66	66.66	33.33
X	0	1	100.00	66.66	33.33
X	1	0	200.00	66.66	33.33
X	1	1	133.33	66.66	33.33
Mid	0	0	Tristate	Tristate	Tristate
Mid	0	1	TCLK/2	TCLK/4	TCLK/8
Mid	1	0	Reserved	Reserved	Reserved
Mid	1	1	Reserved	Reserved	Reserved

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Pin Configuration

PIN NUMBER	PIN NAME	TYPE	DESCRIPTION
1	VDDREF	PWR	Ref, XTAL power supply, nominal 3.3V
2	X1	IN	Crystal input,nominally 14.318MHz.
3	X2	OUT	Crystal output, nominally 14.318MHz.
4	GND	PWR	Ground pin for 3V outputs.
5	PCICLK_F0	OUT	Free running PCI clock not affected by PCI_STOP# .
6	PCICLK_F1	OUT	Free running PCI clock not affected by PCI_STOP# .
7	PCICLK_F2	OUT	Free running PCI clock not affected by PCI_STOP# .
8	VDDPCI	PWR	Power supply for PCICLK_F and PCICLK, nominal 3.3V
9	GND	PWR	Ground pin for 3V outputs.
10	PCICLK0	OUT	PCI clock outputs.
11	PCICLK1	OUT	PCI clock outputs.
12	PCICLK2	OUT	PCI clock outputs.
13	PCICLK3	OUT	PCI clock outputs.
14	VDDPCI	PWR	Power supply for PCICLK_F and PCICLK, nominal 3.3V
15	GND	PWR	Ground pin for 3V outputs.
16	PCICLK4	OUT	PCI clock outputs.
17	PCICLK5	OUT	PCI clock outputs.
18	PCICLK6	OUT	PCI clock outputs.
19	VDD3V66	PWR	Power pin for the 3V66 clocks.
20	GND	PWR	Ground pin for 3V outputs.
21	3V66_2	OUT	66MHz outputs at 3.3V.
22	3V66_3	OUT	66MHz outputs at 3.3V.
23	3V66_4	OUT	66MHz outputs at 3.3V.
24	3V66_5	OUT	66MHz input/output at 3.3V.
25	PD#	IN	Asynchronous active low input pin used to power down the device into a low power state. The internal clocks are disabled and the VCO and the crystal are stopped. The latency of the power down will not be greater than 3ms.
26	VDDA	PWR	3.3V power for the PLL core.
27	GND	PWR	Ground pin for 3V outputs.

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Pin Configuration (Continued)

PIN NUMBER	PIN NAME	TYPE	DESCRIPTION
28	Vtt_PWRGD#	IN	This 3.3V LVTTL input is a level sensitive strobe used to determine when FS[2:0] and MULTISEL0 inputs are valid and are ready to be sampled. (active low)
29	SDATA	I/O	Data pin for I2C circuitry 5V tolerant
30	SCLK	IN	Clock pin of I2C circuitry 5V tolerant
31	GND	PWR	Ground pin for 3V outputs.
32	VDD3V66	PWR	Power pin for the 3V66 clocks.
33	3V66_0	OUT	66MHz outputs at 3.3V.
34	PCI_STOP#	IN	Stops all PCICLKs besides the PCICLK_F clocks at logic 0 level, when input low
35	3V66_1/VCH_CLK	OUT	Selectable 48MHz non-SSC or 66MHz SSC clock output
36	GND	PWR	Ground pin for 3V outputs.
37	VDD48	PWR	Power for 48MHz output buffers and fixed PLL core.
38	48MHz_DOT	OUT	48MHz output clock
39	48MHz_USB	OUT	48MHz output clock
40	FS2	IN	Frequency select pin.
41	GND	PWR	Ground pin for 3V outputs.
42	IREF	OUT	This pin festablishes the reference current for the CPUCLK pairs. This pin requires a fixed precision resistor tied to ground in order to establish the appropriate current.
43	MULTSEL0	IN	3.3V LVTTL input for selection the current multiplier for CPU outputs
44	CPUCLKC2	OUT	"Complementary" clocks of differential pair CPU outputs. These are current mode outputs. External resistors are required for voltage bias.
45	CPUCLKT2	OUT	"True" clocks of differential pair CPU outputs. These are current mode outputs. External resistors are required for voltage bias.
46	VDDCPU	PWR	Supply for CPU clocks,3.3V nominal
47	GND	PWR	Ground pin for 3V outputs.
48	CPUCLKC1	OUT	"Complementary" clocks of differential pair CPU outputs. These are current mode outputs. External resistors are required for voltage bias.
49	CPUCLKT1	OUT	"True" clocks of differential pair CPU outputs. These are current mode outputs. External resistors are required for voltage bias.
50	VDDCPU	PWR	Supply for CPU clocks,3.3V nominal
51	CPUCLKC0	OUT	"Complementary" clocks of differential pair CPU outputs. These are current mode outputs. External resistors are required for voltage bias.
52	CPUCLKT0	OUT	"True" clocks of differential pair CPU outputs. These are current mode outputs. External resistors are required for voltage bias.
53	CPU_STOP#	IN	This asynchronous input halts to active low level when driven low.
54	FS0	IN	Frequency select pin.
55	FS1	IN	Frequency select pin.
56	REF	OUT	14.318 MHz reference clock.

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Power Groups

(Analog)
VDDA = PLL1
VDD48 = 48MHz, PLL
VDDREF = VDD for Xtal, POR

(Digital)
VDDPCI
VDD3V66
VDDCPU

Truth Table

FS2	FS1	FS0	CPU (MHz)	3V66 (5:0) (MHz)	PCI_F PCI (MHz)	REF0 (MHz)	USB/DOT (MHz)
X	0	0	166.66	66.66	33.33	14.318	48.00
X	0	1	100.00	66.66	33.33	14.318	48.00
X	1	0	200.00	66.66	33.33	14.318	48.00
X	1	1	133.33	66.66	33.33	14.318	48.00
Mid	0	0	Tristate	Tristate	Tristate	Tristate	Tristate
Mid	0	1	TCLK/2	TCLK/4	TCLK/8	TCLK	TCLK/2
Mid	1	0	Reserved	Reserved	Reserved	Reserved	Reserved
Mid	1	1	Reserved	Reserved	Reserved	Reserved	Reserved

Maximum Allowed Current

Condition	Max 3.3V supply consumption Max discrete cap loads, Vdd = 3.465V All static inputs = Vdd or GND
Powerdown Mode (PWRDWN# = 0)	25mA
Full Active	360mA

Host Swing Select Functions

MULTISEL0	Board Target Trace/Term Z	Reference R, Iref = V_{DD}/(3*Rr)	Output Current	Voh @ Z
0	-	-	-	-
1	50 ohms	Rr = 475 1%, Iref = 2.32mA	Ioh = 6* I REF	0.7V @ 50

NOTE: MULTSEL0 = 0 not supported in ICS950810. Refer to ICS950805 for Buffered Mode support.

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Power Management

PD#	CPU_STOP#	PCI_STOP#	VCO	CPU	CPU#	PCICLK	3v66	48MHz	REF
0	X	X	STOP	Iref*2	FLOAT	LOW	LOW	LOW	LOW
1	1	1	RUN	RUN	RUN	RUN	RUN	RUN	RUN
1	0	1	RUN	Iref*2	FLOAT	RUN	RUN	RUN	RUN
1	1	0	RUN	RUN	RUN	LOW	RUN	RUN	RUN
1	1	1	RUN	RUN	RUN	RUN	RUN	RUN	RUN

Note: PCI_F is not affected by PCI_STOP# and CPU_STOP#

Tri-State Control of CPU Outputs

State	Byte0 bit6 PD#	Byte1bit6 Cpu_stop#	Pin PD#	Pin Cpu_Stop#	Stoppable CPU outputs	Free-Running CPU outputs
0	0	0	1	1	Running	Running
1	0	0	1	0	Irefx6	Running
2	0	0	0	1	Irefx2	Irefx2
3	0	0	0	0	Irefx2	Irefx2
4	0	1	1	1	Running	Running
5	0	1	1	0	Hi-Z	Running
6	0	1	0	1	Hi-Z	Irefx2
7	0	1	0	0	Hi-Z	Irefx2
8	1	0	1	1	Running	Running
9	1	0	1	0	Irefx6	Running
10	1	0	0	1	Hi-Z	Hi-Z
11	1	0	0	0	Hi-Z	Hi-Z
12	1	1	1	1	Running	Running
13	1	1	1	0	Hi-Z	Running
14	1	1	0	1	Hi-Z	Hi-Z
15	1	1	0	0	Hi-Z	Hi-Z

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Absolute Maximum Ratings

Supply Voltage . . . . . 5.5 V

Logic Inputs . . . . . GND –0.5 V to V_{DD} +0.5 V

Ambient Operating Temperature . . . . . 0°C to +85°C

Case Temperature . . . . . 115°C

Storage Temperature . . . . . –65°C to +150°C

Stresses above those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only and functional operation of the device at these or any other conditions above those listed in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Electrical Characteristics - Input/Supply/Common Output Parameters

T_A = 0 - 70°C; Supply Voltage V_{DD} = 3.3 V +/-5%

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input High Voltage	V_{IH}		2		V_{DD} +0.3	V
Input Low Voltage	V_{IL}		V_{SS} -0.3		0.8	V
Input High Current	I_{IH}	V_{IN} = V_{DD}	-5		5	µA
Input Low Current	I_{IL1}	V_{IN} = 0 V; Inputs with no pull-up resistors	-5			µA
	I_{IL2}	V_{IN} = 0 V; Inputs with pull-up resistors	-200			µA
Operating Supply Current	$I_{DD3.3OP}$	C_L = Full load; Select @ 100 MHz	229	230	360	mA
	$I_{DD3.3OP}$	C_L =Full load; Select @ 133 MHz	220	233	360	mA
Powerdown Current	$I_{DD3.3PD}$	IREF=2.32 mA		22	25	mA
Input Frequency	F_i	V_{DD} = 3.3 V		14.318		MHz
Pin Inductance	L_{pin}				7	nH
Input Capacitance[1]	C_{IN}	Logic Inputs			5	pF
	C_{OUT}	Output pin capacitance			6	pF
	C_{INX}	X1 & X2 pins	27	30	45	pF
Clk Stabilization[1,2]	T_{STAB}	From PowerUp or deassertion of PowerDown to 1st clock.		1	1.8	ms
Delay[1]	t_{PZH},t_{PZL}	Output enable delay (all outputs)	1		10	ns
	t_{PHZ},t_{PLZ}	Output disable delay (all outputs)	1		10	ns

[1]Guaranteed by design, not 100% tested in production.

[2]See timing diagrams for buffered and un-buffered timing requirements.

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Electrical Characteristics - CPU (0.7V Select)

T_A = 0 - 70°C; VDD=3.3V +/-5%; C_L = 10-20 pF (unless otherwise specified)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Current Source Output Impedance	Zo[1]	$V_O = V_x$	3000			Ω
Voltage High	VHigh	Statistical measurement on single ended signal using	660	810	850	mV
Voltage Low	VLow		-150	20	150	
Max Voltage	Vovs	Measurement on single ended signal using absolute value.		850	1150	mV
Min Voltage	Vuds		-450	-15		
Crossing Voltage (abs)	Vcross(abs)		250	380	550	mV
Crossing Voltage (var)	d-Vcross	Variation of crossing over all edges		22	140	mV
Rise Time	t_r	V_{OL} = 0.175V, V_{OH} = 0.525V	175	290	700	ps
Fall Time	t_f	V_{OH} = 0.525V V_{OL} = 0.175V	175	310	700	ps
Rise Time Variation	d-t_r			10	125	ps
Fall Time Variation	d-t_f			10	125	ps
Duty Cycle	d_{t3}	Measurement from differential wavefrom	45	51	55	%
Skew	t_{sk3}	V_T = 50%		16	100	ps
Jitter, Cycle to cycle	$t_{jcyc-cyc}$[1]	V_T = 50%		48	150	ps

[1]Guaranteed by design, not 100% tested in production.

[2] I_{OWT} can be varied and is selectable thru the MULTSEL pin.

Electrical Characteristics - PCICLK

T_A = 0 - 70°C; VDD=3.3V +/-5%; C_L = 10-30 pF (unless otherwise specified)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output Impedance	R_{DSP1}[1]	$V_O = V_{DD}$*(0.5)	12	33	55	W
Output High Voltage	V_{OH}[1]	I_{OH} = -1 mA	2.4	3.28		V
Output Low Voltage	V_{OL}[1]	I_{OL} = 1 mA		0.08	0.55	V
Output High Current	I_{OH}[1]	$V_{OH@MIN}$ = 1.0 V	-33	-110		
		$V_{OH@MAX}$ = 3.135 V		-20	-33	mA
Output Low Current	I_{OL}[1]	$V_{OL@MIN}$ = 1.95 V	30	110		
		$V_{OL@MAX}$ = 0.4 V		37	38	mA
Rise Time	t_{r1}[1]	V_{OL} = 0.4 V, V_{OH} = 2.4 V	0.5	1.28	2	ns
Fall Time	t_{f1}[1]	V_{OH} = 2.4 V, V_{OL} = 0.4 V	0.5	1.37	2	ns
Duty Cycle	d_{t1}[1]	V_T = 1.5 V	45	51.1	55	%
Skew	t_{sk1}[1]	V_T = 1.5 V		127	500	ps
Jitter,cycle to cyc	$t_{jcyc-cyc}$[1]	V_T = 1.5 V		164	250	ps

[1]Guaranteed by design, not 100% tested in production.

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Electrical Characteristics - 3V66 Mode: 3V66 [5:0]

T_A = 0 - 70°C; VDD=3.3V +/-5%; C_L = 10-30 pF (unless otherwise specified)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output Impedance	R_{DSP1}[1]	$V_O = V_{DD}*(0.5)$	12	33	55	Ω
Output High Voltage	V_{OH}[1]	I_{OH} = -1 mA	2.4	3.28		V
Output Low Voltage	V_{OL}[1]	I_{OL} = 1 mA		0.08	0.55	V
Output High Current	I_{OH}[1]	$V_{OH@MIN}$ = 1.0 V	-33	-110		
		$V_{OH@MAX}$ = 3.135 V		-20	-33	mA
Output Low Current	I_{OL}[1]	$V_{OL@MIN}$ = 1.95 V	30	110		
		$V_{OL@MAX}$ = 0.4 V		37	38	mA
Rise Time	t_{r1}[1]	V_{OL} = 0.4 V, V_{OH} = 2.4 V	0.5	1.15	2	ns
Fall Time	t_{f1}[1]	V_{OH} = 2.4 V, V_{OL} = 0.4 V	0.5	1.53	2	ns
Duty Cycle	d_{t1}[1]	V_T = 1.5 V	45	51.3	55	%
Skew	t_{sk1}[1]	V_T = 1.5 V		67	250	ps
Jitter	$t_{icyc-cyc}$[1]	V_T = 1.5 V 3V66		175	250	ps

[1]Guaranteed by design, not 100% tested in production.

Electrical Characteristics - VCH, 48MHz DOT, 48MHz, USB

T_A = 0 - 70°C; VDD=3.3V +/-5%; C_L = 10-20 pF (unless otherwise specified)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output Impedance	R_{DSP1}[1]	$V_O = V_{DD}*(0.5)$	20	48	60	Ω
Output High Voltage	V_{OH}[1]	I_{OH} = -1 mA	2.4	3.27		V
Output Low Voltage	V_{OL}[1]	I_{OL} = 1 mA		0.08	0.4	V
Output High Current	I_{OH}[1]	$V_{OH@MIN}$ = 1.0 V	-29	-61		
		$V_{OH@MAX}$ = 3.135 V		-12	-23	mA
Output Low Current	I_{OL}[1]	$V_{OL@MIN}$ = 1.95 V	29			
		$V_{OL@MAX}$ = 0.4 V			27	mA
48DOT Rise Time	t_{r1}[1]	V_{OL} = 0.4 V, V_{OH} = 2.4 V	0.5	0.69	1	ns
48DOT Fall Time	t_{f1}[1]	V_{OH} = 2.4 V, V_{OL} = 0.4 V	0.5	0.81	1	ns
VCH 48 USB Rise Time	t_{r1}[1]	V_{OL} = 0.4 V, V_{OH} = 2.4 V	1	1.37	2	ns
VCH 48 USB Fall Time	t_{f1}[1]	V_{OH} = 2.4 V, V_{OL} = 0.4 V	1	1.47	2	ns
48 DOT Duty Cycle	d_{t1}[1]	V_T = 1.5 V	45	51.2	55	%
VCH 48 USB Duty Cycle	d_{t1}[1]	V_T = 1.5 V	45	53.5	55	%
48 DOT Jitter	$t_{icyc-cyc}$[1]	V_T = 1.5 V		111	350	ps
48 USB Jitter	$t_{icyc-cyc}$[1]	V_T = 1.5 V		99	350	ps
USB to DOT Skew	t_{sk1}[1]	V_T = 1.5 V (0 OR 180 degrees)			1	ns
VCH Jitter	$t_{icyc-cyc}$[1]	V_T = 1.5 V		147	350	ps

[1]Guaranteed by design, not 100% tested in production.

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Electrical Characteristics - REF

T_A = 0 - 70°C; VDD=3.3V +/-5%; C_L = 10-20 pF (unless otherwise specified)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output Impedance	R_{DSP1}[1]	$V_O = V_{DD}*(0.5)$	20	48	60	Ω
Output High Voltage	V_{OH}[1]	I_{OH} = -1 mA	2.4	3.28		V
Output Low Voltage	V_{OL}[1]	I_{OL} = 1 mA		0.08	0.4	V
Output High Current	I_{OH}[1]	$V_{OH@MIN}$ = 1.0 V	-33	-110		
		$V_{OH@MAX}$ = 3.135 V		-20	-33	mA
Output Low Current	I_{OL}[1]	$V_{OL@MIN}$ = 1.95 V	30	110		
		$V_{OL@MAX}$ = 0.4 V		37	38	mA
Rise Time	t_{r1}[1]	V_{OL} = 0.4 V, V_{OH} = 2.4 V	1	1.69	2	ns
Fall Time	t_{f1}[1]	V_{OH} = 2.4 V, V_{OL} = 0.4 V	1	1.56	2	ns
Duty Cycle	d_{t1}[1]	V_T = 1.5 V	45	53	55	%
Jitter	$t_{jcyc-cyc}$[1]	V_T = 1.5 V		152	1000	ps

[1]Guaranteed by design, not 100% tested in production.

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General I²C serial interface information

The information in this section assumes familiarity with I²C programming.
For more information, contact ICS for an I²C programming application note.

How to Write:

- Controller (host) sends a start bit.
- Controller (host) sends the write address D2 (H)
- ICS clock will ***acknowledge***
- Controller (host) sends a dummy command code
- ICS clock will ***acknowledge***
- Controller (host) sends a dummy byte count
- ICS clock will ***acknowledge***
- Controller (host) starts sending first byte (Byte 0) through byte 5
- ICS clock will ***acknowledge*** each byte ***one at a time***.
- Controller (host) sends a Stop bit

How to Write:	
Controller (Host)	**ICS (Slave/Receiver)**
Start Bit	
Address D2(H)	
	ACK
Dummy Command Code	
	ACK
Dummy Byte Count	
	ACK
Byte 0	
	ACK
Byte 1	
	ACK
Byte 2	
	ACK
Byte 3	
	ACK
Byte 4	
	ACK
Byte 5	
	ACK
Byte 6	
	ACK
Stop Bit	

How to Read:

- Controller (host) will send start bit.
- Controller (host) sends the read address D3 (H)
- ICS clock will ***acknowledge***
- ICS clock will send the ***byte count***
- Controller (host) acknowledges
- ICS clock sends first byte ***(Byte 0) through byte 6***
- Controller (host) will need to acknowledge each byte
- Controller (host) will send a stop bit

How to Read:	
Controller (Host)	**ICS (Slave/Receiver)**
Start Bit	
Address D3(H)	
	ACK
	Byte Count
ACK	
	Byte 0
ACK	
	Byte 1
ACK	
	Byte 2
ACK	
	Byte 3
ACK	
	Byte 4
ACK	
	Byte 5
ACK	
	Byte 6
ACK	
Stop Bit	

Notes:

1. The ICS clock generator is a slave/receiver, I²C component. It can read back the data stored in the latches for verification. **Read-Back will support Intel PIIX4 "Block-Read" protocol**.
2. The data transfer rate supported by this clock generator is 100K bits/sec or less (standard mode)
3. The input is operating at 3.3V logic levels.
4. The data byte format is 8 bit bytes.
5. To simplify the clock generator I²C interface, the protocol is set to use only "**Block-Writes**" from the controller. The bytes must be accessed in sequential order from lowest to highest byte with the ability to stop after any complete byte has been transferred. The Command code and Byte count shown above must be sent, but the data is ignored for those two bytes. The data is loaded until a Stop sequence is issued.
6. At power-on, all registers are set to a default condition, as shown.

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I2C Tables

BYTE 0	Affected Pin		Control Function	Type	Bit Control		
	Pin #	Name			0	1	PWD
Bit 7	-	Spread Enabled	Spread Spectrum Control	RW	OFF	ON	0
Bit 6	-	CPU_T(2:0)	Power down mode output level 0= CPU driven in power down 1= undriven	RW	HIGH	LOW	0
Bit 5	35	3V66_1/VCH_CLK	VCH/66.66 Select	RW	66.66	48.00	0
Bit 4	53	CPU_STOP#*	Reflects value of pin	R	Stop	Active	X
Bit 3	34	PCI_STOP#*	Reflects value of pin at power up. Also can be set.	R/RW	Stop	Active	1
Bit 2	40	FS2	Frequency Selection	RW	-	-	X
Bit 1	55	FS1	Frequency Selection	RW	-	-	X
Bit 0	54	FS0	Frequency Selection	RW	-	-	X

BYTE 1	Affected Pin		Control Function	Type	Bit Control		
	Pin #	Name			0	1	PWD
Bit 7	43	MULTSEL0*	Reflects value of pin	R	-	-	x
Bit 6	-	CPU_T(2:0)	CPU_Stop mode output level 0= CPU driven when stopped 1 = undriven	RW	HIGH	LOW	0
Bit 5	45, 44	CPUCLKT2 CPUCLKC2	Allow control of output with assertion of CPU_STOP#.	RW	Not Freerun	Freerun	0
Bit 4	49, 48	CPUCLKT1 CPUCLKC1	Allow control of output with assertion of CPU_STOP#.	RW	Not Freerun	Freerun	0
Bit 3	52, 51	CPUCLKT0 CPUCLKC0	Allow control of output with assertion of CPU_STOP#.	RW	Not Freerun	Freerun	0
Bit 2	45, 44	CPUCLKT2 CPUCLKC2	Output control	RW	Disable	Enable	1
Bit 1	49, 48	CPUCLKT1 CPUCLKC1	Output control	RW	Disable	Enable	1
Bit 0	52, 51	CPUCLKT2 CPUCLKC2	Output control	RW	Disable	Enable	1

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BYTE 2	Affected Pin		Control Function	Type	Bit Control		
	Pin #	Name			0	1	PWD
Bit 7	-	-	(Reserved)	-	-	-	0
Bit 6	18	PCICLK6	Output control	RW	Disable	Enable	1
Bit 5	17	PCICLK5	Output control	RW	Disable	Enable	1
Bit 4	16	PCICLK4	Output control	RW	Disable	Enable	1
Bit 3	13	PCICLK3	Output control	RW	Disable	Enable	1
Bit 2	12	PCICLK2	Output control	RW	Disable	Enable	1
Bit 1	11	PCICLK1	Output control	RW	Disable	Enable	1
Bit 0	10	PCICLK0	Output control	RW	Disable	Enable	1

BYTE 3	Affected Pin		Control Function	Type	Bit Control		
	Pin #	Name			0	1	PWD
Bit 7	38	48MHz_DOT	Output control	RW	Disable	Enable	1
Bit 6	39	48MHz_USB	Output control	RW	Disable	Enable	1
Bit 5	7	PCICLK_F2	Allow control of output with assertion of PCI_STOP#.	RW	Freerun	Not Freerun	0
Bit 4	6	PCICLK_F1	Allow control of output with assertion of PCI_STOP#.	RW	Freerun	Not Freerun	0
Bit 3	5	PCICLK_F0	Allow control of output with assertion of PCI_STOP#.	RW	Freerun	Not Freerun	0
Bit 2	7	PCICLK_F2	Output control	RW	Disable	Enable	1
Bit 1	6	PCICLK_F1	Output control	RW	Disable	Enable	1
Bit 0	5	PCICLK_F0	Output control	RW	Disable	Enable	1

BYTE 4	Affected Pin		Control Function	Type	Bit Control		
	Pin #	Name			0	1	PWD
Bit 7	-	-	(Reserved)	RW	Disable	Enable	0
Bit 6	-	-	(Reserved)	RW	Disable	Enable	0
Bit 5	33	3V66_0	Output control	RW	Disable	Enable	1
Bit 4	35	3V66_1/VCH_CLK	Output control	RW	Disable	Enable	1
Bit 3	24	3V66_5	Output control	RW	Disable	Enable	1
Bit 2	23	3V66_4	Output control	RW	Disable	Enable	1
Bit 1	22	3V66_3	Output control	RW	Disable	Enable	1
Bit 0	21	3V66_2	Output control	RW	Disable	Enable	1

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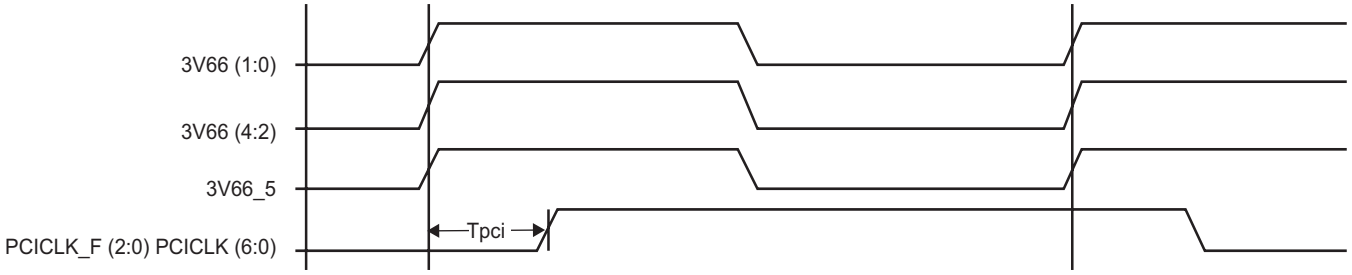
BYTE 5	Affected Pin		Control Function	Type	Bit Control		
	Pin #	Name			0	1	PWD
Bit 7	X	-	(Reserved)	-	-	-	0
Bit 6	X	-	(Reserved)	-	-	-	0
Bit 5	X	-	(Reserved)	-	-	-	0
Bit 4	X	-	(Reserved)	-	-	-	0
Bit 3	X	-	(Reserved)	-	-	-	0
Bit 2	X	-	(Reserved)	-	-	-	0
Bit 1	X	-	(Reserved)	-	-	-	0
Bit 0	X	-	(Reserved)	-	-	-	0

BYTE 6	Affected Pin		Control Function	Type	Bit Control		
	Pin #	Name			0	1	PWD
Bit 7	X	Revision ID Bit 3	(Reserved)	R	-	-	1
Bit 6	X	Revision ID Bit 2	(Reserved)	R	-	-	1
Bit 5	X	Revision ID Bit 1	(Reserved)	R	-	-	1
Bit 4	X	Revision ID Bit 0	(Reserved)	R	-	-	1
Bit 3	X	Vendor ID Bit 3	(Reserved)	R	-	-	1
Bit 2	X	Vendor ID Bit 2	(Reserved)	R	-	-	1
Bit 1	X	Vendor ID Bit 1	(Reserved)	R	-	-	1
Bit 0	X	Vendor ID Bit 0	(Reserved)	R	-	-	1

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3V66 & PCI Phase Relationship

All 3V66 clocks are to be in pphase with each other. In the case where 3V66_1 is configured as 48MHz VCH clock, there is no defined phase relationship between 3V66_1/VCH and other 3V66 clocks. The PCI group should lag 3V66 by the standard skew described below as Tpci.



Skews at Common Transition Edges

GROUP	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
PCI	PCI t_{sk}[1]	V_T = 1.5 V		127	500	ps
3V66	3V66 t_{sk}[1]	V_T = 1.5 V		67	250	ps
3V66 to PCI	$S_{3V66-PCI}$	3V66 (5:0) leads 33MHz PCI	1.5		3.5	ns

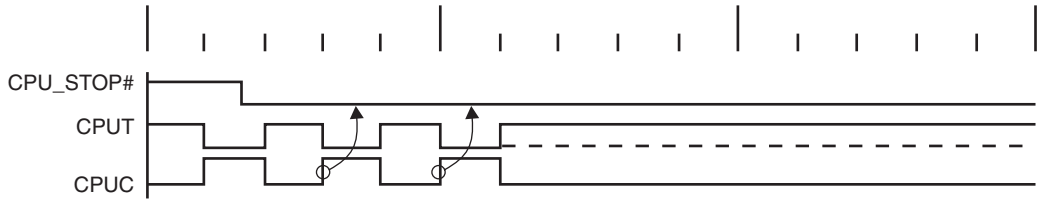
[1]Guarenteed by design, not 100% tested in production.

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CPU_STOP# - Assertion (transition from logic "1" to logic "0")

The impact of asserting the CPU_STOP# pin is all CPU outputs that are set in the I^2C configuration to be stoppable via assertion of CPU_STOP# are to be stopped after their next transition. When the I^2C Bit 6 of Byte 1 is programmed to '0' the final state of the stopped CPU signals is CPU = High and CPU# = Low. There is to be no change to the output drive current values. The CPU will be driven high with a current value equal to (Mult 0 'select') x (Iref), the CPU# signal will not be driven . When the I^2C Bit 6 of Byte 1 is programmed to '1' then final state of the stopped CPU signals is Low, both CPU and CPU# outputs will not be driven.

Assertion of CPU_STOP# Waveforms



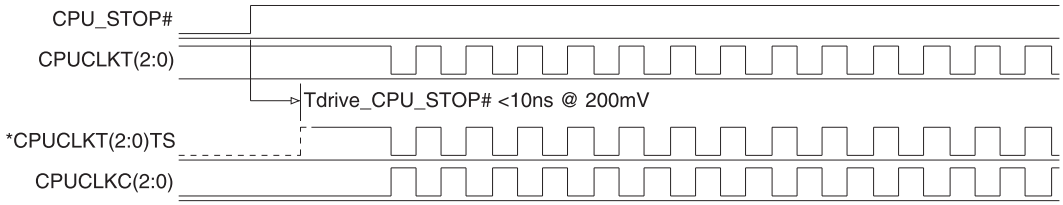
CPU_STOP# Functionality

CPU_STOP#	CPUT	CPUC
1	Normal	Normal
0	iref * Mult	Float

CPU_STOP# - De-assertion (transition from logic "0" to logic "1")

All CPU outputs that were stopped are to resume normal operation in a glitch free manner. The maximum latency from the de-assertion to active outputs is to be defined to be tetween 2 - 6 CPU clock periods (2 clocks are shown). If the I2C Bit 6 of Byte 1 is programmed to "1" then the stopped CPU outputs will be driven High within 3 nS of CPU_Stop# de-assertion.

De-assertion of CPU_STOP# Waveforms



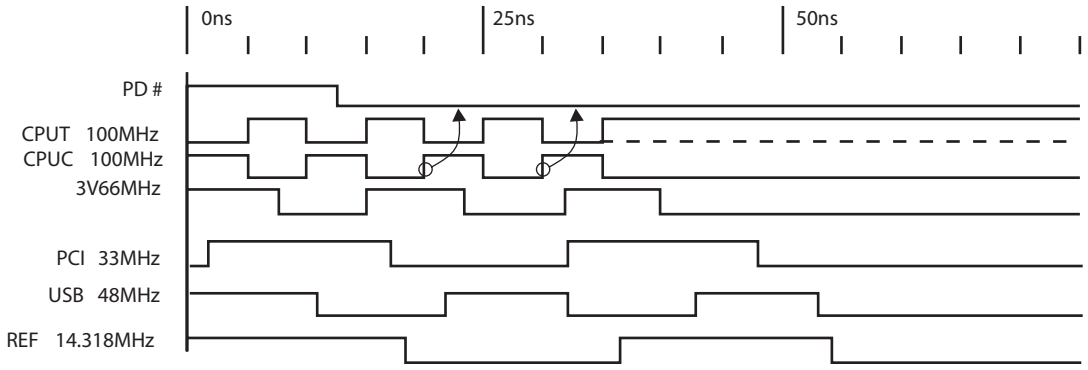
*Signal TS is CPUCLKT in Tri-State mode

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PD# - Assertion (transition from logic "1" to logic "0")

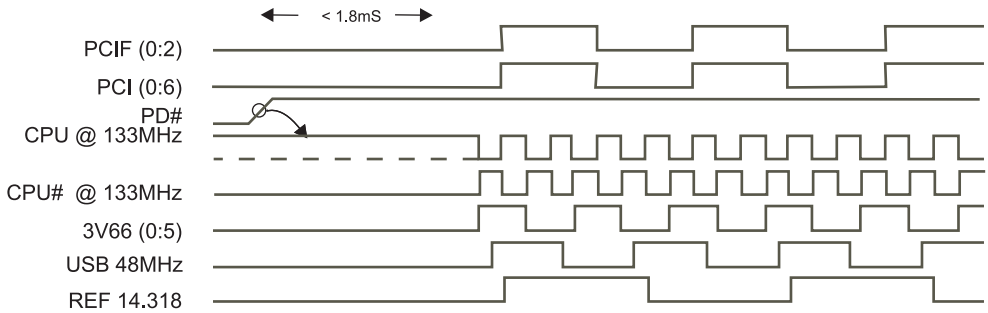
When PWRDWN# is sampled low by two consecutive rising edges of CPU clock, then all clock outputs except CPU clocks must be held low on their next high to low transitions. When the I2C Bit 6 of Byte 0 is programmed to '0' CPU clocks must be held with the CPU clock pin driven high with a value of 2 x Iref, and CPU# undriven. If Bit 6 of Byte 0 is '1' then both CPU and CPU# are undriven. Note the example below shows CPU = 133 MHz and Bit 6 of Byte 0 = '0', this diagram and description is applicable for all valid CPU frequencies 66, 100, 133, 200 MHz.
Due to the state if the internal logic, stopping and holding the REF clock outputs in the LOW state may require more than one clock cycle to complete.

Power Down Assertion of Waveforms



Power Down De-Assertion Mode

The power-up latency needs to be less than 1.8mS. this is the time from the de-asseration of the powerdown of the ramping of the power supply until the time that stable clocks are output from the clock chip. If the I^2C Bit 6 of Byte 0 is programmed to "1" then the stopped CPU outputs will be driven high within 3 nS of PD# de-asseration.

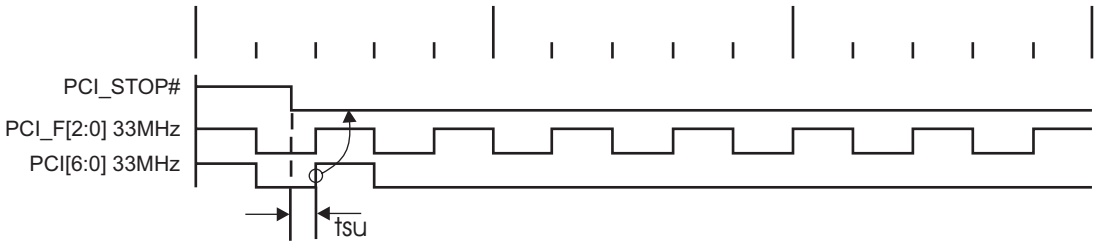


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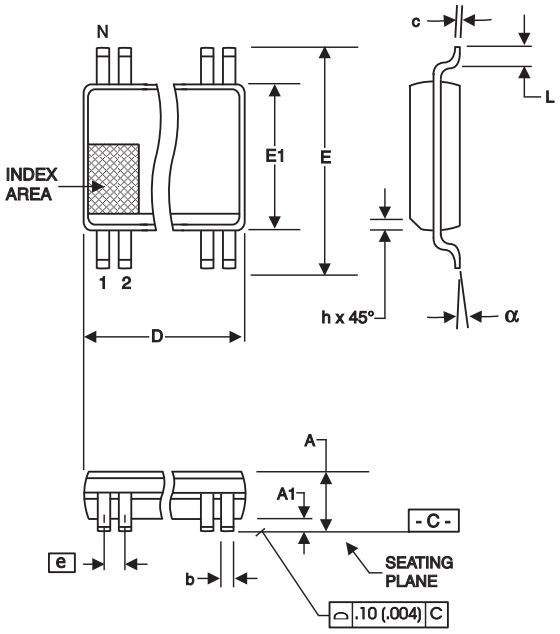
PCI_STOP# - Assertion (transition from logic "1" to logic "0")

The impact of asserting the PCI_STOP# signal will be the following. All PCI[6:0] and stoppable PCI_F[2,0] clocks will latch low in their next high to low transition. The PCI_STOP# setup time tsu is 10 ns, for transitions to be recognized by the next rising edge.

Assertion of PCI_STOP# Waveforms



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300 mil SSOP Package

SYMBOL	In Millimeters COMMON DIMENSIONS		In Inches COMMON DIMENSIONS	
	MIN	MAX	MIN	MAX
A	2.41	2.80	.095	.110
A1	0.20	0.40	.008	.016
b	0.20	0.34	.008	.0135
c	0.13	0.25	.005	.010
D	SEE VARIATIONS		SEE VARIATIONS	
E	10.03	10.68	.395	.420
E1	7.40	7.60	.291	.299
e	0.635 BASIC		0.025 BASIC	
h	0.38	0.64	.015	.025
L	0.50	1.02	.020	.040
N	SEE VARIATIONS		SEE VARIATIONS	
α	0°	8°	0°	8°

VARIATIONS

N	D mm.		D (inch)	
	MIN	MAX	MIN	MAX
56	18.31	18.55	.720	.730

Reference Doc.: JEDEC Publication 95, MO-118

10-0034

Ordering Information

ICS950810yFLF-T

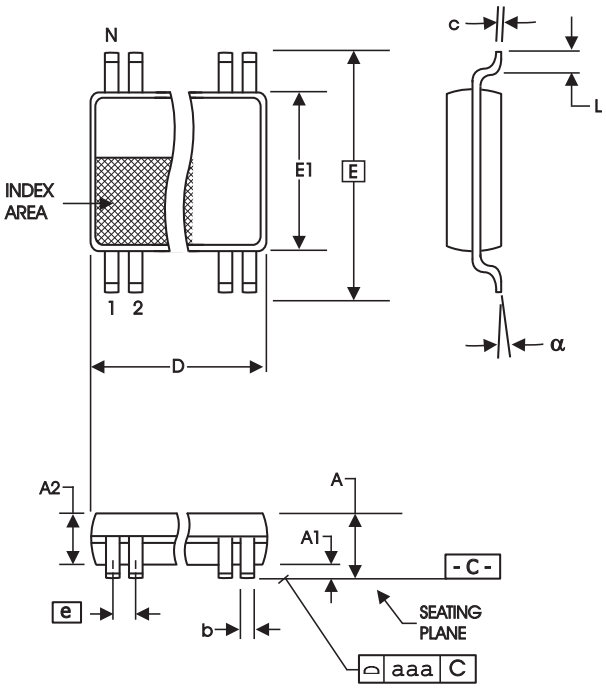
Example:

ICS XXXX y F LF- T

- **Designation for tape and reel packaging**
- **Lead Free (Optional)**
- **Package Type**
  F = SSOP
- **Revision Designator** (will not correlate with datasheet revision)
- **Device Type**
- **Prefix**
  ICS = Standard Device

0472F—01/12/04

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SYMBOL	In Millimeters COMMON DIMENSIONS		In Inches COMMON DIMENSIONS	
	MIN	MAX	MIN	MAX
A	--	1.20	--	.047
A1	0.05	0.15	.002	.006
A2	0.80	1.05	.032	.041
b	0.17	0.27	.007	.011
c	0.09	0.20	.0035	.008
D	SEE VARIATIONS		SEE VARIATIONS	
E	8.10 BASIC		0.319 BASIC	
E1	6.00	6.20	.236	.244
e	0.50 BASIC		0.020 BASIC	
L	0.45	0.75	.018	.030
N	SEE VARIATIONS		SEE VARIATIONS	
α	0°	8°	0°	8°
aaa	--	0.10	--	.004

'ARIATIONS

N	D mm.		D (inch)	
	MIN	MAX	MIN	MAX
56	13.90	14.10	.547	.555

Reference Doc.: JEDEC Publication 95, MO-153

10-0039

6.10 mm. Body, 0.50 mm. pitch TSSOP
(240 mil) (20 mil)

Ordering Information

ICS950810yGLF-T

Example:

ICS XXXX y G LF- T

- **Designation for tape and reel packaging**
- **Lead Free (Optional)**
- **Package Type**
  G = TSSOP
- **Revision Designator** (will not correlate with datasheet revision)
- **Device Type**
- **Prefix**
  ICS = Standard Device

0472F—01/12/04

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