Frequency Generator with 200MHz Differential CPU Clocks

ICS950812

Recommended Application:

CK-408 clock with Buffered/Unbuffered mode supporting Almador, Brookdale, ODEM, and Montara-G chipsets with PIII/P4 processor. Programmable for group to group skew.

Output Features:

- 3 0.7V Differential CPU Clock Pairs
- 7 PCI (3.3V) @ 33.3MHz including 2 early PCI clocks
- 3 PCI_F (3.3V) @ 33.3MHz
- 1 USB (3.3V) @ 48MHz, 1 DOT (3.3V) @ 48MHz
- 1 REF (3.3V) @ 14.318MHz
- 5 3V66 (3.3V) @ 66.6MHz
- 1 VCH/3V66 (3.3V) @ 48MHz or 66.6MHz

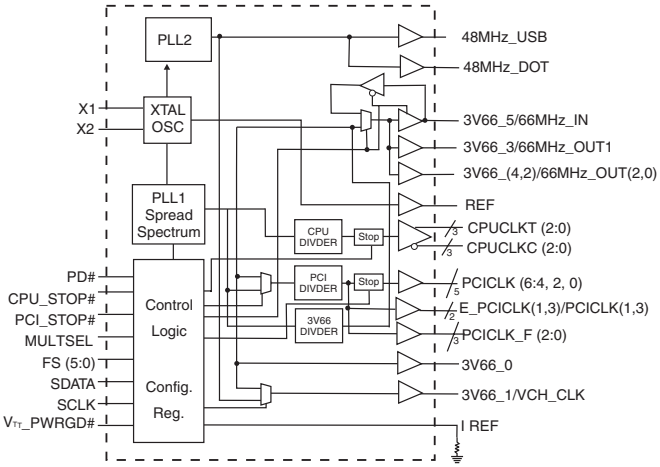
Features:

- Provides standard frequencies and additional 5% and 10% over-clocked frequencies
- Supports spread spectrum modulation: No spread, Center Spread (±0.35%, ±0.5%, or ±0.75%), or Down Spread (-0.5%, -1.0%, or -1.5%)
- Offers adjustable PCI early clock via latch inputs
- Selectable 1X or 2X strength for REF via I^2C interface
- Efficient power management scheme through PD#, CPU_STOP# and PCI_STOP#.
- Uses external 14.318MHz crystal
- Stop clocks and functional control available through I^2C interface.

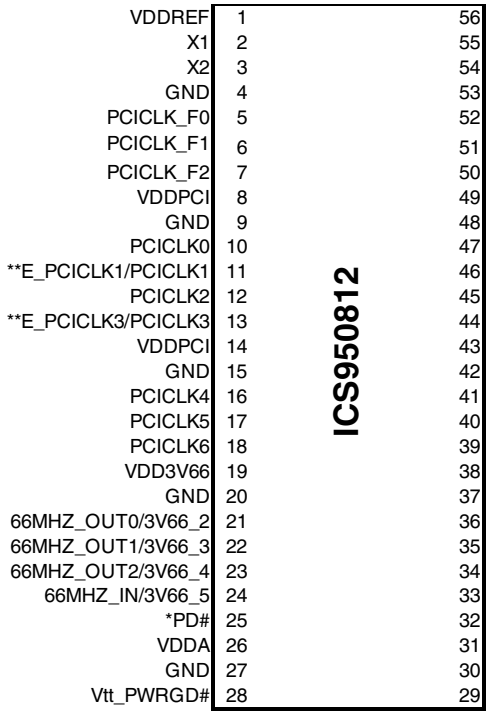
Key Specifications:

- CPU Output Jitter <150ps
- 3V66 Output Jitter <250ps
- 66MHz Output Jitter (Additive) (Buffered Mode) <100ps
- CPU Output Skew <100ps

Block Diagram



Pin Configuration



56-Pin 300mil SSOP
6.10 mm. Body, 0.50 mm. pitch TSSOP

*These inputs have 120K internal pull-up resistors to VDD.
**Internal pull-down resistors to ground.

Note:
Almador board level designs MUST use pin 22, 66MHZ_OUT1, as the feedback connection from the clock buffer path to the Almador (GMCH) chipset.

Frequency Select

Bit			CPUCLK	3V66	66MHz_OUT (2:0)	66MHz_IN	PCICLK_F
					3V66 (4:2)	3V66_5	PCICLK
FS2	FS1	FS0	MHz	MHz	MHz	MHz	MHz
0	0	0	66.66	66.66	66.66	66.66	33.33
0	0	1	100.00	66.66	66.66	66.66	33.33
0	1	0	200.00	66.66	66.66	66.66	33.33
0	1	1	133.33	66.66	66.66	66.66	33.33
1	0	0	66.66	66.66	66MHz_IN	Input	66MHz_IN/2
1	0	1	100.00	66.66	66MHz_IN	Input	66MHz_IN/2
1	1	0	200.00	66.66	66MHz_IN	Input	66MHz_IN/2
1	1	1	133.33	66.66	66MHz_IN	Input	66MHz_IN/2

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Pin Description

PIN #	PIN NAME	PIN TYPE	DESCRIPTION
1	VDDREF	PWR	Ref, XTAL power supply, nominal 3.3V
2	X1	IN	Crystal input, Nominally 14.318MHz.
3	X2	OUT	Crystal output, Nominally 14.318MHz
4	GND	PWR	Ground pin.
5	PCICLK_F0	OUT	Free running PCI clock not affected by PCI_STOP# .
6	PCICLK_F1	OUT	Free running PCI clock not affected by PCI_STOP# .
7	PCICLK_F2	OUT	Free running PCI clock not affected by PCI_STOP# .
8	VDDPCI	PWR	Power supply for PCI clocks, nominal 3.3V
9	GND	PWR	Ground pin.
10	PCICLK0	OUT	PCI clock output.
11	**E_PCICLK1/PCICLK1	I/O	Early/Normal PCI clock output latched at power up.
12	PCICLK2	OUT	PCI clock output.
13	**E_PCICLK3/PCICLK3	I/O	Early/Normal PCI clock output latched at power up.
14	VDDPCI	PWR	Power supply for PCI clocks, nominal 3.3V
15	GND	PWR	Ground pin.
16	PCICLK4	OUT	PCI clock output.
17	PCICLK5	OUT	PCI clock output.
18	PCICLK6	OUT	PCI clock output.
19	VDD3V66	PWR	Power pin for the 3V66 clocks.
20	GND	PWR	Ground pin.
21	66MHZ_OUT0/3V66_2	OUT	3.3V 66.66MHz clock output selected via buffered or internal VCO.
22	66MHZ_OUT1/3V66_3	OUT	3.3V 66.66MHz clock output selected via buffered or internal VCO.
23	66MHZ_OUT2/3V66_4	OUT	3.3V 66.66MHz clock output selected via buffered or internal VCO.
24	66MHZ_IN/3V66_5	I/O	3.3V 66.66MHz clock from internal VCO, 66MHZ input to 66MHz output and PCI.
25	*PD#	IN	Asynchronous active low input pin used to power down the device into a low power state. The internal clocks are disabled and the VCO and the crystal are stopped. The latency of the power down will not be greater than 1.8ms.
26	VDDA	PWR	3.3V power for the PLL core.
27	GND	PWR	Ground pin.
28	Vtt_PWRGD#	IN	This 3.3V LVTTL input is a level sensitive strobe used to determine when latch inputs are valid and are ready to be sampled. This is an active low input.

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Pin Description (continued)

PIN #	PIN NAME	PIN TYPE	DESCRIPTION
29	SDATA	I/O	Data pin for I2C circuitry 5V tolerant
30	SCLK	IN	Clock pin of I2C circuitry 5V tolerant
31	GND	PWR	Ground pin.
32	VDD3V66	PWR	Power pin for the 3V66 clocks.
33	3V66_0/FS5**	I/O	Frequency select latch input pin / 3.3V 66.66MHz clock output.
34	PCI_STOP#*	IN	Stops all PCICLKs besides the PCICLK_F clocks at logic 0 level, when input low
35	3V66_1/VCH_CLK/FS4**	I/O	Frequency select latch input pin / 3.3V 66.66MHz clock output / 48MHz VCH clock output.
36	GND	PWR	Ground pin.
37	VDD48	PWR	Power pin for the 48MHz output.3.3V
38	48MHz_DOT	OUT	48MHz clock output.
39	48MHz_USB/FS3**	I/O	Frequency select latch input pin / 3.3V 48MHz clock output.
40	FS2	IN	Frequency select pin.
41	GND	PWR	Ground pin.
42	IREF	OUT	This pin establishes the reference current for the differential current-mode output pairs. This pin requires a fixed precision resistor tied to ground in order to establish the appropriate current. 475 ohms is the standard value.
43	MULTSEL*	IN	3.3V LVTTL input for selection the current multiplier for CPU outputs
44	CPUCLKC2	OUT	Complimentary clock of differential pair CPU outputs. These are current mode outputs. External resistors are required for voltage bias.
45	CPUCLKT2	OUT	True clock of differential pair CPU outputs. These are current mode outputs. External resistors are required for voltage bias.
46	VDDCPU	PWR	Supply for CPU clocks, 3.3V nominal
47	GND	PWR	Ground pin.
48	CPUCLKC1	OUT	Complimentary clock of differential pair CPU outputs. These are current mode outputs. External resistors are required for voltage bias.
49	CPUCLKT1	OUT	True clock of differential pair CPU outputs. These are current mode outputs. External resistors are required for voltage bias.
50	VDDCPU	PWR	Supply for CPU clocks, 3.3V nominal
51	CPUCLKC0	OUT	Complimentary clock of differential pair CPU outputs. These are current mode outputs. External resistors are required for voltage bias.
52	CPUCLKT0	OUT	True clock of differential pair CPU outputs. These are current mode outputs. External resistors are required for voltage bias.
53	CPU_STOP#*	IN	Stops all CPUCLK besides the free running clocks
54	FS0	IN	Frequency select pin.
55	FS1	IN	Frequency select pin.
56	REF	OUT	14.318 MHz reference clock.

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Frequency Select Table 1

Freq Sel				CPU MHz	3V66 MHz	66MHz_OUT (2:0)	66MHz_IN	PCI MHz	REF MHz	USB/DOT MHz	Clocking Mode
FS(5:3)	FS2	FS1	FS0			3V66 (4:2)	3V66 _5				
From 000 to 101 (See table 2)	0	0	0	66.66	66.66	66.66	66.66	33.33	14.318	48.008	Standard Clocking
	0	0	1	100.00	66.66	66.66	66.66	33.33	14.318	48.008	
	0	1	0	200.00	66.66	66.66	66.66	33.33	14.318	48.008	
	0	1	1	133.33	66.66	66.66	66.66	33.33	14.318	48.008	
	1	0	0	66.66	66.66	66MHz_IN	Input	66MHz_IN/2	14.318	48.008	Standard Clocking
	1	0	1	100.00	66.66	66MHz_IN	Input	66MHz_IN/2	14.318	48.008	
	1	1	0	200.00	66.66	66MHz_IN	Input	66MHz_IN/2	14.318	48.008	
	1	1	1	133.33	66.66	66MHz_IN	Input	66MHz_IN/2	14.318	48.008	
110 (See table 2)	0	0	0	70.00	70.00	70.00	70.00	35.00	14.318	48.008	5% Overclocking
	0	0	1	105.00	70.00	70.00	70.00	35.00	14.318	48.008	
	0	1	0	Tristate	Tristate	Tristate	Tristate	Tristate	Tristate	Tristate	Tristate
	0	1	1	140.00	70.00	70.00	70.00	35.00	14.318	48.008	5% Overclocking
	1	0	0	70.00	70.00	66MHz_IN	Input	66MHz_IN/2	14.318	48.008	
	1	0	1	105.00	70.00	66MHz_IN	Input	66MHz_IN/2	14.318	48.008	
	1	1	0	Tristate	Tristate	Tristate	Tristate	Tristate	Tristate	Tristate	Tristate
	1	1	1	140.00	70.00	66MHz_IN	Input	66MHz_IN/2	14.318	48.008	5% Overclocking
111 (See table 2)	0	0	0	73.32	73.32	73.32	73.32	36.66	14.318	48.008	10% Overclocking
	0	0	1	110.00	73.32	73.32	73.32	36.66	14.318	48.008	
	0	1	0	Test/2	Test/4	Test/4	Test/4	Test/8	Test	Test/2	Test
	0	1	1	146.60	73.32	73.32	73.32	36.66	14.318	48.008	10% Overclocking
	1	0	0	73.32	73.32	66MHz_IN	Input	66MHz_IN/2	14.318	48.008	
	1	0	1	110.00	73.32	66MHz_IN	Input	66MHz_IN/2	14.318	48.008	
	1	1	0	Test/2	Test/4	Test/4	Test/4	Test/8	Test	Test/2	Test
	1	1	1	146.60	73.32	66MHz_IN	Input	66MHz_IN/2	14.318	48.008	10% Overclocking

Frequency Select Table 2

Freq Sel			CPU, 3V66, 66MHz_OUT, 66MHz_IN, PCI	Clocking Mode
FS5	FS4	FS3		
0	0	0	Standard Clocking	No Spread (default) or +/-0.4%
0	0	1	Standard Clocking	0 to -0.5%, Down Spread
0	1	0	Standard Clocking	0 to -1.0%, Down Spread
0	1	1	Standard Clocking	0 to -1.5%, Down Spread
1	0	0	Standard Clocking	+/-0.5%, Center Spread
1	0	1	Standard Clocking	+/-0.75%, Center Spread
1	1	0	5% Overclocking	+/-0.35%, Center Spread
1	1	1	10% Overclocking	+/-0.35%, Center Spread

Note: To enable spread, Byte 0 Bit 7 must be set to 1.

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Maximum Allowed Current

Condition	Max 3.3V supply consumption Max discrete cap loads, Vdd = 3.465V All static inputs = Vdd or GND
Powerdown Mode (PD# = 0)	40mA
Active Full	280mA

Host Swing Select Functions

MULTSEL	Board Target Trace/Term Z	Reference R, Iref = V_{DD}/3*Rr	Output Current	Voh @ Z
0	50 ohms	Rr = 221 1%, Iref = 5.00mA	Ioh = 4 * I REF	1.0V @ 50 ohm
1	50 ohms	Rr = 475 1%, Iref = 2.32mA	Ioh = 6 * I REF	0.7V @ 50 ohm

PCI Select Functions

E_PCICLK1 (11)	E_PCICLK3 (13)	E_PCICLK(3,1)*
0	0	0ns
0	1	0.5ns
1	0	1.0ns
1	1	1.5ns

Note:
E_PCICLK1 = 10Kohm resistor.
E_PCICLK3 = 10Kohm resistor.
0 = No resistor
1 = 10Kohm pull-up to V_{DD}.
* Approximate values

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Table 3

PCI_STOP# I²C Control Table-Byte 0, Bit 3

PCI_STOP# (Pin 34)	Byte 0 Bit 3 Write Bit	Byte 0, Bit 3 Read Bit (Internal Status)
0	0	0
0	1	0
1	0	0
1	1	1`

Note: When this Byte 0, Bit 3 is low (0), all PCI clocks are stopped.

Table 4

CPUCLKT/C (2:0) Outputs I²C Control Table

CPU_STOP# (Pin 53)	Byte 1 Bit 3, 4, 5	CPUCLKT/C (2:0) Outputs
0	0	Stop
0	1	Running
1	0	Running
1	1	Running

Note: Individual CPUCLK outputs are controlled by Byte 1, Bit 3, 4, and 5.

Table 5

PCICLK_F (2:0) Outputs I²C Control Table

PCI_STOP# (Pin 34)	Byte 3 Bit 3, 4, 5	PCICLK (2:0) Outputs
0	0	Stop
0	1	Running
1	0	Running
1	1	Running

Note: Individual PCICLK outputs are controlled by Byte 3, Bit 3, 4, and 5.

Table 6

3V66 (5:2)/66MHz_OUT(2:0)/66MHz_IN I²C Control Table

CPU_STOP# (Pin 53)	Byte 5 Bit 5	3V66 (5:2) (Driven) 66MHZ_OUT(2:0)/66MHZ_IN (Buffered)
0	0	Running
0	1	Stopped
1	0	Running
1	1	Running

Note: Activating Byte 5, Bit 5 will allow CPU_STOP# to control stop of pins 21, 22, 23, and 24.

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Table 7

3V66 (0:1) I²C Control Table

CPU_STOP# (Pin 53)	Byte 5 Bit 4	3V66 (1:0)
0	0	Running
0	1	Stopped
1	0	Running
1	1	Running

Note: Activating Byte 5, Bit 4 will allow CPU_STOP# to control stop of pins 33 and 35.

Table 8: Byte 11-14 Defaults

	ADDRESS					CPU	Spread		Bytes							
									I2C read back values in Hex.				I2C read back values in binary.			
	FS5	FS4	FS3	FS1	FS0	Freq	Center Down		11	12	13	14	11	12	13	14
0	0	0	0	0	0	66.66	Center	0.40%	8D	9B	02	18	10001101	10011011	00000010	00011000
1	0	0	0	0	1	99.99	Center	0.40%	8D	9B	02	18	10001101	10011011	00000010	00011000
2	0	0	0	1	0	199.98	Center	0.40%	8D	9B	02	18	10001101	10011011	00000010	00011000
3	0	0	0	1	1	133.32	Center	0.40%	8D	9B	02	18	10001101	10011011	00000010	00011000
4	0	0	1	0	0	66.50	Down	-0.48%	8D	9A	EF	17	10001101	10011010	11101111	00010111
5	0	0	1	0	1	99.75	Down	-0.48%	8D	9A	EF	17	10001101	10011010	11101111	00010111
6	0	0	1	1	0	199.50	Down	-0.48%	8D	9A	EF	17	10001101	10011010	11101111	00010111
7	0	0	1	1	1	133.00	Down	-0.48%	8D	9A	EF	17	10001101	10011010	11101111	00010111
8	0	1	0	0	0	66.34	Down	-0.98%	8D	99	E7	17	10001101	10011001	11100111	00010111
9	0	1	0	0	1	99.51	Down	-0.98%	8D	99	E7	17	10001101	10011001	11100111	00010111
10	0	1	0	1	0	199.02	Down	-0.98%	8D	99	E7	17	10001101	10011001	11100111	00010111
11	0	1	0	1	1	132.68	Down	-0.98%	8D	99	E7	17	10001101	10011001	11100111	00010111
12	0	1	1	0	0	66.16	Down	-1.52%	90	EB	DD	17	10010000	11101011	11011101	00010111
13	0	1	1	0	1	99.23	Down	-1.52%	90	EB	DD	17	10010000	11101011	11011101	00010111
14	0	1	1	1	0	198.47	Down	-1.52%	90	EB	DD	17	10010000	11101011	11011101	00010111
15	0	1	1	1	1	132.31	Down	-1.52%	90	EB	DD	17	10010000	11101011	11011101	00010111
16	1	0	0	0	0	66.66	Center	0.51%	8D	9B	05	18	10001101	10011011	00000101	00011000
17	1	0	0	0	1	99.99	Center	0.51%	8D	9B	05	18	10001101	10011011	00000101	00011000
18	1	0	0	1	0	199.98	Center	0.51%	8D	9B	05	18	10001101	10011011	00000101	00011000
19	1	0	0	1	1	133.32	Center	0.51%	8D	9B	05	18	10001101	10011011	00000101	00011000
20	1	0	1	0	0	66.66	Center	0.74%	8D	9B	0B	18	10001101	10011011	00001011	00011000
21	1	0	1	0	1	99.99	Center	0.74%	8D	9B	0B	18	10001101	10011011	00001011	00011000
22	1	0	1	1	0	199.98	Center	0.74%	8D	9B	0B	18	10001101	10011011	00001011	00011000
23	1	0	1	1	1	133.32	Center	0.74%	8D	9B	0B	18	10001101	10011011	00001011	00011000
24	1	1	0	0	0	70.00	Center	0.35%	8D	B0	35	19	10001101	10110000	00110101	00011001
25	1	1	0	0	1	105.00	Center	0.35%	8D	B0	35	19	10001101	10110000	00110101	00011001
26	1	1	0	1	0	210.00	Center	0.35%	8D	B0	35	19	10001101	10110000	00110101	00011001
27	1	1	0	1	1	140.00	Center	0.35%	8D	B0	35	19	10001101	10110000	00110101	00011001
28	1	1	1	0	0	73.33	Center	0.34%	89	4A	68	1A	10001001	01001010	01101000	00011010
29	1	1	1	0	1	109.99	Center	0.34%	89	4A	68	1A	10001001	01001010	01101000	00011010
30	1	1	1	1	0	219.98	Center	0.34%	89	4A	68	1A	10001001	01001010	01101000	00011010
31	1	1	1	1	1	146.65	Center	0.34%	89	4A	68	1A	10001001	01001010	01101000	00011010

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Absolute Maximum Ratings

Supply Voltage	5.5 V
Logic Inputs	GND –0.5 V to V_{DD} +0.5 V
Ambient Operating Temperature	0°C to +90°C
Case Temperature	115°C
Storage Temperature	–65°C to +150°C

Stresses above those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only and functional operation of the device at these or any other conditions above those listed in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Electrical Characteristics - Input/Supply/Common Output Parameters

T_A = 0 - 90°C; Supply Voltage V_{DD} = 3.3 V +/-5%

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input High Voltage	V_{IH}		2		V_{DD}+0.3	V
Input Low Voltage	V_{IL}		V_{SS}-0.3		0.8	V
Input High Current	I_{IH}	V_{IN} = V_{DD}; Inputs with no pull-down resistors			5.75	mA
	I_{IH}	V_{IN} = V_{DD}; Inputs with pull-down resistors			200	µA
Input Low Current	I_{IL1}	V_{IN} = 0 V; Inputs with no pull-up resistors	-5.75			mA
	I_{IL2}	V_{IN} = 0 V; Inputs with pull-up resistors	-200			µA
Operating Supply Current	$I_{DD3.3OP}$	C_L = Full load; Select @ 100 MHz		233	280	mA
	$I_{DD3.3OP}$	C_L =Full load; Select @ 133 MHz		234	280	mA
Powerdown Current	$I_{DD3.3PD}$	IREF=5 mA		20	52	mA
	$I_{DD3.3PDHIz}$			0.289	0.5	mA
Input Frequency	F_i	V_{DD} = 3.3 V		14.32		MHz
Pin Inductance	L_{pin}				7	nH
Input Capacitance[1]	C_{IN}	Logic Inputs			5	pF
	C_{OUT}	Output pin capacitance			6	pF
	C_{INX}	X1 & X2 pins	27	30	45	pF
Clk Stabilization[1,2]	T_{STAB}	From PowerUp or deassertion of PowerDown to 1st clock.		1	2.1	ms
Delay[1]	t_{PZH},t_{PZL}	Output enable delay (all outputs)	1		12	ns
	t_{PHZ},t_{PLZ}	Output disable delay (all outputs)	1		12	ns

[1]Guaranteed by design, not 100% tested in production.

[2]See timing diagrams for buffered and un-buffered timing requirements.

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Electrical Characteristics - CPU (1V Select) 100MHz

T_A = 0 - 90°C; VDD=3.3V +/-5%; C_L = 10-20 pF (unless otherwise specified)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Current Source Output Impedance	Zo[1]	$V_O = V_x$	2500			Ω
Average Period	T_{PERIOD}	Fig. 5	10.00	10.01	10.20	ns
Output High Voltage	V_{OH3}	Measured from Single Ended Waveform	0.92		1.45	V
Output Low Voltage	V_{OL3}		-0.2		0.35	
Rise Time	t_{r3}	V_{OL} = 0.41V, V_{OH} = 0.86V (Fig. 6)	175	390	540	ps
Fall Time	t_{f3}	V_{OH} = 0.86V V_{OL} = 0.41V (Fig.6)	175	305	540	ps
Duty Cycle	d_{t3}	Fig. 5	45	51	55	%
Skew	t_{sk3}	V_T = 50%		10	100	ps
Jitter, Cycle to cycle	$t_{jcyc-cyc}$[1]	V_T = 50%		40	175	ps

[1]Guaranteed by design, not 100% tested in production.

[2] I_{OWT} can be varied and is selectable thru the MULTSEL pin.

Electrical Characteristics - CPU (0.7V Select) 100MHz

T_A = 0 - 90°C; VDD=3.3V +/-5%; (unless otherwise specified)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Current Source Output Impedance	Zo[1]	$V_O = V_x$	3000			Ω
Average Period	T_{PERIOD}	Fig. 1	10.00	10.01	10.20	ns
Voltage High	VHigh	Statistical measurement on single ended signal using oscilloscope math function.	660	720	850	mV
Voltage Low	VLow		-150	15	150	
Max Voltage	Vovs	Measurement on single ended signal using absolute value.		750	1150	mV
Min Voltage	Vuds		-450	-2		
Crossing Voltage (abs)	Vcross(abs)	Fig. 3	250	319	550	mV
Crossing Voltage (var)	d-Vcross	Variation of crossing over all edges (Fig. 4)		12	140	mV
Rise Time	t_r	V_{OL} = 0.175V, V_{OH} = 0.525V (Fig. 3)	175	310	810	ps
Fall Time	t_f	V_{OH} = 0.525V V_{OL} = 0.175V (Fig. 3)	175	300	810	ps
Rise Time Variation	d-t_r			10	125	ps
Fall Time Variation	d-t_f			10	125	ps
Duty Cycle	d_{t3}	Measurement from differential wavefrom (Fig 1)	45	51	55	%
Skew	t_{sk3}	V_T = 50%		16	100	ps
Jitter, Cycle to cycle	$t_{jcyc-cyc}$[1]	V_T = 50% (Fig. 1)		48	175	ps

[1]Guaranteed by design, not 100% tested in production.

[2] I_{OWT} can be varied and is selectable thru the MULTSEL pin.

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Electrical Characteristics - CPU (0.7V Select) 133.33MHz

T_A = 0 - 90°C; VDD=3.3V +/-5%; (unless otherwise specified)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Current Source Output Impedance	Zo[1]	$V_O = V_x$	3000			Ω
Average Period	T_{PERIOD}	Fig. 1	7.50	7.51	7.65	ns
Voltage High	VHigh	Statistical measurement on single ended signal using oscilloscope math function.	660	718	850	mV
Voltage Low	VLow		-150	17	150	
Max Voltage	Vovs	Measurement on single ended signal using absolute value.		730	1150	mV
Min Voltage	Vuds		-450	7		
Crossing Voltage (abs)	Vcross(abs)	Fig. 3	250	340	550	mV
Crossing Voltage (var)	d-Vcross	Variation of crossing over all edges (Fig. 4)		15	140	mV
Rise Time	t_r	V_{OL} = 0.175V, V_{OH} = 0.525V (Fig. 3)	175	310	810	ps
Fall Time	t_f	V_{OH} = 0.525V V_{OL} = 0.175V (Fig. 3)	175	315	810	ps
Rise Time Variation	d-t_r			5	125	ps
Fall Time Variation	d-t_f			5	125	ps
Duty Cycle	d_{t3}	Measurement from differential wavefrom (Fig 1)	45	51	55	%
Skew	t_{sk3}	V_T = 50%		14	100	ps
Jitter, Cycle to cycle	$t_{jcyc-cyc}$[1]	V_T = 50% (Fig. 1)		75	175	ps

[1]Guaranteed by design, not 100% tested in production.

[2] I_{OWT} can be varied and is selectable thru the MULTSEL pin.

Electrical Characteristics - PCICLK Buffered Mode

T_A = 0 - 90°C; VDD = 3.3V +/-5%; C_L = 10-30 pF (unless otherwise specified)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output Impedance	R_{DSP1}[1]	$V_O = V_{DD}$*(0.5)	12	33	65	Ω
Output High Voltage	V_{OH}[1]	I_{OH} = -1 mA	2.05			V
Output Low Voltage	V_{OL}[1]	I_{OL} = 1 mA			0.65	V
Output High Current	I_{OH}[1]	$V_{OH@MIN}$ = 1.0V, $V_{OH@MAX}$ = 3.135V	-33		-28	mA
Output Low Current	I_{OL}[1]	$V_{OL\ @MIN}$ = 1.95V, $V_{OL\ @MAX}$ = 0.4V	26		38	mA
Rise Time	t_{r1}[1]	V_{OL} = 0.4 V, V_{OH} = 2.4 V (Fig. 7)	0.5	1.4	2.3	ns
Fall Time	t_{f1}[1]	V_{OH} = 2.4 V, V_{OL} = 0.4 V (Fig. 7)	0.5	1.2	2.3	ns
Duty Cycle	d_{t1}[1]	V_T = 1.5 V	45	52	55	%
Skew	t_{sk1}[1]	V_T = 1.5 V		35	500	ps
Jitter,cycle to cyc	$t_{jcyc-cyc}$[1]	V_T = 1.5 V (Additive) (Fig. 8)		60	120	ps

[1]Guaranteed by design, not 100% tested in production.

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Electrical Characteristics - PCICLK Un-Buffered Mode

T_A = 0 - 90°C; VDD=3.3V +/-5%; C_L = 10-30 pF (unless otherwise specified)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output Impedance	R_{DSP1}[1]	$V_O = V_{DD}*(0.5)$	12	33	65	Ω
Average Period	T_{PERIOD}	Fig. 8	30.00	30.01		ns
Output High Voltage	V_{OH}[1]	I_{OH} = -1 mA	2.05			V
Output Low Voltage	V_{OL}[1]	I_{OL} = 1 mA			0.65	V
Output High Current	I_{OH}[1]	$V_{OH@MIN}$ = 1.0V, $V_{OH@MAX}$ = 3.135V	-33		-28	mA
Output Low Current	I_{OL}[1]	$V_{OL\ @MIN}$ = 1.95 V, $V_{OL\ @MAX}$ = 0.4 V	26		38	mA
Rise Time	t_{r1}[1]	V_{OL} = 0.4 V, V_{OH} = 2.4 V (Fig. 7)	0.5	1.4	2.3	ns
Fall Time	t_{f1}[1]	V_{OH} = 2.4 V, V_{OL} = 0.4 V (Fig. 7)	0.5	1.2	2.3	ns
Duty Cycle	d_{t1}[1]	V_T = 1.5 V (Fig. 8)	45	50	55	%
Skew	t_{sk1}[1]	V_T = 1.5 V		65	500	ps
Jitter,cycle to cyc	$t_{jcyc-cyc}$[1]	V_T = 1.5 V (Fig. 8)		101	290	ps

[1]Guaranteed by design, not 100% tested in production.

Electrical Characteristics- 3V66 - Buffered Mode: 66MHz_OUT [2:0]

T_A = 0 - 90°C; VDD=3.3V +/-5%; C_L = 10-30 pF (unless otherwise specified)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output Impedance	R_{DSP1}[1]	$V_O = V_{DD}*(0.5)$	12	33	65	Ω
Output High Voltage	V_{OH}[1]	I_{OH} = -1 mA	2.05			V
Output Low Voltage	V_{OL}[1]	I_{OL} = 1 mA			0.65	V
Output High Current	I_{OH}[1]	$V_{OH@MIN}$ = 1.0 V, $V_{OH@MAX}$ = 3.135 V	-33		-28	mA
Output Low Current	I_{OL}[1]	$V_{OL\ @MIN}$ = 1.95 V, $V_{OL\ @MAX}$ = 0.4 V	26		38	mA
Rise Time	t_{r1}[1]	V_{OL} = 0.4 V, V_{OH} = 2.4 V (Fig. 7)	0.5	1.6	2.3	ns
Fall Time	t_{f1}[1]	V_{OH} = 2.4 V, V_{OL} = 0.4 V (Fig. 7)	0.5	1	2.3	ns
Duty Cycle	d_{t1}[1]	V_T = 1.5 V (Fig. 8)	45	52	55	%
Jitter	$t_{jcyc-cyc}$[1]	V_T = 1.5 V 66MHz_OUT [2:0] (Additive) (Fig. 8)		83	120	ps
Skew	t_{sk1}[1]	V_T = 1.5 V 66MHz_OUT [2:0]		169	250	ps

[1]Guaranteed by design, not 100% tested in production.

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Electrical Characteristics - 3V66 -Un-Buffered Mode: 3V66 [5:0]

T_A = 0 - 90°C; VDD=3.3V +/-5%; C_L = 10-30 pF (unless otherwise specified)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output Impedance	R_{DSP1}[1]	$V_O = V_{DD}*(0.5)$	12	33	65	Ω
Average Period	T_{PERIOD}	Fig. 8	15.00	15.01	15.30	ns
Output High Voltage	V_{OH}[1]	I_{OH} = -1 mA	2.05			V
Output Low Voltage	V_{OL}[1]	I_{OL} = 1 mA			0.65	V
Output High Current	I_{OH}[1]	$V_{OH@MIN}$ = 1.0 V, $V_{OH@MAX}$ = 3.135 V	-33		-28	mA
Output Low Current	I_{OL}[1]	$V_{OL@MIN}$ = 1.95 V, $V_{OL@MAX}$ = 0.4 V	26		38	mA
Rise Time	t_{r1}[1]	V_{OL} = 0.4 V, V_{OH} = 2.4 V (Fig. 7)	0.5	1.6	2.3	ns
Fall Time	t_{f1}[1]	V_{OH} = 2.4 V, V_{OL} = 0.4 V (Fig. 7)	0.5	1.2	2.3	ns
Duty Cycle	d_{t1}[1]	V_T = 1.5 V (Fig. 8)	45	48	55	%
Skew	t_{sk1}[1]	V_T = 1.5 V		40	250	ps
Jitter	$t_{jcyc-cyc}$[1]	V_T = 1.5 V (Fig. 8)		133	290	ps

[1]Guaranteed by design, not 100% tested in production.

Electrical Characteristics - VCH, 48MHz DOT, 48MHz, USB

T_A = 0 - 90°C; VDD=3.3V +/-5%; C_L = 10-20 pF (unless otherwise specified)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output Frequency	F_{O1}	Fig. 8		48		MHz
Output Impedance	R_{DSP1}[1]	$V_O = V_{DD}*(0.5)$	20	48	70	Ω
Output High Voltage	V_{OH}[1]	I_{OH} = -1 mA	2.05			V
Output Low Voltage	V_{OL}[1]	I_{OL} = 1 mA			0.5	V
Output High Current	I_{OH}[1]	$V_{OH@MIN}$ = 1.0 V, $V_{OH@MAX}$ = 3.135 V	-29		-20	mA
Output Low Current	I_{OL}[1]	$V_{OL@MIN}$ = 1.95 V, $V_{OL@MAX}$ = 0.4 V	25		27	mA
48DOT Rise Time	t_{r1}[1]	V_{OL} = 0.4 V, V_{OH} = 2.4 V (Fig. 7)	0.5	0.7	1.15	ns
48DOT Fall Time	t_{f1}[1]	V_{OH} = 2.4 V, V_{OL} = 0.4 V (Fig. 7)	0.5	0.8	1.15	ns
VCH 48 USB Rise Time	t_{r1}[1]	V_{OL} = 0.4 V, V_{OH} = 2.4 V (Fig. 7)	1	1.2	2.3	ns
VCH 48 USB Fall Time	t_{f1}[1]	V_{OH} = 2.4 V, V_{OL} = 0.4 V (Fig. 7)	1	1.4	2.3	ns
48 DOT Duty Cycle	d_{t1}[1]	V_T = 1.5 V (Fig. 8)	45	53	55	%
VCH 48 USB Duty Cycle	d_{t1}[1]	V_T = 1.5 V (Fig. 8)	45	53	55	%
48 DOT Jitter	$t_{jcyc-cyc}$[1]	V_T = 1.5 V (Fig. 8)		183	410	ps
USB to DOT Skew	t_{sk1}[1]	V_T = 1.5 V (180 degrees out of phase)		0.43	1	ns
VCH Jitter	$t_{jcyc-cyc}$[1]	V_T = 1.5 V (Fig. 8)		157	410	ps

[1]Guaranteed by design, not 100% tested in production.

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Electrical Characteristics - REF (1X select)

T_A = 0 - 90°C; VDD=3.3V +/-5%; C_L = 10-20 pF (unless otherwise specified)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output Frequency	F_{O1}	Fig. 8		14.318		MHz
Output Impedance	R_{DSP1}[1]	$V_O = V_{DD}*(0.5)$	20	48	70	Ω
Output High Voltage	V_{OH}[1]	I_{OH} = -1 mA	2.05			V
Output Low Voltage	V_{OL}[1]	I_{OL} = 1 mA			0.45	V
Output High Current	I_{OH}[1]	$V_{OH@MIN}$ = 1.0 V, $V_{OH@MAX}$ = 3.135 V	-29		-25	mA
Output Low Current	I_{OL}[1]	$V_{OL@MIN}$ = 1.95 V, $V_{OL@MAX}$ = 0.4 V	25		27	mA
Rise Time	t_{r1}[1]	V_{OL} = 0.4 V, V_{OH} = 2.4 V (Fig. 7)	0.5	1.1	2.3	ns
Fall Time	t_{f1}[1]	V_{OH} = 2.4 V, V_{OL} = 0.4 V (Fig. 7)	0.5	1.4	2.3	ns
Duty Cycle	d_{t1}[1]	V_T = 1.5 V	45	53	55	%
Jitter	$t_{jcyc-cyc}$[1]	V_T = 1.5 V (Fig. 8)		180	1200	ps

[1]Guaranteed by design, not 100% tested in production.

Electrical Characteristics - REF (2X select)

T_A = 0 - 90°C; VDD=3.3V +/-5%; C_L = 20-40 pF (unless otherwise specified)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output Frequency	F_{O1}	Fig. 8		14.318		MHz
Output Impedance	R_{DSP1}[1]	$V_O = V_{DD}*(0.5)$	12	33	65	Ω
Output High Voltage	V_{OH}[1]	I_{OH} = -1 mA	2.05			V
Output Low Voltage	V_{OL}[1]	I_{OL} = 1 mA			0.65	V
Output High Current	I_{OH}[1]	$V_{OH@MIN}$ = 1.0 V, $V_{OH@MAX}$ = 3.135 V	-33		-28	mA
Output Low Current	I_{OL}[1]	$V_{OL@MIN}$ = 1.95 V, $V_{OL@MAX}$ = 0.4 V	26		38	mA
Rise Time	t_{r1}[1]	V_{OL} = 0.4 V, V_{OH} = 2.4 V (Fig. 7)	0.5	1.1	2.3	ns
Fall Time	t_{f1}[1]	V_{OH} = 2.4 V, V_{OL} = 0.4 V (Fig. 7)	0.5	0.9	2.3	ns
Duty Cycle	d_{t1}[1]	V_T = 1.5 V	45	53	55	%
Jitter	$t_{jcyc-cyc}$[1]	V_T = 1.5 V (Fig. 8)		180	1200	ps

[1]Guaranteed by design, not 100% tested in production.

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Figure 1 - Differential (CPUCLK - CPUCLK#) Measurement Points (Tperiod, Duty Cycle, Jitter)

Figure 1 - Differential (CPUCLK - CPUCLK#) Measurement Points (Tperiod, Duty Cycle, Jitter)

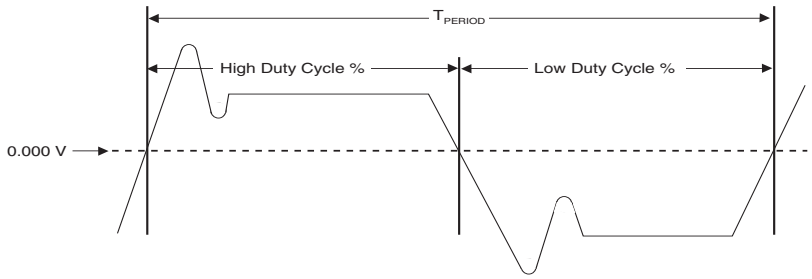
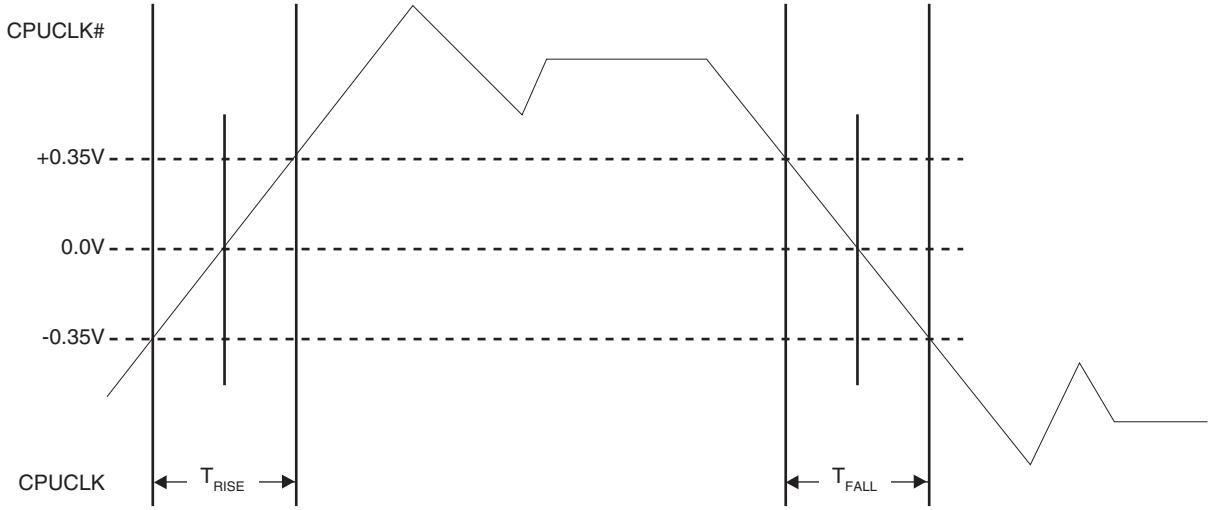


Figure 2 - 0.7V Differential TRise and TFall Measurement Points



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Figure 3 - 0.7V Single Ended Measurement Points for TRise, TFall

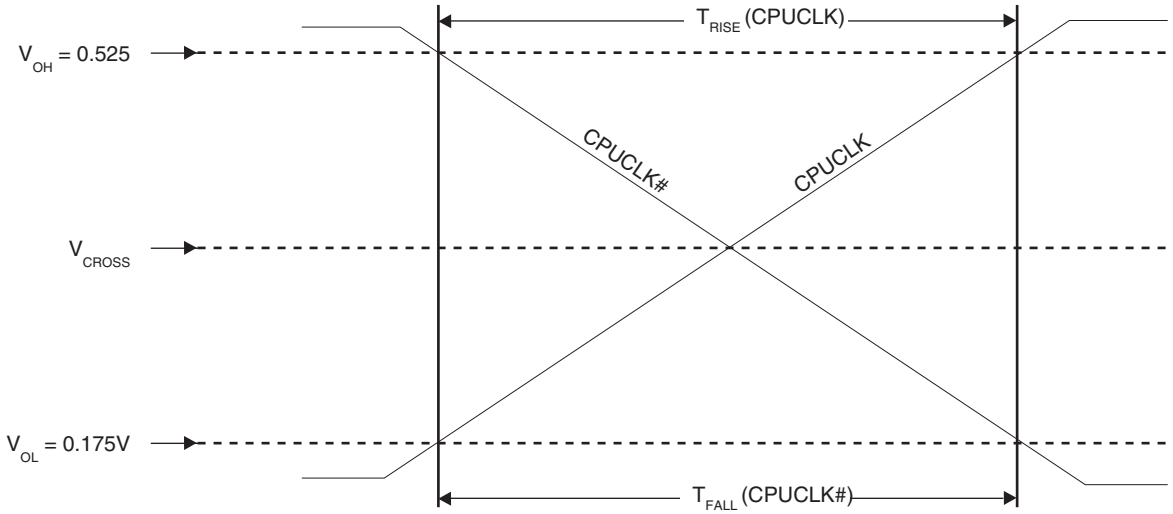
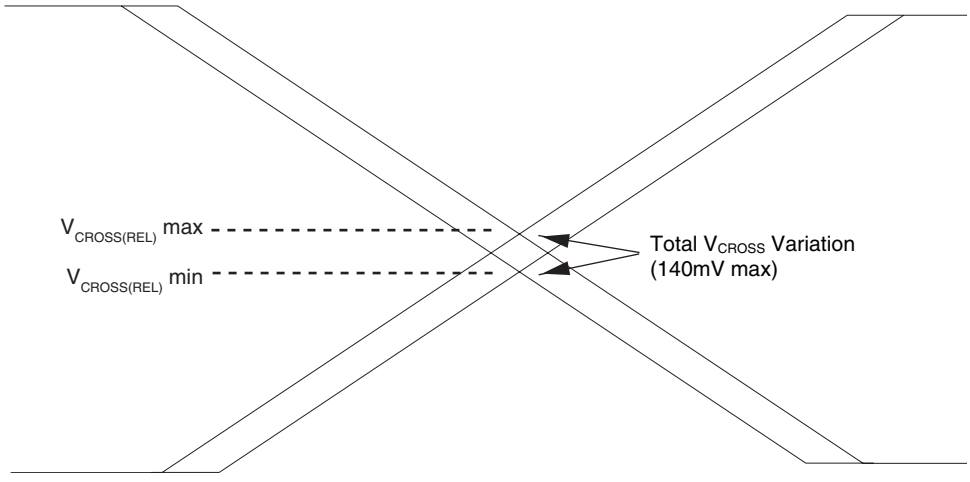


Figure 4 - 0.7V VCross Range Measurement Clarification



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Figure 5 - 1.0V Single Ended VCross, VOH and VOL Measurement Points

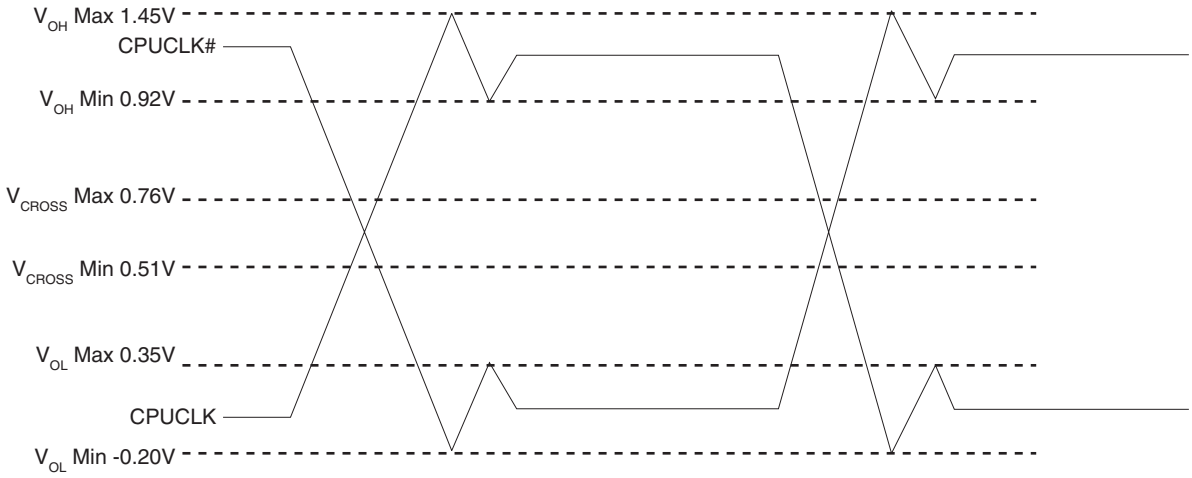
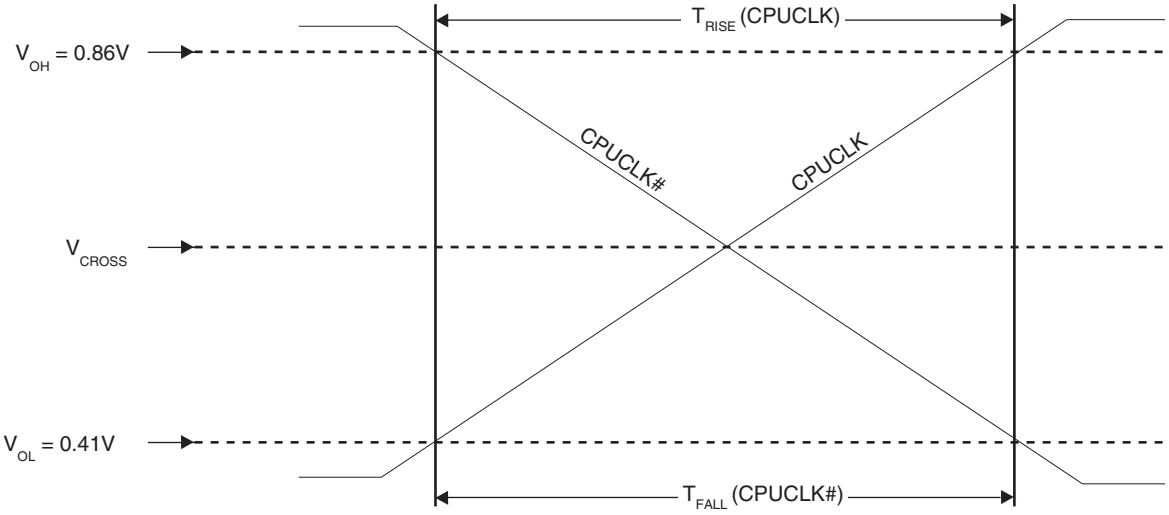


Figure 6 - 1.0V Single Ended Measurement Points for TRise, TFall



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Figure 7 - Measurement Points for TRise, TFall with Lumped Load

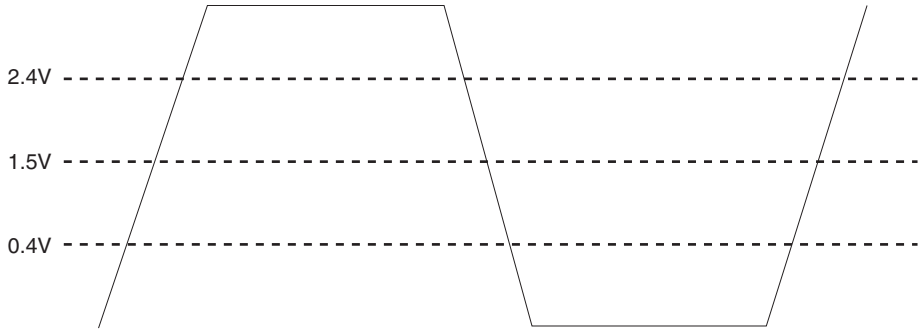
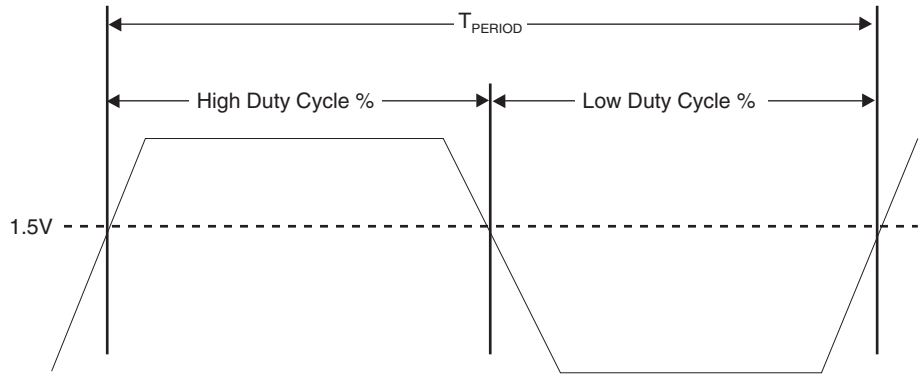


Figure 8 - Measurement Points for TPeriod, Duty Cycle and Jitter



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General SMBus serial interface information for the ICS950812

How to Write:

- Controller (host) sends a start bit.
- Controller (host) sends the write address D2 (H)
- ICS clock will ***acknowledge***
- Controller (host) sends the beginning byte location = N
- ICS clock will ***acknowledge***
- Controller (host) sends the data byte count = X
- ICS clock will ***acknowledge***
- Controller (host) starts sending ***Byte N through Byte N + X -1***
- ICS clock will ***acknowledge*** each byte ***one at a time***
- Controller (host) sends a Stop bit

How to Read:

- Controller (host) will send start bit.
- Controller (host) sends the write address D2 (H)
- ICS clock will ***acknowledge***
- Controller (host) sends the begining byte location = N
- ICS clock will ***acknowledge***
- Controller (host) will send a separate start bit.
- Controller (host) sends the read address D3 (H)
- ICS clock will ***acknowledge***
- ICS clock will send the data byte count = X
- ICS clock sends ***Byte N + X -1***
- ICS clock sends ***Byte 0 through byte X (if X(H) was written to byte 8)***.
- Controller (host) will need to acknowledge each byte
- Controller (host) will send a not acknowledge bit
- Controller (host) will send a stop bit

Index Block Write Operation

Controller (Host)		ICS (Slave/Receiver)
T	starT bit	
Slave Address D2(H)		
WR	WRite	
		ACK
Beginning Byte = N		
		ACK
Data Byte Count = X		
		ACK
Beginning Byte N	X Byte	
		ACK
O		
O		O
O		O
		O
Byte N + X - 1		
		ACK
P	stoP bit	

Index Block Read Operation

Controller (Host)		ICS (Slave/Receiver)	
T	starT bit		
Slave Address D2(H)			
WR	WRite		
		ACK	
Beginning Byte = N			
		ACK	
RT	Repeat starT		
Slave Address D3(H)			
RD	ReaD		
		ACK	
		Data Byte Count = X	
ACK			
		X Byte	Beginning Byte N
ACK			
			O
O			O
O			O
O			
			Byte N + X - 1
N	Not acknowledge		
P	stoP bit		

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BYTE 0	Affected Pin		Control Function	Type	Bit Control		
	Pin #	Name			0	1	PWD
Bit 7	-	Spread Enabled	Spread Spectrum Control	RW	OFF	ON	0
Bit 6	-	CPUCLKT(2:0)	Power down mode output level 0= CPU driven in power down 1= undriven	RW	HIGH	LOW	0
Bit 5	35	3V66_1/VCH_CLK/FS4**	VCH/66.66 Select	RW	66.66	48.00	0
Bit 4	53	CPU_STOP#*	Reflects value of pin	R	Stop	Active	X
Bit 3	34	PCI_STOP#*	Reflects value of pin at power up. Also can be set.	RW	Stop	Active	X
Bit 2	39	FS3	Frequency Selection	RW	-	-	X
Bit 1	55	FS1	Frequency Selection	R	-	-	X
Bit 0	54	FS0	Frequency Selection	R	-	-	X

Note: For PCI_STOP# function, refer to table 3.

BYTE 1	Affected Pin		Control Function	Type	Bit Control		
	Pin #	Name			0	1	PWD
Bit 7	43	MULTSEL*	Reflects value of pin	R	-	-	x
Bit 6	-	CPUCLKT(2:0)	CPU_Stop mode output level 0= CPU driven when stopped 1 = undriven	RW	HIGH	LOW	0
Bit 5	45, 44	CPUCLKT2, CPUCLKC2 (see note)	Allow control of output with assertion of CPU_STOP#.	RW	Not Freerun	Freerun	0
Bit 4	49, 48	CPUCLKT1, CPUCLKC1 (see note)	Allow control of output with assertion of CPU_STOP#.	RW	Not Freerun	Freerun	0
Bit 3	52, 51	CPUCLKT0, CPUCLKC0 (see note)	Allow control of output with assertion of CPU_STOP#.	RW	Not Freerun	Freerun	0
Bit 2	45, 44	CPUCLKT2, CPUCLKC2	Output control	RW	Disable	Enable	1
Bit 1	49, 48	CPUCLKT1, CPUCLKC1	Output control	RW	Disable	Enable	1
Bit 0	52, 51	CPUCLKT0, CPUCLKC0	Output control	RW	Disable	Enable	1

Note: CPUCLK(2:0) can be turned on/off by CPU_STOP#. Refer to table 4.

BYTE 2	Affected Pin		Control Function	Type	Bit Control		
	Pin #	Name			0	1	PWD
Bit 7	56	REF	1X or 2X Strength control	RW	1X	2X	0
Bit 6	18	PCICLK6	Output control	RW	Disable	Enable	1
Bit 5	17	PCICLK5	Output control	RW	Disable	Enable	1
Bit 4	16	PCICLK4	Output control	RW	Disable	Enable	1
Bit 3	13	**E_PCICLK3/PCICLK3	Output control	RW	Disable	Enable	1
Bit 2	12	PCICLK2	Output control	RW	Disable	Enable	1
Bit 1	11	**E_PCICLK1/PCICLK1	Output control	RW	Disable	Enable	1
Bit 0	10	PCICLK0	Output control	RW	Disable	Enable	1

Note: PCICLK(6:0) can be turned on/off by PCI_STOP#. Refer to table 3.

BYTE 3	Affected Pin		Control Function	Type	Bit Control		
	Pin #	Name			0	1	PWD
Bit 7	38	48MHz_DOT	Output control	RW	Disable	Enable	1
Bit 6	39	48MHz_USB/FS3**	Output control	RW	Disable	Enable	1
Bit 5	7	PCICLK_F2 (see note)	Allow control of output with assertion of PCI_STOP#.	RW	Freerun	Not Freerun	0
Bit 4	6	PCICLK_F1 (see note)	Allow control of output with assertion of PCI_STOP#.	RW	Freerun	Not Freerun	0
Bit 3	5	PCICLK_F0 (see note)	Allow control of output with assertion of PCI_STOP#.	RW	Freerun	Not Freerun	0
Bit 2	7	PCICLK_F2	Output control	RW	Disable	Enable	1
Bit 1	6	PCICLK_F1	Output control	RW	Disable	Enable	1
Bit 0	5	PCICLK_F0	Output control	RW	Disable	Enable	1

Note: PCICLK_F(2:0) can be turned on/off by PCI_STOP#. Refer to table 5.

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BYTE 4	Affected Pin		Control Function	Type	Bit Control		
	Pin #	Name			0	1	PWD
Bit 7	35	FS4	Frequency Selection	RW	Disable	Enable	X
Bit 6	33	FS5	Frequency Selection	RW	Disable	Enable	X
Bit 5	33	3V66_0/FS5**	Output control	RW	Disable	Enable	1
Bit 4	35	3V66_1/VCH_CLK/FS4**	Output control	RW	Disable	Enable	1
Bit 3	24	66MHZ_IN/3V66_5	Output control	RW	Disable	Enable	1
Bit 2	23	66MHZ_OUT2/3V66_4	Output control	RW	Disable	Enable	1
Bit 1	22	66MHZ_OUT1/3V66_3	Output control	RW	Disable	Enable	1
Bit 0	21	66MHZ_OUT0/3V66_2	Output control	RW	Disable	Enable	1

BYTE 5	Affected Pin		Control Function	Type	Bit Control		
	Pin #	Name			0	1	PWD
Bit 7	X	-	Unused	-	-	-	0
Bit 6	X	-	Reserved	X	-	-	0
Bit 5	X	3V66(5:2)/66MHZ_OUT(2:0) (See table 6)	Allow control of output with assertion of CPU_STOP#.	X	Freerun	Not Freerun	0
Bit 4	X	3V66(1:0) (See table 7)	Allow control of output with assertion of CPU_STOP#.	X	Freerun	Not Freerun	0
Bit 3	38	48MHz_DOT Slew Control	00 = Medium (default), 01 = Low, 11,10 =High	RW	-	-	0
Bit 2				RW	-	-	0
Bit 1	39	48MHz_USB Slew Control	00 = Medium (default), 01 = Low, 11,10 =High	RW	-	-	0
Bit 0				RW	-	-	0

Note: Functions in Byte 5 of CK408 were intended as a test and debug byte only.

BYTE 6	Affected Pin		Control Function	Type	Bit Control		
	Pin #	Name			0	1	PWD
Bit 7	X	Revision ID Bit 3	Revision ID Value Based on Device Revision	R	-	-	X
Bit 6	X	Revision ID Bit 2		R	-	-	X
Bit 5	X	Revision ID Bit 1		R	-	-	X
Bit 4	X	Revision ID Bit 0		R	-	-	X
Bit 3	X	Vendor ID Bit 3	(Reserved)	R	-	-	0
Bit 2	X	Vendor ID Bit 2	(Reserved)	R	-	-	0
Bit 1	X	Vendor ID Bit 1	(Reserved)	R	-	-	0
Bit 0	X	Vendor ID Bit 0	(Reserved)	R	-	-	1

BYTE 7	Affected Pin		Control Function	Type	Bit Control		
	Pin #	Name			0	1	PWD
Bit 7	X	-	Unused	R	-	-	0
Bit 6	X	-	Unused	R	-	-	0
Bit 5	X	-	Unused	R	-	-	0
Bit 4	X	-	Unused	R	-	-	0
Bit 3	X	-	Unused	R	-	-	0
Bit 2	X	-	Unused	R	-	-	0
Bit 1	X	-	Unused	R	-	-	0
Bit 0	X	-	Unused	R	-	-	0

BYTE 8	Affected Pin		Control Function	Type	Bit Control		
	Pin #	Name			0	1	PWD
Bit 7	X	-	(Reserved)	X	-	-	0
Bit 6	X	-	(Reserved)	X	-	-	0
Bit 5	X	-	(Reserved)	X	-	-	0
Bit 4	X	-	(Reserved)	X	-	-	0
Bit 3	X	-	Readback Byte Count	R	-	-	1
Bit 2	X	-		R	-	-	1
Bit 1	X	-		R	-	-	1
Bit 0	X	-		R	-	-	1

Note: Byte 8 is for ICS test only. Do not write as system damage may occur. Bit(3:0) contain the readback Byte count.

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BYTE 9	Affected Pin		Control Function	Type	Bit Control		
	Pin #	Name			0	1	PWD
Bit 7	35	VCHCLK Slew Control	00 = High(default), 01 = Low, 11,10 = Medium	RW	-	-	0
Bit 6				RW	-	-	0
Bit 5	7, 6, 5	PCICLK_F (2:0) Slew Contol	00 (default), 11 = Medium 01 = Low, 10 =High	RW	-	-	0
Bit 4				RW	-	-	0
Bit 3	13, 12, 11, 10	PCICLK (3:0) Slew Contol	00 (default), 11 = Medium 10 = Low, 01 =High	RW	-	-	0
Bit 2				RW	-	-	0
Bit 1	18, 17, 16, 13, 12, 11, 10	PCICLK (6:0) Slew Contol	00 (default), 11 = Medium 10 = Low, 01 =High	RW	-	-	0
Bit 0				RW	-	-	0

BYTE 10	Affected Pin		Control Function	Type	Bit Control		
	Pin #	Name			0	1	PWD
Bit 7	X	-	M/N Enable (Enable access to Byte 11 - 14)	RW	HW/B0	Byte (11-14)	0
Bit 6	X	-	Unused	-	-	-	0
Bit 5	24, 23, 22, 21	3V66(5:2)/66MHZ_OUT(2:0) Skew	Approx 250ps per bit (Ref to PCI)	RW	-	-	0
Bit 4				RW	-	-	0
Bit 3	33, 35	3V66(1:0) Skew	Approx 250ps per bit (Ref to PCI)	RW	-	-	0
Bit 2				RW	-	-	0
Bit 1	X	-	Unused	-	-	-	0
Bit 0	X	-	Unused	-	-	-	0

BYTE 11	Affected Pin		Control Function	Type	Bit Control		
	Pin #	Name			0	1	PWD
Bit 7	X	-	VCO Divider Bit8	RW	-	-	X
Bit 6	X	-	REF Divider Bit6	RW	-	-	X
Bit 5	X	-	REF Divider Bit5	RW	-	-	X
Bit 4	X	-	REF Divider Bit4	RW	-	-	X
Bit 3	X	-	REF Divider Bit3	RW	-	-	X
Bit 2	X	-	REF Divider Bit2	RW	-	-	X
Bit 1	X	-	REF Divider Bit1	RW	-	-	X
Bit 0	X	-	REF Divider Bit0	RW	-	-	X

Note: The decimal representation of these 7 bits (Byte 11 bit[6:0]) + 2 is equal to the REF divider value.

BYTE 12	Affected Pin		Control Function	Type	Bit Control		
	Pin #	Name			0	1	PWD
Bit 7	X	-	VCO Divider Bit7	RW	-	-	X
Bit 6	X	-	VCO Divider Bit6	RW	-	-	X
Bit 5	X	-	VCO Divider Bit5	RW	-	-	X
Bit 4	X	-	VCO Divider Bit4	RW	-	-	X
Bit 3	X	-	VCO Divider Bit3	RW	-	-	X
Bit 2	X	-	VCO Divider Bit2	RW	-	-	X
Bit 1	X	-	VCO Divider Bit1	RW	-	-	X
Bit 0	X	-	VCO Divider Bit0	RW	-	-	X

Note: The decimal representation of these 9 bits (Byte 12 bit[7:0]) and Byte 11 bit [7]) + 8 is equal to the VCO divider value.

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BYTE 13	Affected Pin		Control Function	Type	Bit Control		
	Pin #	Name			0	1	PWD
Bit 7	X	-	Spread Spectrum Bit7	RW	-	-	X
Bit 6	X	-	Spread Spectrum Bit6	RW	-	-	X
Bit 5	X	-	Spread Spectrum Bit5	RW	-	-	X
Bit 4	X	-	Spread Spectrum Bit4	RW	-	-	X
Bit 3	X	-	Spread Spectrum Bit3	RW	-	-	X
Bit 2	X	-	Spread Spectrum Bit2	RW	-	-	X
Bit 1	X	-	Spread Spectrum Bit1	RW	-	-	X
Bit 0	X	-	Spread Spectrum Bit0	RW	-	-	X

Note: Please utilize software utility provided by ICS Application Engineering to configure spread spectrum. Incorrect spread percentage may cause system failure.

BYTE 14	Affected Pin		Control Function	Type	Bit Control		
	Pin #	Name			0	1	PWD
Bit 7	X	-	(Reserved)	RW	-	-	X
Bit 6	X	-	(Reserved)	RW	-	-	X
Bit 5	X	-	Spread Spectrum Bit13	RW	-	-	X
Bit 4	X	-	Spread Spectrum Bit12	RW	-	-	X
Bit 3	X	-	Spread Spectrum Bit11	RW	-	-	X
Bit 2	X	-	Spread Spectrum Bit10	RW	-	-	X
Bit 1	X	-	Spread Spectrum Bit9	RW	-	-	X
Bit 0	X	-	Spread Spectrum Bit8	RW	-	-	X

Note: Please utilize software utility provided by ICS Application Engineering to configure spread spectrum. Incorrect spread percentage may cause system failure.

Note: See table 8 for Byte 11-14 default information

Spread Spectrum Enable Procedure

Step 1: Power-up ---- Latched inputs, FS(5:0), set frequency per Hardware default on board. SS is off. BIOS program set IIC Byte0, bit7 to 1, SS will be enable Spread. Note that Byte 10, bit 7 is default to 0. This allows all setup to be controlled by the Frequency Select Tables, 1 and 2.

Step 2: After power up, SS% can be changed to the fixed selections shown in Frequency Table 2. This is achieved by Writing to Byte 4, bit 6/7 (FS5:4) and/or Byte 0 (FS3), The data written to these bytes will overwrite the existing contents and switch to the desired selection.

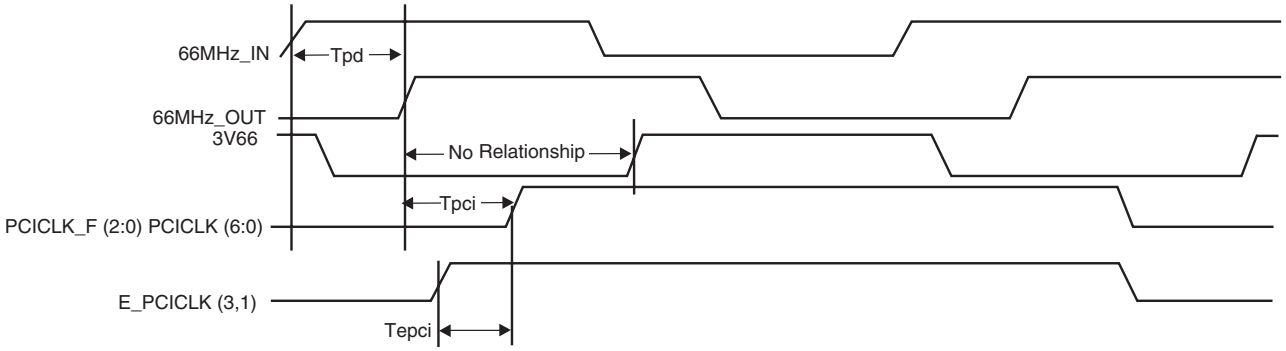
Step 3: To set up Linear programming and SS% adjust using Byte 11 through 14, the BIOS must set Byte 10, bit 7 to a 1. This will enable access to Byte 11 and 12, M/N linear programming and Byte 13 and 14, Spread Spectrum % adjust.

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Buffered Mode - 3V66[0:1], 66MHz_IN, 66MHz_OUT[0:2] and PCI Phase Relationship

All 3V66 clocks are to be in phase with each other. All 66MHz_OUT clocks are to be in phase with each other. There is NO phase relationship between the 3V66 clocks and the 66MHz_OUT and PCI clocks. In the case where 3V66_1 is configured as 48MHz VCH clock, there is no defined phase relationship between 3V66_1_VCH and other 3V66 clocks. The PCI group should lag 3V66 by the standard skew described below as Tpci.

The 66MHz_IN to 66MHz_OUT delay is shown in the figure below and is specified to be within a min and max propagation value.



Group to Group Skews at Common Transition Edges: Buffered Mode

GROUP	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
66MHz_IN 66MHz_OUT[1,2]	Tpd	Propogation delay from 66MHz_IN to 66MHz_OUT (2:0)	2.5	2.9	4.5	ns
66MHz_OUT to PCI[1,2]	Tpci	66MHz_OUT (2:0) leads 33 MHz PCICLK	1.5		3.5	ns

[1]Guaranteed by design, not 100% tested in production.

[2]500ps Tolerance

E_PCICLK to PCICLK Skews

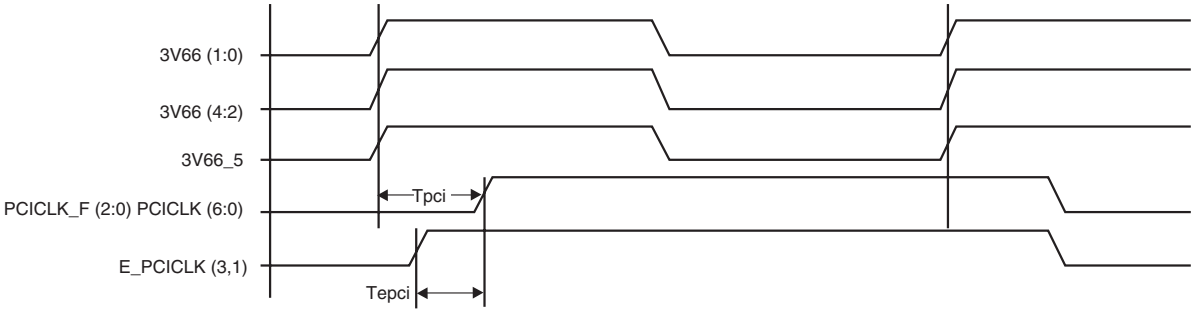
GROUP	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
E_PCICLK to PCICLK[1]	$T_{E_PCI-PCI1}$	E_PCICLK1 (pin 11)=0 E_PCICLK3 (pin 13)=1	0.3	0.5	0.7	ns
	$T_{E_PCI-PCI2}$	E_PCICLK1 (pin 11)=1 E_PCICLK3 (pin 13)=0	0.8	1.0	1.2	ns
	$T_{E_PCI-PCI3}$	E_PCICLK1 (pin 11)=1 E_PCICLK3 (pin 13)=1	1.3	1.5	1.7	ns

[1]Guaranteed by design, not 100% tested in production.

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Un-Buffered Mode 3V66 & PCI Phase Relationship

All 3V66 clocks are to be in pphase with each other. In the case where 3V66_1 is configured as 48MHz VCH clock, there is no defined phase relationship between 3V66_1_VCH and other 3V66 clocks. The PCI group should lag 3V66 by the standard skew described below as Tpci.



Group to Group Skews at Common Transition Edges: Unbuffered Mode

GROUP	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
3V66 to PCI[1,2]	$S_{3V66-PCI}$	3V66 (5:0) leads 33MHz PCI	1.5	2.55	3.5	ns

[1]Guarenteed by design, not 100% tested in production.

[2]500ps Tolerance

E_PCICLK to PCICLK Skews

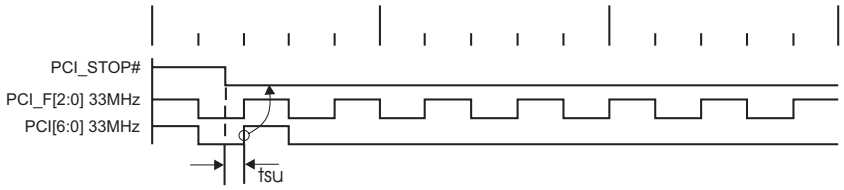
GROUP	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
E_PCICLK to PCICLK[1]	$T_{E_PCI-PCI0}$	E_PCICLK1 (pin 11)=0 E_PCICLK3 (pin 13)=0	-0.2	0	0.2	ns
	$T_{E_PCI-PCI1}$	E_PCICLK1 (pin 11)=0 E_PCICLK3 (pin 13)=1	0.3	0.5	0.7	ns
	$T_{E_PCI-PCI2}$	E_PCICLK1 (pin 11)=1 E_PCICLK3 (pin 13)=0	0.8	1.0	1.2	ns
	$T_{E_PCI-PCI3}$	E_PCICLK1 (pin 11)=1 E_PCICLK3 (pin 13)=1	1.3	1.5	1.7	ns

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PCI_STOP# - Assertion (transition from logic "1" to logic "0")

The impact of asserting the PCI_STOP# signal will be the following. All PCI[6:0] and stoppable PCI_F[2,0] clocks will latch low in their next high to low transition. The PCI_STOP# setup time tsu is 10 ns, for transitions to be recognized by the next rising edge.

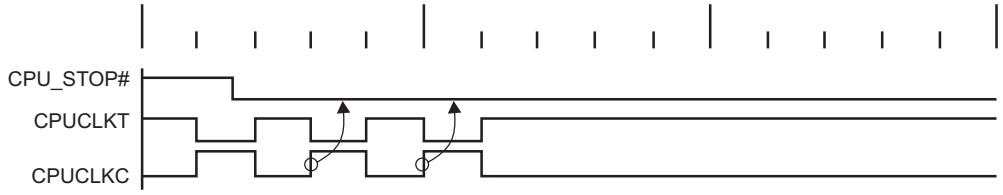
Assertion of PCI_STOP# Waveforms



CPU_STOP# - Assertion (transition from logic "1" to logic "0")

The impact of asserting the CPU_STOP# pin is all CPU outputs that are set in the I^2C configuration to be stoppable via assertion of CPU_STOP# are to be stopped after their next transition. When the I^2C Bit 6 of Byte 1 is programmed to '0' the final state of the stopped CPU signals is CPU = High and CPU# = Low. There is to be no change to the output drive current values. The CPU will be driven high with a current value equal to (Mult 0 'select') x (Iref), the CPU# signal will not be driven . When the I^2C Bit 6 of Byte 1 is programmed to '1' then final state of the stopped CPU signals is Low, both CPU and CPU# outputs will not be driven.

Assertion of CPU_STOP# Waveforms



CPU_STOP# Functionality

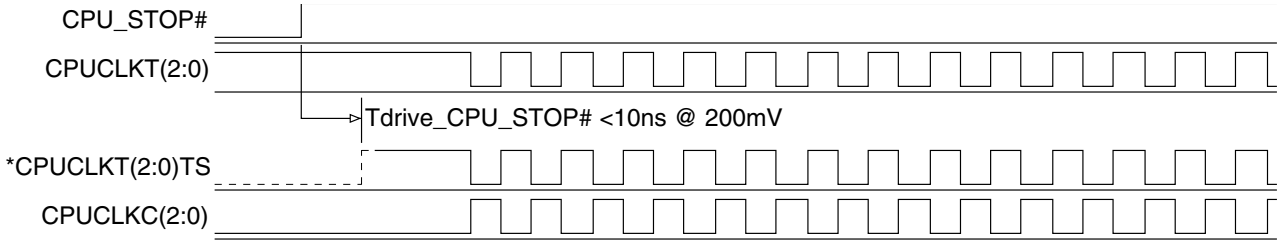
CPU_STOP#	CPUT	CPUC
1	Normal	Normal
0	iref * Mult	Float

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CPU_STOP# - De-assertion (transition from logic "0" to logic "1")

All CPU outputs that were stopped are to resume normal operation in a glitch free manner. The maximum latency from the de-assertion to active outputs is to be defined to be between 2 - 6 CPU clock periods (2 clocks are shown). If the I2C Bit 6 of Byte 1 is programmed to "1" then the stopped CPU outputs will be driven High within 10 nS of CPU_Stop# de-assertion.

De-assertion of CPU_STOP# Waveforms

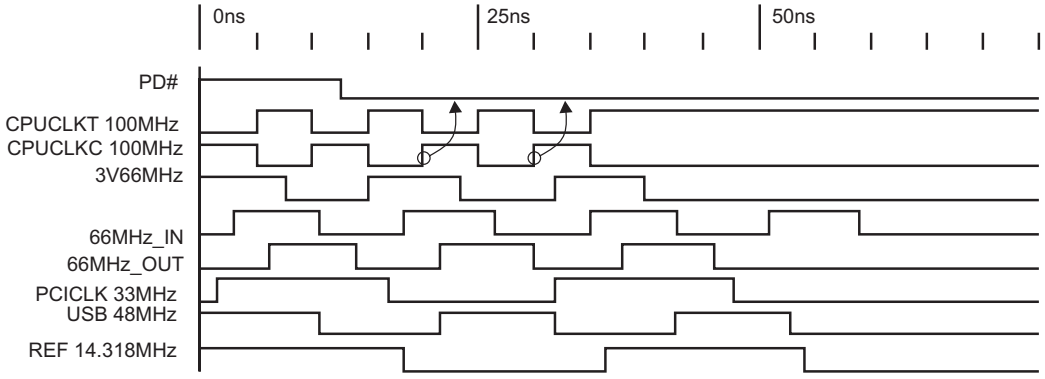


*Signal TS is CPUCLKT in Tri-State mode

PD# - Assertion (transition from logic "1" to logic "0")

When PWRDWN# is sampled low by two consecutive rising edges of CPU clock, then all clock outputs except CPU clocks must be held low on their next high to low transitions. When the I2C Bit 6 of Byte 0 is programmed to '0' CPU clocks must be held with the CPU clock pin driven high with a value of 2 x Iref, and CPU# undriven. If Bit 6 of Byte 0 is '1' then both CPU and CPU# are undriven. Note the example below shows CPU = 133 MHz and Bit 6 of Byte 0 = '0', this diagram and description is applicable for all valid CPU frequencies 66, 100, 133, 200 MHz.
Due to the state if the internal logic, stopping and holding the REF clock outputs in the LOW state may require more than one clock cycle to complete.

Power Down Assertion of Waveforms



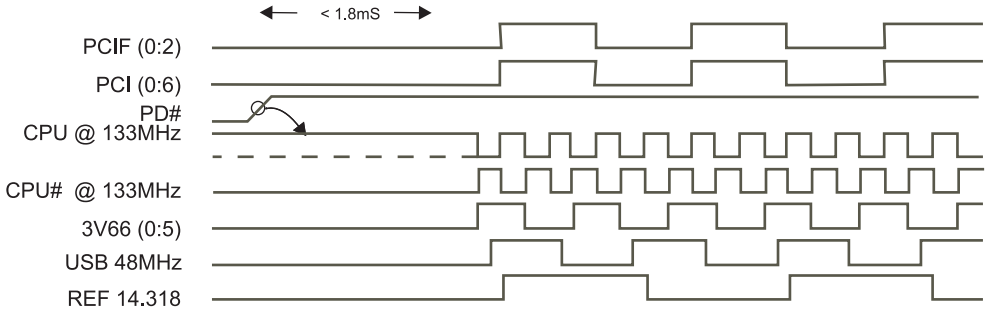
PD# Functionality

PD#	CPUCLKT	CPUCLKC	3V66	66MHz_OUT	PCICLK_F PCICLK	PCICLK	USB/DOT 48MHz
1	Normal	Normal	66MHz	66MHz_IN	66MHz_IN/2	66MHz_IN/2	48MHz
0	iref * Mult	Float	Low	Low	Low	Low	Low

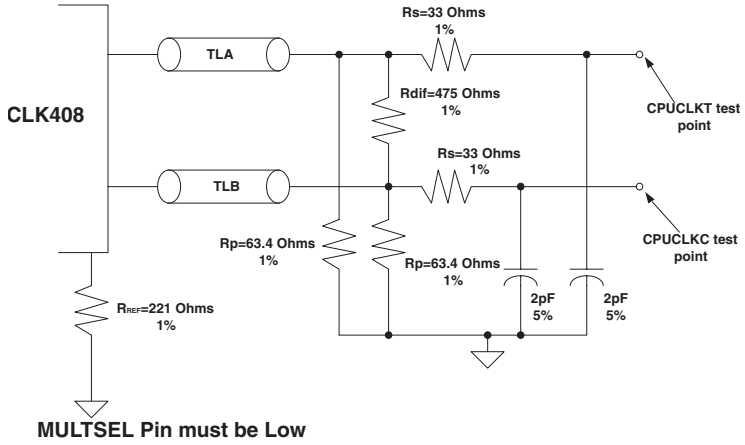
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Power Down De-Assertion Mode

The power-up latency needs to be less than 1.8mS. this is the time from the de-asseration of the powerdown of the ramping of the power supply until the time that stable clocks are output from the clock chip. If the I^2C Bit 6 of Byte 0 is programmed to "1" then the stopped CPU outputs will be driven high within 3 nS of PD# de-asseration.

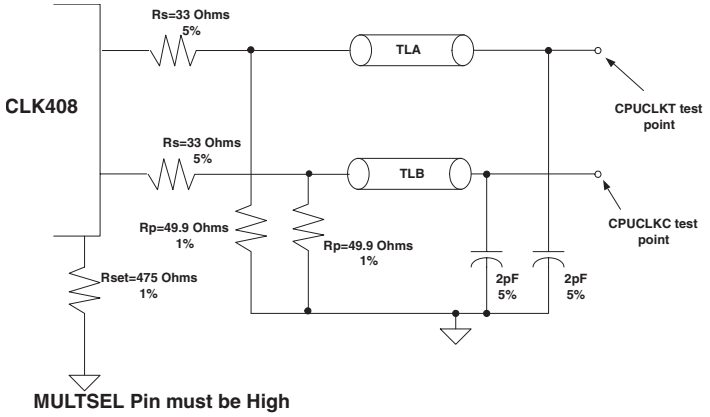


Test Configuration Diagrams



MULTSEL Pin must be Low

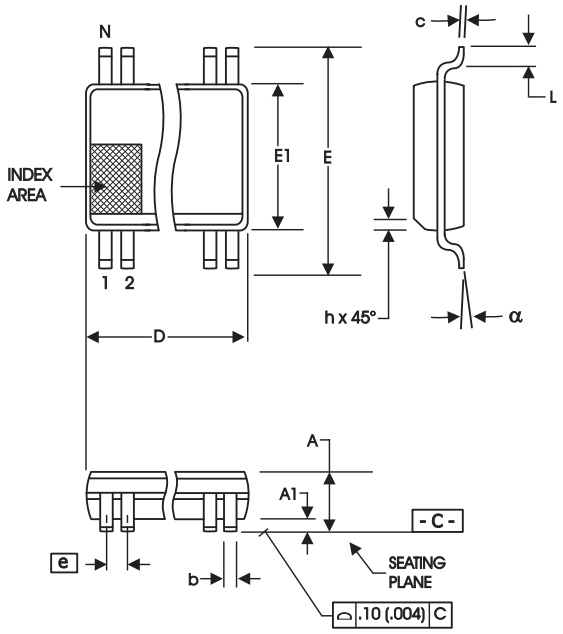
CPU 1.0V Configuration test load board termination



MULTSEL Pin must be High

CPU 0.7V Configuration test load board termination

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300 mil SSOP Package

SYMBOL	In Millimeters COMMON DIMENSIONS		In Inches COMMON DIMENSIONS	
	MIN	MAX	MIN	MAX
A	2.41	2.80	.095	.110
A1	0.20	0.40	.008	.016
b	0.20	0.34	.008	.0135
c	0.13	0.25	.005	.010
D	SEE VARIATIONS		SEE VARIATIONS	
E	10.03	10.68	.395	.420
E1	7.40	7.60	.291	.299
e	0.635 BASIC		0.025 BASIC	
h	0.38	0.64	.015	.025
L	0.50	1.02	.020	.040
N	SEE VARIATIONS		SEE VARIATIONS	
α	0°	8°	0°	8°

VARIATIONS

N	D mm.		D (inch)	
	MIN	MAX	MIN	MAX
56	18.31	18.55	.720	.730

Reference Doc.: JEDEC Publication 95, MO-118

10-0034

Ordering Information

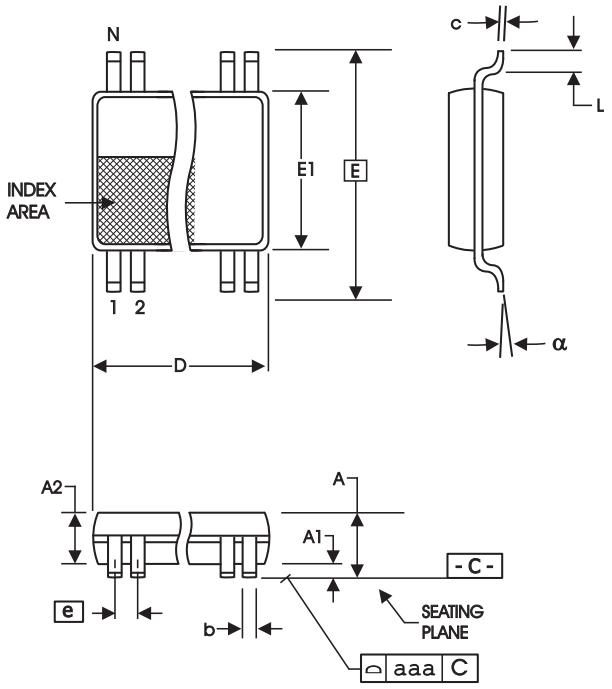
950812yFLFT

Example:

XXXX y F LF T

- **Designation for tape and reel packaging**
- **RoHS Compliant (Optional)**
- **Package Type**
  F = SSOP
- **Revision Designator** (will not correlate with datasheet revision)
- **Device Type (consists of 3 to 7 digit numbers)**

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6.10 mm. Body, 0.50 mm. pitch TSSOP
(240 mil) (20 mil)

SYMBOL	In Millimeters COMMON DIMENSIONS		In Inches COMMON DIMENSIONS	
	MIN	MAX	MIN	MAX
A	--	1.20	--	.047
A1	0.05	0.15	.002	.006
A2	0.80	1.05	.032	.041
b	0.17	0.27	.007	.011
c	0.09	0.20	.0035	.008
D	SEE VARIATIONS		SEE VARIATIONS	
E	8.10 BASIC		0.319 BASIC	
E1	6.00	6.20	.236	.244
e	0.50 BASIC		0.020 BASIC	
L	0.45	0.75	.018	.030
N	SEE VARIATIONS		SEE VARIATIONS	
α	0°	8°	0°	8°
aaa	--	0.10	--	.004

VARIATIONS

N	D mm.		D (inch)	
	MIN	MAX	MIN	MAX
56	13.90	14.10	.547	.555

Reference Doc.: JEDEC Publication 95, MO-153

10-0039

Ordering Information

950812yGLFT

Example:

XXXX y G LF T

- **Designation for tape and reel packaging**
- **RoHS Compliant (Optional)**
- **Package Type**
  G = TSSOP
- **Revision Designator** (will not correlate with datasheet revision)
- **Device Type (consists of 3 to 7 digit numbers)**

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Revision History

Rev.	Issue Date	Description	Page #
I	8/4/2005	1. Moved SMBus after page 22. 2. Corrected 3V66 Buffered mode on Electrical Characteristics Table. 3. Added DC Characteristics to REF2X Electrical Characteristics Table. 4. Updated LF Ordering Information to RoHS Compliant.	11, 13, 28, 29
J	1/25/2010	Updated document template	
K	3/23/2016	Updated block diagram and Output Features	1

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