Programmable Timing Control Hub™ for P4™

Recommended Application:

VIA Pro266/PN266/CLE266/CM400 chipset for PIII/Tualatin/C3 Processor

Output Features:

- 1 - Pair of differential CPU clocks @ 3.3V (CK408)/
- 1 - Pair of differential open drain CPU clocks (K7)
- 2 - Push pull CPUT_CS clocks @ 2.5V
- 3 - AGP @ 3.3V
- 7 - PCI @ 3.3V
- 1 - 48MHz @ 3.3V fixed
- 1 - 24_48MHz @ 3.3V
- 2 - REF @ 3.3V, 14.318MHz

Key Specifications:

- CPU_CS - CPUT/C: <±250ps
- CPU_CS - AGP: <±250ps
- CPU - DDR/SD: <±250ps
- PCI - PCI: <500ps

Features/Benefits:

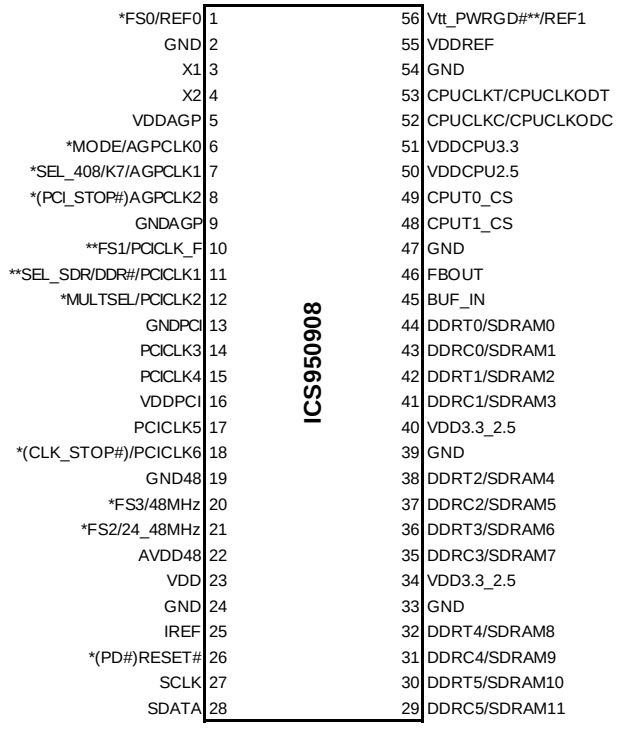
- Programmable output frequency.
- Programmable output divider ratios.
- Programmable output rise/fall time.
- Programmable output skew.
- Programmable spread percentage for EMI control.
- Watchdog timer technology to reset system if system malfunctions.
- Programmable watch dog safe frequency.
- Support I^2C Index read/write and block read/write operations.
- Uses external 14.318MHz crystal.

Frequency Table

FS3	FS2	FS1	FS0	CPUCLK MHz	AGP MHz	PCICLK MHz
0	0	0	0	160.00	80.00	40.00
0	0	0	1	164.00	82.00	41.00
0	0	1	0	166.60	66.60	33.30
0	0	1	1	170.00	68.00	34.00
0	1	0	0	175.00	70.00	35.00
0	1	0	1	180.00	72.00	36.00
0	1	1	0	185.00	74.00	37.00
0	1	1	1	190.00	76.00	38.00
1	0	0	0	66.80	66.80	33.40
1	0	0	1	100.90	67.27	33.63
1	0	1	0	133.60	66.80	33.40
1	0	1	1	200.40	66.80	33.40
1	1	0	0	66.60	66.60	32.30
1	1	0	1	100.00	66.60	33.30
1	1	1	0	200.00	66.60	33.30
1	1	1	1	133.30	66.60	33.30

MULTISEL0	Board Target Trace/Term Z	Reference R, Iref = $V_{DD}/(3*Rr)$	Output Current	Voh @ Z
0	50 ohms	Rr = 221 1%, Iref = 5.00mA	Ioh = 4* I REF	1.0V @ 50
1	50 ohms	Rr = 475 1%, Iref = 2.32mA	Ioh = 6* I REF	0.7V @ 50

Pin Configuration



* Internal 120K pull-up resistor to VDD.

** Internal 120K pull-down resistor to GND.

56-Pin 300-mil SSOP

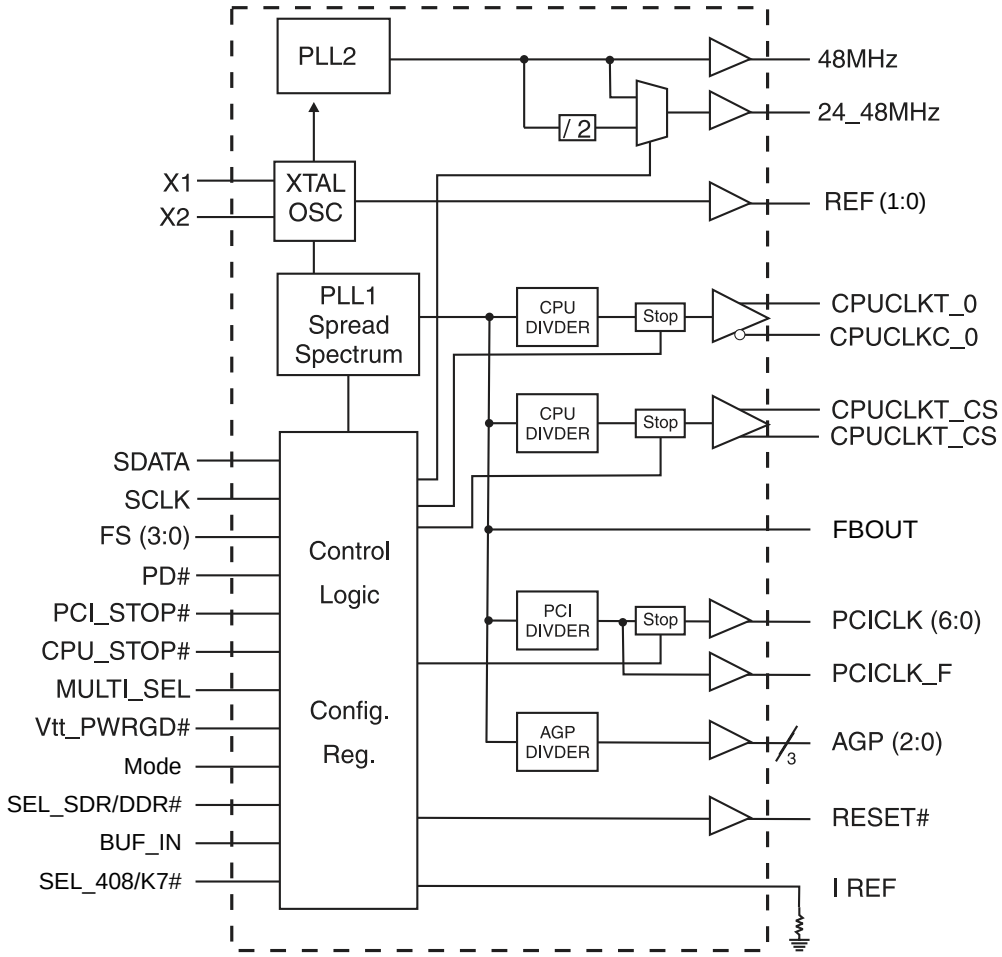
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General Description

The **ICS950908** is a single chip clock solution for desktop designs using the VIA Pro266/PN266/CLE266/CM400 chipset with PC133 or DDR memory.

The **ICS950908** is part of a whole new line of ICS clock generators and buffers called TCH™ (Timing Control Hub). This part incorporates ICS's newest clock technology which offers more robust features and functionality. Employing the use of a serially programmable I^2C interface, this device can adjust the output clocks by configuring the frequency setting, the output divider ratios, selecting the ideal spread percentage, the output skew, the output strength, and enabling/disabling each individual output clock. M/N control can configure output frequency with resolution up to 0.1MHz increment.

Block Diagram



Power Groups

Pin Number		Description
VDD	GND	
55	2	Xtal, Ref
5	9	AGP [0:2], CPU digital, CPU PLL
16	13	PCI [0:5], PCI_F outputs
22	19	48MHz, Fix Digital, Fix Analog
23	24	Master clock, CPU Analog
34, 40	33, 39	DDR/SDR outputs
50	47	2.5V CPUT_CS output
51	54	3.3V CPUT/C & CPUOD_T/C

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Pin Description

PIN #	PIN NAME	PIN TYPE	DESCRIPTION
1	*FS0/REF0	I/O	Frequency select latch input pin / 14.318 MHz reference clock.
2	GND	PWR	Ground pin.
3	X1	IN	Crystal input, Nominally 14.318MHz.
4	X2	OUT	Crystal output, Nominally 14.318MHz
5	VDDAGP	PWR	Power supply for AGP clocks, nominal 3.3V
6	*MODE/AGPCLK0	I/O	Function select latch input pin, 1=Desktop Mode, 0=Mobile Mode / AGP clock output.
7	*SEL_408/K7/AGPCLK1	I/O	CPU output type select latch input pin 0= K7, 1= CK408 / AGP clock output.
8	*(PCI_STOP#)AGPCLK2	I/O	Stops all PCICLKs besides the PCICLK_F clocks at logic 0 level, when input low. This input is activated by the MODE selection pin / AGP clock output.
9	GNDAGP	PWR	Ground pin for the AGP outputs
10	**FS1/PCICLK_F	I/O	Frequency select latch input pin / 3.3V PCI free running clock output.
11	**SEL_SDR/DDR#/PCICLK1	I/O	Memory type select latch input pin 0= DDR, 1= PC133 SDRAM / 3.3V PCI clock output.
12	*MULTSEL/PCICLK2	I/O	3.3V LVTTL input for selection the current multiplier for CPU outputs / 3.3V PCI clock output.
13	GNDPCI	PWR	Ground pin for the PCI outputs
14	PCICLK3	OUT	PCI clock output.
15	PCICLK4	OUT	PCI clock output.
16	VDDPCI	PWR	Power supply for PCI clocks, nominal 3.3V
17	PCICLK5	OUT	PCI clock output.
18	*(CLK_STOP#)/PCICLK6	I/O	Stops all CPU, DDR/SDRAM and FB_OUT clocks at logic 0 level, when input low. This input is activated by the MODE selection pin / PCI clock output.
19	GND48	PWR	Ground pin for the 48MHz outputs
20	*FS3/48MHz	I/O	Frequency select latch input pin / Fixed 48MHz clock output. 3.3V
21	*FS2/24_48MHz	I/O	Frequency select latch input pin / Fixed 24 or 48MHz clock output. 3.3V.
22	AVDD48	PWR	Analog power for 48MHz outputs and fixed PLL core, nominal 3.3V
23	VDD	PWR	Power supply, nominal 3.3V
24	GND	PWR	Ground pin.
25	IREF	OUT	This pin establishes the reference current for the differential current-mode output pairs. This pin requires a fixed precision resistor tied to ground in order to establish the appropriate current. 475 ohms is the standard value.
26	*(PD#)RESET#	I/O	Asynchronous active low input pin used to power down the device into a low power state. This input is activated by the MODE selection pin / Real time system reset signal for frequency gear ratio change or watchdog timer timeout. This signal is active low.
27	SCLK	IN	Clock pin of SMBus circuitry, 5V tolerant.
28	SDATA	I/O	Data pin for SMBus circuitry, 5V tolerant.

* Internal Pull-Up Resistor
** Internal Pull-Down Resistor
~ This output has 2X drive strength

Pin description continued on next page.

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Pin Description Continued

PIN #	PIN NAME	PIN TYPE	DESCRIPTION
29	DDRC5/SDRAM11	OUT	"Complimentary" Clock of differential memory output / 3.3V SDRAM clock output
30	DDRT5/SDRAM10	OUT	"True" Clock of differential memory output / 3.3V SDRAM clock output
31	DDRC4/SDRAM9	OUT	"Complimentary" Clock of differential memory output / 3.3V SDRAM clock output
32	DDRT4/SDRAM8	OUT	"True" Clock of differential memory output / 3.3V SDRAM clock output
33	GND	PWR	Ground pin.
34	VDD3.3_2.5	PWR	2.5V or 3.3V nominal power supply voltage.
35	DDRC3/SDRAM7	OUT	"Complimentary" Clock of differential memory output / 3.3V SDRAM clock output
36	DDRT3/SDRAM6	OUT	"True" Clock of differential memory output / 3.3V SDRAM clock output
37	DDRC2/SDRAM5	OUT	"Complimentary" Clock of differential memory output / 3.3V SDRAM clock output
38	DDRT2/SDRAM4	OUT	"True" Clock of differential memory output / 3.3V SDRAM clock output
39	GND	PWR	Ground pin.
40	VDD3.3_2.5	PWR	2.5V or 3.3V nominal power supply voltage.
41	DDRC1/SDRAM3	OUT	"Complimentary" Clock of differential memory output / 3.3V SDRAM clock output
42	DDRT1/SDRAM2	OUT	"True" Clock of differential memory output / 3.3V SDRAM clock output
43	DDRC0/SDRAM1	OUT	"Complimentary" Clock of differential memory output / 3.3V SDRAM clock output
44	DDRT0/SDRAM0	OUT	"True" Clock of differential memory output / 3.3V SDRAM clock output
45	BUF_IN	IN	Input Buffers for memory outputs.
46	FBOUT	OUT	Memory feed back output.
47	GND	PWR	Ground pin.
48	CPUT1_CS	OUT	True clock of differential pair 2.5V push-pull CPU outputs.
49	CPUT0_CS	OUT	True clock of differential pair 2.5V push-pull CPU outputs.
50	VDDCPU2.5	PWR	Power pin for the CPUCLKs. 2.5V
51	VDDCPU3.3	PWR	Power pin for the CPUCLKs. 3.3V
52	CPUCLKC/CPUCLKODC	OUT	"Complementary" clocks of differential pair CPU outputs. These are current mode outputs. External resistors are required for voltage bias / "Complementary" clocks of differential pair CPU outputs. These open drain outputs need an external 1.5V pull-up / 2.5V CPU clock output.
53	CPUCLKT/CPUCLKODT	OUT	"True" clocks of differential pair CPU outputs. These are current mode outputs. External resistors are required for voltage bias / "True" clocks of differential pair CPU outputs. These open drain outputs need an external 1.5V pull-up / 2.5V CPU clock output.
54	GND	PWR	Ground pin.
55	VDDREF	PWR	Ref, XTAL power supply, nominal 3.3V
56	Vtt_PWRGD#**/REF1	I/O	This 3.3V LVTTL input is a level sensitive strobe used to determine when latch inputs are valid and are ready to be sampled. This is an active low input. / 14.318 MHz reference clock.

Mode Pin - Power Management Input Control

MODE, Pin 6 (Latched Input)	Pin 26	Pin 18	Pin 8
0	PD# (Input)	CPU_STOP# (Input)	PCI_STOP# (Input)
1	RESET# (Output)	PCICLK5 (Output)	AGP2 (Output)

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General I²C serial interface information

How to Write:

- Controller (host) sends a start bit.
- Controller (host) sends the write address D2 (H)
- ICS clock will ***acknowledge***
- Controller (host) sends the begining byte location = N
- ICS clock will ***acknowledge***
- Controller (host) sends the data byte count = X
- ICS clock will ***acknowledge***
- Controller (host) starts sending ***Byte N through Byte N + X -1***
  (see Note 2)
- ICS clock will ***acknowledge*** each byte ***one at a time***
- Controller (host) sends a Stop bit

How to Read:

- Controller (host) will send start bit.
- Controller (host) sends the write address D2 (H)
- ICS clock will ***acknowledge***
- Controller (host) sends the begining byte location = N
- ICS clock will ***acknowledge***
- Controller (host) will send a separate start bit.
- Controller (host) sends the read address D3 (H)
- ICS clock will ***acknowledge***
- ICS clock will send the data byte count = X
- ICS clock sends ***Byte N + X -1***
- ICS clock sends ***Byte 0 through byte X (if X(H) was written to byte 8)***.
- Controller (host) will need to acknowledge each byte
- Controllor (host) will send a not acknowledge bit
- Controller (host) will send a stop bit

Index Block Write Operation

Controller (Host)		ICS (Slave/Receiver)
T	starT bit	
Slave Address D2(H)		
WR	WRite	
		ACK
Beginning Byte = N		
		ACK
Data Byte Count = X		
		ACK
Beginning Byte N	X Byte	
		ACK
O		
O		O
O		O
		O
Byte N + X - 1		
		ACK
P	stoP bit	

Index Block Read Operation

Controller (Host)		ICS (Slave/Receiver)
T	starT bit	
Slave Address D2(H)		
WR	WRite	
		ACK
Beginning Byte = N		
		ACK
RT	Repeat starT	
Slave Address D3(H)		
RD	ReaD	
		ACK
		Data Byte Count = X
ACK		
	X Byte	Beginning Byte N
ACK		
		O
O		O
O		O
O		
		Byte N + X - 1
N	Not acknowledge	
P	stoP bit	

*See notes on the following page.

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Byte 0: Functionality and frequency select register (Default=0)

Bit		Description								PWD
	Bit2	Bit7	Bit6	Bit5	Bit4	CPUCLK MHz	AGPCLK MHz	PCICLK MHz	Spread %	
		FS3	FS2	FS1	FS0					
Bit (2,7:4)	0	0	0	0	0	102.00	68.00	34.00	+/- 0.30% Center Spread	Notes 1, 2
	0	0	0	0	1	105.00	70.00	35.00	+/- 0.30% Center Spread	
	0	0	0	1	0	108.00	72.00	36.00	+/- 0.30% Center Spread	
	0	0	0	1	1	111.00	74.00	27.00	+/- 0.30% Center Spread	
	0	0	1	0	0	114.00	76.00	38.00	+/- 0.30% Center Spread	
	0	0	1	0	1	117.00	78.00	39.00	+/- 0.30% Center Spread	
	0	0	1	1	0	120.00	80.00	40.00	+/- 0.30% Center Spread	
	0	0	1	1	1	123.00	82.00	41.00	+/- 0.30% Center Spread	
	0	1	0	0	0	126.00	72.00	36.00	+/- 0.30% Center Spread	
	0	1	0	0	1	130.00	74.30	37.10	+/- 0.30% Center Spread	
	0	1	0	1	0	133.90	66.95	33.48	+/- 0.30% Center Spread	
	0	1	0	1	1	140.00	70.00	35.00	+/- 0.30% Center Spread	
	0	1	1	0	0	144.00	72.00	36.00	+/- 0.30% Center Spread	
	0	1	1	0	1	148.00	74.00	37.00	+/- 0.30% Center Spread	
	0	1	1	1	0	152.00	76.00	38.00	+/- 0.30% Center Spread	
	0	1	1	1	1	156.00	78.00	39.00	+/- 0.30% Center Spread	
	1	0	0	0	0	160.00	80.00	40.00	+/- 0.30% Center Spread	
	1	0	0	0	1	164.00	82.00	41.00	+/- 0.30% Center Spread	
	1	0	0	1	0	166.60	66.60	33.30	+/- 0.30% Center Spread	
	1	0	0	1	1	170.00	68.00	34.00	+/- 0.30% Center Spread	
	1	0	1	0	0	175.00	70.00	35.00	+/- 0.50% Center Spread	
	1	0	1	0	1	180.00	72.00	36.00	+/- 0.50% Center Spread	
	1	0	1	1	0	185.00	74.00	37.00	+/- 0.50% Center Spread	
	1	0	1	1	1	190.00	76.00	38.00	+/- 0.30% Center Spread	
	1	1	0	0	0	66.80	66.80	33.40	+/- 0.30% Center Spread	
	1	1	0	0	1	100.90	67.27	33.63	+/- 0.30% Center Spread	
	1	1	0	1	0	133.60	66.80	33.40	+/- 0.30% Center Spread	
	1	1	0	1	1	200.40	66.80	33.40	+/- 0.30% Center Spread	
	1	1	1	0	0	66.60	66.60	32.30	0 to - 0.6% Down Spread	
	1	1	1	0	1	100.00	66.60	33.30	0 to - 0.6% Down Spread	
	1	1	1	1	0	200.00	66.60	33.30	0 to - 0.6% Down Spread	
	1	1	1	1	1	133.30	66.60	33.30	0 to - 0.6% Down Spread	
Bit 3	0 - Frequency is selected by hardware select, latched inputs 1 - Frequency is selected by Bit 2,7:4									0
Bit 1	0 - Normal 1 - Spread spectrum enable									1
Bit 0	0 - Running 1 - Tristate all outputs									0

Notes:

1. Default at power-up will be for latched logic inputs to define frequency, as displayed by Bit 3.
2. B0b2 default = 0.

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Byte 1: CPU Active/Inactive Register
(1 = enable, 0 = disable)

Bit	Pin#	PWD	Description
Bit7	29	1	SDRAM11/DDRC5 (Active/Inactive)
Bit6	10	1	PCICLK_F (Active/Inactive)
Bit5	30	1	SDRAM10/DDRT5 (Active/Inactive)
Bit4	31	1	SDRAM9/DDRC4 (Active/Inactive)
Bit3	49	1	CPUT0_CS Free running control; 1 = free running; 0 = not free running
Bit2	32	1	SDRAM8/DDRT4 (Active/Inactive)
Bit1	53, 52	1	CPUCLKT/C (Active/Inactive)
Bit0	48	1	CPUCLKT1_CS (Active/Inactive)

Byte 2: PCI Active/Inactive Register
(1 = enable, 0 = disable)

Bit	Pin#	PWD	Description
Bit7	46	1	FB_OUT Free running control; 1 = free running; 0 = not free running
Bit6	18	1	PCICLK5 (Active/Inactive)
Bit5	17	1	PCICLK4 (Active/Inactive)
Bit4	15	1	PCICLK3 (Active/Inactive)
Bit3	14	1	PCICLK2 (Active/Inactive)
Bit2	12	1	PCICLK1 (Active/Inactive)
Bit1	11	1	PCICLK0 (Active/Inactive)
Bit0	53, 52	1	CPUCLKT/C Free running control; 1 = free running; 0 = not free running

Byte 3: Active/Inactive Register
(1 = enable, 0 = disable)

Bit	Pin#	PWD	Description
Bit7	46	1	FB_OUT (Active/Inactive)
Bit6	-	1	SEL 24_48, 0=24Mhz 1=48MHz
Bit5	-	1	SD/DDR free running control; 1 = free running; 0 not free running
Bit4	56	1	REF1 (Active/Inactive)
Bit3	48	1	CPUT1_CS free running control; 1 = free running; 0 not free running
Bit2	8	1	AGPCLK 2 (Active/Inactive)
Bit1	7	1	AGPCLK 1 (Active/Inactive)
Bit0	6	1	AGPCLK 0 (Active/Inactive)

Byte 4: Frequency Select Active/Inactive Register
(1 = enable, 0 = disable)

Bit	Pin#	PWD	Description
Bit 7	-	X	Latched FS3
Bit 6	-	X	Latched FS2
Bit 5	-	X	Latched FS1
Bit 4	-	X	Latched FS0
Bit 3	20	1	48MHz (Active/Inactive)
Bit 2	21	1	24_48MHz (Active/Inactive)
Bit 1	49	1	CPUT0_CS (Active/Inactive)
Bit 0	1	1	REF0 (Active/Inactive)

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Byte 5: Peripheral Active/Inactive Register
(1 = enable, 0 = disable)

Bit	Pin#	PWD	Description
Bit 7	35	1	SDRAM7/DDRC3 (Active/Inactive)
Bit 6	36	1	SDRAM6/DDRT3 (Active/Inactive)
Bit 5	37	1	SDRAM5/DDRC2 (Active/Inactive)
Bit 4	38	1	SDRAM4/DDRT2 (Active/Inactive)
Bit 3	41	1	SDRAM3/DDRC1 (Active/Inactive)
Bit 2	42	1	SDRAM2/DDRT1 (Active/Inactive)
Bit 1	43	1	SDRAM1/DDRC0 (Active/Inactive)
Bit 0	44	1	SDRAM0/DDRT0 (Active/Inactive)

Byte 6: Vendor ID Register
(1 = enable, 0 = disable)

Bit	Name	PWD	Description
Bit 7	Revision ID Bit3	X	Revision ID values will be based on individual device's revision
Bit 6	Revision ID Bit2	X	
Bit 5	Revision ID Bit1	X	
Bit 4	Revision ID Bit0	X	
Bit 3	Vendor ID Bit3	0	(Reserved)
Bit 2	Vendor ID Bit2	0	(Reserved)
Bit 1	Vendor ID Bit1	0	(Reserved)
Bit 0	Vendor ID Bit0	1	(Reserved)

Byte 7: Revision ID and Device ID Register

Bit	Name	PWD	Description
Bit 7	Device ID7	0	Device ID values will be based on individual device "01h" in this case.
Bit 6	Device ID6	0	
Bit 5	Device ID5	0	
Bit 4	Device ID4	1	
Bit 3	Device ID3	0	
Bit 2	Device ID2	1	
Bit 1	Device ID1	1	
Bit 0	Device ID0	1	

Byte 8: Byte Count Read Back Register

Bit	Name	PWD	Description
Bit 7	Byte7	0	Note: Writing to this register will configure byte count and how many bytes will be read back, default is $0F_H$ = 15 bytes.
Bit 6	Byte6	0	
Bit 5	Byte5	0	
Bit 4	Byte4	0	
Bit 3	Byte3	1	
Bit 2	Byte2	1	
Bit 1	Byte1	1	
Bit 0	Byte0	1	

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Byte 9: Watchdog Timer Count Register

Bit	Name	PWD	Description
Bit 7	WD7	0	The decimal representation of these 8 bits correspond to X • 290ms the watchdog timer will wait before it goes to alarm mode and reset the frequency to the safe setting. Default at power up is 16 • 290ms = 4.6 seconds.
Bit 6	WD6	0	
Bit 5	WD5	0	
Bit 4	WD4	1	
Bit 3	WD3	0	
Bit 2	WD2	0	
Bit 1	WD1	0	
Bit 0	WD0	0	

Byte 10: Programming Enable bit 8 Watchdog Control Register

Bit	Name	PWD	Description
Bit 7	Program Enable	0	Programming Enable bit 0 = no programming. Frequencies are selected by HW latches or Byte0 1 = enable all I²C programing.
Bit 6	WD Enable	0	Software Watchdog Enable bit. This bit will over write WDEN latched value. 0 = disable, 1 = Enable.
Bit 5	WD Alarm	0	Watchdog Alarm Status 0 = normal 1= alarm status
Bit 4	SF4	0	Watchdog safe frequency bits. Writing to these bits will configure the safe frequency corrsponding to Byte 0 Bit 2, 7:4 table
Bit 3	SF3	0	
Bit 2	SF2	0	
Bit 1	SF1	0	
Bit 0	SF0	0	

Byte 11: VCO Frequency M Divider (Reference divider) Control Register

Bit	Name	PWD	Description
Bit 7	Ndiv 8	X	N divider bit 8
Bit 6	Mdiv 6	X	The decimal respresentation of Mdiv (6:0) corresposd to the reference divider value. Default at power up is equal to the latched inputs selection.
Bit 5	Mdiv 5	X	
Bit 4	Mdiv 4	X	
Bit 3	Mdiv 3	X	
Bit 2	Mdiv 2	X	
Bit 1	Mdiv 1	X	
Bit 0	Mdiv 0	X	

Byte 12: VCO Frequency N Divider (VCO divider) Control Register

Bit	Name	PWD	Description
Bit 7	Ndiv 7	X	The decimal representation of Ndiv (8:0) correspond to the VCO divider value. Default at power up is equal to the latched inputs selecton. Notice Ndiv 8 is located in Byte 11.
Bit 6	Ndiv 6	X	
Bit 5	Ndiv 5	X	
Bit 4	Ndiv 4	X	
Bit 3	Ndiv 3	X	
Bit 2	Ndiv 2	X	
Bit 1	Ndiv 1	X	
Bit 0	Ndiv 0	X	

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Byte 13: Spread Spectrum Control Register

Bit	Name	PWD	Description
Bit 7	SS 7	X	The Spread Spectrum (12:0) bit will program the spread precentage. Spread precent needs to be calculated based on the VCO frequency, spreading profile, spreading amount and spread frequency. It is recommended to use ICS software for spread programming. Default power on is latched FS divider.
Bit 6	SS 6	X	
Bit 5	SS 5	X	
Bit 4	SS 4	X	
Bit 3	SS 3	X	
Bit 2	SS 2	X	
Bit 1	SS 1	X	
Bit 0	SS 0	X	

Byte 14: Spread Spectrum Control Register

Bit	Name	PWD	Description
Bit 7	Reserved	X	Reserved
Bit 6	Reserved	X	Reserved
Bit 5	Reserved	X	Reserved
Bit 4	SS 12	X	Spread Spectrum Bit 12
Bit 3	SS 11	X	Spread Spectrum Bit 11
Bit 2	SS 10	X	Spread Spectrum Bit 10
Bit 1	SS 9	X	Spread Spectrum Bit 9
Bit 0	SS 8	X	Spread Spectrum Bit 8

Byte 15: Output Divider Control Register

Bit	Name	PWD	Description
Bit 7	CPU Div 3	0	CPUCLKC/T clock divider ratio can be configured via these 4 bits individually. For divider selection table refer to Table 1. Default at power up is latched FS divider.
Bit 6	CPU Div 2	1	
Bit 5	CPU Div 1	0	
Bit 4	CPU Div 0	1	
Bit 3	CPU Div 3	0	CPUCLKT_CS clock divider ratio can be configured via these 4 bits individually. For divider selection table refer to Table 1. Default at power up is latched FS divider.
Bit 2	CPU Div 2	1	
Bit 1	CPU Div 1	0	
Bit 0	CPU Div 0	1	

Byte 16: Output Divider Control Register

Bit	Name	PWD	Description
Bit 7	AGP Div 3	0	AGP clock divider ratio can be configured via these 4 bits individually. For divider selection table refer to Table 1. Default at power up is latched FS divider.
Bit 6	AGP Div 2	1	
Bit 5	AGP Div 1	0	
Bit 4	AGP Div 0	1	
Bit 3	Reserved	-	Reserved
Bit 2	Reserved	-	
Bit 1	Reserved	-	
Bit 0	Reserved	-	

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Byte 17: Output Divider Control Register

Bit	Name	PWD	Description
Bit 7	AGP_INV	0	AGP Phase Inversion bit
Bit 6	Reserved	0	Reserved
Bit 5	CPU_INV	0	CPU T/C Phase Inversion bit
Bit 4	CPU_INV	0	CPUT/C_CS Phase Inversion bit
Bit 3	PCI Div 3	1	PCI clock divider ratio can be configured via these 4 bits individually. For divider selection table refer to Table 2. Default at power up is latched FS divider.
Bit 2	PCI Div 2	0	
Bit 1	PCI Div 1	0	
Bit 0	PCI Div 0	1	

Table 1

Div (3:2) / Div (1:0)	00	01	10	11
00	/2	/4	/8	/16
01	/3	/6	/12	/24
10	/5	/10	/20	/40
11	/7	/14	/28	/56

Table 2

Div (3:2) / Div (1:0)	00	01	10	11
00	/4	/8	/16	/32
01	/3	/6	/12	/24
10	/5	/10	/20	/40
11	/9	/18	/36	/72

Byte 18: Group Skew Control Register

Bit	Name	PWD	Description
Bit 7	CPUCLKT_CS Group Skew Control	1	These 2 bits delay the CPUCLKT/C_CS with respect to CPUCLKT_CS 00 = 0ps 01 = 250ps 10 = 500ps 11 =750ps
Bit 6		0	
Bit 5	CPUCLKT/C Group Skew Control	1	These 2 bits delay the CPUCLKT/C clock with respect to CPUCLKT/C_CS 00 = 0ps 01 = 250ps 10 = 500ps 11 = 750ps
Bit 4		0	
Bit 3	AGPCLK Group Skew Control	1	These 2 bits delay the AGPCLK clocks with respect to CPUCLK 00 = 0ps 01 = 250ps 10 = 500ps 11 = 750ps
Bit 2		0	
Bit 1	Reserved	X	Reserved
Bit 0	Reserved	X	Reserved

Byte 19: Group Skew Control Register

Bit	Name	PWD	Description
Bit 7	Reserved	1	Reserved
Bit 6		0	
Bit 5		0	
Bit 4		0	
Bit 3	PCICLK(5:0) Group Skew Control	1	These 4 bits can change the CPU to PCI (5:0) skew from 1.4ns - 2.9ns. Default at power up is - 2.5ns. Each binary increment or decrement of Bits (3:0) will increase or decrease the delay of the PCI clocks by 100ps.
Bit 2		0	
Bit 1		0	
Bit 0		0	

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Byte 20: Group Skew Control Register

Bit	Name	PWD	Description
Bit 7	PCICLK_F Group Skew Control	1	These 4 bits can change the CPU to PCIF skew from 1.4ns - 2.9ns. Default at power up is - 2.5ns. Each binary increment or decrement of Bit (3:0) will increase or decrease the delay of the PCI clocks by 100ps.
Bit 6		0	
Bit 5		0	
Bit 4		0	
Bit 3	Reserved	1	Reserved
Bit 2		0	
Bit 1		0	
Bit 0		0	

Byte 21: Slew Rate Control Register

Bit	Name	PWD	Description
Bit 7	Reserved	0	Reserved
Bit 6		1	
Bit 5		0	
Bit 4		1	
Bit 3	CPUCLKT/C OD/CS	0	CPUCLKT/C OD/CS clock slew rate control bits.
Bit 2		1	01 = strong: 10= normal; 00 = weak
Bit 1	AGP_0	0	AGP_0 clock slew rate control bits.
Bit 0	Slew Rate Control	1	01 = strong: 10 = normal; 00 = weak

Byte 22: Slew Rate Control Register

Bit	Name	PWD	Description
Bit 7	AGP(2:1)	0	AGP(2:1) clock slew rate control bits.
Bit 6	Slew Rate Control	1	01 = strong:10 = normal; 00 = weak
Bit 5	PCICLK_F	0	PCICLK_F clock slew rate control bits.
Bit 4	Slew Rate Control	1	01 = strong: 10= normal; 00 = weak
Bit 3	PCICLK(7:4)	0	PCICLK(7:4) clock slew rate control bits.
Bit 2	Slew Rate Control	1	01 = strong: 10= normal; 00 = weak
Bit 1	PCICLK(3:0)	0	PCICLK(3:0) clock slew rate control bits.
Bit 0	Slew Rate Control	1	01 = strong: 10 = normal; 00 = weak

Byte 23: Slew Rate Control Register

Bit	Name	PWD	Description
Bit 7	REF (1:0)	0	REF clock slew rate control bits.
Bit 6	Slew Rate Control	1	01 = strong:10 = normal; 00 = weak
Bit 5	Reserved	0	Reserved
Bit 4		1	
Bit 3	48MHz	0	48MHz clock slew rate control bits.
Bit 2	Slew Rate Control	1	01 = strong: 10= normal; 00 = weak
Bit 1	24_48MHz	0	24_48MHz clock slew rate control bits.
Bit 0	Slew Rate Control	1	01 = strong: 10 = normal; 00 = weak

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Absolute Maximum Ratings

Supply Voltage . . . . . 5.5 V
Logic Inputs . . . . . GND –0.5 V to V_{DD} +0.5 V
Ambient Operating Temperature . . . . . 0°C to +70°C
Case Temperature . . . . . 115°C
Storage Temperature . . . . . –65°C to +150°C

Stresses above those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only and functional operation of the device at these or any other conditions above those listed in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Electrical Characteristics - Input/Supply/Common Output Parameters

T_A = 0 - 70°C; Supply Voltage V_{DD} = 3.3 V ±5%

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input High Voltage	V_{IH}		2		V_{DD} + 0.3	V
Input Low Voltage	V_{IL}		V_{SS} - 0.3		0.8	V
Input High Current	I_{IH}	V_{IN} = V_{DD}	-5		5	mA
Input Low Current	I_{IL1}	V_{IN} = 0 V; Inputs with no pull-up resistors	-5			mA
Input Low Current	I_{IL2}	V_{IN} = 0 V; Inputs with pull-up resistors	-200			mA
Operating Supply Current	$I_{DD3.3OP}$	C_L = 0 pF; Select @ 66M			100	mA
		C_L = Full load			280	mA
Power Down Supply Current	$I_{DD3.3PD}$	IREF=2.32			20	mA
		IREF= 5mA			37	mA
Input frequency	F_i	V_{DD} = 3.3 V;				MHz
Pin Inductance	L_{pin}				7	nH
Input Capacitance[1]	C_{IN}	Logic Inputs			5	pF
	C_{out}	Out put pin capacitance			6	pF
	C_{INX}	X1 & X2 pins	27		45	pF
Transition Time[1]	T_{trans}	To 1st crossing of target Freq.			3	mS
Settling Time[1]	T_s	From 1st crossing to 1% target Freq.			3	mS
Clk Stabilization[1]	T_{STAB}	From V_{DD} = 3.3 V to 1% target Freq.			3	mS
Delay	t_{PZH},t_{PZH}	output enable delay (all outputs)	1		10	nS
	t_{PLZ},t_{PZH}	output disable delay (all outputs)	1		10	nS

[1]Guaranteed by design, not 100% tested in production.

TARGET SPECIFICATION SUBJECT TO CHANGE PRODUCT CHARACTERIZATION

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Electrical Characteristics - CPUCLKC/T

T_A = 0 - 70º C; V_{DD} = 3.3 V +/-5%; (unless otherwise stated)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Current Source Output Impedance	Z_O	$V_O = V_X$	3000			W
Output High Voltage	V_{OH}	V_R = 475Ω ±1%; IREF = 2.32mA; I_{OH} = 6*IREF		0.71	1.2	V
Output High Current	I_{OH}			-13.92		mA
Rise Time[1]	t_r	V_{OL} = 20%, V_{OH} = 80%	175		700	ps
Differential Crossover Voltage[1]	V_X	Note 3	45	50	55	%
Duty Cycle[1]	d_t	V_T = 50%	45	51	55	%
Skew[1], CPU to CPU	t_{sk}	V_T = 50%			150	ps
Jitter, Cycle-to-cycle[1]	$t_{jcyc-cyc}$	$V_T = V_X$			200	ps

Notes:

1 - Guaranteed by design, not 100% tested in production.

TARGET SPECIFICATION SUBJECT TO CHANGE WITH FULL PRODUCT CHARACTERIZATION

Electrical Characteristics - CPUCLKT/C_CS

T_A = 0 - 70ÜC; V_{DD} = 2.5 V +/-5%; C_L = 20 pF (unless otherwise stated)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output High Voltage	V_{OH2B}	I_{OH} = -12.0 mA	2			V
Output Low Voltage	V_{OL2B}	I_{OL} = 12 mA			0.4	V
Output High Current	I_{OH2B}	V_{OH} = 1.7 V			-19	mA
Output Low Current	I_{OL2B}	V_{OL} = 0.7 V	19			mA
Rise Time	t_{r2B}[1]	V_{OL} = 0.4 V, V_{OH} = 2.0 V			1.6	ns
Differential Crossover Voltage[1]	V_X	Note 3	45	50	55	%
Duty Cycle	d_{t2B}[1]	V_T = 1.25 V	45		55	%
Skew	t_{sk2B}[1]	V_T = 1.25 V			175	ps
Jitter, Cycle-to-cycle	$t_{jcyc-cyc2B}$[1]	V_T = 1.25 V			250	ps
Jitter, One Sigma	t_{j1s2B}[1]	V_T = 1.25 V			150	ps
Jitter, Absolute	t_{jabs2B}[1]	V_T = 1.25 V	-250		+250	ps

[1]Guaranteed by design, not 100% tested in production.

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Electrical Characteristics - SDRAM

T_A = 0 - 70°C; V_{DD} = 3.3V +/-5%, V_{DDL} = 2.5V +/-5%; C_L = 30 pF (unless otherwise stated)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output High Voltage	V_{OH3}	I_{OH} = -28 mA	2.4			V
Output Low Voltage	V_{OL3}	I_{OL} = 20 mA			0.4	V
Output High Current	I_{OH3}	V_{OH} = 2.0 V			-40	mA
Output Low Current	I_{OL3}	V_{OL} = 0.8 V	41			mA
Rise Time[1]	t_{r3}	V_{OL} = 0.4 V, V_{OH} = 2.4 V			2	ns
Fall Time[1]	t_{f3}	V_{OH} = 2.4 V, V_{OL} = 0.4 V			2	ns
Duty Cycle[1]	d_{t3}	V_T = 1.5 V	45		55	%
Skew window[1]	t_{sk3}	V_T = 1.5 V			250	ps
Propagation Time[1] (Buffer In to Output)	Tprop	V_T = 1.5 V			5	ns

[1]Guaranteed by design, not 100% tested in production.

TARGET SPECIFICATION SUBJECT TO CHANGE WITH FULL PRODUCT CHARACTERIZATION

Electrical Characteristics - DDRT/C

T_A = 0 - 70°C; V_{DDL} = 2.5 V +/-5%, C_L = 20 pF (unless otherwise stated)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output High Voltage	V_{OH3}	I_{OH} = -11 mA	2			V
Output Low Voltage	V_{OL3}	I_{OL} = 11 mA			0.4	V
Output High Current	I_{OH3}	V_{OH} = 2.0 V			-12	mA
Output Low Current	I_{OL3}	V_{OL} = 0.8 V	12			mA
Rise Time[1]	T_{r3}[1]	20% to 80%			2.2	ns
Fall Time[1]	T_{f3}[1]	80% to 20%			2.2	ns
Duty Cycle[1]	D_{t3}[1]	V_T = 50%	47		53	%
Skew[1](window)	T_{sk}[1]	VT = 50%			250	ps
Jitter	$t_{jcyc-cyc}$[1]	V_T = 1.25 V			250	ps

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Electrical Characteristics - PCICLK

T_A = 0 - 70°C; V_{DD} = 3.3 V +/-5%; C_L = 10-30 pF (unless otherwise stated)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output Frequency	F0[1]			33.33		MHz
Output Impedance	R_{DSN1}[1]	$V_O = V_{DD}*(0.5)$	12		55	Ω
Output High Voltage	V_{OH1}	I_{OH} = -1 mA	2.4			V
Output Low Voltage	V_{OL1}	I_{OL} = 1 mA			0.55	V
Output High Current	I_{OH1}	VOH@ MIN = 1.0 V, VOH@ MAX = 3.135 V	-33		-33	mA
Output Low Current	I_{OL1}	VOL@ MIN = 1.95 V, VOL@ MAX= 0.4	30		38	mA
Rise Time	t_{r1}[1]	V_{OL} = 0.4 V, V_{OH} = 2.4 V	0.5		2	ns
Fall Time	t_{f1}[1]	V_{OH} = 2.4 V, V_{OL} = 0.4 V	0.5		2	ns
Duty Cycle	d_{t1}[1]	V_T = 1.5 V	45		55	%
Skew	t_{sk1}[1]	V_T = 1.5 V			500	ps
Jitter	$t_{jcyc-cyc}$[1]	V_T = 1.5 V			250	ps

[1]Guaranteed by design, not 100% tested in production.

TARGET SPECIFICATION SUBJECT TO CHANGE WITH FULL PRODUCT CHARACTERIZATION

Electrical Characteristics - AGP

T_A = 0 - 70°C; V_{DD} = 3.3 V +/-5%; C_L =10-30 pF (unless otherwise stated)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output Frequency	F_{O1}			66.66		MHz
Output Impedance	R_{DSP1}[1]	$V_O = V_{DD}*(0.5)$	12		55	Ω
Output High Voltage	V_{OH1}	I_{OH} = -1 mA	2.4			V
Output Low Voltage	V_{OL1}	I_{OL} = 1 mA			0.4	V
Output High Current	I_{OH1}	VOH@ MIN = 1.0 V, VOH@ MAX = 3.135 V	-33		-33	mA
Output Low Current	I_{OL1}	VOL@ MIN = 1.95 V, VOL@ MAX= 0.4	30		38	mA
Rise Time	t_{r1}[1]	V_{OL} = 0.4 V, V_{OH} = 2.4 V	0.5		2	ns
Fall Time	t_{f1}[1]	V_{OH} = 2.4 V, V_{OL} = 0.4 V	0.5		2	ns
Duty Cycle	d_{t1}[1]	V_T = 1.5 V	45		55	%
Skew	t_{sk1}[1]	V_T = 1.5 V			500	ps
Jitter	tjcyc-cyc[1]	V_T = 1.5 V			250	ps

[1]Guaranteed by design, not 100% tested in production.

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Electrical Characteristics - 48MHz

T_A = 0 - 70°C; V_{DD} = 3.3 V +/-5%; C_L = 10-30 pF (unless otherwise stated)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output Frequency	F_O[1]	$V_O = V_{DD}*(0.5)$		48		MHz
Output Impedance	R_{DSN1}[1]	$V_O = V_{DD}*(0.5)$	12		55	Ω
Output High Voltage	V_{OH1}	I_{OH} = -1 mA	2.4			V
Output Low Voltage	V_{OL1}	I_{OL} = 1 mA			0.55	V
Output High Current	I_{OH1}	VOH@ MIN = 1.0 V, VOH@ MAX = 3.135 V	-29		-23	mA
Output Low Current	I_{OL1}	VOL@ MIN = 1.95 V, VOL@ MAX= 0.4	29		27	mA
48DOT Rise Time	t_{r1}[1]	V_{OL} = 0.4 V, V_{OH} = 2.4 V	0.5		1	ns
48DOT Fall Time	t_{f1}[1]	V_{OH} = 2.4 V, V_{OL} = 0.4 V	0.5		1	ns
VCH 48 USB Rise Time	t_r[1]	V_{OL} = 0.4 V, V_{OH} = 2.4 V	1		2	ns
VCH 48 USB Fall Time	tf[1]	V_{OH} = 2.4 V, V_{OL} = 0.4 V	1		2	ns
48 DOT to 48 USB Skew	tskew[1]	VT=1.5V			1	ns
Duty Cycle	d_{t1}[1]	V_T = 1.5 V	45		55	%
Jitter	$t_{jcyc-cyc}$[1]	V_T = 1.5 V			350	ps

[1]Guaranteed by design, not 100% tested in production.

Electrical Characteristics - REF

T_A = 0 - 70°C; V_{DD} = 3.3 V +/-5%; C_L =10-20 pF (unless otherwise stated)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output Frequency	F_{O1}					MHz
Output Impedance	R_{DSP1}[1]	$V_O = V_{DD}*(0.5)$	20		60	Ω
Output High Voltage	V_{OH1}	I_{OH} = -1 mA	2.4			V
Output Low Voltage	V_{OL1}	I_{OL} = 1 mA			0.4	V
Output High Current	I_{OH1}	VOH@ MIN = 1.0 V, VOH@ MAX = 3.135 V	-29		-23	mA
Output Low Current	I_{OL1}	VOL@ MIN = 1.95 V, VOL@ MAX= 0.4	29		27	mA
Rise Time	t_{r1}[1]	V_{OL} = 0.4 V, V_{OH} = 2.4 V	1		4	ns
Fall Time	t_{f1}[1]	V_{OH} = 2.4 V, V_{OL} = 0.4 V	1		4	ns
Duty Cycle	d_{t1}[1]	V_T = 1.5 V	45		55	%
Jitter	$t_{jcyc-cyc}$	V_T = 1.5 V			500	ps

[1]Guaranteed by design, not 100% tested in production.

TARGET SPECIFICATION SUBJECT TO CHANGE WITH FULL PRODUCT CHARACTERIZATION

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Shared Pin Operation - Input/Output Pins

The I/O pins designated by (input/output) serve as dual signal functions to the device. During initial power-up, they act as input pins. The logic level (voltage) that is present on these pins at this time is read and stored into a 5-bit internal data latch. At the end of Power-On reset, (see AC characteristics for timing values), the device changes the mode of operations for these pins to an output function. In this mode the pins produce the specified buffered clocks to external loads.

To program (load) the internal configuration register for these pins, a resistor is connected to either the VDD (logic 1) power supply or the GND (logic 0) voltage potential. A 10 Kilohm (10K) resistor is used to provide both the solid CMOS programming voltage needed during the power-up programming period and to provide an insignificant load on the output clock during the subsequent operating period.

Figure 1 shows a means of implementing this function when a switch or 2 pin header is used. With no jumper is installed the pin will be pulled high. With the jumper in place the pin will be pulled low. If programmability is not necessary, than only a single resistor is necessary. The programming resistors should be located close to the series termination resistor to minimize the current loop area. It is more important to locate the series termination resistor close to the driver than the programming resistor.

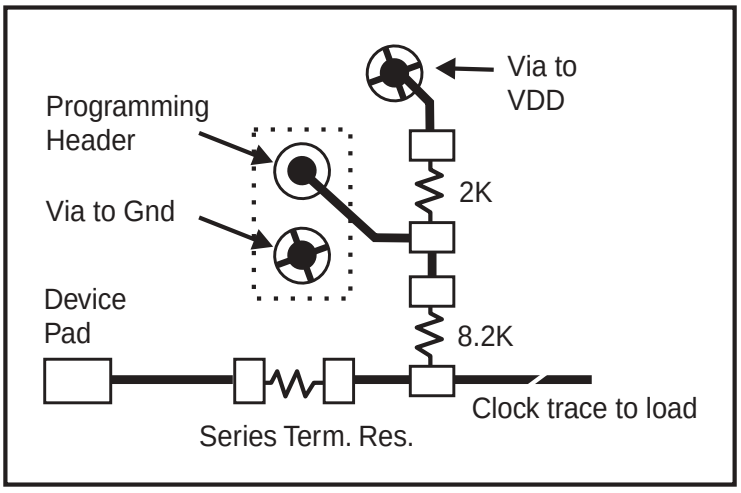
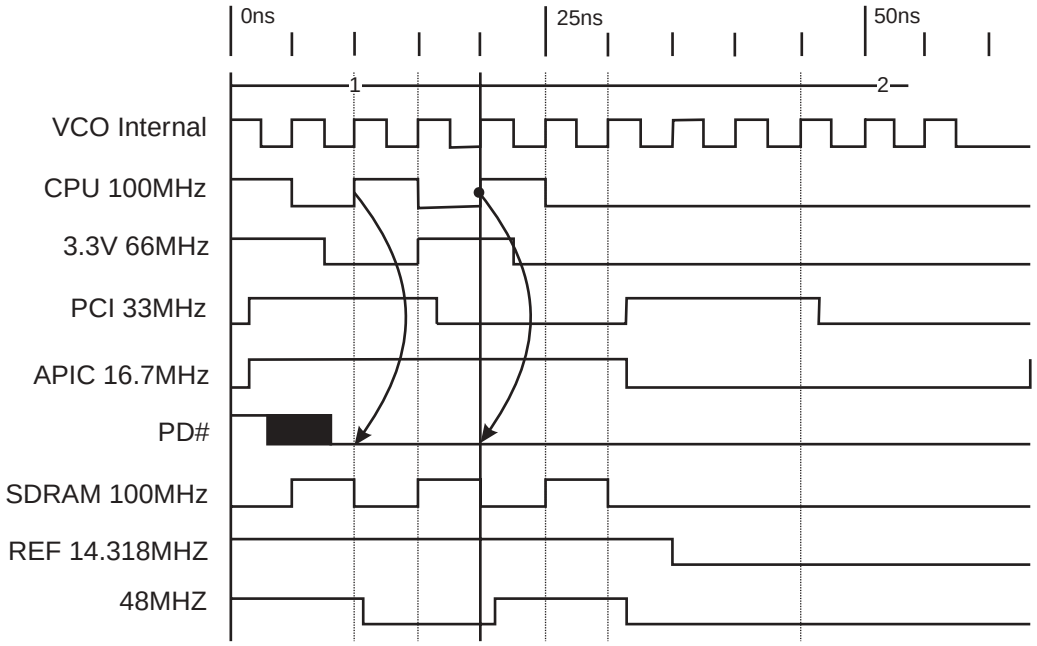


Fig. 1

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Power Down Waveform



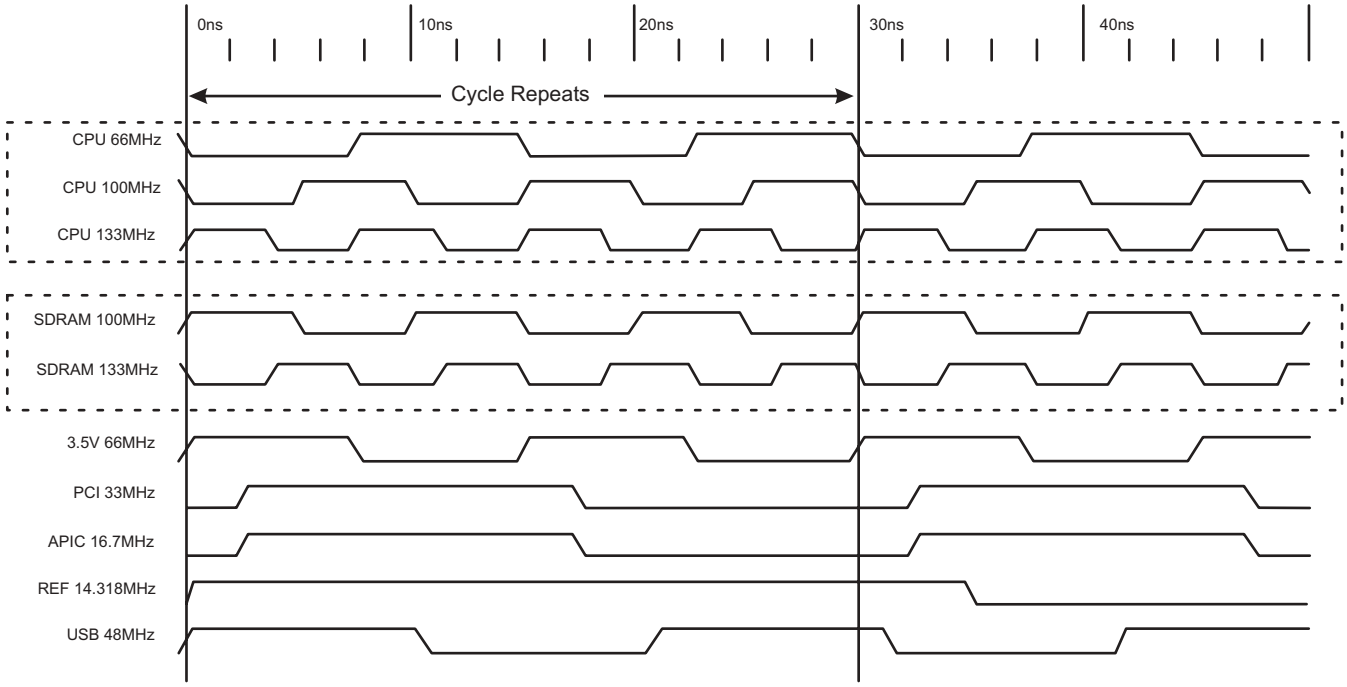
Note

1. After PD# is sampled active (Low) for 2 consective rising edges of CPUCLKs, all the output clocks are driven Low on their next High to Low tranistiion.

2. Power-up latency <3ms.

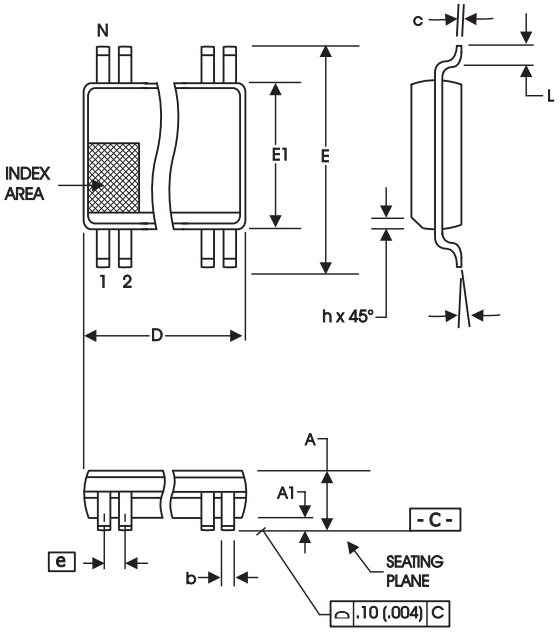
3. Waveform shown for 100MHz

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Group Offset Waveforms

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SYMBOL	In Millimeters COMMON DIMENSIONS		In Inches COMMON DIMENSIONS	
	MIN	MAX	MIN	MAX
A	2.41	2.80	.095	.110
A1	0.20	0.40	.008	.016
b	0.20	0.34	.008	.0135
c	0.13	0.25	.005	.010
D	SEE VARIATIONS		SEE VARIATIONS	
E	10.03	10.68	.395	.420
E1	7.40	7.60	.291	.299
e	0.635 BASIC		0.025 BASIC	
h	0.38	0.64	.015	.025
L	0.50	1.02	.020	.040
N	SEE VARIATIONS		SEE VARIATIONS	
α	0°	8°	0°	8°

VARIATIONS

N	D mm.		D (inch)	
	MIN	MAX	MIN	MAX
56	18.31	18.55	.720	.730

Reference Doc.: JEDEC Publication 95, MO-118

10-0034

Ordering Information

ICS950908yFLF-T

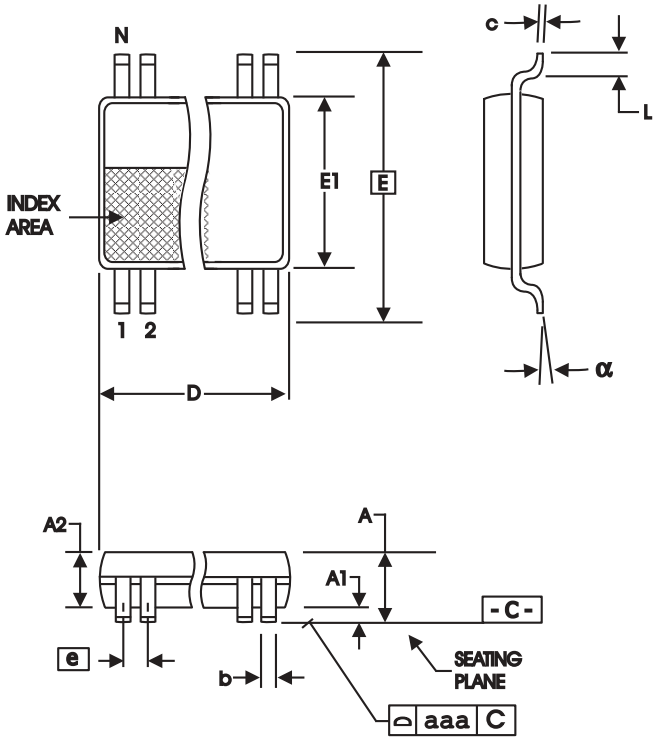
Example:

ICS XXXX y F LF- T

- **Designation for tape and reel packaging**
- **Lead Free (Optional)**
- **Package Type**
  F = SSOP
- **Revision Designator** (will not correlate with datasheet revision)
- **Device Type**
- **Prefix**
  ICS = Standard Device

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56-Lead 6.10 mm. Body, 0.50 mm. Pitch TSSOP
(240 mil) (20 mil)

SYMBOL	In Millimeters COMMON DIMENSIONS		In Inches COMMON DIMENSIONS	
	MIN	MAX	MIN	MAX
A	--	1.20	--	.047
A1	0.05	0.15	.002	.006
A2	0.80	1.05	.032	.041
b	0.17	0.27	.007	.011
c	0.09	0.20	.0035	.008
D	SEE VARIATIONS		SEE VARIATIONS	
E	8.10 BASIC		0.319 BASIC	
E1	6.00	6.20	.236	.244
e	0.50 BASIC		0.020 BASIC	
L	0.45	0.75	.018	.030
N	SEE VARIATIONS		SEE VARIATIONS	
a	0°	8°	0°	8°
aaa	--	0.10	--	.004

VARIATIONS

N	D mm.		D (inch)	
	MIN	MAX	MIN	MAX
56	13.90	14.10	.547	.555

Reference Doc.: JEDEC Publication 95, MO-153

10-0039

Ordering Information

ICS950908yGLF-T

Example:

ICS XXXX y G LF- T

- **Designation for tape and reel packaging**
- **Lead Free (Optional)**
- **Package Type**
  G = TSSOP
- **Revision Designator** (will not correlate with datasheet revision)
- **Device Type**
- **Prefix**
  ICS = Standard Device

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