# Programmable Timing Control Hub™ for Next Gen P4™ Processor

ICS952601

**Recommended Application:**

CK409 clock, Intel Yellow Cover part

**Output Features:**

- 3 - 0.7V current-mode differential CPU pairs
- 1 - 0.7V current-mode differential SRC pair
- 7 - PCI (33MHz)
- 3 - PCICLK_F, (33MHz) free-running
- 1 - USB, 48MHz
- 1 - DOT, 48MHz
- 2 - REF, 14.318MHz
- 4 - 3V66, 66.66MHz
- 1 - VCH/3V66, selectable 48MHz or 66MHz

**Key Specifications:**

- CPU/SRC outputs cycle-cycle jitter < 125ps
- 3V66 outputs cycle-cycle jitter < 250ps
- PCI outputs cycle-cycle jitter < 250ps
- CPU outputs skew: < 100ps
- +/- 300ppm frequency accuracy on CPU & SRC clocks

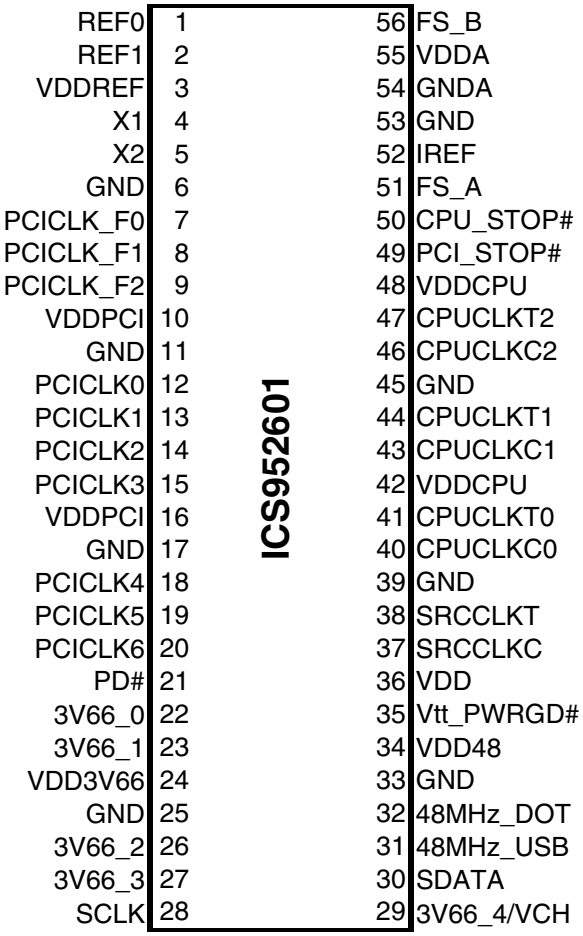
**Features/Benefits:**

- Supports tight ppm accuracy clocks for Serial-ATA.
- Supports spread spectrum modulation, 0 to -0.5% down spread.
- Supports CPU clks up to 400MHz in test mode.
- Uses external 14.318MHz crystal, external crystal load caps are required for frequency tuning.
- Supports undriven differential CPU, SRC pair in PD# and CPU_STOP# for power management.

**Functionality**

| B6b5 | FS_A | FS_B | CPU MHz | SRC MHz | 3V66 MHz | PCI MHz | REF MHz | USB/DOT MHz |
|---|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 100 | 100/200 | 66.66 | 33.33 | 14.318 | 48.00 |
| | 0 | MID | $Ref/N_0$ | $Ref/N_1$ | $Ref/N_2$ | $Ref/N_3$ | $Ref/N_4$ | $Ref/N_5$ |
| | 0 | 1 | 200 | 100/200 | 66.66 | 33.33 | 14.318 | 48.00 |
| | 1 | 0 | 133 | 100/200 | 66.66 | 33.33 | 14.318 | 48.00 |
| | 1 | 1 | 166 | 100/200 | 66.66 | 33.33 | 14.318 | 48.00 |
| | 1 | MID | Hi-Z | Hi-Z | Hi-Z | Hi-Z | Hi-Z | Hi-Z |
| 1 | 0 | 0 | 200 | 100/200 | 66.66 | 33.33 | 14.318 | 48.00 |
| | 0 | 1 | 400 | 100/200 | 66.66 | 33.33 | 14.318 | 48.00 |
| | 1 | 0 | 266 | 100/200 | 66.66 | 33.33 | 14.318 | 48.00 |
| | 1 | 1 | 333 | 100/200 | 66.66 | 33.33 | 14.318 | 48.00 |

**Pin Configuration**




**56-pin SSOP & TSSOP**



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## Pin Description

| PIN # | PIN NAME | PIN TYPE | DESCRIPTION |
|---|---|---|---|
| 1 | REF0 | OUT | 14.318 MHz reference clock. |
| 2 | REF1 | OUT | 14.318 MHz reference clock. |
| 3 | VDDREF | PWR | Ref, XTAL power supply, nominal 3.3V |
| 4 | X1 | IN | Crystal input, Nominally 14.318MHz. |
| 5 | X2 | OUT | Crystal output, Nominally 14.318MHz |
| 6 | GND | PWR | Ground pin. |
| 7 | PCICLK_F0 | OUT | Free running PCI clock not affected by PCI_STOP# . |
| 8 | PCICLK_F1 | OUT | Free running PCI clock not affected by PCI_STOP# . |
| 9 | PCICLK_F2 | OUT | Free running PCI clock not affected by PCI_STOP# . |
| 10 | VDDPCI | PWR | Power supply for PCI clocks, nominal 3.3V |
| 11 | GND | PWR | Ground pin. |
| 12 | PCICLK0 | OUT | PCI clock output. |
| 13 | PCICLK1 | OUT | PCI clock output. |
| 14 | PCICLK2 | OUT | PCI clock output. |
| 15 | PCICLK3 | OUT | PCI clock output. |
| 16 | VDDPCI | PWR | Power supply for PCI clocks, nominal 3.3V |
| 17 | GND | PWR | Ground pin. |
| 18 | PCICLK4 | OUT | PCI clock output. |
| 19 | PCICLK5 | OUT | PCI clock output. |
| 20 | PCICLK6 | OUT | PCI clock output. |
| 21 | PD# | IN | Asynchronous active low input pin used to power down the device into a low power state. The internal clocks are disabled and the VCO and the crystal are stopped. The latency of the power down will not be greater than 1.8ms. Internal pull-up of 150K nomina |
| 22 | 3V66_0 | OUT | 3.3V 66.66MHz clock output |
| 23 | 3V66_1 | OUT | 3.3V 66.66MHz clock output |
| 24 | VDD3V66 | PWR | Power pin for the 3V66 clocks. |
| 25 | GND | PWR | Ground pin. |
| 26 | 3V66_2 | OUT | 3.3V 66.66MHz clock output |
| 27 | 3V66_3 | OUT | 3.3V 66.66MHz clock output |
| 28 | SCLK | IN | Clock pin of SMBus circuitry, 5V tolerant. |


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## Pin Description (continued)

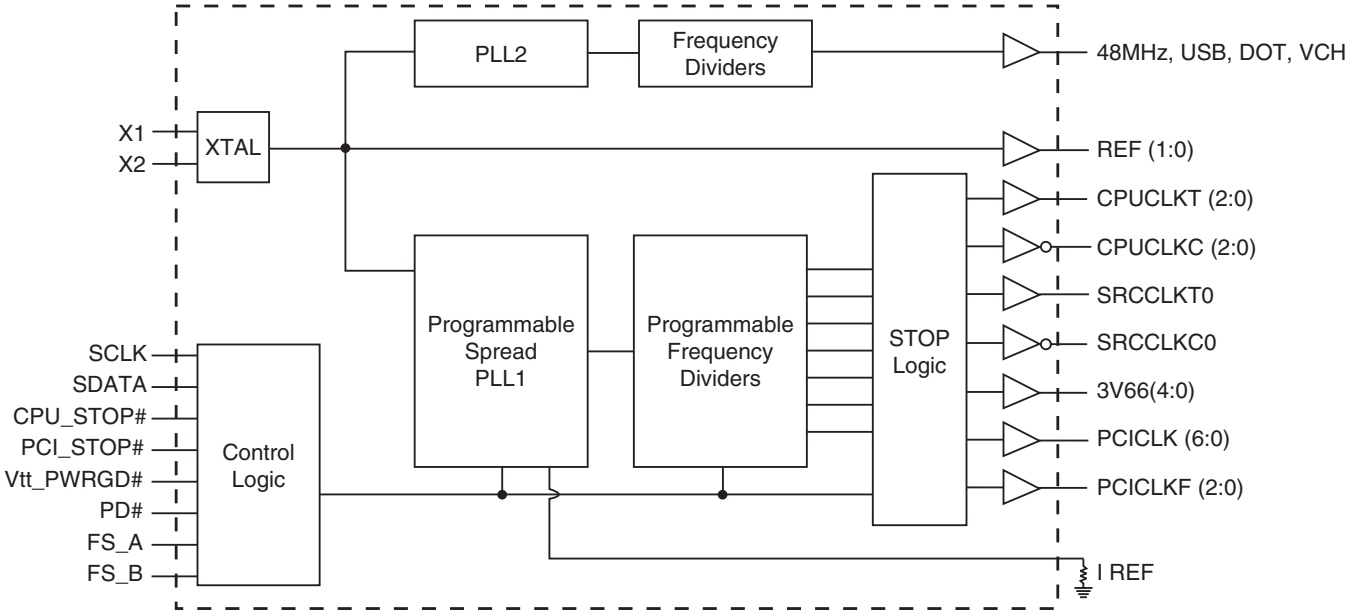
| PIN # | PIN NAME | PIN TYPE | DESCRIPTION |
|---|---|---|---|
| 29 | 3V66_4/VCH | OUT | 66.66MHz clock output for AGP support. AGP-PCI should be aligned with a skew window tolerance of 500ps. VCH is 48MHz clock output for video controller hub. |
| 30 | SDATA | I/O | Data pin for SMBus circuitry, 5V tolerant. |
| 31 | 48MHz_USB | OUT | 48MHz clock output. |
| 32 | 48MHz_DOT | OUT | 48MHz clock output. |
| 33 | GND | PWR | Ground pin. |
| 34 | VDD48 | PWR | Power pin for the 48MHz output.3.3V |
| 35 | Vtt_PWRGD# | IN | This 3.3V LVTTL input is a level sensitive strobe used to determine when latch inputs are valid and are ready to be sampled. This is an active low input. |
| 36 | VDD | PWR | Power supply for SRC clocks, nominal 3.3V |
| 37 | SRCCLKC | OUT | Complement clock of differential pair for S-ATA support. +/- 300ppm accuracy required. |
| 38 | SRCCLKT | OUT | True clock of differential pair for S-ATA support. +/- 300ppm accuracy required. |
| 39 | GND | PWR | Ground pin. |
| **40** | CPUCLKC0 | OUT | Complimentary clock of differential pair CPU outputs. These are current mode outputs. External resistors are required for voltage bias. |
| 41 | CPUCLKT0 | OUT | True clock of differential pair CPU outputs. These are current mode outputs. External resistors are required for voltage bias. |
| 42 | VDDCPU | PWR | Supply for CPU clocks, 3.3V nominal |
| 43 | CPUCLKC1 | OUT | Complimentary clock of differential pair CPU outputs. These are current mode outputs. External resistors are required for voltage bias. |
| 44 | CPUCLKT1 | OUT | True clock of differential pair CPU outputs. These are current mode outputs. External resistors are required for voltage bias. |
| 45 | GND | PWR | Ground pin. |
| 46 | CPUCLKC2 | OUT | Complimentary clock of differential pair CPU outputs. These are current mode outputs. External resistors are required for voltage bias. |
| 47 | CPUCLKT2 | OUT | True clock of differential pair CPU outputs. These are current mode outputs. External resistors are required for voltage bias. |
| 48 | VDDCPU | PWR | Supply for CPU clocks, 3.3V nominal |
| 49 | PCI_STOP# | IN | Stops all PCICLKs and SRC pair besides the PCICLK_F clocks at logic 0 level, when input low. PCI and SRC clocks can be set to Free_Running through I2C. Internal pull-up of 150K nominal. |
| 50 | CPU_STOP# | IN | Stops all CPUCLK besides the free running clocks. Internal pull-up of 150K nominal |
| 51 | FS_A | IN | Frequency select pin, see Frequency table for functionality |
| 52 | IREF | OUT | This pin establishes the reference current for the differential current-mode output pairs. This pin requires a fixed precision resistor tied to ground in order to establish the appropriate current. 475 ohms is the standard value. |
| 53 | GND | PWR | Ground pin. |
| 54 | GNDA | PWR | Ground pin for core. |
| 55 | VDDA | PWR | 3.3V power for the PLL core. |
| 56 | FS_B | IN | Frequency select pin, see Frequency table for functionality |


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## General Description

**ICS952601** follows Intel CK409 Yellow Cover specification. This clock synthesizer provides a single chip solution for next generation P4 Intel processors and Intel chipsets. ICS952601 is driven with a 14.318MHz crystal. It generates CPU outputs up to 200MHz. It also provides a tight ppm accuracy output for Serial ATA support.

## Block Diagram




## Power Groups

| Pin Number | | Description |
|---|---|---|
| VDD | GND | |
| 3 | 6 | Xtal, Ref |
| 24 | 25 | 3V66 [0:3] |
| 10,16 | 11,17 | PCICLK outputs |
| 36 | 39 | SRCCLK outputs |
| 55 | 54 | Master clock, CPU Analog |
| 34 | 33 | 48MHz, PLL, SCLK, SDATA |
| N/A | 53 | IREF |
| 48, 42 | 45 | CPUCLK clocks |


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## Absolute Maximum Ratings

| Symbol | Parameter | Min | Max | Units | Notes |
|---|---|---|---|---|---|
| VDD_A | 3.3V Core Supply Voltage | | VDD + 0.5V | V | |
| VDD_In | 3.3V Logic Input Supply Voltage | GND - 0.5 | VDD + 0.5V | V | |
| Ts | Storage Temperature | -65 | 150 | °C | |
| Tambient | Ambient Operating Temp | 0 | 70 | °C | |
| Tcase1 | Case Temperature 1 | | 115 | °C | 1 |
| Tcase2 | Case Temperature 2 | | 94 | °C | 2 |
| ESD prot | Input ESD protection human body model | 2000 | | V | |

1. This case temperature limits the junction temperature to <150 °C for package reliabilty
2. This case temperature limits the junction temperature to <125 °C for long term silicon reliability

### Electrical Characteristics - Input/Supply/Common Output Parameters

$T_A$ = 0 - 70°C; Supply Voltage $V_{DD}$ = 3.3 V +/-5%

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS | NOTES |
|---|---|---|---|---|---|---|---|
| Input High Voltage | $V_{IH}$ | 3.3 V +/-5% | 2 | | $V_{DD}$ + 0.3 | V | |
| Input MID Voltage | $V_{MID}$ | 3.3 V +/-5% | 1 | | 1.8 | V | |
| Input Low Voltage | $V_{IL}$ | 3.3 V +/-5% | $V_{SS}$ - 0.3 | | 0.8 | V | |
| Input High Current | $I_{IH}$ | $V_{IN}$ = $V_{DD}$ | -5 | | 5 | uA | |
| Input Low Current | $I_{IL1}$ | $V_{IN}$ = 0 V; Inputs with no pull-up resistors | -5 | | | uA | |
| | $I_{IL2}$ | $V_{IN}$ = 0 V; Inputs with pull-up resistors | -200 | | | uA | |
| Operating Supply Current | $I_{DD3.3OP}$ | Full Active, $C_L$ = Full load; | | 258 | 350 | mA | |
| Powerdown Current | $I_{DD3.3PD}$ | all diff pairs driven | | 29 | 35 | mA | |
| | | all differential pairs tri-stated | | 0.3 | 12 | mA | |
| Input Frequency[3] | $F_i$ | $V_{DD}$ = 3.3 V | | 14.31818 | | MHz | 3 |
| Pin Inductance[1] | $L_{pin}$ | | | | 7 | nH | 1 |
| Input Capacitance[1] | $C_{IN}$ | Logic Inputs | | | 5 | pF | 1 |
| | $C_{OUT}$ | Output pin capacitance | | | 6 | pF | 1 |
| | $C_{INX}$ | X1 & X2 pins | | | 5 | pF | 1 |
| Clk Stabilization[1,2] | $T_{STAB}$ | From $V_{DD}$ Power-Up or de-assertion of PD# to 1st clock | | | 1.8 | ms | 1,2 |
| Modulation Frequency | | Triangular Modulation | 30 | | 33 | kHz | 1 |
| Tdrive_SRC | | SRC output enable after PCI_Stop# de-assertion | | | 15 | ns | 1 |
| Tdrive_PD# | | CPU output enable after PD# de-assertion | | | 300 | us | 1 |
| Tfall_Pd# | | PD# fall time of | | | 5 | ns | 1 |
| Trise_Pd# | | PD# rise time of | | | 5 | ns | 2 |
| Tdrive_CPU_Stop# | | CPU output enable after CPU_Stop# de-assertion | | | 10 | us | 1 |
| Tfall_CPU_Stop# | | PD# fall time of | | | 5 | ns | 1 |
| Trise_CPU_Stop# | | PD# rise time of | | | 5 | ns | 2 |
| SMBus Voltage | $V_{DD}$ | | 2.7 | | 5.5 | V | 1 |
| Low-level Output Voltage | $V_{OL}$ | @ $I_{PULLUP}$ | | | 0.4 | V | 1 |
| Current sinking at $V_{OL}$ = 0.4 V | $I_{PULLUP}$ | | 4 | | | mA | 1 |
| SCLK/SDATA Clock/Data Rise Time[3] | $T_{RI2C}$ | (Max VIL - 0.15) to (Min VIH + 0.15) | | | 1000 | ns | 1 |
| SCLK/SDATA Clock/Data Fall Time[3] | $T_{FI2C}$ | (Min VIH + 0.15) to (Max VIL - 0.15) | | | 300 | ns | 1 |

[1]Guaranteed by design, not 100% tested in production.

[2]See timing diagrams for timing requirements.

[3] Input frequency should be measured at the REF output pin and tuned to ideal 14.31818MHz to meet ppm frequency accuracy on PLL outputs.



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## Electrical Characteristics - CPU & SRC 0.7V Current Mode Differential Pair

$T_A$ = 0 - 70°C; $V_{DD}$ = 3.3 V +/-5%; $C_L$ =2pF

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS | NOTES |
|---|---|---|---|---|---|---|---|
| Current Source Output Impedance | Zo[1] | $V_O = V_x$ | 3000 | | | Ω | 1 |
| Voltage High | VHigh | Statistical measurement on single ended signal using oscilloscope math function. | 660 | 770 | 850 | mV | 1 |
| Voltage Low | VLow | | -150 | 5 | 150 | | 1 |
| Max Voltage | Vovs | Measurement on single ended signal using absolute value. | | 756 | 1150 | mV | 1 |
| Min Voltage | Vuds | | -300 | -7 | | | 1 |
| Crossing Voltage (abs) | Vcross(abs) | | 250 | 350 | 550 | mV | 1 |
| Crossing Voltage (var) | d-Vcross | Variation of crossing over all edges | | 12 | 140 | mV | 1 |
| Long Accuracy | ppm | see Tperiod min-max values | -300 | | 300 | ppm | 1,2 |
| Average period | Tperiod | 200MHz nominal | 4.9985 | 5.0000 | 5.0015 | ns | 2 |
| | | 200MHz spread | 4.9985 | | 5.0266 | ns | 2 |
| | | 166.66MHz nominal | 5.9982 | 6.0000 | 6.0018 | ns | 2 |
| | | 166.66MHz spread | 5.9982 | | 6.0320 | ns | 2 |
| | | 133.33MHz nominal | 7.4978 | 7.5000 | 7.5023 | ns | 2 |
| | | 133.33MHz spread | 7.4978 | | 5.4000 | ns | 2 |
| | | 100.00MHz nominal | 9.9970 | 10.0000 | 10.0030 | ns | 2 |
| | | 100.00MHz spread | 9.9970 | | 10.0533 | ns | 2 |
| Absolute min period | $T_{absmin}$ | 200MHz nominal | 4.8735 | | | ns | 1,2 |
| | | 166.66MHz nominal/spread | 5.8732 | | | ns | 1,2 |
| | | 133.33MHz nominal/spread | 7.3728 | | | ns | 1,2 |
| | | 100.00MHz nominal/spread | 9.8720 | | | ns | 1,2 |
| Rise Time | $t_r$ | $V_{OL}$ = 0.175V, $V_{OH}$ = 0.525V | 175 | 332 | 700 | ps | 1 |
| Fall Time | $t_f$ | $V_{OH}$ = 0.525V $V_{OL}$ = 0.175V | 175 | 344 | 700 | ps | 1 |
| Rise Time Variation | d-$t_r$ | | | 30 | 125 | ps | 1 |
| Fall Time Variation | d-$t_f$ | | | 30 | 125 | ps | 1 |
| Duty Cycle | $d_{t3}$ | Measurement from differential wavefrom | 45 | 49 | 55 | % | 1 |
| Skew | $t_{sk3}$ | $V_T$ = 50% | | 8 | 100 | ps | 1 |
| Jitter, Cycle to cycle | $t_{jcyc-cyc}$ | Measurement from differential wavefrom | | 37 | 125 | ps | 1 |

[1]Guaranteed by design, not 100% tested in production.

[2] All Long Term Accuracy and Clock Period specifications are guaranteed with the assumption that Ref output is at 14.31818MHz

**SRC clock outputs run at only 100MHz or 200MHz, specs for 133.33 and 166.66 do not apply to SRC clock pair.**


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## Electrical Characteristics - 3V66 Mode: 3V66 [4:0]

$T_A$ = 0 - 70°C; $V_{DD}$ = 3.3 V +/-5%; $C_L$ = 10-30 pF (unless otherwise specified)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS | Notes |
|---|---|---|---|---|---|---|---|
| Long Accuracy | ppm | see Tperiod min-max values | -300 | | 300 | ppm | 1,2 |
| Clock period | $T_{period}$ | 66.66MHz output nominal | 14.9955 | 15 | 15.0045 | ns | 2 |
| | | 66.66MHz output spread | 14.9955 | | 15.0799 | ns | 2 |
| Output High Voltage | $V_{OH}$ | $I_{OH}$ = -1 mA | 2.4 | | | V | |
| Output Low Voltage | $V_{OL}$ | $I_{OL}$ = 1 mA | | | 0.55 | V | |
| Output High Current | $I_{OH}$ | $V_{OH}$ @ MIN = 1.0 V | -33 | | | mA | |
| | | $V_{OH}$ @ MAX = 3.135 V | | | -33 | mA | |
| Output Low Current | $I_{OL}$ | $V_{OL}$ @ MIN = 1.95 V | 30 | | | mA | |
| | | $V_{OL}$ @ MAX = 0.4 V | | | 38 | mA | |
| Edge Rate | | Rising edge rate | 1 | | 4 | V/ns | 1 |
| Edge Rate | | Falling edge rate | 1 | | 4 | V/ns | 1 |
| Rise Time | $t_{r1}$ | $V_{OL}$ = 0.4 V, $V_{OH}$ = 2.4 V | 0.5 | 1.92 | 2 | ns | 1 |
| Fall Time | $t_{f1}$ | $V_{OH}$ = 2.4 V, $V_{OL}$ = 0.4 V | 0.5 | 1.97 | 2 | ns | 1 |
| Duty Cycle | $d_{t1}$ | $V_T$ = 1.5 V | 45 | 53.1 | 55 | % | 1 |
| Skew | $t_{sk1}$ | $V_T$ = 1.5 V | | 38 | 250 | ps | 1 |
| Jitter | $t_{jcyc-cyc}$ | $V_T$ = 1.5 V 3V66 | | 139 | 250 | ps | 1 |

[1]Guaranteed by design, not 100% tested in production.

[2] All Long Term Accuracy and Clock Period specifications are guaranteed with the assumption that Ref output is at 14.31818MHz

## Electrical Characteristics - PCICLK/PCICLK_F

$T_A$ = 0 - 70°C; $V_{DD}$ = 3.3 V +/-5%; $C_L$ = 10-30 pF (unless otherwise specified)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS | Notes |
|---|---|---|---|---|---|---|---|
| Long Accuracy | ppm | see Tperiod min-max values | -300 | | 300 | ppm | 1,2 |
| Clock period | $T_{period}$ | 33.33MHz output nominal | 29.9910 | 30 | 30.0090 | ns | 2 |
| | | 33.33MHz output spread | 29.9910 | | 30.1598 | ns | 2 |
| Output High Voltage | $V_{OH}$ | $I_{OH}$ = -1 mA | 2.4 | | | V | |
| Output Low Voltage | $V_{OL}$ | $I_{OL}$ = 1 mA | | | 0.55 | V | |
| Output High Current | $I_{OH}$ | $V_{OH}$ @MIN = 1.0 V | -33 | | | mA | |
| | | $V_{OH}$@ MAX = 3.135 V | | | -33 | mA | |
| Output Low Current | $I_{OL}$ | $V_{OL}$ @ MIN = 1.95 V | 30 | | | mA | |
| | | $V_{OL}$ @ MAX = 0.4 V | | | 38 | mA | |
| Edge Rate | | Rising edge rate | 1 | | 4 | V/ns | 1 |
| Edge Rate | | Falling edge rate | 1 | | 4 | V/ns | 1 |
| Rise Time | $t_{r1}$ | $V_{OL}$ = 0.4 V, $V_{OH}$ = 2.4 V | 0.5 | 1.92 | 2 | ns | 1 |
| Fall Time | $t_{f1}$ | $V_{OH}$ = 2.4 V, $V_{OL}$ = 0.4 V | 0.5 | 1.9 | 2 | ns | 1 |
| Duty Cycle | $d_{t1}$ | $V_T$ = 1.5 V | 45 | 51.4 | 55 | % | 1 |
| Skew | $t_{sk1}$ | $V_T$ = 1.5 V | | 18 | 500 | ps | 1 |
| Jitter | $t_{jcyc-cyc}$ | $V_T$ = 1.5 V 3V66 | | 92 | 250 | ps | 1 |

[1]Guaranteed by design, not 100% tested in production.

[2] All Long Term Accuracy and Clock Period specifications are guaranteed with the assumption that Ref output is at 14.31818MHz



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## Electrical Characteristics - 48MHz DOT Clock

$T_A$ = 0 - 70°C; $V_{DD}$ = 3.3 V +/-5%; $C_L$ = 5-10 pF (unless otherwise specified)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS | Notes |
|---|---|---|---|---|---|---|---|
| Long Accuracy | ppm | see Tperiod min-max values | -200 | | 200 | ppm | 1,2 |
| Clock period | $T_{period}$ | 66.66MHz output nominal | 20.8257 | | 20.8340 | ns | 2 |
| Output High Voltage | $V_{OH}$ | $I_{OH}$ = -1 mA | 2.4 | | | V | |
| Output Low Voltage | $V_{OL}$ | $I_{OL}$ = 1 mA | | | 0.55 | V | |
| Output High Current | $I_{OH}$ | $V_{OH}$ @ MIN = 1.0 V | -33 | | | mA | |
| | | $V_{OH}$ @ MAX = 3.135 V | | | -33 | mA | |
| Output Low Current | $I_{OL}$ | $V_{OL}$ @ MIN = 1.95 V | 30 | | | mA | |
| | | $V_{OL}$ @ MAX = 0.4 V | | | 38 | mA | |
| Edge Rate | | Rising edge rate | 2 | | 4 | V/ns | 1 |
| Edge Rate | | Falling edge rate | 2 | | 4 | V/ns | 1 |
| Rise Time | $t_{r1}$ | $V_{OL}$ = 0.4 V, $V_{OH}$ = 2.4 V | 0.5 | 0.71 | 1 | ns | 1 |
| Fall Time | $t_{f1}$ | $V_{OH}$ = 2.4 V, $V_{OL}$ = 0.4 V | 0.5 | 0.77 | 1 | ns | 1 |
| Duty Cycle | $d_{t1}$ | $V_T$ = 1.5 V | 45 | 49 | 55 | % | 1 |
| Long Term Jitter | | 125us period jitter (8kHz frequency modulation amplitude) | | 0.7 | 2 | ns | 1 |

[1]Guaranteed by design, not 100% tested in production.
[2] All Long Term Accuracy and Clock Period specifications are guaranteed with the assumption that Ref output is at 14.31818MHz

## Electrical Characteristics - VCH, 48MHz, USB

$T_A$ = 0 - 70°C; $V_{DD}$ = 3.3 V +/-5%; $C_L$ = 10-20 pF (unless otherwise specified)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS | Notes |
|---|---|---|---|---|---|---|---|
| Long Accuracy | ppm | see Tperiod min-max values | -200 | | 200 | ppm | 1,2 |
| Clock period | $T_{period}$ | 66.66MHz output nominal | 20.8257 | | 20.8340 | ns | 2 |
| Output High Voltage | $V_{OH}$ | $I_{OH}$ = -1 mA | 2.4 | | | V | |
| Output Low Voltage | $V_{OL}$ | $I_{OL}$ = 1 mA | | | 0.55 | V | |
| Output High Current | $I_{OH}$ | $V_{OH}$ @ MIN = 1.0 V | -33 | | | mA | |
| | | $V_{OH}$@ MAX = 3.135 V | | | -33 | mA | |
| Output Low Current | $I_{OL}$ | $V_{OL}$ @MIN = 1.95 V | 30 | | | mA | |
| | | $V_{OL}$ @ MAX = 0.4 V | | | 38 | mA | |
| Edge Rate | | Rising edge rate | 1 | | 2 | V/ns | 1 |
| Edge Rate | | Falling edge rate | 1 | | 2 | V/ns | 1 |
| Rise Time | $t_{r1}$ | $V_{OL}$ = 0.4 V, $V_{OH}$ = 2.4 V | 1 | 1.43 | 2 | ns | 1 |
| Fall Time | $t_{f1}$ | $V_{OH}$ = 2.4 V, $V_{OL}$ = 0.4 V | 1 | 1.33 | 2 | ns | 1 |
| Duty Cycle | $d_{t1}$ | $V_T$ = 1.5 V | 45 | 48 | 55 | % | 1 |
| Long Term Jitter | | 125us period jitter (8kHz frequency modulation amplitude) | | 0.7 | 6 | ns | 1 |

[1]Guaranteed by design, not 100% tested in production.
[2] All Long Term Accuracy and Clock Period specifications are guaranteed with the assumption that Ref output is at 14.31818MHz


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## Electrical Characteristics - REF-14.318MHz

$T_A$ = 0 - 70°C; $V_{DD}$ = 3.3 V +/-5%; $C_L$ = 10-20 pF (unless otherwise specified)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| Long Accuracy | ppm[1] | see Tperiod min-max values | -300 | | 300 | ppm |
| Clock period | $T_{period}$ | 14.318MHz output nominal | 69.8270 | | 69.8550 | ns |
| Output High Voltage | $V_{OH}$[1] | $I_{OH}$ = -1 mA | 2.4 | | | V |
| Output Low Voltage | $V_{OL}$[1] | $I_{OL}$ = 1 mA | | | 0.4 | V |
| Output High Current | $I_{OH}$[1] | $V_{OH}$@MIN = 1.0 V, $V_{OH}$@MAX = 3.135 V | -29 | | -23 | mA |
| Output Low Current | $I_{OL}$[1] | $V_{OL}$@MIN = 1.95 V, $V_{OL}$@MAX = 0.4 V | 29 | | 27 | mA |
| Rise Time | $t_{r1}$[1] | $V_{OL}$ = 0.4 V, $V_{OH}$ = 2.4 V | 1 | 1.92 | 2 | ns |
| Fall Time | $t_{f1}$[1] | $V_{OH}$ = 2.4 V, $V_{OL}$ = 0.4 V | 1 | 1.92 | 2 | ns |
| Skew | $t_{sk1}$[1] | $V_T$ = 1.5 V | | 26 | 500 | ps |
| Duty Cycle | $d_{t1}$[1] | $V_T$ = 1.5 V | 45 | 53.4 | 55 | % |
| Jitter | $t_{jcyc-cyc}$[1] | $V_T$ = 1.5 V | | 284 | 1000 | ps |

[1]Guaranteed by design, not 100% tested in production.

## Group to Group Skews at Common Transition Edges

| GROUP | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| 200MHZ CPU to 3V66[1] | $S_{CPU200-3V66}$ | 3V66 (4:0) leads 200MHZ CPU | -2.1 | -1.6 | -1.1 | ns |
| 3V66 to PCI | $S_{3V66-PCI}$ | 3V66 (4:0) leads 33MHz PCI | 1.50 | 2.59 | 3.50 | ns |
| DOT-USB | $S_{DOT_USB}$ | 180 degrees out of phase | 0.00 | | 1.00 | ns |
| DOT-VCH | $S_{DOT_VCH}$ | in phase | 0.00 | | 1.00 | ns |

1. 3V66 MHz $C_L$ = 0pf, Rseries = 33 ohm. CPU CL = 2 pf, Rseries = 33 ohm, Rshunt = 49.9 ohms. Measured at the pins of the 952601.


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# General I²C serial interface information for the ICS952601

## How to Write:

- Controller (host) sends a start bit.
- Controller (host) sends the write address D2 (H)
- ICS clock will ***acknowledge***
- Controller (host) sends the begining byte location = N
- ICS clock will ***acknowledge***
- Controller (host) sends the data byte count = X
- ICS clock will ***acknowledge***
- Controller (host) starts sending ***Byte N through Byte N + X -1***
  (see Note 2)
- ICS clock will ***acknowledge*** each byte ***one at a time***
- Controller (host) sends a Stop bit

## How to Read:

- Controller (host) will send start bit.
- Controller (host) sends the write address D2 (H)
- ICS clock will ***acknowledge***
- Controller (host) sends the begining byte location = N
- ICS clock will ***acknowledge***
- Controller (host) will send a separate start bit.
- Controller (host) sends the read address D3 (H)
- ICS clock will ***acknowledge***
- ICS clock will send the data byte count = X
- ICS clock sends ***Byte N + X -1***
- ICS clock sends ***Byte 0 through byte X (if X(H) was written to byte 8)***.
- Controller (host) will need to acknowledge each byte
- Controllor (host) will send a not acknowledge bit
- Controller (host) will send a stop bit

**Index Block Write Operation**

| Controller (Host) | | ICS (Slave/Receiver) |
|---|---|---|
| T | starT bit | |
| Slave Address D2(H) | | |
| WR | WRite | |
| | | ACK |
| Beginning Byte = N | | |
| | | ACK |
| Data Byte Count = X | | |
| | | ACK |
| Beginning Byte N | X Byte | |
| | | ACK |
| ○ | | |
| ○ | | ○ |
| ○ | | ○ |
| | | ○ |
| Byte N + X - 1 | | |
| | | ACK |
| P | stoP bit | |

**Index Block Read Operation**

| Controller (Host) | | ICS (Slave/Receiver) | |
|---|---|---|---|
| T | starT bit | | |
| Slave Address D2(H) | | | |
| WR | WRite | | |
| | | ACK | |
| Beginning Byte = N | | | |
| | | ACK | |
| RT | Repeat starT | | |
| Slave Address D3(H) | | | |
| RD | ReaD | | |
| | | ACK | |
| | | | |
| | | Data Byte Count = X | |
| ACK | | | |
| | X Byte | | Beginning Byte N |
| ACK | | | |
| | | | ○ |
| ○ | | | ○ |
| ○ | | | ○ |
| ○ | | | |
| | | | Byte N + X - 1 |
| N | Not acknowledge | | |
| P | stoP bit | | |


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**I²C Table: Read-Back Register**

| Byte 0 | Pin # | Name | Control Function | Type | 0 | 1 | PWD |
|---|---|---|---|---|---|---|---|
| Bit 7 | - | RESERVED | RESERVED | - | RESERVED | | X |
| Bit 6 | - | RESERVED | RESERVED | - | RESERVED | | X |
| Bit 5 | - | RESERVED | RESERVED | - | RESERVED | | X |
| Bit 4 | - | RESERVED | RESERVED | - | RESERVED | | X |
| Bit 3 | - | PCI_STOP# | PCI STOP# Read Back | R | READBACK | | X |
| Bit 2 | - | CPU_STOP# | CPU STOP Read Back | R | READBACK | | X |
| Bit 1 | - | FSB | Freq Select 1 Read Back | R | READBACK of CPU(2:0) Frequency | | X |
| Bit 0 | - | FSA | Freq Select 0 Read Back | R | | | X |

**I²C Table: Spreading and Device Behavior Control Register**

| Byte 1 | Pin # | Name | Control Function | Type | 0 | 1 | PWD |
|---|---|---|---|---|---|---|---|
| Bit 7 | 37,38 | SRC/SRC# | SRC Free-Running Control | RW | FREE-RUN | STOPPABLE | 0 |
| Bit 6 | 37,38 | SRC | Output Control | RW | Disable | Enable | 1 |
| Bit 5 | 46,47 | CPUT2/CPUC2 | CPU FREE-RUNNING CONTROL | RW | FREE-RUN | STOPPABLE | 1 |
| Bit 4 | 43,44 | CPUT1/CPUC1 | | RW | FREE-RUN | STOPPABLE | 1 |
| Bit 3 | 40,41 | CPUT0/CPUC0 | | RW | FREE-RUN | STOPPABLE | 1 |
| Bit 2 | 46,47 | CPUT2/CPUC2 | Output Control | RW | Disable | Enable | 1 |
| Bit 1 | 43,44 | CPUT1/CPUC1 | Output Control | RW | Disable | Enable | 1 |
| Bit 0 | 40,41 | CPUT0/CPUC0 | Output Enable | RW | Disable | Enable | 1 |

**I²C Table: Output Control Register**

| Byte 2 | Pin # | Name | Control Function | Type | 0 | 1 | PWD |
|---|---|---|---|---|---|---|---|
| Bit 7 | 37,38 | SRC_PD# Drive Mode | 0: Driven in PD# | RW | Driven | Hi-Z | 0 |
| Bit 6 | 37,38 | SRC_Stop# Drive Mode | 0: Driven in PCI_Stop# | RW | Driven | Hi-Z | 0 |
| Bit 5 | 46,47 | CPUT2_PD# Drive Mode | 0:driven in PD# 1: Tri-stated | RW | Driven | Hi-Z | 0 |
| Bit 4 | 43,44 | CPUT1_PD# Drive Mode | | RW | Driven | Hi-Z | 0 |
| Bit 3 | 40,41 | CPUT0_PD# Drive Mode | | RW | Driven | Hi-Z | 0 |
| Bit 2 | 46,47 | CPUT2_Stop Drive Mode | 0:driven when stopped 1: Tri-stated | RW | Driven | Hi-Z | 0 |
| Bit 1 | 43,44 | CPUT1_Stop Drive Mode | | RW | Driven | Hi-Z | 0 |
| Bit 0 | 40,41 | CPUT0_Stop Drive Mode | | RW | Driven | Hi-Z | 0 |


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**I²C Table: Output Control Register**

| Byte 3 | Pin # | Name | Control Function | Type | 0 | 1 | PWD |
|---|---|---|---|---|---|---|---|
| **Bit 7** | 7,8,9,12,13,14,15, 18,19,20,37,38, | PCI_Stop# | PCI_Stop# Control 0:all stoppable PCI and SRC are stopped | RW | Enable | Disable | 1 |
| **Bit 6** | 20 | PCICLK6 | Output Control | RW | Disable | Enable | 1 |
| **Bit 5** | 19 | PCICLK5 | Output Control | RW | Disable | Enable | 1 |
| **Bit 4** | 18 | PCICLK4 | Output Control | RW | Disable | Enable | 1 |
| **Bit 3** | 15 | PCICLK3 | Output Control | RW | Disable | Enable | 1 |
| **Bit 2** | 14 | PCICLK2 | Output Control | RW | Disable | Enable | 1 |
| **Bit 1** | 13 | PCICLK1 | Output Control | RW | Disable | Enable | 1 |
| **Bit 0** | 12 | PCICLK0 | Output Control | RW | Disable | Enable | 1 |

**I²C Table: Output Control Register**

| Byte 4 | Pin # | Name | Control Function | Type | 0 | 1 | PWD |
|---|---|---|---|---|---|---|---|
| **Bit 7** | 31 | 48MHz_USB 2x output drive | 0=2x drive | RW | 2x drive | normal | 0 |
| **Bit 6** | 31 | 48MHz_USB | Output Control | RW | Disable | Enable | 1 |
| **Bit 5** | 9 | PCIF2 | PCI FREE-RUN NING CONTROL | RW | FREE-RUN | STOPPABLE | 0 |
| **Bit 4** | 8 | PCIF1 | | RW | FREE-RUN | STOPPABLE | 0 |
| **Bit 3** | 7 | PCIF0 | | RW | FREE-RUN | STOPPABLE | 0 |
| **Bit 2** | 9 | PCICLK_F2 | Output Control | RW | Disable | Enable | 1 |
| **Bit 1** | 8 | PCICLK_F1 | Output Control | RW | Disable | Enable | 1 |
| **Bit 0** | 7 | PCICLK_F0 | Output Control | RW | Disable | Enable | 1 |

**I²C Table: Output Control Register**

| Byte 5 | Pin # | Name | Control Function | Type | 0 | 1 | PWD |
|---|---|---|---|---|---|---|---|
| **Bit 7** | 32 | 48MHZ_DOT | Output Control | RW | Disable | Enable | 1 |
| **Bit 6** | - | RESERVED | RESERVED | ` | - | - | 0 |
| **Bit 5** | 29 | 3V66_4/VCH Select | Output Select | RW | 3V66 | VCH | 0 |
| **Bit 4** | 29 | 3V66_4/VCH | Output Control | RW | Disable | Enable | 1 |
| **Bit 3** | 27 | 3V66_3 | Output Control | RW | Disable | Enable | 1 |
| **Bit 2** | 26 | 3V66_2 | Output Control | RW | Disable | Enable | 1 |
| **Bit 1** | 23 | 3V66_1 | Output Control | RW | Disable | Enable | 1 |
| **Bit 0** | 22 | 3V66_0 | Output Control | RW | Disable | Enable | 1 |


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**I²C Table: Output Control and Fix Frequency Register**

| Byte 6 | Pin # | Name | Control Function | Type | 0 | 1 | PWD |
|---|---|---|---|---|---|---|---|
| **Bit 7** | 1,2,7,8,9,12,13,14,15,18,19,20,22,23,26,27,29,31,32,37,38,40,41,43,44,46,47 | Test Clock Mode | Test Clock Mode | - | Disable | Enable | 0 |
| **Bit 6** | - | RESERVED | - | - | - | - | 0 |
| **Bit 5** | 40,41,43,44,46,47 | RESERVED | FS_A and FS_B Operation | - | Normal | Test Mode | 0 |
| **Bit 4** | 37,38 | RESERVED | SRC Frequency Select | - | 100MHz | 200MHz | 0 |
| **Bit 3** | | RESERVED | - | - | - | - | 0 |
| **Bit 2** | 7,8,9,12,13,14,15,18,19,20,22,23,26,27,29,31,32,37,38,40,41,43,44,46,47 | Spread Spectrum Mode | | | Spread OFF | Spread ON | 0 |
| **Bit 1** | 2 | REF1 | Output Control | RW | Disable | Enable | 1 |
| **Bit 0** | 1 | REF0 | Output Control | RW | Disable | Enable | 1 |

**I²C Table: Vendor & Revision ID Register**

| Byte 7 | Pin # | Name | Control Function | Type | 0 | 1 | PWD |
|---|---|---|---|---|---|---|---|
| **Bit 7** | - | RID3 | REVISION ID | R | - | - | X |
| **Bit 6** | - | RID2 | | R | - | - | X |
| **Bit 5** | - | RID1 | | R | - | - | X |
| **Bit 4** | - | RID0 | | R | - | - | X |
| **Bit 3** | - | VID3 | VENDOR ID | R | - | - | 0 |
| **Bit 2** | - | VID2 | | R | - | - | 0 |
| **Bit 1** | - | VID1 | | R | - | - | 0 |
| **Bit 0** | - | VID0 | | R | - | - | 1 |


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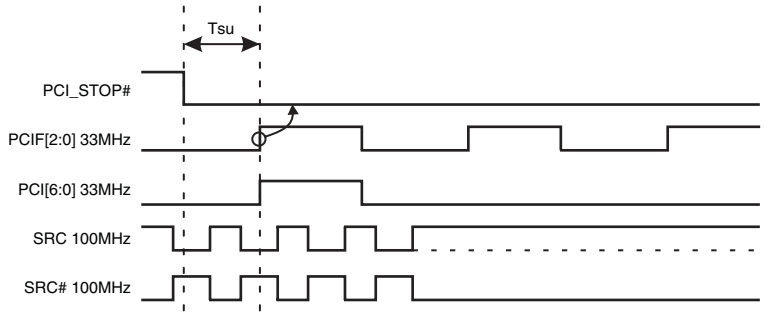
## PCI Stop Functionality

The PCI_STOP# signal is on an active low input controlling PCI and SRC outputs. If PCIF (2:0) and SRC clocks can be set to be free-running through I2C programming. Outputs set to be free-running will ignore both the PCI_STOP pin and the PCI_STOP register bit.

| PCI_STOP# | CPU | CPU # | SRC | SRC# | 3V66 | PCIF/PCI | USB/DOT | REF | Note |
|---|---|---|---|---|---|---|---|---|---|
| 1 | Normal | Normal | Normal | Normal | 66MHz | 33MHz | 48MHz | 14.318MHz | |
| 0 | Normal | Normal | Iref * 6 or Float | Low | 66MHz | Low | 48MHz | 14.318MHz | |

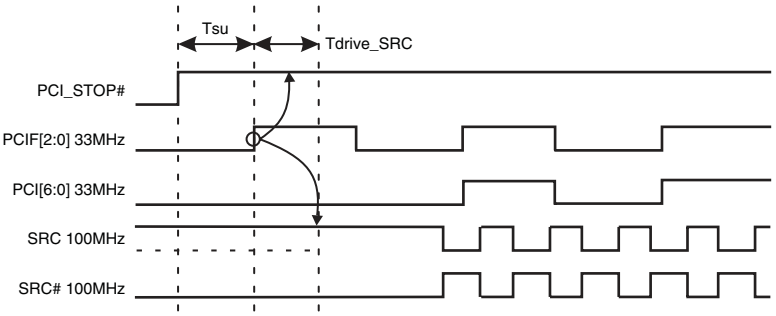
## PCI_STOP# Assertion (transition from '1' to '0')

The clock samples the PCI_STOP# signal on a rising edge of PCIF clock. After detecting the PCI_STOP# assertion low, all PCI[6:0] and stoppable PCIF[2:0] clocks will latch low on their next high to low transition. After the PCI clocks are latched low, the SRC clock, (if set to stoppable) will latch high at Iref * 6 (or tristate if Byte 2 Bit 6 = 1) upon its next low to high transition and the SRC# will latch low as shown below.




## PCI_STOP# - De-assertion

The de-assertion of the PCI_Stop# signal is to be sampled on the rising edge of the PCIF free running clock domain. After detecting PCI_Stop# de-assertion, all PCI[6:0], stoppable PCIF[2:0] and stoppable SRC clocks will resume in a glitch free manner.





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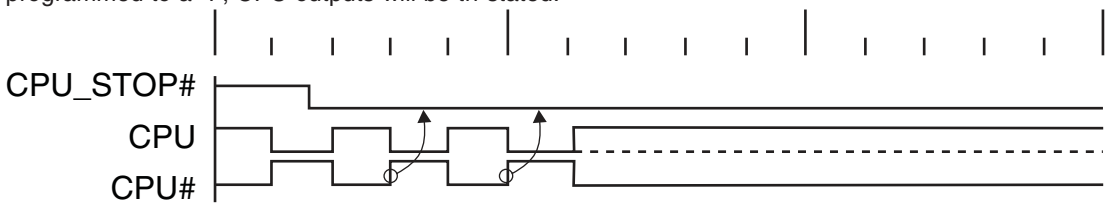
## CPU_STOP# Functionality

The CPU_STOP# signal is an active low input controlling the CPU outputs. This signal can be asserted asynchronously.

| CPU_STOP# | CPU | CPU # | SRC | SRC# | 3V66 | PCIF/PCI | USB/DOT | REF | Note |
|---|---|---|---|---|---|---|---|---|---|
| 1 | Normal | Normal | Normal | Normal | 66MHz | 33MHz | 48MHz | 14.318MHz | |
| 0 | Iref * 6 or Float | Low | Normal | Normal | 66MHz | 33MHz | 48MHz | 14.318MHz | |

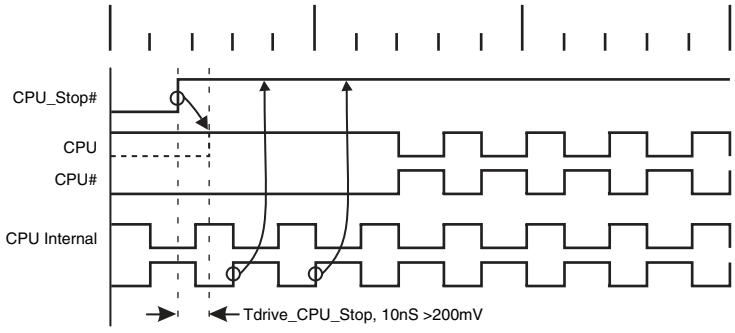
## CPU_STOP# - Assertion (transition from '1' to '0')

Asserting CPU_STOP# pin stops all CPU outputs that are set to be stoppable after their next transition. When the I2C CPU_STOP tri-state bit corresponding to the CPU output of interest is programmed to a '0', CPU output will stop CPU_True = HIGH and CPU_Complement = LOW. When the I2C CPU_Stop tri-state bit corresponding to the CPU output of interest is programmed to a '1', CPU outputs will be tri-stated.




## CPU_STOP# - De-assertion (transition from '0' to '1')

With the de-assertion of CPU_Stop# all stopped CPU outputs will resume without a glitch. The maximum latency from the de-assertion to active outputs is 2 - 6 CPU clock periods. If the control register tristate bit corresponding to the output of interest is programmed to '1', then the stopped CPU outputs will be driven High within 10nS of CPU_Stop# de-assertion to a voltage greater than 200mV.





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## PD#, Power Down

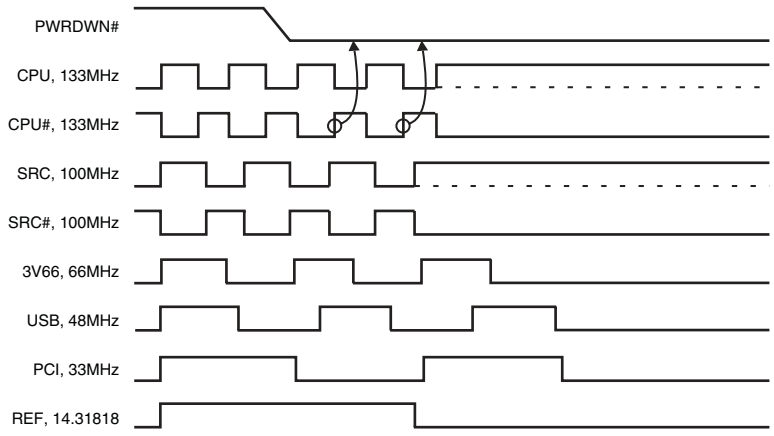
PD# is an asynchronous active low input used to shut off all clocks cleanly prior to clock power.
When PD# is asserted low all clocks will be driven low before turning off the VCO. In PD# de-assertion all clocks will start without glitches.

| PWRDWN# | CPU | CPU # | SRC | SRC# | 3V66 | PCIF/PCI | USB/DOT | REF | Note |
|---|---|---|---|---|---|---|---|---|---|
| 1 | Normal | Normal | Normal | Normal | 66MHz | 33MHz | 48MHz | 14.318MHz | |
| 0 | Iref * 2 or Float | Float | Iref * 2 or Float | Float | Low | Low | Low | Low | |

Notes:
1. Refer to tristate control of CPU and SRC clocks in section 7.7 for tristate timing and operation.
2. Refer to Control Registers in section 16 for CPU_Stop, SRC_Stop and PwrDwn SMBus tristate control addresses.

## PD# Assertion

PD# should be sampled low by 2 consecutive CPU# rising edges before stopping clocks. All single ended clocks will be held low on their next high to low transition.
All differential clocks will be held high on the next high to low transition of the complimentary clock. If the control register determining to drive mode is set to 'tri-state', the differential pair will be stopped in tri-state mode, undriven.
When the drive mode but corresponding to the CPU or SRC clock of interest is set to '0' the true clock will be driven high at 2 x Iref and the complementary clock will be tristated. If the control register is programmed to '1' both clocks will be tristated.

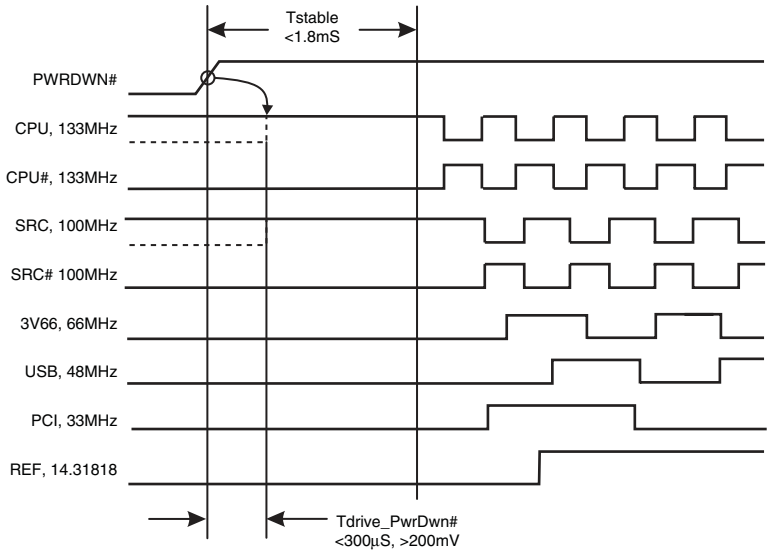




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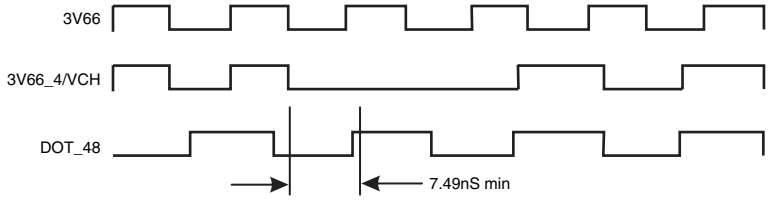
## PD# De-assertion

The time from the de-assertion of PD# or until power supply ramps to get stable clocks will be less than 1.8ms. If the drive mode control bit for PD# tristate is programmed to '1' the stopped differential pair must first be driven high to a minimum of 200mV in less than 300µs of PD# deassertion.




## 3V66_4/VCH Pin Functionality

The 3V66_4/VCH pin can be configured to be a 66.66MHz modulated output or a non-spread 48MHz output. The default is 3V66 clock. The switching is controlled by Byte 5 Bit 5. If it is set to '1' this pin will output the 48MHz VCH clock. The output will go low on the falling edge of 3V66 for a minimum of 7.49ns. Then the output will transition to 48MHz on the next rising edge of DOT_48 clock.





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## Differential Clock Tristate

To minimize power consumption, CPU[2:0] clock outputs are individually configurable through SMBus to be driven or tristated during PwrDwn# and CPU_Stop# mode and the SRC clock is configurable to be driven or tristated during PCI_Stop# and PwrDwn# mode. Each differential clock (SRC, CPU[2:0]) output can be disabled by setting the corresponding output's register OE bit to "0" (disable). Disabled outputs are to be tristated regardless of "CPU_Stop", "SRC_Stop" and "PwrDwn" register bit settings.

| Signal | Pin PD# | Pin CPU_Stop# | CPU_Stop Tristate Bit | Pwrdwn Tristate Bit | Non-Stoppable Outputs | Stoppable Outputs |
|---|---|---|---|---|---|---|
| CPU[2:0} | 1 | 1 | X | X | Running | Running |
| CPU[2:0} | 1 | 0 | 0 | X | Running | Driven @ Iref x 6 |
| CPU[2:0} | 1 | 0 | 1 | X | Running | Tristate |
| CPU[2:0} | 0 | X | X | 0 | Driven @ Iref x 2 | Driven @ Iref x 2 |
| CPU[2:0} | 0 | X | X | 1 | Tristate | Tristate |

Notes:
1. Each output has four corresponding control register bits, OE, PwrDwn, CPU_Stop and "Free Running"
2. Iref x 6 and Iref x 2 is the output current in the corresponding mode
3. See Control Registers section for bit address

| Signal | Pin PD# | Pin PCI_Stop# | PCI_Stop Tristate Bit | Pwrdwn Tristate Bit | Non-Stoppable Output | Stoppable Output |
|---|---|---|---|---|---|---|
| SRC | 1 | 1 | X | X | Running | Running |
| SRC | 1 | 0 | 0 | X | Running | Driven @ Iref x 6 |
| SRC | 1 | 0 | 1 | X | Running | Tristate |
| SRC | 0 | X | X | 0 | Driven @ Iref x 2 | Driven @ Iref x 2 |
| SRC | 0 | X | X | 1 | Tristate | Tristate |

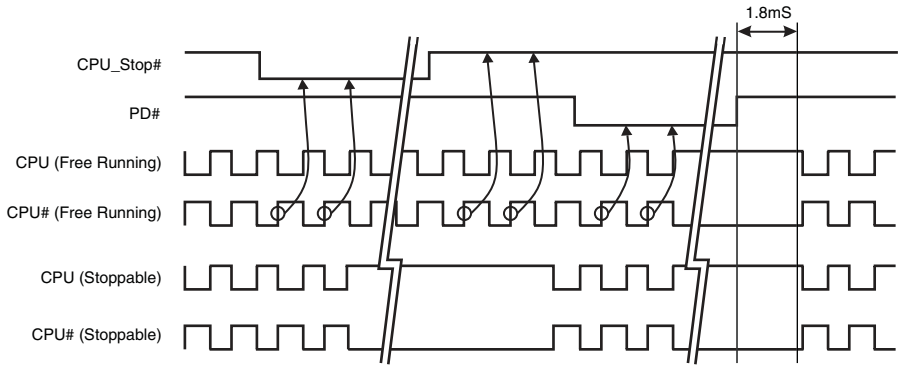
Notes:
1. SRC output has four corresponding control register bits, OE, PwrDwn, SRC_Stop and "Free Running"
2. Iref x 6 and Iref x 2 is the output current in the corresponding mode
3. See Control Registers section for bit address


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## CPU Clock Tristate Timing

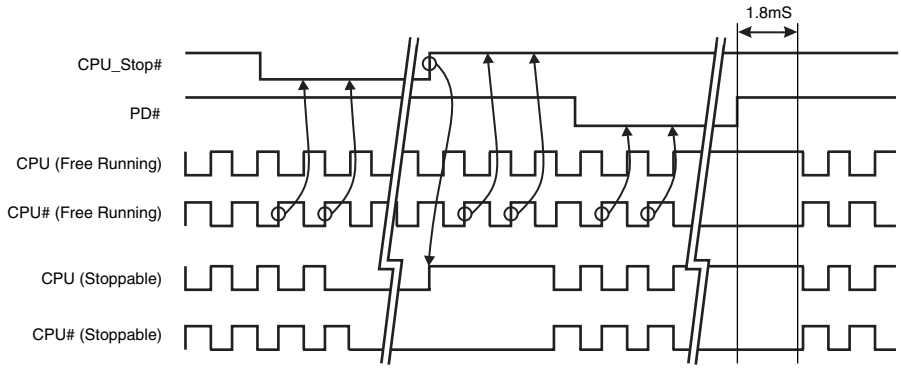
The following diagrams illustrate CPU clock timing during CPU_Stop# and PwrDwn# modes with CPU_PwrDwn and CPU_Stop tristate control bits set to driven or tristate in byte 2 of the control register.

**CPU_Stop = Driven, CPU_Pwrdwn = Driven**




Notes:
1. When both bits (CPU_Stop & CPU_Pwrdown tristate bits) are low, the clock chip will never tristate CPU output clocks (assuming clock's OE bit is set to "1")

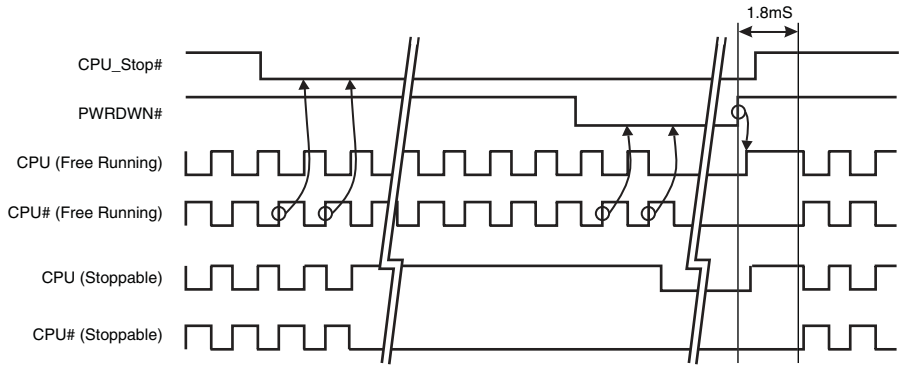
**CPU_Stop = Tristate, CPU_Pwrdwn = Driven**




Notes:
1. Tristate outputs are pulled low by output termination resistors as shown here.

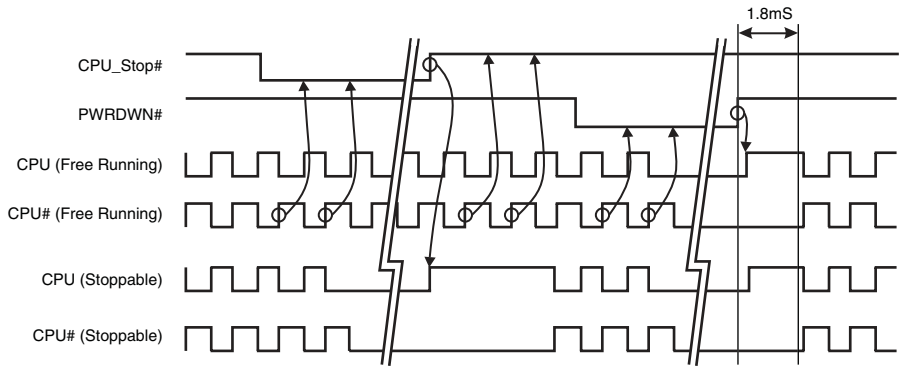

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**CPU_Stop = Driven, CPU_Pwrdwn = Tristate**




Notes:
1. When CPU_Pwrdwn is set to tristate and CPU_Stop is set to driven, the clock chip will tristate outputs only during the assertion of PWRDWN#. Differential clock behavior during the assertion/de-assertion of CPU_Stop# will be unaffected.
2. In the case that CPU_Stop# is de-asserted during the 1.8mS PWRDWN# de-assertion resume delay, the clock chip can sample the CPU_Stop# high with the internal rising edges of clock#. This will result in CPU clocks resuming immediately after the 1.8mS windows expires. This applies to all control register bit changes as well.
3. Tristate outputs are pulled low by output termination resistors as shown here.

**CPU_Stop = Tristate, CPU_Pwrdwn = Tristate**



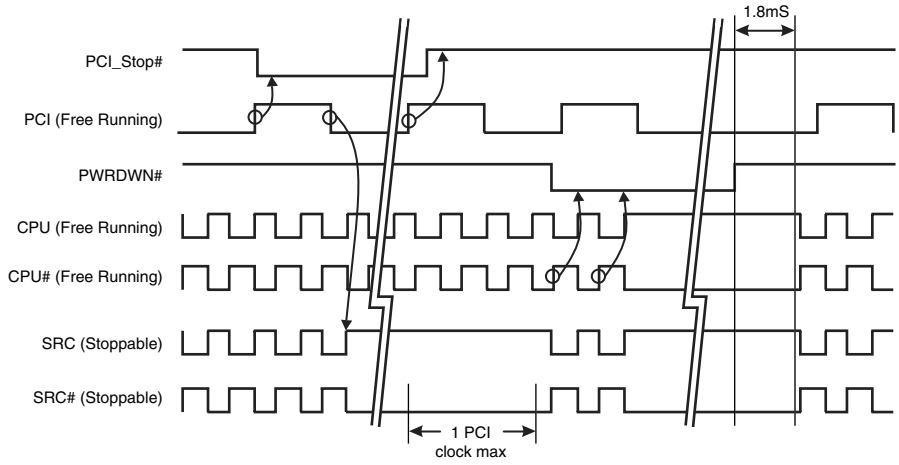

Notes:
1. When CPU_Stop and CPU_Pwrdwn bits are set to tristate, the clock chip will tristate the outputs during the assertion of CPU_Stop# and PWRDWN#.
2. Tristate outputs are pulled low by output termination resistors as shown here.


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## SRC Clock Tristate Timing

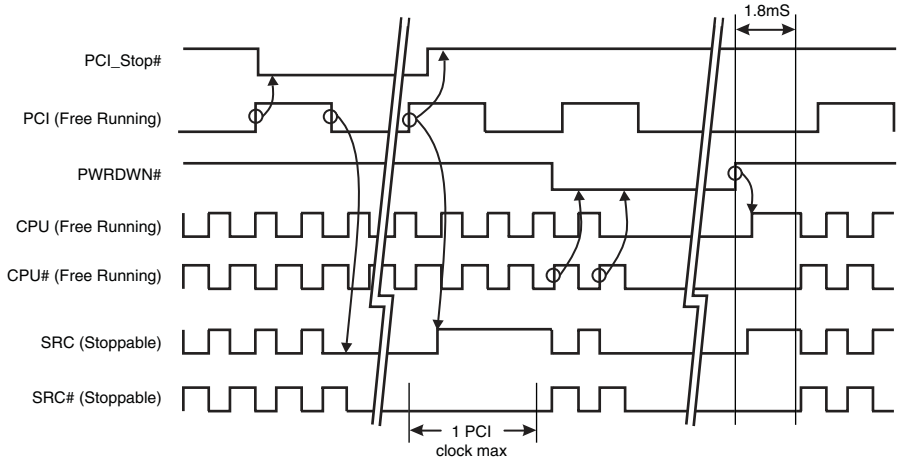
The following diagrams illustrate SRC clock timing during PCI_Stop# and PwrDwn# modes with SRC_Pwrdwn and SRC_Stop tristate control bits set to driven or tristate in byte 2 of the control register.

**SRC_Stop = Driven, SRC_Pwrdwn = Driven**




Notes:
1. When both bits (SRC_Stop & SRC_Pwrdown tristate bits) are set to driven, the clock chip will never tristate the SRC output clock (assuming clock's OE bit is set to "1")

**SRC_Stop = Tristate, Pwrdwn = Tristate**

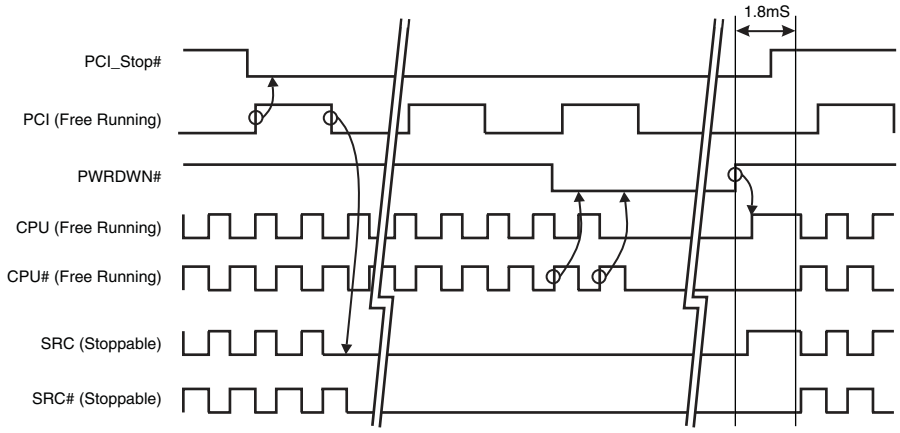



Notes:
1. When SRC_Stop and SRC_Pwrdwn bits are set to tristate, the clock chip will tristate outputs during the assertion of PCI_Stop# and PWRDWN#.
2. Tristate outputs are pulled low by output termination resistors as shown here.


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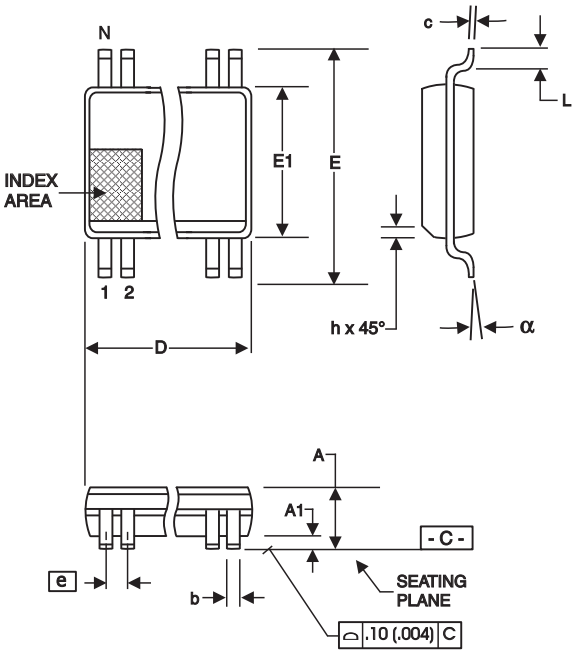
**PCI_STOP Asserted**

**SRC_Stop = Tristate, SRC_Pwrdwn = Tristate**




Notes:
1. When SRC_Pwrdwn and SRC_Stop are set to tristate, the clock chip will tristate outputs during the assertion of PCI_Stop# and PWRDWN#.
2. In the case that PCI_Stop# is de-asserted during the 1.8mS PWRDWN# de-assertion resume delay, the clock chip can sample the PCI_Stop# high with the internal rising edges of CPU clock#. This will result in SRC clocks resuming immediately after the 1.8mS window expires. This applies to all control register bit changes as well.
3. Tristate outputs are pulled low by output termination resistors as shown here.


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**56-Lead, 300 mil Body, 25 mil, SSOP**

| SYMBOL | In Millimeters COMMON DIMENSIONS | | In Inches COMMON DIMENSIONS | |
|---|---|---|---|---|
| | MIN | MAX | MIN | MAX |
| A | 2.41 | 2.80 | .095 | .110 |
| A1 | 0.20 | 0.40 | .008 | .016 |
| b | 0.20 | 0.34 | .008 | .0135 |
| c | 0.13 | 0.25 | .005 | .010 |
| D | SEE VARIATIONS | | SEE VARIATIONS | |
| E | 10.03 | 10.68 | .395 | .420 |
| E1 | 7.40 | 7.60 | .291 | .299 |
| e | 0.635 BASIC | | 0.025 BASIC | |
| h | 0.38 | 0.64 | .015 | .025 |
| L | 0.50 | 1.02 | .020 | .040 |
| N | SEE VARIATIONS | | SEE VARIATIONS | |
| a | 0° | 8° | 0° | 8° |

VARIATIONS

| N | D mm. | | D (inch) | |
|---|---|---|---|---|
| | MIN | MAX | MIN | MAX |
| 56 | 18.31 | 18.55 | .720 | .730 |

Reference Doc.: JEDEC Publication 95, MO-118

10-0034

## Ordering Information

**952601yFLFT**

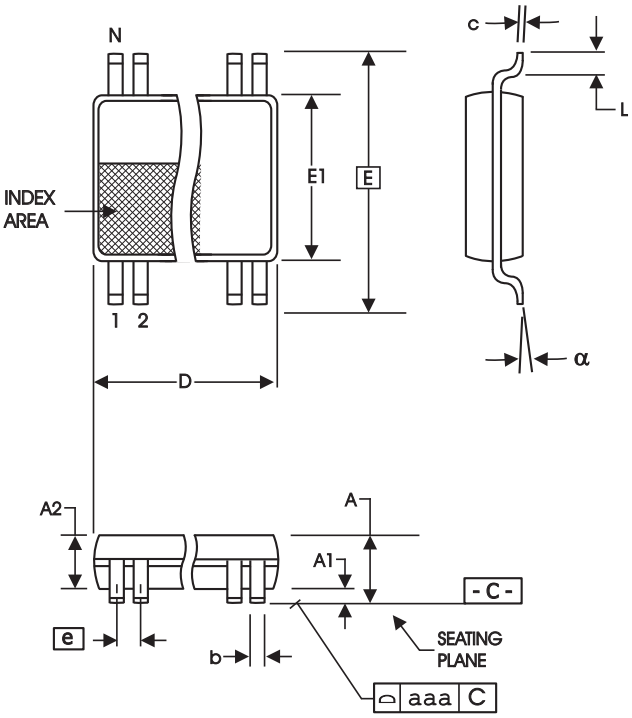
Example:

**XXXX y F LF T**

- **Designation for tape and reel packaging**
- **Annealed Lead Free (optional)**
- **Package Type**
  F = SSOP
- **Revision Designator** (will not correlate with datasheet revision)
- **Device Type (consists of 3 or 4 digit numbers)**



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**56-Lead 6.10 mm. Body, 0.50 mm. Pitch TSSOP**
**(240 mil) (20 mil)**

| SYMBOL | In Millimeters COMMON DIMENSIONS | | In Inches COMMON DIMENSIONS | |
|---|---|---|---|---|
| | MIN | MAX | MIN | MAX |
| A | -- | 1.20 | -- | .047 |
| A1 | 0.05 | 0.15 | .002 | .006 |
| A2 | 0.80 | 1.05 | .032 | .041 |
| b | 0.17 | 0.27 | .007 | .011 |
| c | 0.09 | 0.20 | .0035 | .008 |
| D | SEE VARIATIONS | | SEE VARIATIONS | |
| E | 8.10 BASIC | | 0.319 BASIC | |
| E1 | 6.00 | 6.20 | .236 | .244 |
| e | 0.50 BASIC | | 0.020 BASIC | |
| L | 0.45 | 0.75 | .018 | .030 |
| N | SEE VARIATIONS | | SEE VARIATIONS | |
| a | 0° | 8° | 0° | 8° |
| aaa | -- | 0.10 | -- | .004 |

VARIATIONS

| N | D mm. | | D (inch) | |
|---|---|---|---|---|
| | MIN | MAX | MIN | MAX |
| 56 | 13.90 | 14.10 | .547 | .555 |

Reference Doc.: JEDEC Publication 95, MO-153

10-0039

## Ordering Information

**952601yGLFT**

Example:

**XXXX y G LF T**

- **Designation for tape and reel packaging**
- **Annealed Lead Free (optional)**
- **Package Type**
  G = TSSOP
- **Revision Designator** (will not correlate with datasheet revision)
- **Device Type (consists of 3 or 4 digit numbers)**



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## Revision History

| Rev. | Issue Date | Description | Page # |
|---|---|---|---|
| I | 5/4/2005 | Updated Ordering Information from "Lead Free" to "Annealed Lead Free" | 23-24 |
| J | 1/25/2010 | Update document template | |
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