Programmable Timing Control Hub™ for Next Gen P4™ processor

Recommended Application:

CK410 compliant clock

Output Features:

- 2 - 0.7V current-mode differential CPU pairs
- 6 - 0.7V current-mode differential SRC pair
- 1 - 0.7V current-mode differential CPU_ITP/SRC selectable pair
- 6 - PCI (33MHz)
- 3 - PCICLK_F, (33MHz) free-running
- 1 - USB, 48MHz
- 1 - DOT, 96MHz, 0.7V current differential pair
- 1 - REF, 14.318MHz

Key Specifications:

- CPU/SRC outputs cycle-cycle jitter < 85ps
- PCI outputs cycle-cycle jitter < 250ps
- +/- 300ppm frequency accuracy on CPU & SRC clocks

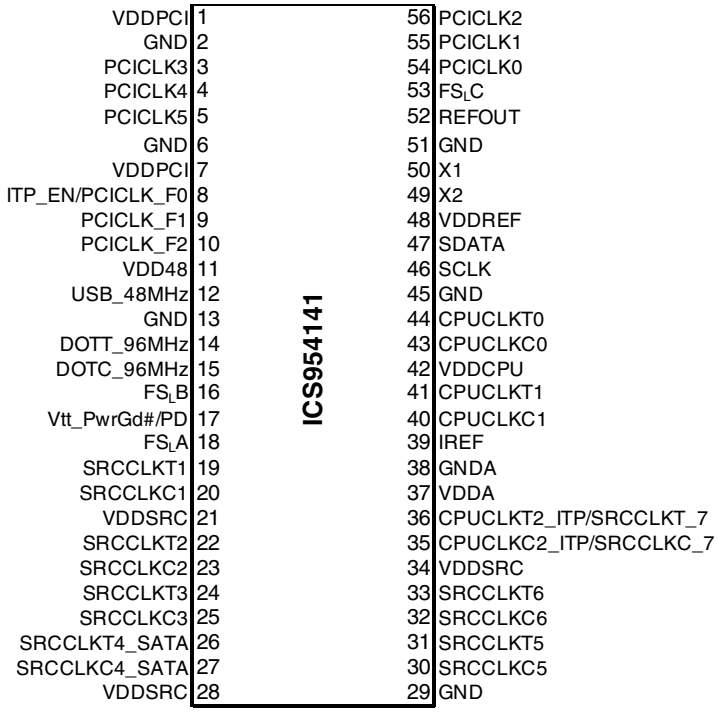
Features/Benefits:

- Programmable output frequencies
- Programmable output skew.
- Programmable spread percentage for EMI control.
- Programmable watch dog safe frequency.
- Supports tight ppm accuracy clocks for Serial-ATA
- Supports spread spectrum modulation, 0 to -0.5% down spread, ±0.25% center spread, and ±0.3% center spread
- Uses external 14.318MHz crystal, external crystal load caps are required for frequency tuning
- Supports undriven differential CPU, SRC pair in PD# for power management.

Functionality

Bit4	Bit3	Bit2	Bit1	Bit0	CPU	SRC	SATA	PCI
		FSLC	FSLB	FSLA	MHz	MHz	MHz	MHz
0	0	0	0	0	266.66	100.00	100.00	33.33
0	0	0	0	1	133.33	100.00	100.00	33.33
0	0	0	1	0	200.00	100.00	100.00	33.33
0	0	0	1	1	166.66	100.00	100.00	33.33
0	0	1	0	0	333.33	100.00	100.00	33.33
0	0	1	0	1	100.00	100.00	100.00	33.33
0	0	1	1	0	400.00	100.00	100.00	33.33
0	0	1	1	1	200.00	100.00	100.00	33.33
0	1	0	0	0	266.66	133.33	133.33	33.33
0	1	0	0	1	133.33	133.33	133.33	33.33
0	1	0	1	0	200.00	133.33	133.33	33.33
0	1	0	1	1	166.66	125.00	125.00	33.33
0	1	1	0	0	333.33	125.00	125.00	33.33
0	1	1	0	1	100.00	133.33	133.33	33.33
0	1	1	1	0	400.00	133.33	133.33	33.33
0	1	1	1	1	200.00	133.33	133.33	33.33
1	0	0	0	0	269.33	101.00	101.00	33.67
1	0	0	0	1	134.66	101.00	101.00	33.67
1	0	0	1	0	202.00	101.00	101.00	33.67
1	0	0	1	1	168.33	101.00	101.00	33.67
1	0	1	0	0	274.66	103.00	103.00	34.33
1	0	1	0	1	137.33	103.00	103.00	34.33
1	0	1	1	0	206.00	103.00	103.00	34.33
1	0	1	1	1	171.66	103.00	103.00	34.33
1	1	0	0	0	279.99	105.00	105.00	35.00
1	1	0	0	1	140.00	105.00	105.00	35.00
1	1	0	1	0	210.00	105.00	105.00	35.00
1	1	0	1	1	174.99	105.00	105.00	35.00
1	1	1	0	0	287.99	108.00	108.00	36.00
1	1	1	0	1	144.00	108.00	108.00	36.00
1	1	1	1	0	216.00	108.00	108.00	36.00
1	1	1	1	1	179.99	108.00	108.00	36.00

Pin Configuration



56-Pin SSOP and TSSOP

* Internal Pull-Up Resistor

** Internal Pull-Down Resistor

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Pin Description

PIN #	PIN NAME	TYPE	DESCRIPTION
1	VDDPCI	PWR	Power supply for PCI clocks, nominal 3.3V
2	GND	PWR	Ground pin.
3	PCICLK3	OUT	PCI clock output.
4	PCICLK4	OUT	PCI clock output.
5	PCICLK5	OUT	PCI clock output.
6	GND	PWR	Ground pin.
7	VDDPCI	PWR	Power supply for PCI clocks, nominal 3.3V
8	ITP_EN/PCICLK_F0	I/O	Free running PCI clock not affected by PCI_STOP#. ITP_EN: latched input to select pin functionality 1 = CPU_ITP pair 0 = SRC pair
9	PCICLK_F1	OUT	Free running PCI clock not affected by PCI_STOP# .
10	PCICLK_F2	OUT	Free running PCI clock not affected by PCI_STOP# .
11	VDD48	PWR	Power pin for the 48MHz output.3.3V
12	USB_48MHz	OUT	48.00MHz USB clock
13	GND	PWR	Ground pin.
14	DOTT_96MHz	OUT	True clock of differential pair for 96.00MHz DOT clock.
15	DOTC_96MHz	OUT	Complement clock of differential pair for 96.00MHz DOT clock.
16	FSLB	IN	3.3V tolerant input for CPU frequency selection. Refer to input electrical characteristics for Vil_FS and Vih_FS values.
17	Vtt_PwrGd#/PD	IN	Vtt_PwrGd# is an active low input used to determine when latched inputs are ready to be sampled. PD is an asynchronous active high input pin used to put the device into a low power state. The internal clocks, PLLs and the crystal oscillator are stopped.
18	FSLA	IN	3.3V tolerant input for CPU frequency selection. Refer to input electrical characteristics for Vil_FS and Vih_FS values.
19	SRCCLKT1	OUT	True clock of differential SRC clock pair.
20	SRCCLKC1	OUT	Complement clock of differential SRC clock pair.
21	VDDSRC	PWR	Supply for SRC clocks, 3.3V nominal
22	SRCCLKT2	OUT	True clock of differential SRC clock pair.
23	SRCCLKC2	OUT	Complement clock of differential SRC clock pair.
24	SRCCLKT3	OUT	True clock of differential SRC clock pair.
25	SRCCLKC3	OUT	Complement clock of differential SRC clock pair.
26	SRCCLKT4_SATA	OUT	True clock of differential SRC/SATA pair.
27	SRCCLKC4_SATA	OUT	Complement clock of differential SRC/SATA pair.
28	VDDSRC	PWR	Supply for SRC clocks, 3.3V nominal

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Pin Description

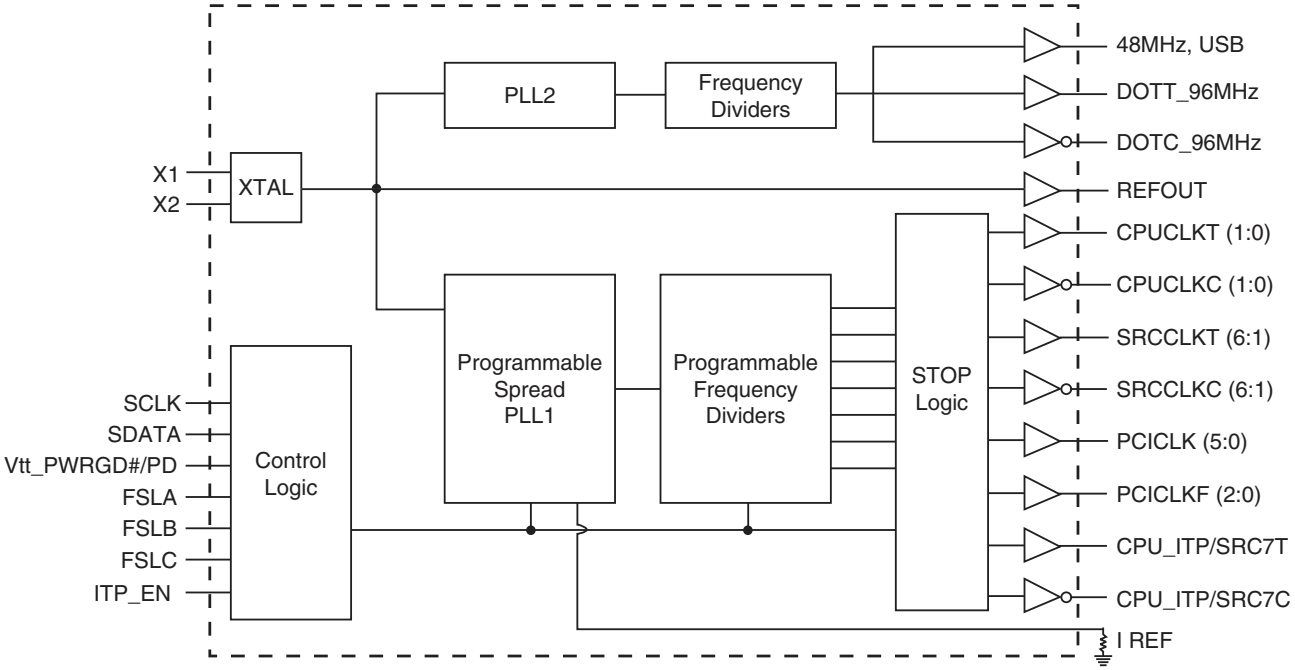
PIN #	PIN NAME	TYPE	DESCRIPTION
29	GND	PWR	Ground pin.
30	SRCCLKC5	OUT	Complement clock of differential SRC clock pair.
31	SRCCLKT5	OUT	True clock of differential SRC clock pair.
32	SRCCLKC6	OUT	Complement clock of differential SRC clock pair.
33	SRCCLKT6	OUT	True clock of differential SRC clock pair.
34	VDDSRC	PWR	Supply for SRC clocks, 3.3V nominal
35	CPUCLKC2_ITP/SRCCLKC_7	OUT	Complimentary clock of CPU_ITP/SRC differential pair CPU_ITP/SRC output. These are current mode outputs. External resistors are required for voltage bias. Selected by ITP_EN input.
36	CPUCLKT2_ITP/SRCCLKT_7	OUT	True clock of CPU_ITP/SRC differential pair CPU_ITP/SRC output. These are current mode outputs. External resistors are required for voltage bias. Selected by ITP_EN input.
37	VDDA	PWR	3.3V power for the PLL core.
38	GNDA	PWR	Ground pin for the PLL core.
39	IREF	OUT	This pin establishes the reference current for the differential current-mode output pairs. This pin requires a fixed precision resistor tied to ground in order to establish the appropriate current. 475 ohms is the standard value.
40	CPUCLKC1	OUT	Complimentary clock of differential pair CPU outputs. These are current mode outputs. External resistors are required for voltage bias.
41	CPUCLKT1	OUT	True clock of differential pair CPU outputs. These are current mode outputs. External resistors are required for voltage bias.
42	VDDCPU	PWR	Supply for CPU clocks, 3.3V nominal
43	CPUCLKC0	OUT	Complimentary clock of differential pair CPU outputs. These are current mode outputs. External resistors are required for voltage bias.
44	CPUCLKT0	OUT	True clock of differential pair CPU outputs. These are current mode outputs. External resistors are required for voltage bias.
45	GND	PWR	Ground pin.
46	SCLK	IN	Clock pin of SMBus circuitry, 5V tolerant.
47	SDATA	I/O	Data pin for SMBus circuitry, 5V tolerant.
48	VDDREF	PWR	Ref, XTAL power supply, nominal 3.3V
49	X2	OUT	Crystal output, Nominally 14.318MHz
50	X1	IN	Crystal input, Nominally 14.318MHz.
51	GND	PWR	Ground pin.
52	REFOUT	OUT	Reference Clock output
53	FSLC	IN	3.3V tolerant input for CPU frequency selection. Refer to input electrical characteristics for Vil_FS and Vih_FS values.
54	PCICLK0	OUT	PCI clock output.
55	PCICLK1	OUT	PCI clock output.
56	PCICLK2	OUT	PCI clock output.

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General Description

ICS954141A follows Intel CK410 Yellow Cover specification. This clock synthesizer provides a single chip solution for next generation P4 Intel processors and Intel chipsets. **ICS954141A** is driven with a 14.318MHz crystal.

Block Diagram



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General I²C serial interface information for the ICS954141A

How to Write:

- Controller (host) sends a start bit.
- Controller (host) sends the write address D2 (H)
- ICS clock will ***acknowledge***
- Controller (host) sends the begining byte location = N
- ICS clock will ***acknowledge***
- Controller (host) sends the data byte count = X
- ICS clock will ***acknowledge***
- Controller (host) starts sending ***Byte N through Byte N + X -1***
  (see Note 2)
- ICS clock will ***acknowledge*** each byte ***one at a time***
- Controller (host) sends a Stop bit

How to Read:

- Controller (host) will send start bit.
- Controller (host) sends the write address D2 (H)
- ICS clock will ***acknowledge***
- Controller (host) sends the begining byte location = N
- ICS clock will ***acknowledge***
- Controller (host) will send a separate start bit.
- Controller (host) sends the read address D3 (H)
- ICS clock will ***acknowledge***
- ICS clock will send the data byte count = X
- ICS clock sends ***Byte N + X -1***
- ICS clock sends ***Byte 0 through byte X (if X (H) was written to byte 8)***.
- Controller (host) will need to acknowledge each byte
- Controllor (host) will send a not acknowledge bit
- Controller (host) will send a stop bit

Index Block Write Operation

Controller (Host)			ICS (Slave/Receiver)
T	starT bit		
Slave Address D2(H)			
WR	WRite		
			ACK
Beginning Byte = N			
			ACK
Data Byte Count = X			
			ACK
Beginning Byte N		X Byte	
			ACK
O			
O			O
O			O
			O
Byte N + X - 1			
			ACK
P	stoP bit		

Index Block Read Operation

Controller (Host)			ICS (Slave/Receiver)
T	starT bit		
Slave Address D2(H)			
WR	WRite		
			ACK
Beginning Byte = N			
			ACK
RT	Repeat starT		
Slave Address D3(H)			
RD	ReaD		
			ACK
			Data Byte Count = X
ACK			
		X Byte	Beginning Byte N
ACK			
			O
O			O
O			O
O			
			Byte N + X - 1
N	Not acknowledge		
P	stoP bit		

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Table1: Frequency Selection Table

Bit4	Bit3	Bit2	Bit1	Bit0	CPU	SRC	SATA	PCI	Spread
		FSLC	FSLB	FSLA	MHz	MHz	MHz	MHz	%
0	0	0	0	0	266.66	100.00	100.00	33.33	0 to -0.5% Down
0	0	0	0	1	133.33	100.00	100.00	33.33	0 to -0.5% Down
0	0	0	1	0	200.00	100.00	100.00	33.33	0 to -0.5% Down
0	0	0	1	1	166.66	100.00	100.00	33.33	0 to -0.5% Down
0	0	1	0	0	333.33	100.00	100.00	33.33	0 to -0.5% Down
0	0	1	0	1	100.00	100.00	100.00	33.33	0 to -0.5% Down
0	0	1	1	0	400.00	100.00	100.00	33.33	0 to -0.5% Down
0	0	1	1	1	200.00	100.00	100.00	33.33	0 to -0.5% Down
0	1	0	0	0	266.66	133.33	133.33	33.33	+/-0.25% Center
0	1	0	0	1	133.33	133.33	133.33	33.33	+/-0.25% Center
0	1	0	1	0	200.00	133.33	133.33	33.33	+/-0.25% Center
0	1	0	1	1	166.66	125.00	125.00	33.33	+/-0.25% Center
0	1	1	0	0	333.33	125.00	125.00	33.33	+/-0.25% Center
0	1	1	0	1	100.00	133.33	133.33	33.33	+/-0.25% Center
0	1	1	1	0	400.00	133.33	133.33	33.33	+/-0.25% Center
0	1	1	1	1	200.00	133.33	133.33	33.33	+/-0.25% Center
1	0	0	0	0	269.33	101.00	101.00	33.67	+/-0.3% Center
1	0	0	0	1	134.66	101.00	101.00	33.67	+/-0.3% Center
1	0	0	1	0	202.00	101.00	101.00	33.67	+/-0.3% Center
1	0	0	1	1	168.33	101.00	101.00	33.67	+/-0.3% Center
1	0	1	0	0	274.66	103.00	103.00	34.33	+/-0.3% Center
1	0	1	0	1	137.33	103.00	103.00	34.33	+/-0.3% Center
1	0	1	1	0	206.00	103.00	103.00	34.33	+/-0.3% Center
1	0	1	1	1	171.66	103.00	103.00	34.33	+/-0.3% Center
1	1	0	0	0	279.99	105.00	105.00	35.00	+/-0.3% Center
1	1	0	0	1	140.00	105.00	105.00	35.00	+/-0.3% Center
1	1	0	1	0	210.00	105.00	105.00	35.00	+/-0.3% Center
1	1	0	1	1	174.99	105.00	105.00	35.00	+/-0.3% Center
1	1	1	0	0	287.99	108.00	108.00	36.00	+/-0.3% Center
1	1	1	0	1	144.00	108.00	108.00	36.00	+/-0.3% Center
1	1	1	1	0	216.00	108.00	108.00	36.00	+/-0.3% Center
1	1	1	1	1	179.99	108.00	108.00	36.00	+/-0.3% Center

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I²C Table: Frequency Select Register

Byte 0	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	-	FS Source	Frequency H/W IIC Select	RW	Latch Inputs	IIC	0
Bit 6	-	SS_EN1	PLL1 Spread Enable	RW	OFF	ON	1
Bit 5	-	SS_EN2	PLL2 Spread Enable	RW	OFF	ON	1
Bit 4	-	Bit4	Freq Select Bit 4	RW	See Table 1: PLL 1 Frequency Selection Table		0
Bit 3	-	Bit3	Freq Select Bit 3	RW			0
Bit 2	-	FSLC	Freq Select Bit 2	RW			Latch
Bit 1	-	FSLB	Freq Select Bit 1	RW			Latch
Bit 0	-	FSLA	Freq Select Bit 0	RW			Latch

I²C Table: Output Control Register

Byte 1	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	-	PCICLK_F0	Output Control	RW	Disable	Enable	1
Bit 6	-	DOTT/C_96MHz	Output Control	RW	Disable	Enable	1
Bit 5	-	USB_48MHz	Output Control	RW	Disable	Enable	1
Bit 4	-	REFOUT	Output Control	RW	Disable	Enable	1
Bit 3	-	Reserved	Reserved	RW	-	-	1
Bit 2	-	CPUCLKT/C1	Output Control	RW	Disable	Enable	1
Bit 1	-	CPUCLKT/C0	Output Control	RW	Disable	Enable	1
Bit 0	-	CPUCLK's	PD Mode Output State Control	RW	Driven	Hi-Z	0

I²C Table: Output Control Register

Byte 2	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	-	PCICLK5	Output Control	RW	Disable	Enable	1
Bit 6	-	PCICLK4	Output Control	RW	Disable	Enable	1
Bit 5	-	PCICLK3	Output Control	RW	Disable	Enable	1
Bit 4	-	PCICLK2	Output Control	RW	Disable	Enable	1
Bit 3	-	PCICLK1	Output Control	RW	Disable	Enable	1
Bit 2	-	PCICLK0	Output Control	RW	Disable	Enable	1
Bit 1	-	PCICLK_F2	Output Control	RW	Disable	Enable	1
Bit 0	-	PCICLK_F1	Output Control	RW	Disable	Enable	1

I²C Table: Output Control Register

Byte 3	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	-	SRCCLK's	PD Mode Output State Control	RW	Driven	Hi-Z	0
Bit 6	-	CPUCLKT/C2 / SRCCLK7	Output Control	RW	Disable	Enable	1
Bit 5	-	SRCCLKT/C6	Output Control	RW	Disable	Enable	1
Bit 4	-	SRCCLKT/C5	Output Control	RW	Disable	Enable	1
Bit 3	-	SRCCLKT/C_SATA4	Output Control	RW	Disable	Enable	1
Bit 2	-	SRCCLKT/C3	Output Control	RW	Disable	Enable	1
Bit 1	-	SRCCLKT/C2	Output Control	RW	Disable	Enable	1
Bit 0	-	SRCCLKT/C1	Output Control	RW	Disable	Enable	1

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I²C Table: Output Control Register

Byte 4	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	-	PCI/SRC Stop EN	Stop all PCI / SRC clocks		Enable	Disable	1
Bit 6	-	PCICLK_F2	Stop Control	RW	Free Running	Stoppable	0
Bit 5	-	PCICLK_F1	Stop Control	RW	Free Running	Stoppable	0
Bit 4	-	PCICLK_F0	Stop Control	RW	Free Running	Stoppable	0
Bit 3	-	SRCCLKT/C (7:5)	Stop Control	RW	Free Running	Stoppable	1
Bit 2	-	SRCCLKT/C 4	Stop Control	RW	Free Running	Stoppable	1
Bit 1	-	SRCCLKT/C (3:1)	Stop Control	RW	Free Running	Stoppable	1
Bit 0	-	Reserved	Reserved	RW	-	-	1

I²C Table: Programmable Skew Control Register

Byte 5	Pin #	Name	Control Function	Type	0		1		PWD
Bit 7	-	PCISkw3	CPU-PCI 7 Steps Skew Control (ps) (Also see Table 3)	RW	0000:0	0100:150	1000:300	1100:450	0
Bit 6	-	PCISkw2		RW	0001:N/A	0101:N/A	1001:N/A	1101:600	0
Bit 5	-	PCISkw1		RW	0010:N/A	0110:N/A	1010:N/A	1110:750	0
Bit 4	-	PCISkw0		RW	0011:N/A	0111:N/A	1011:N/A	1111:900	0
Bit 3	-	ASYNC1	PCI Async Freq (see Table 6)	RW	00 = PLL1/ PLL2		10 = 37.7		0
Bit 2	-	ASYNC0		RW	01 = 33.0		11 = 44.0		0
Bit 1	-	Reserved	Reserved	RW	-		-		0
Bit 0	-	Reserved	Reserved	RW	-		-		0

I²C Table: Output Drive Control Register

Byte 6	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	-	Reserved	Reserved	RW	-	-	1
Bit 6	-	Reserved		RW	-	-	1
Bit 5	-	Reserved	Reserved	RW	-	-	1
Bit 4	-	Reserved		RW	-	-	1
Bit 3	-	Reserved	Reserved	RW	-	-	1
Bit 2	-	Reserved		RW	-	-	1
Bit 1	-	Reserved	Reserved	RW	-	-	1
Bit 0	-	Reserved		RW	-	-	1

I²C Table: Vendor ID Register

Byte 7	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	-	SRC _SOURCE	SRC comes from	RW	PLL1	PLL2	0
Bit 6	-	PCI_SOURCE	PCI comes from	RW	PLL1	PLL2	0
Bit 5	-	SRC_SATA_Source	SATA comes from	RW	PLL1	PLL2	0
Bit 4	-	PLL2 Sync	PLL2 (SATA, SRC,PCI) Synchronization	RW	Async	Sync	0
Bit 3	-	VID3	VENDOR ID	R	-	-	0
Bit 2	-	VID2		R	-	-	0
Bit 1	-	VID1		R	001 = ICS	-	0
Bit 0	-	VID0		R	-	-	1

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I²C Table: Byte Count Register

Byte 8	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	-	BC7	Byte Count Programming b(7:0)	RW	Writing to this register will configure how many bytes will be read back, default is 0F = 15 bytes.		0
Bit 6	-	BC6		RW			0
Bit 5	-	BC5		RW			0
Bit 4	-	BC4		RW			0
Bit 3	-	BC3		RW			1
Bit 2	-	BC2		RW			1
Bit 1	-	BC1		RW			1
Bit 0	-	BC0		RW			1

I²C Table: WD Time Control Register

Byte 9	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	-	WDH_EN	Watchdog Hard Alarm Enable	RW	Disable	Enable	0
Bit 6	-	WDS_EN	Watchdog Soft Alarm Enable	RW	Disable	Enable	0
Bit 5	-	WD Hard Status	WD Hard Alarm Status	R	Normal	Alarm	X
Bit 4	-	WD Soft Status	WD Soft Alarm Status	R	Normal	Alarm	X
Bit 3	-	WDTCtrl	Watch Dog Time base Control	RW	290ms Base	1160ms Base	0
Bit 2	-	WD2	WD Timer Bit 2	RW	These bits represent X*290ms (or 1.16S) the watchdog timer waits before it goes to alarm mode. Default is 7 X 290ms = 2s.		1
Bit 1	-	WD1	WD Timer Bit 1	RW			1
Bit 0	-	WD0	WD Timer Bit 0	RW			1

I²C Table: M/N Programming & WD Safe Frequency Control Register

Byte 10	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	-	M/N_EN	PLL1 M/N Programming Enable	RW	Disable	Enable	0
Bit 6	-	Reserved	Reserved	RW	-	-	0
Bit 5	-	WD Safe Freq Source	WD Safe Freq Source	RW	B10b(4:0)	Latch Inputs/B0(4:0)	0
Bit 4	-	WD SF4	Watch Dog Safe Freq Programming bits	RW	Writing to these bit will configure the safe frequency as Byte0 bit (4:0).		0
Bit 3	-	WD SF3		RW			0
Bit 2	-	WD SF2		RW			0
Bit 1	-	WD SF1		RW			0
Bit 0	-	WD SF0		RW			0

I²C Table: PLL1 Frequency Control Register

Byte 11	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	-	N Div8	N Divider Prog bit 8	RW	The decimal representation of M and N Divier in Byte 11 and 12 will configure the PLL1 VCO frequency. Default at power up = latch-in or Byte 0 Rom table. VCO Frequency = 14.318 x [NDiv(9:0)+8] / [MDiv(5:0)+2]		X
Bit 6	-	N Div9	N Divider Prog bit 9	RW			X
Bit 5	-	M Div5	M Divider Programming bit (5:0)	RW			X
Bit 4	-	M Div4		RW			X
Bit 3	-	M Div3		RW			X
Bit 2	-	M Div2		RW			X
Bit 1	-	M Div1		RW			X
Bit 0	-	M Div0		RW			X

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I²C Table: PLL1 Frequency Control Register

Byte 12	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	-	N Div7	N Divider Programming Byte12 bit(7:0) and Byte11 bit(7:6)	RW	The decimal representation of M and N Divier in Byte 11 and 12 will configure the PLL1 VCO frequency. Default at power up = latch-in or Byte 0 Rom table. VCO Frequency = 14.318 x [NDiv(9:0)+8] / [MDiv(5:0)+2]		X
Bit 6	-	N Div6		RW			X
Bit 5	-	N Div5		RW			X
Bit 4	-	N Div4		RW			X
Bit 3	-	N Div3		RW			X
Bit 2	-	N Div2		RW			X
Bit 1	-	N Div1		RW			X
Bit 0	-	N Div0		RW			X

I²C Table: PLL1 Spread Spectrum Control Register

Byte 13	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	-	SSP7	Spread Spectrum Programming bit(7:0)	RW	These Spread Spectrum bits in Byte 13 and 14 will program the spread pecentage of PLL1		X
Bit 6	-	SSP6		RW			X
Bit 5	-	SSP5		RW			X
Bit 4	-	SSP4		RW			X
Bit 3	-	SSP3		RW			X
Bit 2	-	SSP2		RW			X
Bit 1	-	SSP1		RW			X
Bit 0	-	SSP0		RW			X

I²C Table: PLL1 Spread Spectrum Control Register

Byte 14	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	-	Reserved	Reserved	R	-	-	0
Bit 6	-	SSP14	Spread Spectrum Programming bit(14:8)	RW	These Spread Spectrum bits in Byte 13 and 14 will program the spread pecentage of PLL1		X
Bit 5	-	SSP13		RW			X
Bit 4	-	SSP12		RW			X
Bit 3	-	SSP11		RW			X
Bit 2	-	SSP10		RW			X
Bit 1	-	SSP9		RW			X
Bit 0	-	SSP8		RW			X

I²C Table: PLL2 Frequency Control Register

Byte 15	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	-	N Div8	N Divider Prog bit 8	RW	The decimal representation of M and N Divier in Byte 15 and 16 will configure the PLL2 VCO frequency. Default at power up = latch-in or Byte 0 Rom table. VCO Frequency = 14.318 x [NDiv(9:0)+8] / [MDiv(5:0)+2]		X
Bit 6	-	N Div9	N Divider Prog bit 9	RW			X
Bit 5	-	M Div5	M Divider Programming bits	RW			X
Bit 4	-	M Div4		RW			X
Bit 3	-	M Div3		RW			X
Bit 2	-	M Div2		RW			X
Bit 1	-	M Div1		RW			X
Bit 0	-	M Div0		RW			X

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I²C Table: PLL2 Frequency Control Register

Byte 16	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	-	N Div7	N Divider Programming b(7:0)	RW	The decimal representation of M and N Divier in Byte 15 and 16 will configure the PLL2 VCO frequency. Default at power up = latch-in or Byte 0 Rom table. VCO Frequency = 14.318 x [NDiv(9:0)+8] / [MDiv(5:0)+2]		X
Bit 6	-	N Div6		RW			X
Bit 5	-	N Div5		RW			X
Bit 4	-	N Div4		RW			X
Bit 3	-	N Div3		RW			X
Bit 2	-	N Div2		RW			X
Bit 1	-	N Div1		RW			X
Bit 0	-	N Div0		RW			X

I²C Table: PLL2 Spread Spectrum Control Register

Byte 17	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	-	SSP7	Spread Spectrum Programming b(7:0)	RW	These Spread Spectrum bits in Byte 17 and 18 will program the spread pecentage of PLL2		X
Bit 6	-	SSP6		RW			X
Bit 5	-	SSP5		RW			X
Bit 4	-	SSP4		RW			X
Bit 3	-	SSP3		RW			X
Bit 2	-	SSP2		RW			X
Bit 1	-	SSP1		RW			X
Bit 0	-	SSP0		RW			X

I²C Table: PLL2 Spread Spectrum Control Register

Byte 18	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	-	Reserved	Reserved	R	-	-	0
Bit 6	-	SSP14	Spread Spectrum Programming b(14:8)	RW	These Spread Spectrum bits in Byte 17 and 18 will program the spread pecentage of PLL2		X
Bit 5	-	SSP13		RW			X
Bit 4	-	SSP12		RW			X
Bit 3	-	SSP11		RW			X
Bit 2	-	SSP10		RW			X
Bit 1	-	SSP9		RW			X
Bit 0	-	SSP8		RW			X

I²C Table: Programmable Output Divider Register

Byte 19	Pin #	Name	Control Function	Type	0		1		PWD
Bit 7	-	CPUDiv3	CPU Divider Ratio Programming Bits for PLL1	RW	0000:/2	0100:/4	1000:/8	1100:/16	X
Bit 6	-	CPUDiv2		RW	0001:/3	0101:/6	1001:/12	1101:/24	X
Bit 5	-	CPUDiv1		RW	0010:/5	0110:/10	1010:/20	1110:/40	X
Bit 4	-	CPUDiv0		RW	0011:/7	0111:/14	1011:/28	1111:/56	X
Bit 3	-	SRCDiv3	SRC Divider Ratio Programming Bits for PLL1	RW	0000:/2	0100:/4	1000:/8	1100:/16	X
Bit 2	-	SRCDiv2		RW	0001:/3	0101:/6	1001:/12	1101:/24	X
Bit 1	-	SRCDiv1		RW	0010:/5	0110:/10	1010:/20	1110:/40	X
Bit 0	-	SRCDiv0		RW	0011:/7	0111:/14	1011:/28	1111:/56	X

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Absolute Maximum Rating

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	Notes
3.3V Core Supply Voltage	VDD_A	-			V_{DD} + 0.5V	V	1
3.3V Logic Input Supply Voltage	VDD_In	-	GND - 0.5		V_{DD} + 0.5V	V	1
Storage Temperature	Ts	-	-65		150	˚C	1
Ambient Operating Temp	Tambient	-	0		70	ºC	1
Case Temperature	Tcase	-			115	ºC	1
Input ESD protection HBM	ESD prot	-	2000			V	1

[1]Guaranteed by design and characterization, not 100% tested in production.

Electrical Characteristics - Input/Supply/Common Output Parameters

PARAMETER	SYMBOL	CONDITIONS*	MIN	TYP	MAX	UNITS	Notes
Input High Voltage	V_{IH}	3.3 V +/-5%	2		V_{DD} + 0.3	V	1
Input Low Voltage	V_{IL}	3.3 V +/-5%	V_{SS} - 0.3		0.8	V	1
Input High Current	I_{IH}	$V_{IN} = V_{DD}$	-5		5	uA	1
Input Low Current	I_{IL1}	V_{IN} = 0 V; Inputs with no pull-up resistors	-5			uA	1
	I_{IL2}	V_{IN} = 0 V; Inputs with pull-up resistors	-200			uA	1
Low Threshold Input-High Voltage	V_{IH_FSL}	3.3 V +/-5%	0.7		V_{DD} + 0.3	V	1
Low Threshold Input-Low Voltage	V_{IL_FSL}	3.3 V +/-5%	V_{SS} - 0.3		0.35	V	1
Operating Supply Current	$I_{DD3.3OP}$	Full Active, C_L = Full load;			350	mA	1
Operating Current	$I_{DD3.3OP}$	all outputs driven			400	mA	1
Powerdown Current	$I_{DD3.3PD}$	all diff pairs driven			70	mA	1
		all differential pairs tri-stated			12	mA	1
Input Frequency	F_i	V_{DD} = 3.3 V		14.31818		MHz	2
Pin Inductance	L_{pin}				7	nH	1
Input Capacitance	C_{IN}	Logic Inputs			5	pF	1
	C_{OUT}	Output pin capacitance			6	pF	1
	C_{INX}	X1 & X2 pins			5	pF	1
Clk Stabilization	T_{STAB}	From V_{DD} Power-Up or de-assertion of PD# to 1st clock			1.8	ms	1
Modulation Frequency		Triangular Modulation	30		33	kHz	1
Tdrive_PD#		CPU output enable after PD# de-assertion			300	us	1
Tfall_Pd#		PD# fall time of			5	ns	1
Trise_Pd#		PD# rise time of			5	ns	1
SMBus Voltage	V_{DD}		2.7		5.5	V	1
Low-level Output Voltage	V_{OL}	@ I_{PULLUP}			0.4	V	1
Current sinking at V_{OL} = 0.4 V	I_{PULLUP}		4			mA	1
SCLK/SDATA Clock/Data Rise Time	T_{RI2C}	(Max VIL - 0.15) to (Min VIH + 0.15)			1000	ns	1
SCLK/SDATA Clock/Data Fall Time	T_{FI2C}	(Min VIH + 0.15) to (Max VIL - 0.15)			300	ns	1

*TA = 0 - 70°C; Supply Voltage VDD = 3.3 V +/-5%

[1]Guaranteed by design and characterization, not 100% tested in production.

[2] Input frequency should be measured at the REF pin and tuned to ideal 14.31818MHz to meet ppm frequency accuracy on PLL outputs.

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Electrical Characteristics - CPUCLKT/C -- 0.7V Current Mode Differential Pair

PARAMETER	SYMBOL	CONDITIONS*	MIN	TYP	MAX	UNITS	NOTES
Current Source Output Impedance	Zo	$V_O = V_x$	3000			Ω	1
Voltage High	VHigh	Statistical measurement on single ended signal	660		850	mV	1,3
Voltage Low	VLow		-150		150	mV	1,3
Max Voltage	Vovs	Measurement on single ended signal using absolute value.			1150	mV	1
Min Voltage	Vuds		-300			mV	1
Crossing Voltage (abs)	Vx(abs)		250		550	mV	1
Crossing Voltage (var)	d-Vx	Variation of crossing over all edges			140	mV	1
Long Accuracy	ppm	see Tperiod min-max values	-300		300	ppm	1,2
Average period	Tperiod	400MHz nominal	2.4993		2.5008	ns	2
		400MHz spread	2.4993		2.5133	ns	2
		333.33MHz nominal	2.9991		3.0009	ns	2
		333.33MHz spread	2.9991		3.016	ns	2
		266.66MHz nominal	3.7489		3.7511	ns	2
		266.66MHz spread	3.7489		3.77	ns	2
		200MHz nominal	4.9985		5.0015	ns	2
		200MHz spread	4.9985		5.0266	ns	2
		166.66MHz nominal	5.9982		6.0018	ns	2
		166.66MHz spread	5.9982		6.0320	ns	2
		133.33MHz nominal	7.4978		7.5023	ns	2
		133.33MHz spread	7.4978		7.5400	ns	2
		100.00MHz nominal	9.9970		10.0030	ns	2
		100.00MHz spread	9.9970		10.0533	ns	2
Absolute min period	T_{absmin}	400MHz nominal/spread	2.4143			ns	1,2
		333.33MHz nominal/spread	2.9141			ns	1,2
		266.66MHz nominal/spread	3.6639			ns	1,2
		200MHz nominal/spread	4.8735			ns	1,2
		166.66MHz nominal/spread	5.8732			ns	1,2
		133.33MHz nominal/spread	7.3728			ns	1,2
		100.00MHz nominal/spread	9.8720			ns	1,2
Rise Time	t_r	V_{OL} = 0.175V, V_{OH} = 0.525V	175		700	ps	1
Fall Time	t_f	V_{OH} = 0.525V V_{OL} = 0.175V	175		700	ps	1
Rise Time Variation	d-t_r	V_{OL} = 0.175V, V_{OH} = 0.525V			125	ps	1
Fall Time Variation	d-t_f	V_{OH} = 0.525V V_{OL} = 0.175V			125	ps	1
Duty Cycle	d_{t3}	Measurement from differential wavefrom	45		55	%	1
Skew	t_{sk3}	CPU(1:0), V_T = 50%			100	ps	1
Skew	t_{sk4}	CPU(1:0) to CPU2_ITP, V_T = 50%			150	ps	1
Jitter, Cycle to cycle	$t_{jcyc-cyc}$	Measurement from differential wavefrom (CPU2_ITP)			125	ps	1
Jitter, Cycle to cycle	$t_{jcyc-cyc}$	Measurement from differential wavefrom, (CPU(1:0))			85	ps	1

*T_A = 0 - 70°C; V_{DD} = 3.3 V +/-5%; C_L =2pF, R_S=33.2Ω, R_P=49.9Ω, I_{REF} = 475Ω

[1]Guaranteed by design and characterization, not 100% tested in production.

[2] All Long Term Accuracy and Clock Period specifications are guaranteed assuming that REFOUT is at 14.31818MHz

[3]$I_{REF} = V_{DD}/(3xR_R)$. For R_R = 475Ω (1%), I_{REF} = 2.32mA. I_{OH} = 6 x I_{REF} and V_{OH} = 0.7V @ Z_O=50Ω.

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Electrical Characteristics - SRC/SATA/PCIEX 0.7V Current Mode Differential Pair

PARAMETER	SYMBOL	CONDITIONS*	MIN	TYP	MAX	UNITS	Notes
Current Source Output Impedance	Zo	$V_O = V_x$	3000			Ω	1
Voltage High	VHigh	Statistical measurement on single ended signal	660		850	mV	1,3
Voltage Low	VLow		-150		150	mV	1,3
Max Voltage	Vovs	Measurement on single ended signal using absolute value.			1150	mV	1
Min Voltage	Vuds		-300			mV	1
Crossing Voltage (abs)	Vx(abs)		250		550	mV	1
Crossing Voltage (var)	d-Vx	Variation of crossing over all edges			140	mV	1
Long Accuracy	ppm	see Tperiod min-max values	-300		300	ppm	1,2
Average period	Tperiod	100.00MHz nominal	9.9970		10.0030	ns	2
		100.00MHz spread	9.9970		10.0533	ns	2
Absolute min period	Tabsmin	100.00MHz nominal/spread	9.8720			ns	1,2
Rise Time	t_r	V_{OL} = 0.175V, V_{OH} = 0.525V	175		700	ps	1
Fall Time	t_f	V_{OH} = 0.525V V_{OL} = 0.175V	175		700	ps	1
Rise Time Variation	d-t_r	V_{OL} = 0.175V, V_{OH} = 0.525V			125	ps	1
Fall Time Variation	d-t_f	V_{OH} = 0.525V V_{OL} = 0.175V			125	ps	1
Duty Cycle	d_{t3}	Measurement from differential wavefrom	45		55	%	1
Skew	t_{sk3}	V_T = 50%			250	ps	1
Jitter, Cycle to cycle	$t_{jcyc-cyc}$	Measurement from differential wavefrom			125	ps	1

*T_A = 0 - 70°C; V_{DD} = 3.3 V +/-5%; C_L =2pF, R_S=33.2Ω, R_P=49.9Ω, I_{REF} = 475Ω

[1]Guaranteed by design and characterization, not 100% tested in production.

[2] All Long Term Accuracy and Clock Period specifications are guaranteed assuming that REFOUT is at 14.31818MHz

[3]$I_{REF} = V_{DD}/(3xR_R)$. For R_R = 475Ω (1%), I_{REF} = 2.32mA. I_{OH} = 6 x I_{REF} and V_{OH} = 0.7V @ Z_O=50Ω.

Electrical Characteristics - PCICLK/PCICLK_F

PARAMETER	SYMBOL	CONDITIONS*	MIN	TYP	MAX	UNITS	NOTES
Output Impedance	R_{DSP}	$V_O = V_{DD}$*(0.5)	12		55	Ω	1
Output High Voltage	V_{OH}	I_{OH} = -1 mA	2.4			V	1
Output Low Voltage	V_{OL}	I_{OL} = 1 mA			0.55	V	1
Output High Current	I_{OH}	V_{OH} @MIN = 1.0 V	-33			mA	1
		V_{OH}@MAX = 3.135 V			-33	mA	1
Output Low Current	I_{OL}	V_{OL} @ MIN = 1.95 V	30			mA	1
		V_{OL} @ MAX = 0.4 V			38	mA	1
Edge Rate	$t_{slewr/f}$	Rising/Falling edge rate	1		4	V/ns	1
Rise Time	t_r	V_{OL} = 0.4 V, V_{OH} = 2.4 V	0.5		2	ns	1
Fall Time	t_f	V_{OH} = 2.4 V, V_{OL} = 0.4 V	0.5		2	ns	1
Duty Cycle	d_{t1}	V_T = 1.5 V	45		55	%	1
Group Skew	t_{skew}	V_T = 1.5 V			500	ps	1
Jitter, Cycle to cycle	$t_{jcyc-cyc}$	V_T = 1.5 V			250	ps	1

*TA = 0 - 70°C; Supply Voltage VDD = 3.3 V +/-5%, CL = 4 pF with Rs = 33Ω (unless otherwise specified)

[1]Guaranteed by design and characterization, not 100% tested in production.

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Electrical Characteristics - 48MHz/USB48MHz/24_48MHz

PARAMETER	SYMBOL	CONDITIONS*	MIN	TYP	MAX	UNITS	NOTES
Long Accuracy	ppm	see Tperiod min-max values	-100		100	ppm	1
Clock period	T_{period}	48.00MHz output nominal	20.8313		20.8354	ns	
Output Impedance	R_{DSP}	$V_O = V_{DD}*(0.5)$	12		55	Ω	1
Output High Voltage	V_{OH}	I_{OH} = -1 mA	2.4			V	1
Output Low Voltage	V_{OL}	I_{OL} = 1 mA			0.55	V	1
Output High Current	I_{OH}	V_{OH} @MIN = 1.0 V	-33			mA	1
		V_{OH}@MAX = 3.135 V			-33	mA	1
Output Low Current	I_{OL}	V_{OL} @ MIN = 1.95 V	30			mA	1
		V_{OL} @ MAX = 0.4 V			38	mA	1
Edge Rate	$t_{slewr/f}$	Rising/Falling edge rate	1		4	V/ns	1
Edge Rate	t_{slewr/f_USB}	USB48 Rising/Falling edge rate	1		2	V/ns	1
Rise Time	t_r	V_{OL} = 0.4 V, V_{OH} = 2.4 V	0.5		2	ns	1
Fall Time	t_f	V_{OH} = 2.4 V, V_{OL} = 0.4 V	0.5		2	ns	1
Rise Time	t_{r_USB}	V_{OL} = 0.4 V, V_{OH} = 2.4 V	1		2	ns	1
Fall Time	t_{f_USB}	V_{OH} = 2.4 V, V_{OL} = 0.4 V	1		2	ns	1
Duty Cycle	d_{t1}	V_T = 1.5 V	45		55	%	1
Jitter, Cycle to cycle	$t_{jcyc-cyc}$	V_T = 1.5 V			500	ps	1

*TA = 0 - 70°C; Supply Voltage VDD = 3.3 V +/-5%, CL = 4 pF with Rs = 33Ω (Rs is used in USB48MHz test only)

[1]Guaranteed by design and characterization, not 100% tested in production.

Electrical Characteristics - DOT_96MHz 0.7V Current Mode Differential Pair

PARAMETER	SYMBOL	CONDITIONS*	MIN	TYP	MAX	UNITS	Notes
Current Source Output Impedance	Zo	$V_O = V_x$	3000			Ω	1
Voltage High	VHigh	Statistical measurement on single ended signal	660		850	mV	1,3
Voltage Low	VLow		-150		150	mV	1,3
Max Voltage	Vovs	Measurement on single ended signal using absolute value.			1150	mV	1
Min Voltage	Vuds		-300			mV	1
Crossing Voltage (abs)	Vx(abs)		250		550	mV	1
Crossing Voltage (var)	d-Vcross	Variation of crossing over all edges			140	mV	1
Long Accuracy	ppm	see Tperiod min-max values	-100		100	ppm	1,2
Average period	Tperiod	96.00MHz nominal	10.4135		10.4198	ns	2
Absolute min period	Tabsmin	96.00MHz nominal	10.1635			ns	1,2
Rise Time	t_r	V_{OL} = 0.175V, V_{OH} = 0.525V	175		700	ps	1
Fall Time	t_f	V_{OH} = 0.525V V_{OL} = 0.175V	175		700	ps	1
Rise Time Variation	d-t_r	V_{OL} = 0.175V, V_{OH} = 0.525V			125	ps	1
Fall Time Variation	d-t_f	V_{OH} = 0.525V V_{OL} = 0.175V			125	ps	1
Duty Cycle	d_{t3}	Measurement from differential wavefrom	45		55	%	1
Jitter, Cycle to cycle	$t_{jcyc-cyc}$	Measurement from differential wavefrom			250	ps	1

*T_A = 0 - 70°C; V_{DD} = 3.3 V +/-5%; C_L =2pF, R_S=33.2Ω, R_P=49.9Ω, I_{REF} = 475Ω

[1]Guaranteed by design and characterization, not 100% tested in production.

[2] All Long Term Accuracy and Clock Period specifications are guaranteed assuming that REFOUT is at 14.31818MHz

[3]$I_{REF} = V_{DD}/(3xR_R)$. For R_R = 475Ω (1%), I_{REF} = 2.32mA. I_{OH} = 6 x I_{REF} and V_{OH} = 0.7V @ Z_O=50Ω.

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Electrical Characteristics - REF-14.318MHz

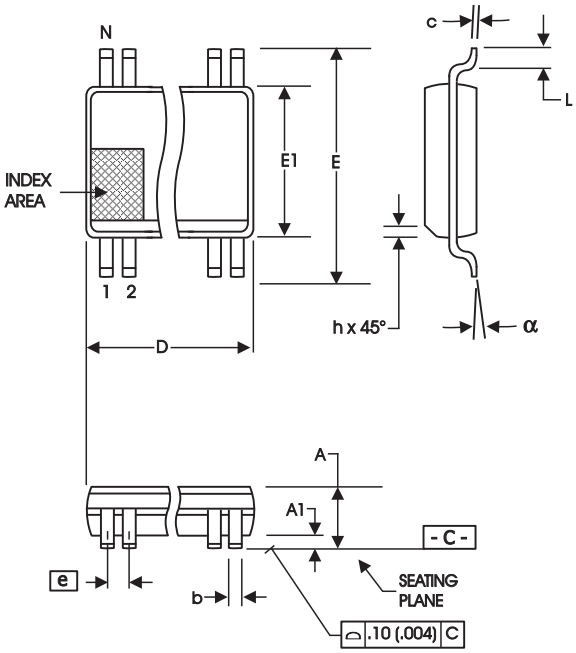
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	Notes
Long Accuracy	ppm	see Tperiod min-max values	-300		300	ppm	1,2
Clock period	T_{period}	14.318MHz output nominal	69.8270		69.8550	ns	2
Output High Voltage	V_{OH}	I_{OH} = -1 mA	2.4			V	1
Output Low Voltage	V_{OL}	I_{OL} = 1 mA			0.4	V	1
Output High Current	I_{OH}	V_{OH}@MIN = 1.0 V, V_{OH}@MAX = 3.135 V	-29		-23	mA	1
Output Low Current	I_{OL}	V_{OL} @MIN = 1.95 V, V_{OL} @MAX = 0.4 V	29		27	mA	1
Edge Rate	$t_{slewr/f}$	Rising/Falling edge rate	1		4	V/ns	1
Rise Time	t_{r1}	V_{OL} = 0.4 V, V_{OH} = 2.4 V	1		2	ns	1
Fall Time	t_{f1}	V_{OH} = 2.4 V, V_{OL} = 0.4 V	1		2	ns	1
Duty Cycle	d_{t1}	V_T = 1.5 V	45		55	%	1
Jitter	$t_{jcyc-cyc}$	V_T = 1.5 V			1000	ps	1

*TA = 0 - 70°C; Supply Voltage VDD = 3.3 V +/-5%, CL = 4 pF with Rs = 39Ω (Rs is used in USB48MHz test only)

[1]Guaranteed by design and characterization, not 100% tested in production.

[2] All Long Term Accuracy and Clock Period specifications are guaranteed assuming that REFOUT is at 14.31818MHz

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56-Lead, 300 mil Body, 25 mil, SSOP

SYMBOL	In Millimeters COMMON DIMENSIONS		In Inches COMMON DIMENSIONS	
	MIN	MAX	MIN	MAX
A	2.41	2.80	.095	.110
A1	0.20	0.40	.008	.016
b	0.20	0.34	.008	.0135
c	0.13	0.25	.005	.010
D	SEE VARIATIONS		SEE VARIATIONS	
E	10.03	10.68	.395	.420
E1	7.40	7.60	.291	.299
e	0.635 BASIC		0.025 BASIC	
h	0.38	0.64	.015	.025
L	0.50	1.02	.020	.040
N	SEE VARIATIONS		SEE VARIATIONS	
a	0°	8°	0°	8°

VARIATIONS

N	D mm.		D (inch)	
	MIN	MAX	MIN	MAX
56	18.31	18.55	.720	.730

Reference Doc.: JEDEC Publication 95, MO-118

10-0034

Ordering Information

954141AFLF-T

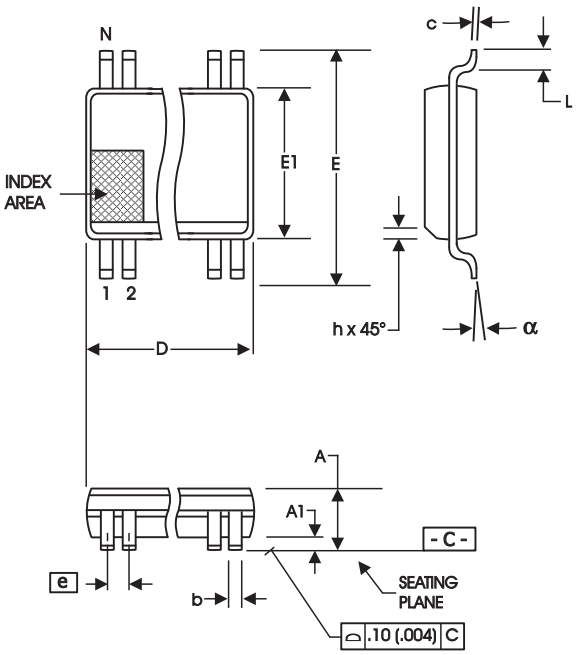
Example:

XXXX A **F** **LF- T**

- **Designation for tape and reel packaging**
- **Annealed Lead Free (Optional)**
- **Package Type**
  F = SSOP
- **Revision Designator** (will not correlate with datasheet revision)
- **Device Type**

0934A—03/30/09

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56-Lead 6.10 mm. Body, 0.50 mm. Pitch TSSOP
(240 mil) (20 mil)

SYMBOL	In Millimeters COMMON DIMENSIONS		In Inches COMMON DIMENSIONS	
	MIN	MAX	MIN	MAX
A	--	1.20	--	.047
A1	0.05	0.15	.002	.006
A2	0.80	1.05	.032	.041
b	0.17	0.27	.007	.011
c	0.09	0.20	.0035	.008
D	SEE VARIATIONS		SEE VARIATIONS	
E	8.10 BASIC		0.319 BASIC	
E1	6.00	6.20	.236	.244
e	0.50 BASIC		0.020 BASIC	
L	0.45	0.75	.018	.030
N	SEE VARIATIONS		SEE VARIATIONS	
a	0°	8°	0°	8°
aaa	--	0.10	--	.004

VARIATIONS

N	D mm.		D (inch)	
	MIN	MAX	MIN	MAX
56	13.90	14.10	.547	.555

Reference Doc.: JEDEC Publication 95, MO-153

10-0039

Ordering Information

954141AGLF-T

Example:

XXXX A **G** **LF- T**

- **Designation for tape and reel packaging**
- **Annealed Lead Free (Optional)**
- **Package Type**
  G = TSSOP
- **Revision Designator** (will not correlate with datasheet revision)
- **Device Type**

0934A—03/30/09

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Revision History

Rev.	Issue Date	Description	Page #
N/A	10/13/2004	Added TSSOP ordering information	18
A	3/30/2009	1. Corrected single-ended clock loading. 2. Updated part ordering information. 3. Removed water marks. 4. Moved to final.	Various

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