2.5V Single-Ended to SSTL_2 Clock Driver (45MHz - 233MHz)

Recommended Application:

Single-ended clock input with zero delay board fan out

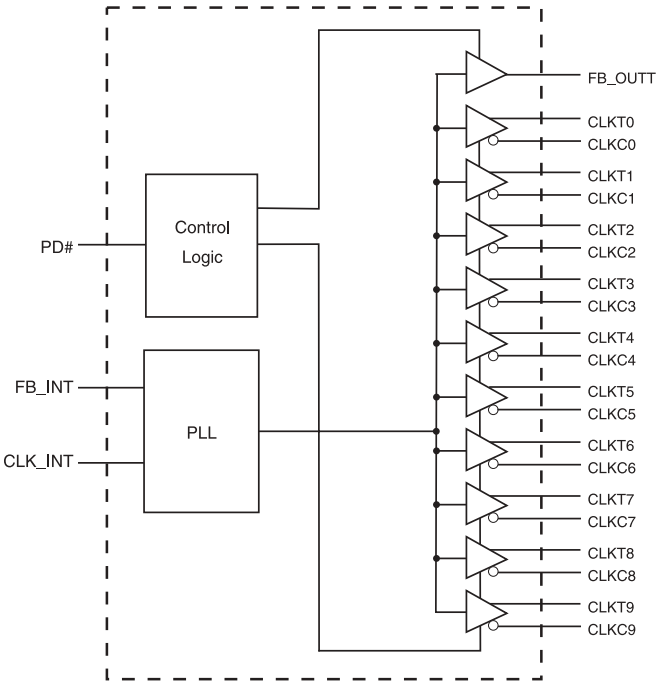
Product Description/Features:

- Low skew, low jitter PLL clock driver
- 1 to 10 differential clock distribution (SSTL_2)
- Feedback pin for input to output synchronization
- PD# for power management
- Spread Spectrum tolerant inputs

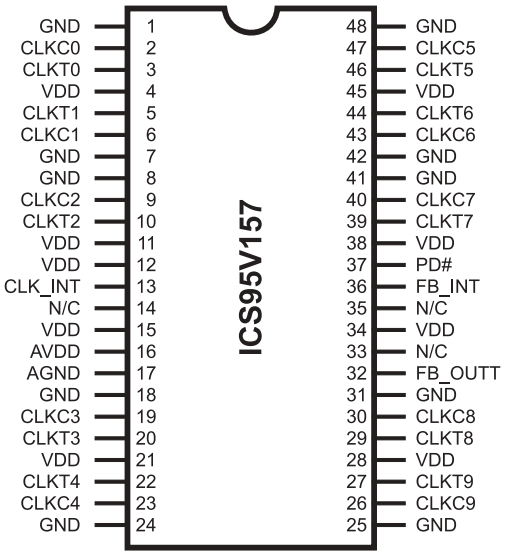
Switching Characteristics:

- CYCLE - CYCLE jitter: <60ps
- OUTPUT - OUTPUT skew: <60ps
- Period jitter: ±30ps
- DUTY CYCLE: 49.5% - 50.5%

Block Diagram



Pin Configuration



48-Pin TSSOP

6.10 mm. Body, 0.50 mm. pitch = TSSOP

Functionality

INPUTS			OUTPUTS			PLL State
AVDD	PD#	CLK_INT	CLKT	CLKC	FB_OUTT	
GND	H	L	L	H	L	Bypassed/off
GND	H	H	H	L	H	Bypassed/off
2.5V (nom)	L	L	Z	Z	Z	off
2.5V (nom)	L	H	Z	Z	Z	off
2.5V (nom)	H	L	L	H	L	on
2.5V (nom)	H	H	H	L	H	on

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Pin Descriptions

PIN NUMBER	PIN NAME	TYPE	DESCRIPTION
4, 11, 12, 15, 21, 28, 34, 38, 45,	VDD	PWR	Power supply, 2.5V
1, 7, 8, 18, 24, 25, 31, 41, 42, 48	GND	PWR	Ground
16	AVDD	PWR	Analog power supply, 2.5V
17	AGND	PWR	Analog ground
27, 29, 39, 44, 46, 22, 20, 10, 5, 3	CLKT[9:0]	OUT	"True" Clock of differential pair outputs
26, 30, 40, 43, 47, 23, 19, 9, 6, 2	CLKC[9:0]	OUT	"Complementary" clocks of differential pair outputs
13	CLK_INT	IN	"True" reference clock input
32	FB_OUTT	OUT	"True" " Feedback output, dedicated for external feedback. It switches at the same frequency as the CLK. This output must be wired to FB_INT
36	FB_INT	IN	"True" Feedback input, provides feedback signal to the internal PLL for synchronization with CLK_INT to eliminate phase error
14, 33, 35	N/C	-	Not connected
37	PD#	IN	Power Down. LVCMOS input

This PLL Clock Buffer is designed for a V_{DD} of 2.5V, an AV_{DD} of 2.5V and differential data input and output levels.

ICS95V157 is a zero delay buffer that distributes a single-ended clock input (CLK_INT) to ten differential pair of clock outputs (CLKT[0:9], CLKC[0:9]) and one single-ended feedback clock output (FB_OUTT). The clock outputs are controlled by the input clocks (CLK_INT), the feedback clock (FB_INT), the 2.5-V LVCMOS input (PD#) and the analog power input (AV_{DD}). When input (PD#) is low while power is applied, the receivers are disabled, the PLL is turned off and the differential clock outputs are tri-stated. When AV_{DD} is grounded, the PLL is turned off and bypassed for test purposes.

The PLL in the **ICS95V157** clock driver uses the input clocks (CLK_INT) and the feedback clock (FB_INT) to provide high-performance, low-skew, low-jitter, output differential clocks (CLKT [0:9], CLKC [0:9]). **ICS95V157** is also able to track Spread Spectrum Clock (SSC) for reduced EMI.

ICS95V157 is characterized for operation from 0°C to 85°C.

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Absolute Maximum Ratings

Supply Voltage (VDD & AVDD) . . . . . -0.5V to 4.6V
Logic Inputs . . . . . GND –0.5 V to V_{DD} + 0.5 V
Ambient Operating Temperature . . . . . 0°C to +85°C
Storage Temperature . . . . . –65°C to +150°C

Stresses above those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only and functional operation of the device at these or any other conditions above those listed in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Electrical Characteristics - Input/Supply/Common Output Parameters

T_A = 0 - 85°C; Supply Voltage A_{VDD}, V_{DD} = 2.5 V +/- 0.2V (unless otherwise stated)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input High Current	I_{IH}	$V_I = V_{DD}$ or GND	5			µA
Input Low Current	I_{IL}	$V_I = V_{DD}$ or GND			5	µA
Operating Supply Current	$I_{DD2.5}$	C_L = 0pf @ 200MHz			148	mA
	I_{DDPD}	C_L = 0pf			100	µA
High Impedance Output Current	I_{OZ}	V_{DD} = 2.7V, Vout = V_{DD} or GND			±10	mA
Input Clamp Voltage	V_{IK}	V_{DD} = 2.3V Iin = -18mA			-1.2	V
High-level output voltage	V_{OH}	I_{OH} = -1 mA	V_{DD} - 0.1			V
		I_{OH} = -12 mA	1.7V			V
Low-level output voltage	V_{OL}	I_{OL} =1 mA			0.1	V
		I_{OH} =12 mA			0.6	V
Input Capacitance[1]	C_{IN}	V_I = GND or V_{DD}	2.5		3.5	pF

[1]Guaranteed by design at 233MHz, not 100% tested in production.

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Recommended Operating Condition (see note1)

T_A = 0 - 85°C; Supply Voltage AVDD, VDD = 2.5 V +/- 0.2V (unless otherwise stated)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Voltage	V_{DD}, A_{VDD}		2.3	2.5	2.7	V
Low level input voltage	V_{IL}	CLK_INT, FB_INT		0.4	V_{DD}/2 - 0.18	V
		PD#	-0.3		0.7	V
High level input voltage	V_{IH}	CLK_INT, FB_INT	V_{DD}/2 + 0.18	2.1		V
		PD#	1.7		V_{DD} + 0.6	V
DC input signal voltage (note 2)	V_{IN}		-0.3		V_{DD} + 0.3	V
Output differential cross-voltage (note 4)	V_{OX}		V_{DD}/2 - 0.15		V_{DD}/2 + 0.15	V
High level output current	I_{OH}				-6.4	mA
Low level output current	I_{OL}				5.5	mA
Operating free-air temperature	T_A		0		85	°C

Notes:

1. Unused inputs must be held high or low to prevent them from floating.
2. DC input signal voltage specifies the allowable DC execution of differential input.
3. Differential inputs signal voltages specifies the differential voltage [VTR-VCP] required for switching, where VT is the true input level and VCP is the complementary input level.
4. Differential cross-point voltage is expected to track variations of V_{DD} and is the voltage at which the differential signal must be crossing.

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Timing Requirements

T_A = 0 - 85°C; Supply Voltage A_{VDD}, V_{DD} = 2.5 V +/- 0.2V (unless otherwise stated)

PARAMETER	SYMBOL	CONDITIONS	MIN	MAX	UNITS
Max clock frequency	$freq_{op}$	2.5V±0.2V @ 25°C	45	233	MHz
Application Frequency Range	$freq_{App}$	2.5V±0.2V @ 25°C	95	210	MHz
Input clock duty cycle	d_{tin}		40	60	%
CLK stabilization	T_{STAB}			15	µs

Switching Characteristics (see note 3)

PARAMETER	SYMBOL	CONDITION	MIN	TYP	MAX	UNITS
Low-to high level propagation delay time	t_{PLH}[1]	CLK_IN to any output		5.5		ns
High-to low level propagation delay time	t_{PLL}[1]	CLK_IN to any output		5.5		ns
Output enable time	t_{EN}	PD# to any output		5		ns
Output disable time	tdis	PD# to any output		5		ns
Period jitter	$T_{jit\ (per)}$	100MHz to 200MHz	-30		30	ps
Half-period jitter	t(jit_hper)	100MHz to 200MHz	-75		30	ps
Input clock slew rate	$t_{sl(i)}$		1		4	V/ns
Output clock slew rate	$t_{sl(o)}$		1		2.5	V/ns
Cycle to Cycle Jitter[1]	T_{cyc}-T_{cyc}	100MHz to 200MHz			60	ps
Phase error	$t_{(phase\ error)}$[4]		-50	0	50	ps
Output to Output Skew	T_{skew}				60	ps

Notes:

1. Refers to transition on noninverting output in PLL bypass mode.
2. While the pulse skew is almost constant over frequency, the duty cycle error increases at higher frequencies. This is due to the formula: duty cycle=t_{wH}/t_c, where the cycle (t_c) decreases as the frequency goes up.
3. Switching characteristics guaranteed for application frequency range.
4. Static phase offset shifted by design.

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Parameter Measurement Information

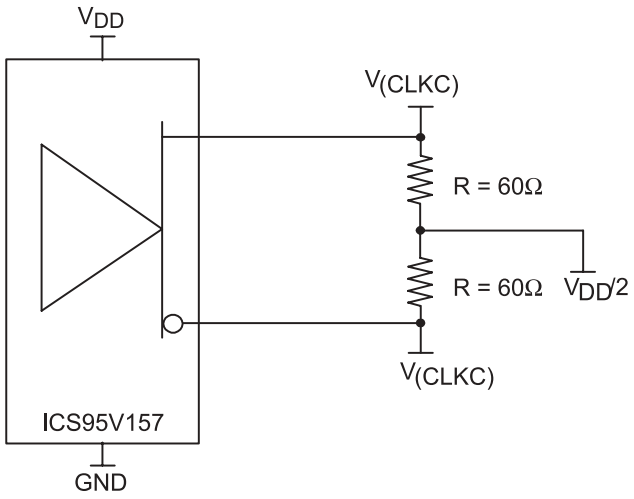
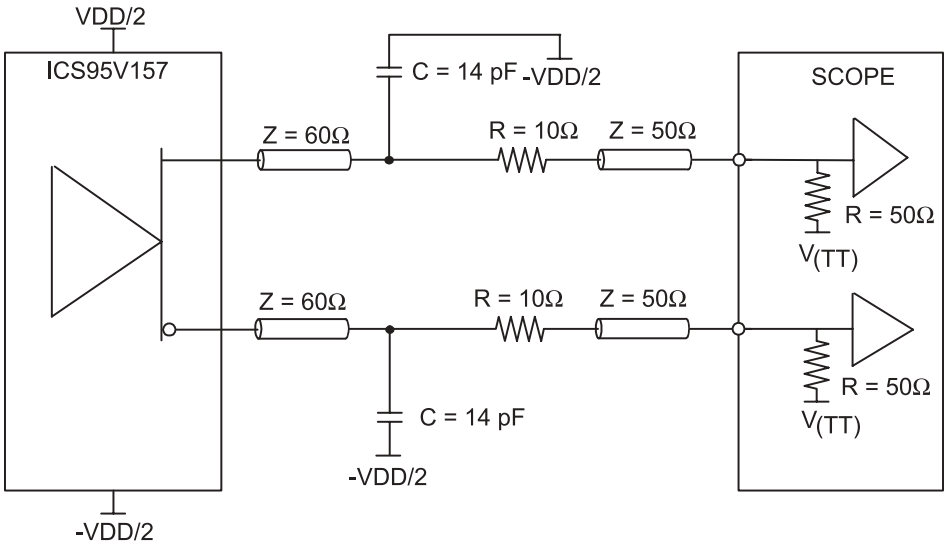
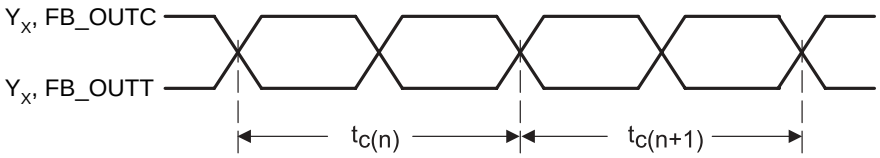


Figure 1. IBIS Model Output Load



NOTE: $V_{(TT)}$ = GND

Figure 2. Output Load Test Circuit



$$t_{jit(cc)} = t_{c(n)} \pm t_{c(n+1)}$$

Figure 3. Cycle-to-Cycle Jitter

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Parameter Measurement Information

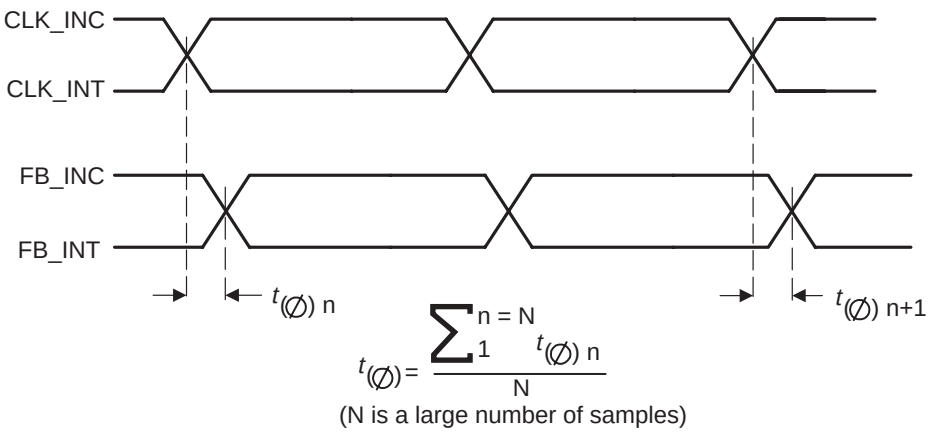


Figure 4. Static Phase Offset

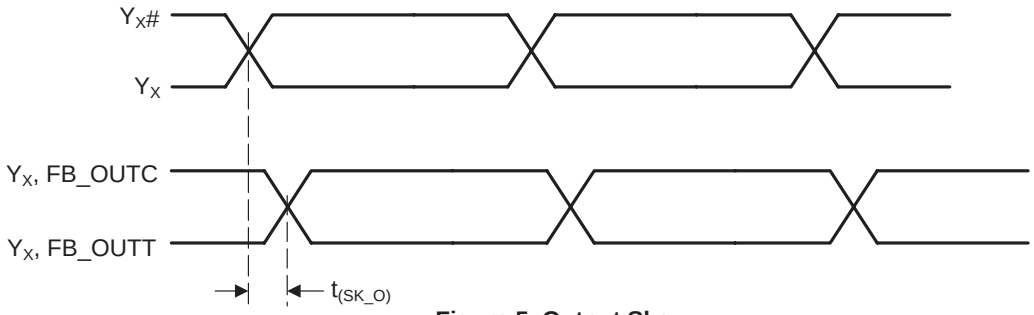


Figure 5. Output Skew

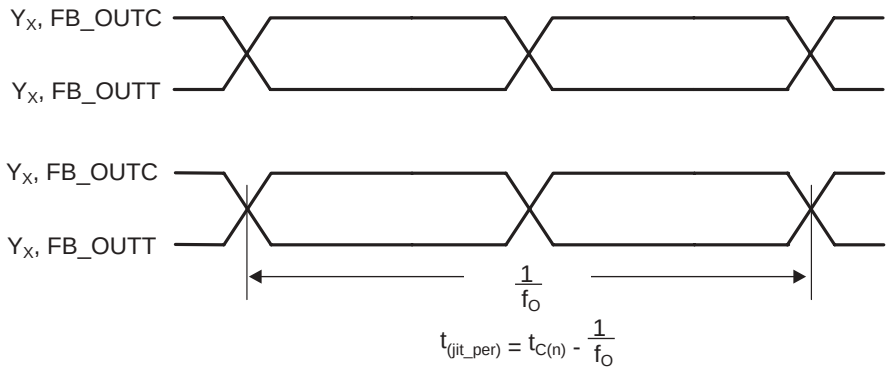


Figure 6. Period Jitter

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Parameter Measurement Information

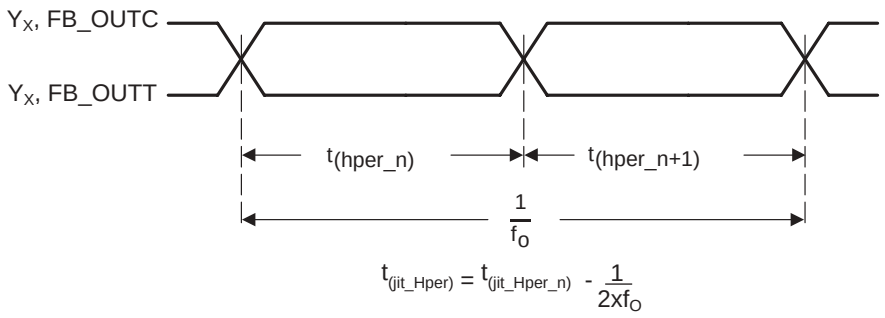


Figure 7. Half-Period Jitter

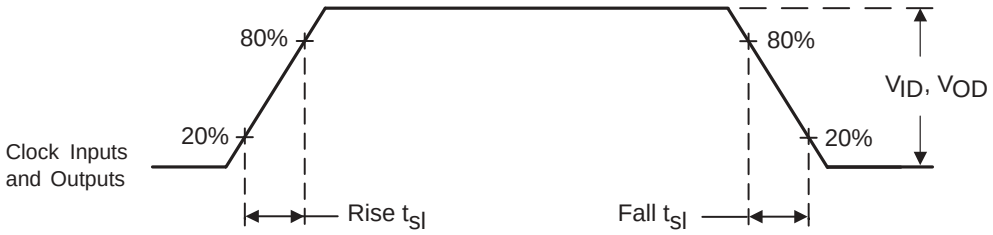
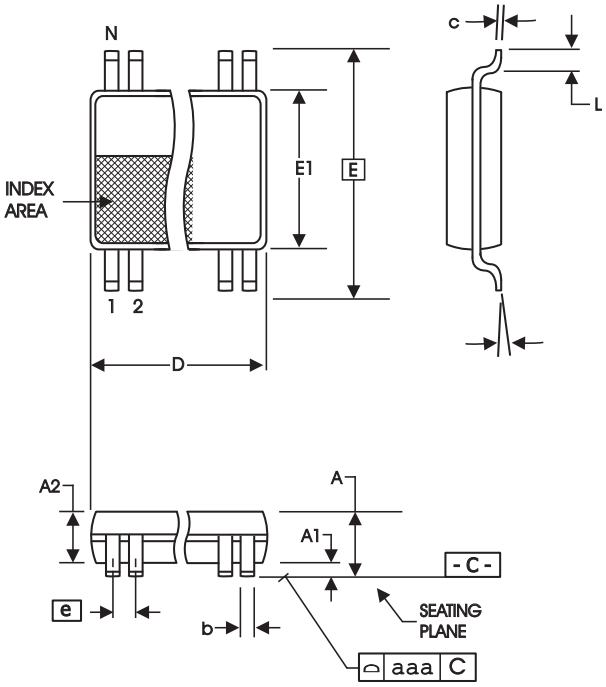


Figure 8. Input and Output Slew Rates

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SYMBOL	In Millimeters COMMON DIMENSIONS		In Inches COMMON DIMENSIONS	
	MIN	MAX	MIN	MAX
A	--	1.20	--	.047
A1	0.05	0.15	.002	.006
A2	0.80	1.05	.032	.041
b	0.17	0.27	.007	.011
c	0.09	0.20	.0035	.008
D	SEE VARIATIONS		SEE VARIATIONS	
E	8.10 BASIC		0.319 BASIC	
E1	6.00	6.20	.236	.244
e	0.50 BASIC		0.020 BASIC	
L	0.45	0.75	.018	.030
N	SEE VARIATIONS		SEE VARIATIONS	
α	0°	8°	0°	8°
aaa	--	0.10	--	.004

VARIATIONS

N	D mm.		D (inch)	
	MIN	MAX	MIN	MAX
48	12.40	12.60	.488	.496

Reference Doc.: JEDEC Publication 95, MO-153

10-0039

6.10 mm. Body, 0.50 mm. pitch TSSOP
(240 mil) (20 mil)

Ordering Information

95V157yG - T

Example:

XXXX y **G - T**

- **Designation for tape and reel packaging**
- **Package Type**
  G = TSSOP
- **Revision Designator** (will not correlate with datasheet revision)
- **Device Type**

0501C—11/24/08

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