2.5V Wide Range Frequency Clock Driver (45MHz - 233MHz)

Recommended Application:

- Zero Delay Board Fan Out, SO-DIMM
- Provides complete DDR registered DIMM solution with ICSSSTV16857, ICSSSTV16859 or ICSSSTV32852

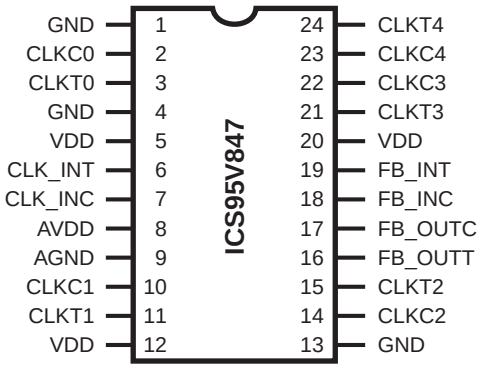
Product Description/Features:

- Low skew, low jitter PLL clock driver
- 1 to 5 differential clock distribution (SSTL_2)
- Feedback pins for input to output synchronization
- Spread Spectrum tolerant inputs

Switching Characteristics:

- CYCLE - CYCLE jitter: <60ps
- OUTPUT - OUTPUT skew: <60ps
- Period jitter: ±30ps
- DUTY CYCLE: 49.5% - 50.5%

Pin Configuration



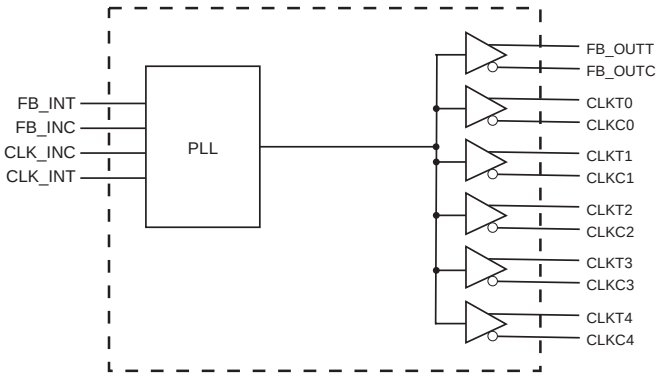
24-Pin TSSOP

4.40 mm. Body, 0.65 mm. pitch

Functionality

INPUTS			OUTPUTS				PLL State
AVDD	CLK_INT	CLK_INC	CLKT	CLKC	FB_OUTT	FB_OUTC	
GND	L	H	L	H	L	H	Bypassed/off
GND	H	L	H	L	H	L	Bypassed/off
2.5V (nom)	L	H	L	H	L	H	on
2.5V (nom)	H	L	H	L	H	L	on

Block Diagram



© 2019 Renesas Electronics Corporation

Pin Descriptions

PIN NUMBER	PIN NAME	TYPE	DESCRIPTION
5, 12, 20	VDD	PWR	Power supply, 2.5V
1, 4, 13	GND	PWR	Ground
8	AVDD	PWR	Analog power supply, 2.5V
9	AGND	PWR	Analog ground
3, 11, 15, 21, 24	CLKT[0:4]	OUT	"True" Clock of differential pair outputs
2, 10, 14, 22, 23	CLKC[0:4]	OUT	"Complementary" clocks of differential pair outputs
6	CLK_INT	IN	"True" reference clock input
7	CLK_INC	IN	"Complementary" reference clock input
16	FB_OUTT	OUT	"True" " Feedback output, dedicated for external feedback. It switches at the same frequency as the CLK. This output must be wired to FB_INT
17	FB_OUTC	OUT	"Complementary" Feedback output, dedicated for external feedback. It switches at the same frequency as the CLK. This output must be wired to FB_INC
19	FB_INT	IN	"True" Feedback input, provides feedback signal to the internal PLL for synchronization with CLK_INT to eliminate phase error
18	FB_INC	IN	"Complementary" Feedback input, provides signal to the internal PLL for synchronization with CLK_INC to eliminate phase error

This PLL Clock Buffer is designed for a V_{DD} of 2.5V, an AV_{DD} of 2.5V and differential data input and output levels.

ICS95V847 is a zero delay buffer that distributes a differential clock input pair (CLK_INT, CLK_INC) to five differential pair of clock outputs (CLKT[4:0], CLKC[4:0]) and one differential pair feedback clock output (FB_OUT, FB_OUTC). The clock outputs are controlled by input clock (CLK_INT, CLK_INC), the feedback clock (FB_INT, FB_INC) and the analog power input (AV_{DD}). When AV_{DD} is grounded, the PLL is turned off and bypassed for test purposes.

The PLL in **ICS95V847** clock driver uses the input clock (CLK_INC, CLK_INT) and the feedback clock (FB_INT, FB_INC) to provide high-performance, low-skew, low-jitter differential output clocks (CLKT[4:0], CLKC[4:0]). **ICS95V847** is also able to track Spread Spectrum Clock (SSC) for reduced EMI.

ICS95V847 is characterized for operation from 0°C to 85°C.

© 2019 Renesas Electronics Corporation

Absolute Maximum Ratings

Supply Voltage (VDD & AVDD) . . . . . -0.5V to 4.6V
Logic Inputs . . . . . GND - 0.5V to V_{DD} + 0.5V
Ambient Operating Temperature . . . . . 0°C to +85°C
Storage Temperature . . . . . -65°C to +150°C

Stresses above those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only and functional operation of the device at these or any other conditions above those listed in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Electrical Characteristics - Input/Supply/Common Output Parameters

T_A = 0 - 85°C; Supply Voltage A_{VDD}, V_{DD} = 2.5 V +/- 0.2V (unless otherwise stated)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input High Current	I_{IH}	$V_I = V_{DD}$ or GND	5			µA
Input Low Current	I_{IL}	$V_I = V_{DD}$ or GND			5	µA
Operating Supply Current	$I_{DD2.5}$	C_L = 0pf @ 200MHz			148	mA
	I_{DDPD}	C_L = 0pf			100	µA
High Impedance Output Current	I_{OZ}	V_{DD} = 2.7V, Vout = V_{DD} or GND			±10	mA
Input Clamp Voltage	V_{IK}	V_{DD} = 2.3V Iin = -18mA			-1.2	V
High-level output voltage	V_{OH}	I_{OH} = -1 mA	V_{DD} - 0.1			V
		I_{OH} = -12 mA	1.7V			V
Low-level output voltage	V_{OL}	I_{OL} =1 mA			0.1	V
		I_{OH} =12 mA			0.6	V
Input Capacitance[1]	C_{IN}	V_I = GND or V_{DD}	2.5		3.5	pF

[1]Guaranteed by design at 233MHz, not 100% tested in production.

© 2019 Renesas Electronics Corporation

Recommended Operating Condition (see note1)

T_A = 0 - 85°C; Supply Voltage AVDD, VDD = 2.5 V +/- 0.2V (unless otherwise stated)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Voltage	V_{DD}, A_{VDD}		2.3	2.5	2.7	V
Low level input voltage	V_{IL}	CLKT, CLKC, FB_INC		0.4	V_{DD}/2 - 0.18	V
		PD#	-0.3		0.7	V
High level input voltage	V_{IH}	CLKT, CLKC, FB_INC	V_{DD}/2 + 0.18	2.1		V
		PD#	1.7		V_{DD} + 0.6	V
DC input signal voltage (note 2)	V_{IN}		-0.3		V_{DD} + 0.3	V
Differential input signal voltage (note 3)	V_{ID}	DC - CLKT, FB_INT	0.36		V_{DD} + 0.6	V
		AC - CLKT, FB_INT	0.7		V_{DD} + 0.6	V
Output differential cross-voltage (note 4)	V_{OX}		V_{DD}/2 - 0.15		V_{DD}/2 + 0.15	V
Input differential cross-voltage (note 4)	V_{IX}		V_{DD}/2 - 0.2	V_{DD}/2	V_{DD}/2 + 0.2	V
High level output current	I_{OH}				-6.4	mA
Low level output current	I_{OL}				5.5	mA
Operating free-air temperature	T_A		0		85	°C

Notes:

1. Unused inputs must be held high or low to prevent them from floating.
2. DC input signal voltage specifies the allowable DC execution of differential input.
3. Differential inputs signal voltages specifies the differential voltage [VTR-VCP] required for switching, where VT is the true input level and VCP is the complementary input level.
4. Differential cross-point voltage is expected to track variations of V_{DD} and is the voltage at which the differential signal must be crossing.

© 2019 Renesas Electronics Corporation

Timing Requirements

T_A = 0 - 85°C; Supply Voltage A_{VDD}, V_{DD} = 2.5 V +/- 0.2V (unless otherwise stated)

PARAMETER	SYMBOL	CONDITIONS	MIN	MAX	UNITS
Max clock frequency	$freq_{op}$	2.5V±0.2V @ 25°C	45	233	MHz
Application Frequency Range	$freq_{App}$	2.5V±0.2V @ 25°C	95	210	MHz
Input clock duty cycle	d_{tin}		40	60	%
CLK stabilization	T_{STAB}			15	µs

Switching Characteristics (see note 3)

PARAMETER	SYMBOL	CONDITION	MIN	TYP	MAX	UNITS
Low-to high level propagation delay time	t_{PLH}[1]	CLK_IN to any output		5.5		ns
High-to low level propagation delay time	t_{PLL}[1]	CLK_IN to any output		5.5		ns
Output enable time	t_{EN}	PD# to any output		5		ns
Output disable time	tdis	PD# to any output		5		ns
Period jitter	$T_{jit\ (per)}$	100MHz to 200MHz	-30		30	ps
Half-period jitter	t(jit_hper)	100MHz to 200MHz	-75		30	ps
Input clock slew rate	$t_{sl(i)}$		1		4	V/ns
Output clock slew rate	$t_{sl(o)}$		1		2.5	V/ns
Cycle to Cycle Jitter[1]	T_{cyc}-T_{cyc}	100MHz to 200MHz			60	ps
Phase error	$t_{(phase\ error)}$[4]		-50	0	50	ps
Output to Output Skew	T_{skew}				60	ps

Notes:

1. Refers to transition on noninverting output in PLL bypass mode.
2. While the pulse skew is almost constant over frequency, the duty cycle error increases at higher frequencies. This is due to the formula: duty cycle=t_{wH}/t_c, where the cycle (t_c) decreases as the frequency goes up.
3. Switching characteristics guaranteed for application frequency range.
4. Static phase offset shifted by design.

© 2019 Renesas Electronics Corporation

Parameter Measurement Information

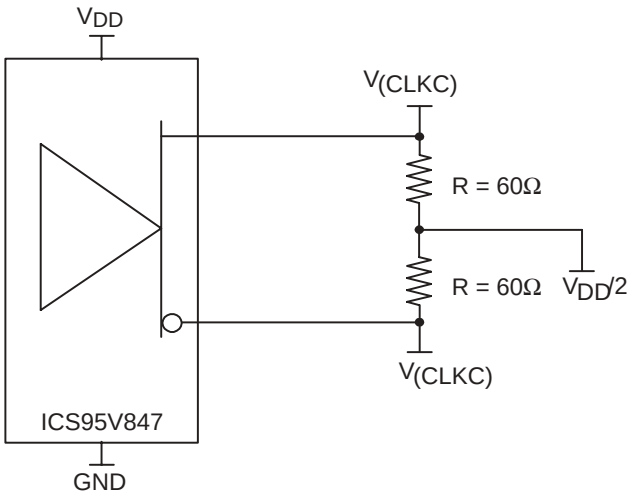
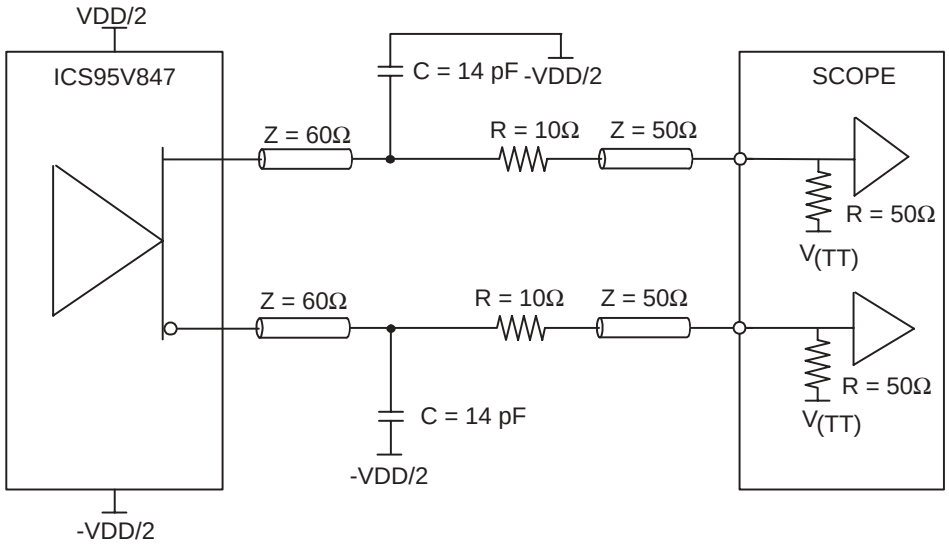
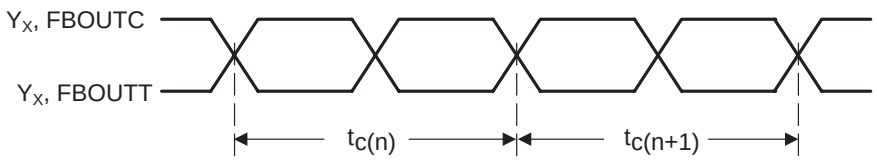


Figure 1. IBIS Model Output Load



NOTE: $V_{(TT)}$ = GND

Figure 2. Output Load Test Circuit



$$t_{jit(cc)} = t_{c(n)} \pm t_{c(n+1)}$$

Figure 3. Cycle-to-Cycle Jitter

© 2019 Renesas Electronics Corporation

Parameter Measurement Information

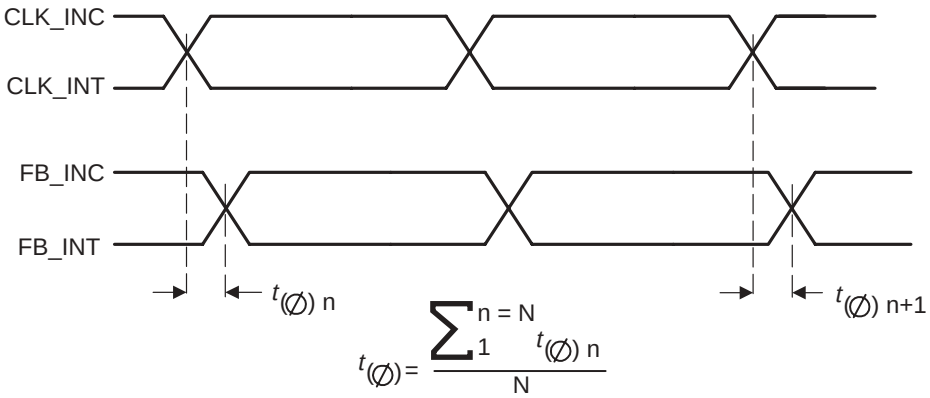


Figure 4. Static Phase Offset

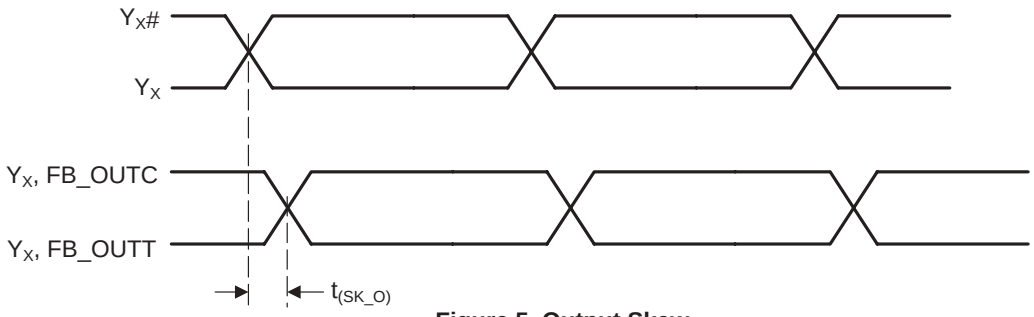


Figure 5. Output Skew

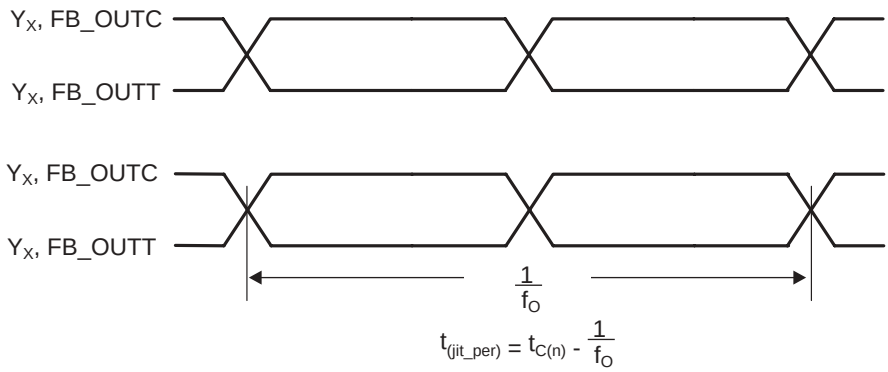


Figure 6. Period Jitter

© 2019 Renesas Electronics Corporation

Parameter Measurement Information

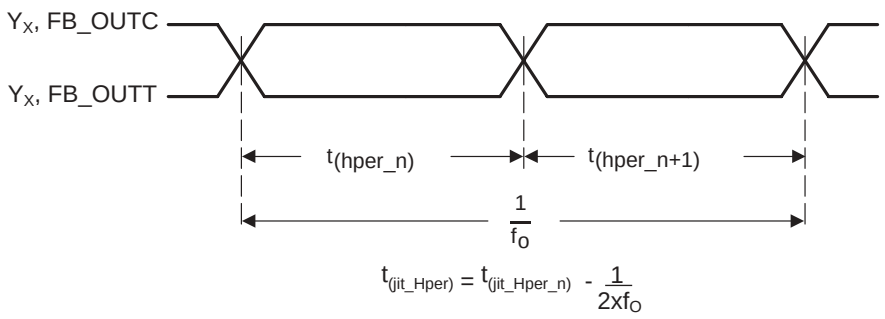


Figure 7. Half-Period Jitter

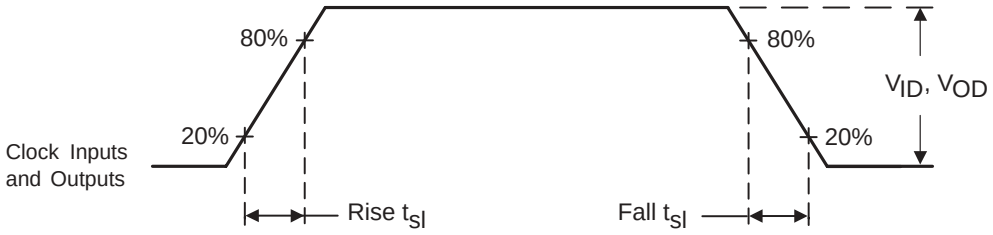
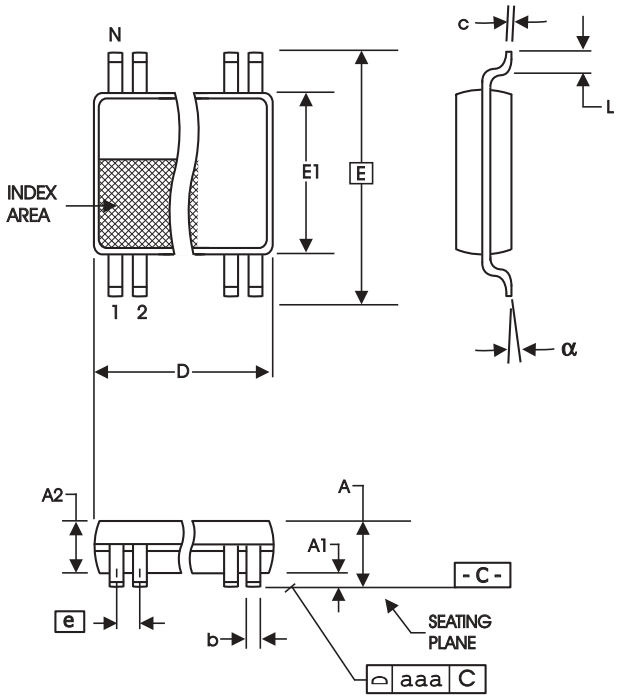


Figure 8. Input and Output Slew Rates

© 2019 Renesas Electronics Corporation



SYMBOL	In Millimeters COMMON DIMENSIONS		In Inches COMMON DIMENSIONS	
	MIN	MAX	MIN	MAX
A	--	1.20	--	.047
A1	0.05	0.15	.002	.006
A2	0.80	1.05	.032	.041
b	0.19	0.30	.007	.012
c	0.09	0.20	.0035	.008
D	SEE VARIATIONS		SEE VARIATIONS	
E	6.40 BASIC		0.252 BASIC	
E1	4.30	4.50	.169	.177
e	0.65 BASIC		0.0256 BASIC	
L	0.45	0.75	.018	.030
N	SEE VARIATIONS		SEE VARIATIONS	
a	0°	8°	0°	8°
aaa	--	0.10	--	.004

VARIATIONS

N	D mm.		D (inch)	
	MIN	MAX	MIN	MAX
24	7.70	7.90	.303	.311

Reference Doc.: JEDEC Publication 95, MO-153
10-0035

4.40 mm. Body, 0.65 mm. pitch TSSOP
(173 mil) (0.0256 Inch)

Ordering Information

95V847yGLF-T

Example:

XXXX y G LF- T

- **Designation for tape and reel packaging**
- **Annealed Lead Free (Optional)**
- **Package Type**
  G = TSSOP
- **Revision Designator** (will not correlate with datasheet revision)
- **Device Type**

0718E—11/24/08

IMPORTANT NOTICE AND DISCLAIMER

RENESAS ELECTRONICS CORPORATION AND ITS SUBSIDIARIES (“RENESAS”) PROVIDES TECHNICAL SPECIFICATIONS AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS OR IMPLIED, INCLUDING, WITHOUT LIMITATION, ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for developers skilled in the art designing with Renesas products. You are solely responsible for (1) selecting the appropriate products for your application, (2) designing, validating, and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. Renesas grants you permission to use these resources only for development of an application that uses Renesas products. Other reproduction or use of these resources is strictly prohibited. No license is granted to any other Renesas intellectual property or to any third party intellectual property. Renesas disclaims responsibility for, and you will fully indemnify Renesas and its representatives against, any claims, damages, costs, losses, or liabilities arising out of your use of these resources. Renesas' products are provided only subject to Renesas' Terms and Conditions of Sale or other applicable terms agreed to in writing. No use of any Renesas resources expands or otherwise alters any applicable warranties or warranty disclaimers for these products.

(Rev.1.0 Mar 2020)

Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,
Koto-ku, Tokyo 135-0061, Japan
www.renesas.com

Contact Information

For further information on a product, technology, the most up-to-date version of a document, or your nearest sales office, please visit:
www.renesas.com/contact/

Trademarks

Renesas and the Renesas logo are trademarks of Renesas Electronics Corporation. All trademarks and registered trademarks are the property of their respective owners.

© 2020 Renesas Electronics Corporation. All rights reserved.