2.5V Low Power Wide Range Frequency Clock Driver (45MHz - 233MHz)

Recommended Application:

- DDR Memory Modules / Zero Delay Board Fan Out
- Provides complete DDR registered DIMM solution with ICSSSTVF16857, ICSSSTVF16859 or ICSSSTV32852

Product Description/Features:

- Lower power version than 95VLP857
- Low skew, low jitter PLL clock driver
- 1 to 10 differential clock distribution (SSTL_2)
- Feedback pins for input to output synchronization
- PD# for power management
- Spread Spectrum-tolerant inputs
- Auto PD when input signal removed

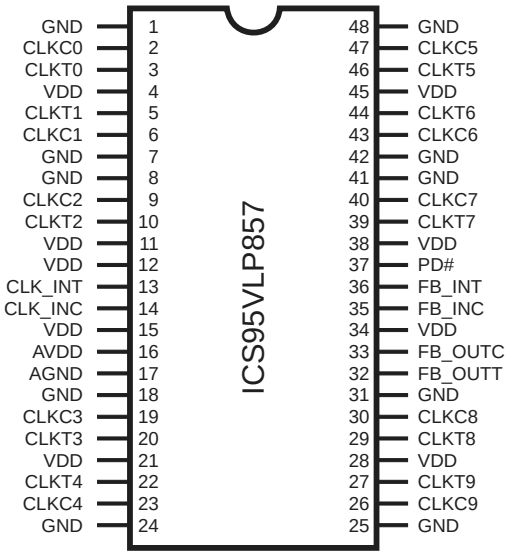
Specifications:

- Meets PC3200 Class A+ specification for DDR-I 400 support
- Covers all DDRI speed grades

Switching Characteristics:

- CYCLE - CYCLE jitter: <50ps
- OUTPUT - OUTPUT skew: <40ps
- Period jitter: ±30ps

Pin Configuration



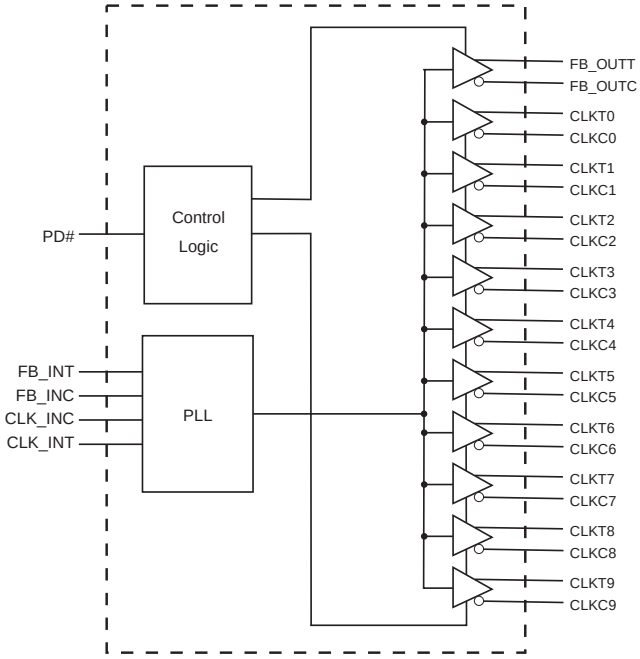
48-Pin TSSOP/TVSOP

6.10 mm Body, 0.50 mm Pitch = TSSOP
4.40 mm Body, 0.40 mm Pitch = TVSOP

Functionality

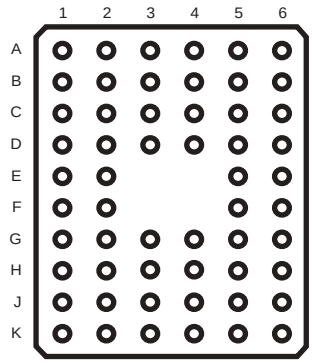
INPUTS				OUTPUTS				PLL State
AVDD	PD#	CLK_INT	CLK_INC	CLKT	CLKC	FB_OUTT	FB_OUTC	
GND	H	L	H	L	H	L	H	Bypassed/off
GND	H	H	L	H	L	H	L	Bypassed/off
2.5V (nom)	L	L	H	Z	Z	Z	Z	off
2.5V (nom)	L	H	L	Z	Z	Z	Z	off
2.5V (nom)	H	L	H	L	H	L	H	on
2.5V (nom)	H	H	L	H	L	H	L	on
2.5V (nom)	X	<20MHz)(1)		Z	Z	Z	Z	off

Block Diagram



© 2019 Renesas Electronics Corporation

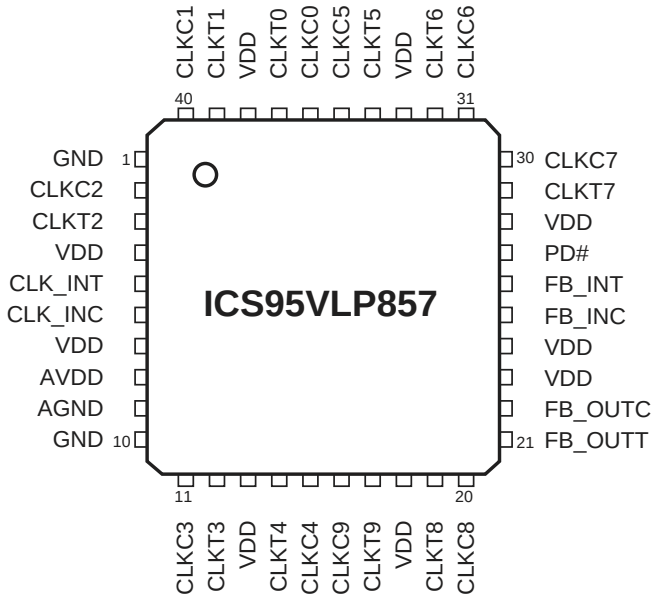
Pin Configuration



56-Ball BGA

Top View

	1	2	3	4	5	6
A	CLKT0	CLKC0	GND	GND	CLKC5	CLKT5
B	CLKC1	CLKT1	VDD	VDD	CLKT6	CLKC6
C	GND	GND	NC	NC	GND	GND
D	CLKT2	CLKC2	NC	NC	CLKC7	CLKT7
E	VDD	VDD	NB	NB	VDD	PD#
F	CLK_INT	CLK_INC	NB	NB	FB_INC	FB_INT
G	VDD	AVDD	NC	NC	FB_OUTC	VDD
H	AGND	GND	NC	NC	GND	FB_OUTT
J	CLKC3	CLKT3	VDD	VDD	CLKT8	CLKC8
K	CLKT4	CLKC4	GND	GND	CLKC9	CLKT9



40-Pin MLF

© 2019 Renesas Electronics Corporation

Pin Descriptions

PIN NAME	TYPE	DESCRIPTION
VDD	PWR	Power supply, 2.5V
GND	PWR	Ground
AVDD	PWR	Analog power supply, 2.5V
AGND	PWR	Analog ground
CLKT(9:0)	OUT	"True" Clock of differential pair outputs
CLKC(9:0)	OUT	"Complementary" clocks of differential pair outputs
CLK_INC	IN	"Complementary" reference clock input
CLK_INT	IN	"True" reference clock input
FB_OUTC	OUT	"Complementary" Feedback output, dedicated for external feedback. It switches at the same frequency as the CLK. This output must be wired to FB_INC
FB_OUTT	OUT	"True" " Feedback output, dedicated for external feedback. It switches at the same frequency as the CLK. This output must be wired to FB_INT
FB_INT	IN	"True" Feedback input, provides feedback signal to the internal PLL for synchronization with CLK_INT to eliminate phase error
FB_INC	IN	"Complementary" Feedback input, provides signal to the internal PLL for synchronization with CLK_INC to eliminate phase error
PD#	IN	Power Down. LVCMOS input

This PLL Clock Buffer is designed for a V_{DD} of 2.5V, an AV_{DD} of 2.5V and differential data input and output levels.

The **ICS95VLP857** is a zero delay buffer that distributes a differential clock input pair (CLK_INC, CLK_INT) to ten differential pair of clock outputs (CLKT[0:9], CLKC[0:9]) and one differential pair feedback clock output (FB_OUT, FB_OUTC). The clock outputs are controlled by the input clocks (CLK_INC, CLK_INT), the feedback clocks (FB_INT, FB_INC), the 2.5-V LVCMOS input (PD#) and the Analog Power input (AV_{DD}). When input (PD#) is low while power is applied, the receivers are disabled, the PLL is turned off and the differential clock outputs are tri-stated. When AV_{DD} is grounded, the PLL is turned off and bypassed for test purposes.

When the input frequency is less than the operating frequency of the PLL, appproximately 20MHz, the device will enter a low power mode. An input frequency detection circuit on the differential inputs, independent from the input buffers, will detect the low frequency condition and perform the same low power features as when the (PD#) input is low. When the input frequency increases to greater than approximately 20 MHz, the PLL will be turned back on, the inputs and outputs will be enabled and PLL will obtain phase lock between the feedback clock pair (FB_INT, FB_INC) and the input clock pair (CLK_INC, CLK_INT).

The PLL to the **ICS95VLP857** clock driver uses the input clocks (CLK_INC, CLK_INT) and the feedback clocks (FB_INT, FB_INC) provide high-performance, low-skew, low-jitter, output differential clocks (CLKT[0:9], CLKC[0:9]). The **ICS95VLP857** is also able to track Spread Spectrum Clock (SSC) for reduced EMI.

The **ICS95VLP857** is characterized for operation from 0°C to 85°C, and will meet JEDEC Standard 82-1 and 82-1A Class A+ for registered DDR clock drivers.

0956B—08/03/04

© 2019 Renesas Electronics Corporation

Absolute Maximum Ratings

Supply Voltage (VDD & AVDD) . . . . . -0.5V to 4.6V
Logic Inputs . . . . . GND –0.5 V to V_{DD} + 0.5 V
Ambient Operating Temperature . . . . . 0°C to +85°C
Storage Temperature . . . . . –65°C to +150°C

Stresses above those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only and functional operation of the device at these or any other conditions above those listed in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Electrical Characteristics - Input/Supply/Common Output Parameters

T_A = 0 - 85°C; Supply Voltage A_{VDD}, V_{DD} = 2.5V ± 0.2V

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input High Current	I_{IH}	$V_I = V_{DD}$ or GND	5			µA
Input Low Current	I_{IL}	$V_I = V_{DD}$ or GND			5	µA
Operating Supply Current	$I_{DD2.5}$	C_L = 0pf @ 200MHz		125	150	mA
	I_{DDPD}	C_L = 0pf			100	µA
Output High Current	I_{OH}	V_{DD} = 2.3V, V_{OUT} = 1V	-18	-32		mA
Output Low Current	I_{OL}	V_{DD} = 2.3V, V_{OUT} = 1.2V	26	35		mA
High Impedance Output Current	I_{OZ}	V_{DD}=2.7V, Vout=V_{DD} or GND			±10	mA
Input Clamp Voltage	V_{IK}	V_{DDQ} = 2.3V Iin = -18mA			-1.2	V
High-level output voltage	V_{OH}	V_{DD} = min to max, I_{OH} = -1 mA	V_{DDQ} - 0.1			V
		V_{DDQ} = 2.3V, I_{OH} = -12 mA	1.7			V
Low-level output voltage	V_{OL}	V_{DD} = min to max I_{OL}=1 mA			0.1	V
		V_{DDQ} = 2.3V I_{OH}=12 mA			0.6	V
Input Capacitance[1]	C_{IN}	V_I = GND or V_{DD}		3		pF
Output Capacitance[1]	C_{OUT}	V_{OUT} = GND or V_{DD}		3		pF

[1]Guaranteed by design at 220MHz, not 100% tested in production.

© 2019 Renesas Electronics Corporation

Recommended Operating Condition (see note1)

T_A = 0 - 85°C; Supply Voltage AVDD, VDD = 2.5 V +/- 0.2V (unless otherwise stated)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Voltage	V_{DD}, A_{VDD}		2.3	2.5	2.7	V
Low level input voltage	V_{IL}	CLKT, CLKC, FB_INC		0.4	V_{DD}/2 - 0.18	V
		PD#	-0.3		0.7	V
High level input voltage	V_{IH}	CLKT, CLKC, FB_INC	V_{DD}/2 + 0.18	2.1		V
		PD#	1.7		V_{DD} + 0.6	V
DC input signal voltage (note 2)	V_{IN}		-0.3		V_{DD} + 0.3	V
Differential input signal voltage (note 3)	V_{ID}	DC - CLKT, FB_INT	0.36		V_{DD} + 0.6	V
		AC - CLKT, FB_INT	0.7		V_{DD} + 0.6	V
Output differential cross-voltage (note 4)	V_{OX}		V_{DD}/2 - 0.15		V_{DD}/2 + 0.15	V
Input differential cross-voltage (note 4)	V_{IX}		V_{DD}/2 - 0.2	V_{DD}/2	V_{DD}/2 + 0.2	V
High level output current	I_{OH}				-6.4	mA
Low level output current	I_{OL}				5.5	mA
Operating free-air temperature	T_A		0		85	°C

Notes:

1. Unused inputs must be held high or low to prevent them from floating.
2. DC input signal voltage specifies the allowable DC execution of differential input.
3. Differential inputs signal voltages specifies the differential voltage [VTR-VCP] required for switching, where VT is the true input level and VCP is the complementary input level.
4. Differential cross-point voltage is expected to track variations of V_{DD} and is the voltage at which the differential signal must be crossing.

© 2019 Renesas Electronics Corporation

Timing Requirements

T_A = 0 - 85°C; Supply Voltage A_{VDD}, V_{DD} = 2.5 V +/- 0.2V (unless otherwise stated)

PARAMETER	SYMBOL	CONDITIONS	MIN	MAX	UNITS
Max clock frequency	$freq_{op}$	2.5V±0.2V @ 25°C	45	233	MHz
Application Frequency Range	$freq_{App}$	2.5V±0.2V @ 25°C	95	220	MHz
Input clock duty cycle	d_{tin}		40	60	%
CLK stabilization	T_{STAB}			15	µs

Switching Characteristics (see note 3)

PARAMETER	SYMBOL	CONDITION	MIN	TYP	MAX	UNITS
Low-to high level propagation delay time	t_{PLH}[1]	CLK_IN to any output		3.5		ns
High-to low level propagation delay time	t_{PLL}[1]	CLK_IN to any output		3.5		ns
Output enable time	t_{EN}	PD# to any output		3		ns
Output disable time	tdis	PD# to any output		3		ns
Period jitter	$T_{jit\ (per)}$	100MHz to 200MHz	-30		30	ps
Half-period jitter	t(jit_hper)	100MHz to 200MHz	-75		75	ps
Input clock slew rate	$t_{sl(i)}$		1		4	V/ns
Output clock slew rate	$t_{sl(o)}$		1		2	V/ns
Cycle to Cycle Jitter[1]	T_{cyc}-T_{cyc}	100MHz to 200MHz	-50		50	ps
Static Phase Offset	$t_{(static\ phase\ offset)}$[4]		-50	0	50	ps
Output to Output Skew	T_{skew}				40	ps

Notes:

1. Refers to transition on noninverting output in PLL bypass mode.
2. While the pulse skew is almost constant over frequency, the duty cycle error increases at higher frequencies. This is due to the formula: duty cycle=t_{WH}/t_C, where the cycle (t_C) decreases as the frequency goes up.
3. Switching characteristics guaranteed for application frequency range.
4. Static phase offset shifted by design.

© 2019 Renesas Electronics Corporation

Parameter Measurement Information

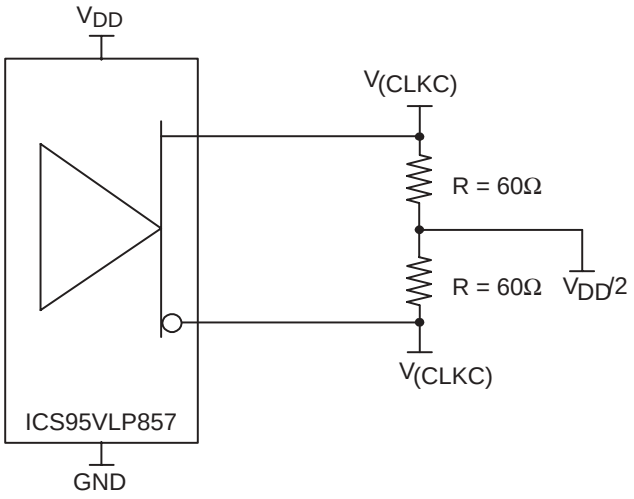
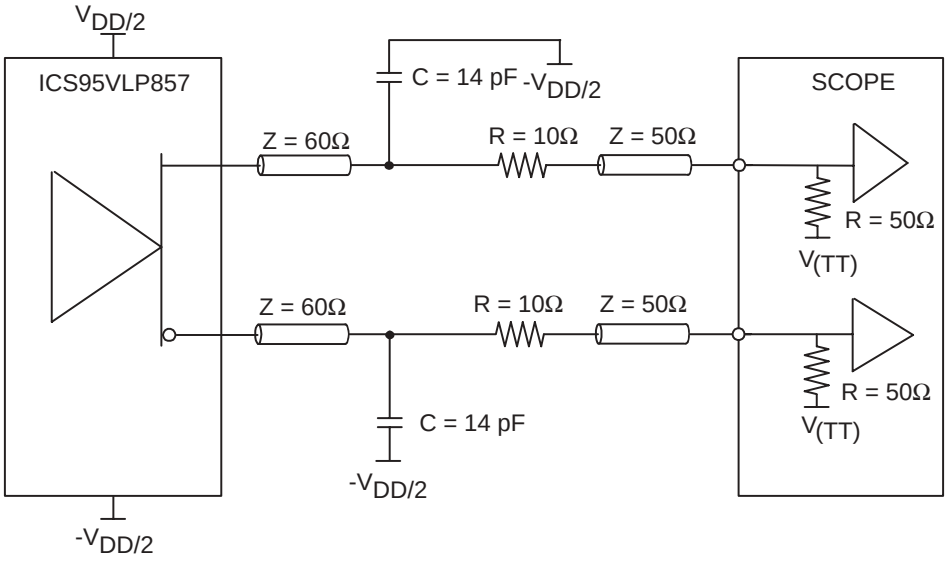
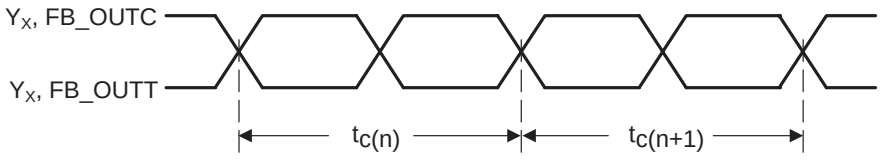


Figure 1. IBIS Model Output Load



NOTE: $V_{(TT)}$ = GND

Figure 2. Output Load Test Circuit



$$t_{jit(cc)} = t_{c(n)} \pm t_{c(n+1)}$$

Figure 3. Cycle-to-Cycle Jitter

© 2019 Renesas Electronics Corporation

Parameter Measurement Information

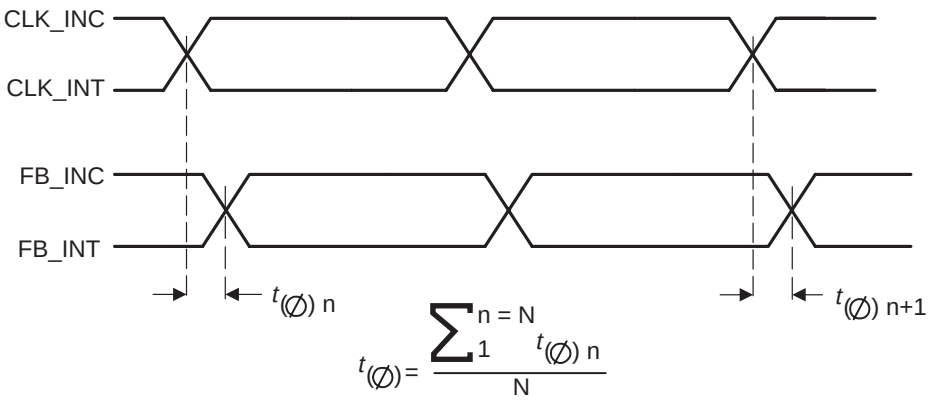


Figure 4. Static Phase Offset

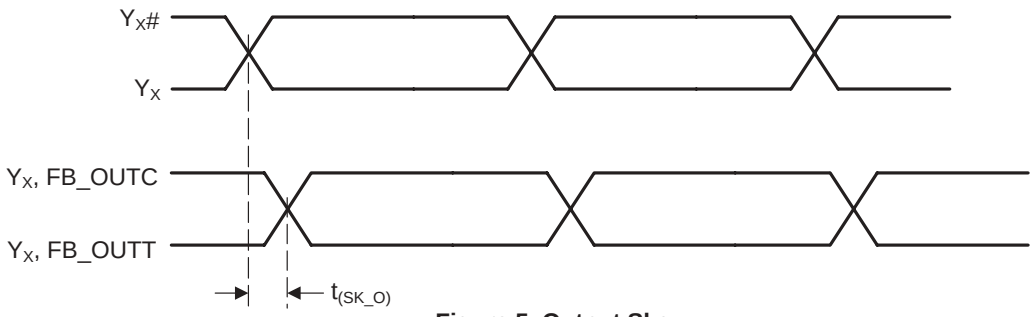


Figure 5. Output Skew

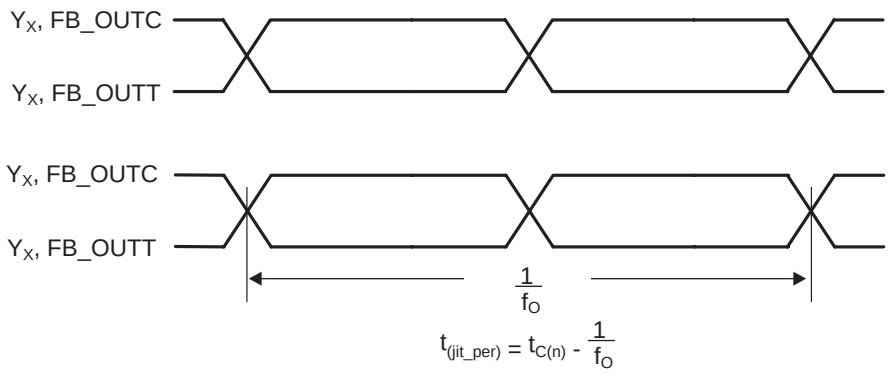


Figure 6. Period Jitter

© 2019 Renesas Electronics Corporation

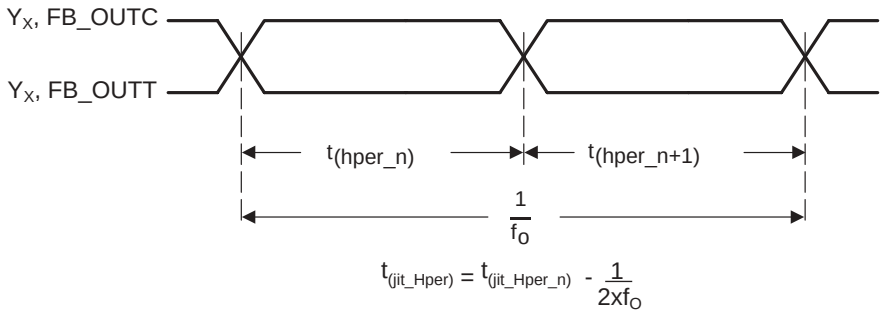


Figure 7. Half-Period Jitter

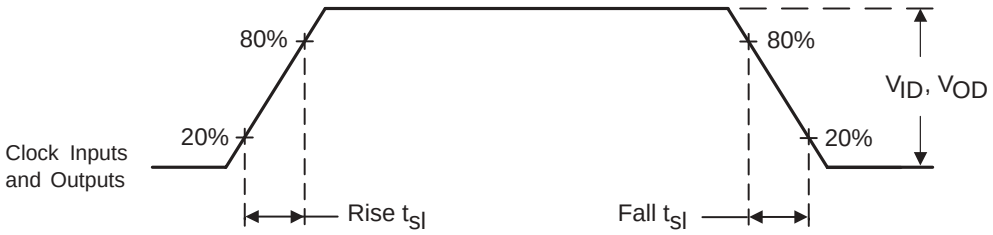
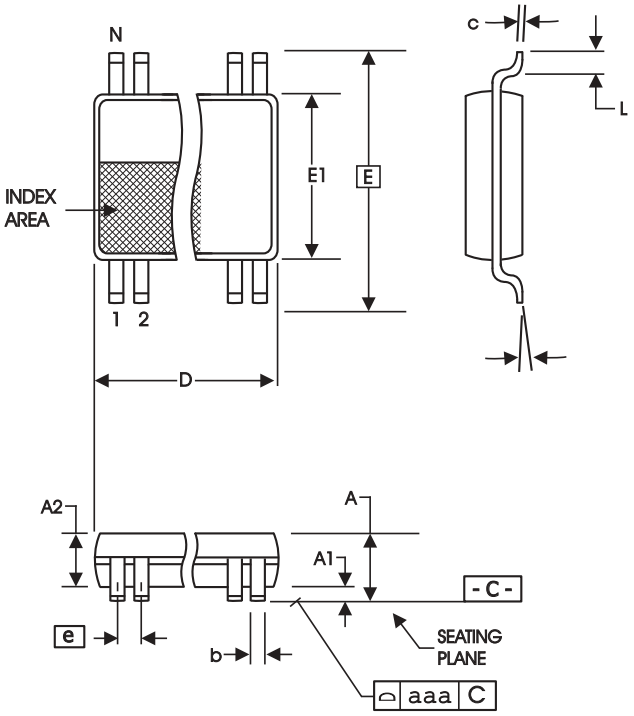


Figure 8. Input and Output Slew Rates

© 2019 Renesas Electronics Corporation



6.10 mm. Body, 0.50 mm. pitch TSSOP
(240 mil) (0.020 mil)

SYMBOL	In Millimeters COMMON DIMENSIONS		In Inches COMMON DIMENSIONS	
	MIN	MAX	MIN	MAX
A	--	1.20	--	.047
A1	0.05	0.15	.002	.006
A2	0.80	1.05	.032	.041
b	0.17	0.27	.007	.011
c	0.09	0.20	.0035	.008
D	SEE VARIATIONS		SEE VARIATIONS	
E	8.10 BASIC		0.319 BASIC	
E1	6.00	6.20	.236	.244
e	0.50 BASIC		0.020 BASIC	
L	0.45	0.75	.018	.030
N	SEE VARIATIONS		SEE VARIATIONS	
a	0°	8°	0°	8°
aaa	--	0.10	--	.004

VARIATIONS

N	D mm.		D (inch)	
	MIN	MAX	MIN	MAX
48	12.40	12.60	.488	.496

Reference Doc.: JEDEC Publication 95, MO-153

10-0039

Ordering Information

ICS XXXX y G LF- T

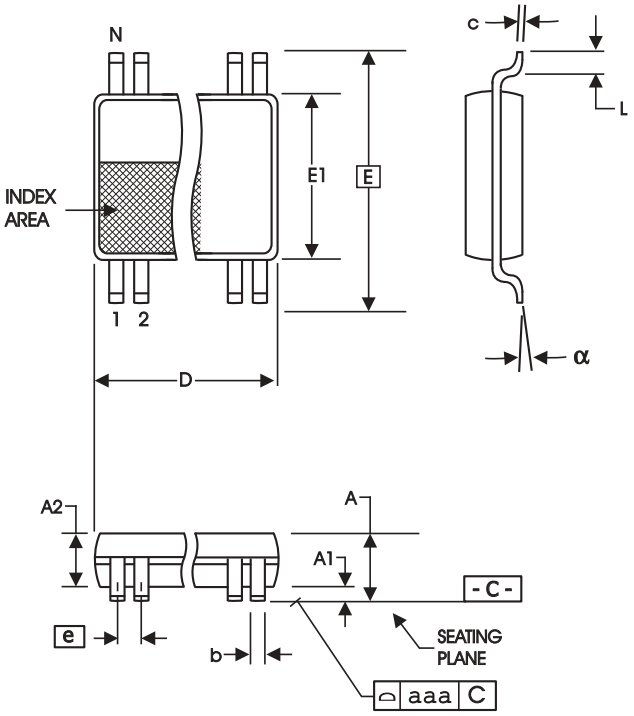
- **Designation for tape and reel packaging**
- **Lead Free (Optional)**
- **Package Type**
  G = TSSOP
- **Revision Designator** (will not correlate with datasheet revision)
- **Device Type**
- **Prefix**
  ICS = Standard Device

Example:

ICS95VLP857AGLF-T, ICS95VLP857AG-130LF-T

0956B—08/03/04

© 2019 Renesas Electronics Corporation



SYMBOL	In Millimeters COMMON DIMENSIONS		In Inches COMMON DIMENSIONS	
	MIN	MAX	MIN	MAX
A	--	1.20	--	.047
A1	0.05	0.15	.002	.006
A2	0.80	1.05	.032	.041
b	0.13	0.23	.005	.009
c	0.09	0.20	.0035	.008
D	SEE VARIATIONS		SEE VARIATIONS	
E	6.40 BASIC		0.252 BASIC	
E1	4.30	4.50	.169	.177
e	0.40 BASIC		0.016 BASIC	
L	0.45	0.75	.018	.030
N	SEE VARIATIONS		SEE VARIATIONS	
a	0°	8°	0°	8°
aaa	--	0.08	--	.003

VARIATIONS

N	D mm.		D (inch)	
	MIN	MAX	MIN	MAX
48	9.60	9.80	.378	.386

Reference Doc.: JEDEC Publication 95, MO-153

10-0037

4.40 mm. Body, 0.40 mm. pitch TSSOP

(173 mil) (16 mil)

Ordering Information

ICS XXXX y K LF- T

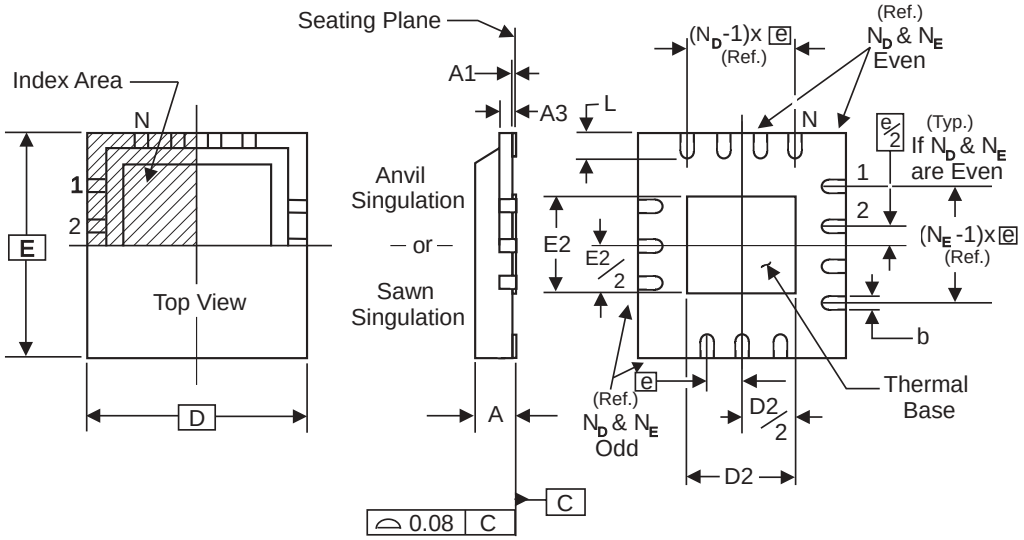
- **Designation for tape and reel packaging**
- **Lead Free (Optional)**
- **Package Type**
  L = TSSOP (TVSOP)
- **Revision Designator** (will not correlate with datasheet revision)
- **Device Type**
- **Prefix**
  ICS = Standard Device

Example:

ICS95VLP857AL-130LF-T

0956B—08/03/04

© 2019 Renesas Electronics Corporation



THERMALLY ENHANCED, VERY THIN, FINE PITCH
QUAD FLAT / NO LEAD PLASTIC PACKAGE

ALL DIMENSIONS IN MILLIMETERS

N	40	SYMBOL	MIN.	MAX.
N_D	10	A	0.80	1.00
N_E	10	A1	0	0.05
D x E BASIC	6.00 x 6.00	A3	0.25 Reference	
D2 MIN. / MAX.	2.75 / 3.05	b	0.18	0.30
E2 MIN. / MAX.	2.75 / 3.05	e	0.50 BASIC	
L MIN. / MAX.	0.30 / 0.50			

	SPECIAL NON-JEDEC
	ALL DIM. SAME EXCEPT AS BELOW:
D2 MIN. / MAX.	4.35 / 4.65
E2 MIN. / MAX.	5.05 / 5.35

Source Reference: MLF2™SEF
10-0053

Ordering Information

ICS XXXX y K LF- T

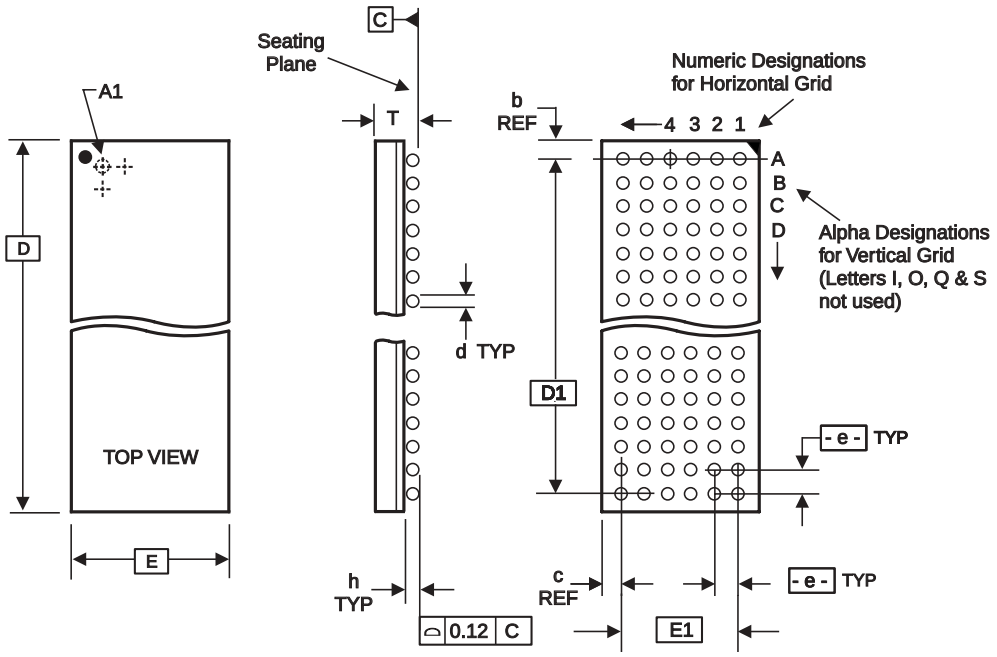
- **Designation for tape and reel packaging**
- **Lead Free (Optional)**
- **Package Type**
  K = MLF
- **Revision Designator** (will not correlate with datasheet revision)
- **Device Type**
- **Prefix**
  ICS = Standard Device

Example:

ICS95VLP857AKLF-T

0956B—08/03/04

© 2019 Renesas Electronics Corporation



ALL DIMENSIONS IN MILLIMETERS

D	E	T Min/Max	e	----- BALL GRID ----- HORIZ	VERT	Max. TOTAL	d Min/Max	h Min/Max	D1	E1	REF. DIMENSIONS b	c	
7.00 Bsc	4.50 Bsc	0.86/1.00	0.65 Bsc	6	10	60	0.35/0.45	0.15/0.21	5.85 Bsc	3.25 Bsc	0.575	0.625	**

Note: Ball grid total indicates maximum ball count for package. Lesser quantity may be used.

* Source Ref.: JEDEC Publication 95, MO-205*, MO-225**

10-0055

Ordering Information

ICS XXXX y H LF- T

- **Designation for tape and reel packaging**
- **Lead Free (Optional)**
- **Package Type**
  H = BGA
- **Revision Designator** (will not correlate with datasheet revision)
- **Device Type**
- **Prefix**
  ICS = Standard Device

Example:

ICS95VLP857AHLF-T

0956B—08/03/04

IMPORTANT NOTICE AND DISCLAIMER

RENESAS ELECTRONICS CORPORATION AND ITS SUBSIDIARIES (“RENESAS”) PROVIDES TECHNICAL SPECIFICATIONS AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS OR IMPLIED, INCLUDING, WITHOUT LIMITATION, ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for developers skilled in the art designing with Renesas products. You are solely responsible for (1) selecting the appropriate products for your application, (2) designing, validating, and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. Renesas grants you permission to use these resources only for development of an application that uses Renesas products. Other reproduction or use of these resources is strictly prohibited. No license is granted to any other Renesas intellectual property or to any third party intellectual property. Renesas disclaims responsibility for, and you will fully indemnify Renesas and its representatives against, any claims, damages, costs, losses, or liabilities arising out of your use of these resources. Renesas' products are provided only subject to Renesas' Terms and Conditions of Sale or other applicable terms agreed to in writing. No use of any Renesas resources expands or otherwise alters any applicable warranties or warranty disclaimers for these products.

(Rev.1.0 Mar 2020)

Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,
Koto-ku, Tokyo 135-0061, Japan
www.renesas.com

Contact Information

For further information on a product, technology, the most up-to-date version of a document, or your nearest sales office, please visit:
www.renesas.com/contact/

Trademarks

Renesas and the Renesas logo are trademarks of Renesas Electronics Corporation. All trademarks and registered trademarks are the property of their respective owners.

© 2020 Renesas Electronics Corporation. All rights reserved.