General Description

The ICS9DB823B is compatible with the Intel DB800Q Differential Buffer Specification. This buffer provides 8 PCI-Express SRC or 8 QPI clocks. The ICS9DB823B is driven by a differential output pair from a CK410B+ or CK509B main clock generator.

Recommended Application

DB800Q compatible part with PCIe Gen1, Gen 2 and QPI support

Output Features

- 8 - 0.7V current-mode differential output pairs
- Supports zero delay buffer mode and fanout mode
- Bandwidth programming available
- 50-133 MHz operation in PLL mode
- 33-400 MHz operation in Bypass mode

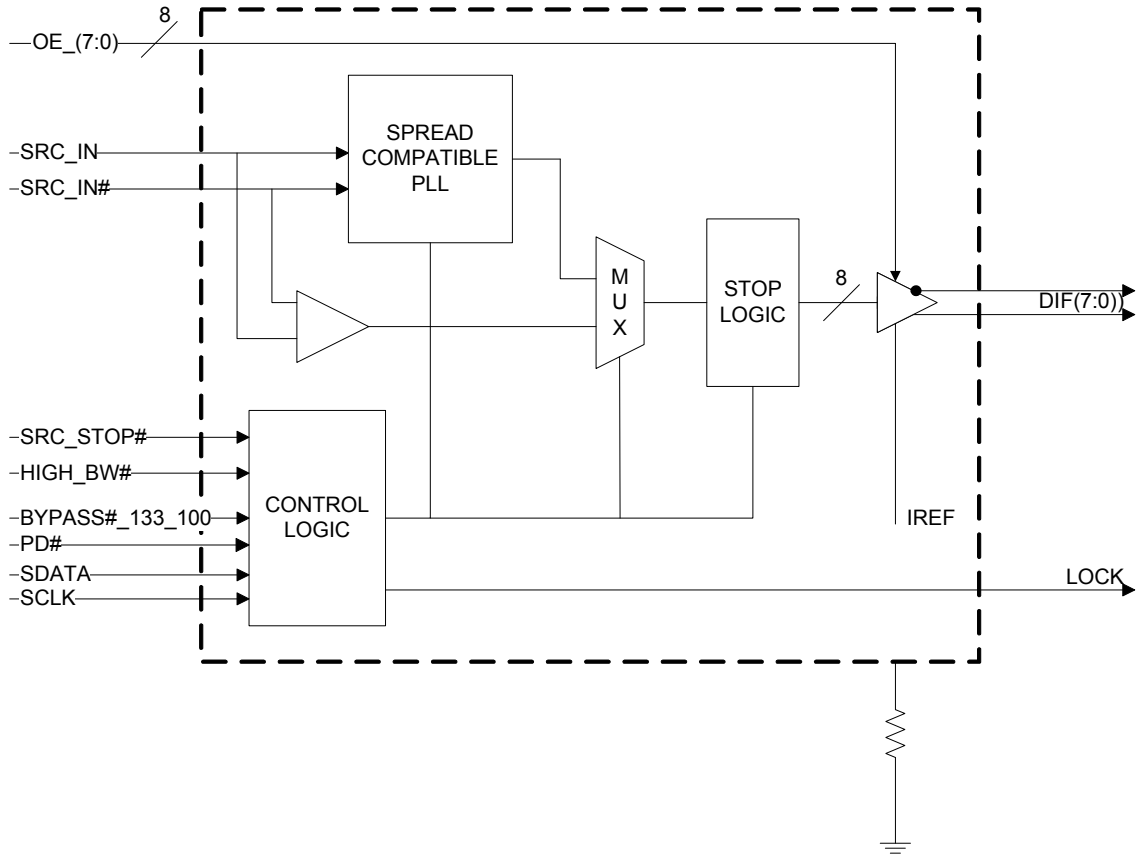
Features/Benefits

- Spread spectrum modulation tolerant, 0 to -0.5% down spread and +/- 0.25% center spread
- Supports undriven differential outputs in Power Down and DIF_STOP# modes for power management.

Key Specifications

- Outputs cycle-cycle jitter < 50ps
- Output to Output skew <50ps
- Phase jitter: PCIe Gen1 < 86ps peak to peak
- Phase jitter: PCIe Gen2 < 3.0/3.1ps rms
- Phase jitter: QPI < 0.5ps rms

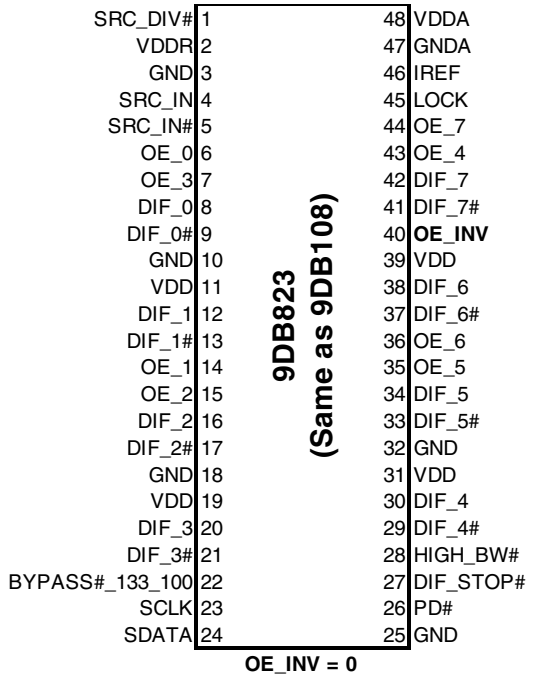
Functional Block Diagram



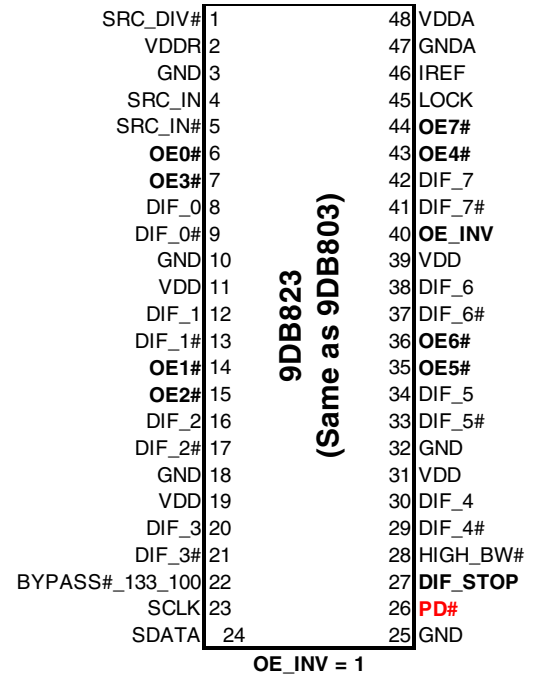
Note: Polarities shown are for OE_INV=0.

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Pin Configuration



OE_INV = 0



OE_INV = 1

Note: Pin 26 is always active low. This is different than 9DB803.

48-pin SSOP and TSSOP

Power Groups

Pin Number		Description
VDD	GND	
2	3	SRC_IN/SRC_IN#
11,19,31,39	10,18, 25,32	DIF(7:0)
N/A	47	IREF
48	47	Analog VDD & GND for PLL core

Bypass Readback Table

BYPASS#_133_100	Byte0, bit 3	Byte 0 bit 1
Low	0	0
Mid	1	0
High	0	1

Frequency Selection

BYPASS#_133_100	Voltage	MODE
Low	<0.8V	Bypass
Mid	1.2<Vin<1.8V	QPI 133MHz
High	Vin > 2.0V	PCIe 100MHz

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Pin Descriptions for OE_INV=0

PIN #	PIN NAME	PIN TYPE	DESCRIPTION
1	SRC_DIV#	IN	Active low Input for determining SRC output frequency SRC or SRC/2. 0 = SRC/2, 1= SRC
2	VDDR	PWR	3.3V power for differential input clock (receiver). This VDD should be treated as an analog power rail and filtered appropriately.
3	GND	PWR	Ground pin.
4	SRC_IN	IN	0.7 V Differential SRC TRUE input
5	SRC_IN#	IN	0.7 V Differential SRC COMPLEMENTARY input
6	OE_0	IN	Active high input for enabling output 0. 0 =disable outputs, 1= enable outputs
7	OE_3	IN	Active high input for enabling output 3. 0 =disable outputs, 1= enable outputs
8	DIF_0	OUT	0.7V differential true clock output
9	DIF_0#	OUT	0.7V differential Complementary clock output
10	GND	PWR	Ground pin.
11	VDD	PWR	Power supply, nominal 3.3V
12	DIF_1	OUT	0.7V differential true clock output
13	DIF_1#	OUT	0.7V differential Complementary clock output
14	OE_1	IN	Active high input for enabling output 1. 0 =disable outputs, 1= enable outputs
15	OE_2	IN	Active high input for enabling output 2. 0 =disable outputs, 1= enable outputs
16	DIF_2	OUT	0.7V differential true clock output
17	DIF_2#	OUT	0.7V differential Complementary clock output
18	GND	PWR	Ground pin.
19	VDD	PWR	Power supply, nominal 3.3V
20	DIF_3	OUT	0.7V differential true clock output
21	DIF_3#	OUT	0.7V differential Complementary clock output
22	BYPASS#_133_100	IN	Input to select Bypass(fan-out), QPI PLL (133MHz) or PCIe PLL (100MHz) mode 0 = Bypass mode, M= QPI, 1= PCIe PLL mode
23	SCLK	IN	Clock pin of SMBus circuitry, 5V tolerant.
24	SDATA	I/O	Data pin for SMBus circuitry, 5V tolerant.

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Pin Descriptions for OE_INV=0 (cont.)

PIN #	PIN NAME	PIN TYPE	DESCRIPTION
25	GND	PWR	Ground pin.
26	PD#	IN	Asynchronous active low input pin used to power down the device. The internal clocks are disabled and the VCO and the crystal osc. (if any) are stopped.
27	DIF_STOP#	IN	Active low input to stop differential output clocks.
28	HIGH_BW#	PWR	3.3V input for selecting PLL Band Width 0 = High, 1= Low
29	DIF_4#	OUT	0.7V differential Complementary clock output
30	DIF_4	OUT	0.7V differential true clock output
31	VDD	PWR	Power supply, nominal 3.3V
32	GND	PWR	Ground pin.
33	DIF_5#	OUT	0.7V differential Complementary clock output
34	DIF_5	OUT	0.7V differential true clock output
35	OE_5	IN	Active high input for enabling output 5. 0 =disable outputs, 1= enable outputs
36	OE_6	IN	Active high input for enabling output 6. 0 =disable outputs, 1= enable outputs
37	DIF_6#	OUT	0.7V differential Complementary clock output
38	DIF_6	OUT	0.7V differential true clock output
39	VDD	PWR	Power supply, nominal 3.3V
40	OE_INV	IN	This latched input selects the polarity of the OE pins. 0 = OE pins active high, 1 = OE pins active low (OE#)
41	DIF_7#	OUT	0.7V differential Complementary clock output
42	DIF_7	OUT	0.7V differential true clock output
43	OE_4	IN	Active high input for enabling output 4. 0 =disable outputs, 1= enable outputs
44	OE_7	IN	Active high input for enabling output 7. 0 =disable outputs, 1= enable outputs
45	LOCK	OUT	3.3V output indicating PLL Lock Status. This pin goes high when lock is achieved.
46	IREF	IN	This pin establishes the reference for the differential current-mode output pairs. It requires a fixed precision resistor to ground. 475ohm is the standard value for 100ohm differential impedance. Other impedances require different values. See data sheet.
47	GNDA	PWR	Ground pin for the PLL core.
48	VDDA	PWR	3.3V power for the PLL core.

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Pin Descriptions for OE_INV=1

PIN #	PIN NAME	PIN TYPE	DESCRIPTION
1	SRC_DIV#	IN	Active low Input for determining SRC output frequency SRC or SRC/2. 0 = SRC/2, 1= SRC
2	VDDR	PWR	3.3V power for differential input clock (receiver). This VDD should be treated as an analog power rail and filtered appropriately.
3	GND	PWR	Ground pin.
4	SRC_IN	IN	0.7 V Differential SRC TRUE input
5	SRC_IN#	IN	0.7 V Differential SRC COMPLEMENTARY input
6	OE0#	IN	Active low input for enabling DIF pair 0. 1 =disable outputs, 0 = enable outputs
7	OE3#	IN	Active low input for enabling DIF pair 3. 1 =disable outputs, 0 = enable outputs
8	DIF_0	OUT	0.7V differential true clock output
9	DIF_0#	OUT	0.7V differential Complementary clock output
10	GND	PWR	Ground pin.
11	VDD	PWR	Power supply, nominal 3.3V
12	DIF_1	OUT	0.7V differential true clock output
13	DIF_1#	OUT	0.7V differential Complementary clock output
14	OE1#	IN	Active low input for enabling DIF pair 1. 1 =disable outputs, 0 = enable outputs
15	OE2#	IN	Active low input for enabling DIF pair 2. 1 =disable outputs, 0 = enable outputs
16	DIF_2	OUT	0.7V differential true clock output
17	DIF_2#	OUT	0.7V differential Complementary clock output
18	GND	PWR	Ground pin.
19	VDD	PWR	Power supply, nominal 3.3V
20	DIF_3	OUT	0.7V differential true clock output
21	DIF_3#	OUT	0.7V differential Complementary clock output
22	BYPASS#_133_100	IN	Input to select Bypass(fan-out), QPI PLL (133MHz) or PCIe PLL (100MHz) mode 0 = Bypass mode, M= QPI, 1= PCIe PLL mode
23	SCLK	IN	Clock pin of SMBus circuitry, 5V tolerant.
24	SDATA	I/O	Data pin for SMBus circuitry, 5V tolerant.

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Pin Descriptions for OE_INV=1 (cont.)

PIN #	PIN NAME	PIN TYPE	DESCRIPTION
25	GND	PWR	Ground pin.
26	PD#	IN	Asynchronous active low input pin used to power down the device. The internal clocks are disabled and the VCO and the crystal osc. (if any) are stopped.
27	DIF_STOP	IN	Active High input to stop differential output clocks.
28	HIGH_BW#	PWR	3.3V input for selecting PLL Band Width 0 = High, 1= Low
29	DIF_4#	OUT	0.7V differential Complementary clock output
30	DIF_4	OUT	0.7V differential true clock output
31	VDD	PWR	Power supply, nominal 3.3V
32	GND	PWR	Ground pin.
33	DIF_5#	OUT	0.7V differential Complementary clock output
34	DIF_5	OUT	0.7V differential true clock output
35	OE5#	IN	Active low input for enabling DIF pair 5. 1 =disable outputs, 0 = enable outputs
36	OE6#	IN	Active low input for enabling DIF pair 6. 1 =disable outputs, 0 = enable outputs
37	DIF_6#	OUT	0.7V differential Complementary clock output
38	DIF_6	OUT	0.7V differential true clock output
39	VDD	PWR	Power supply, nominal 3.3V
40	OE_INV	IN	This latched input selects the polarity of the OE pins. 0 = OE pins active high, 1 = OE pins active low (OE#)
41	DIF_7#	OUT	0.7V differential Complementary clock output
42	DIF_7	OUT	0.7V differential true clock output
43	OE4#	IN	Active low input for enabling DIF pair 4 1 =disable outputs, 0 = enable outputs
44	OE7#	IN	Active low input for enabling DIF pair 7. 1 =disable outputs, 0 = enable outputs
45	LOCK	OUT	3.3V output indicating PLL Lock Status. This pin goes high when lock is achieved.
46	IREF	IN	This pin establishes the reference for the differential current-mode output pairs. It requires a fixed precision resistor to ground. 475ohm is the standard value for 100ohm differential impedance. Other impedances require different values. See data sheet.
47	GNDA	PWR	Ground pin for the PLL core.
48	VDDA	PWR	3.3V power for the PLL core.

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Absolute Maximum Ratings

Stresses above the ratings listed below can cause permanent damage to the ICS9DB823B. These ratings, which are standard values for IDT commercially rated parts, are stress ratings only. Functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods can affect product reliability. Electrical parameters are guaranteed only over the recommended operating temperature range.

Symbol	Parameter	Min	Max	Units
VDDA/R	3.3V Core Supply Voltage		4.6	V
VDD	3.3V Logic Supply Voltage		4.6	V
V_{IL}	Input Low Voltage	GND-0.5		V
V_{IH}	Input High Voltage		V_{DD}+0.5V	V
Ts	Storage Temperature	-65	150	°C
Tambient	Ambient Operating Temp	0	70	°C
Tcase	Case Temperature		115	°C
ESD prot	Input ESD protection human body model	2000		V

Electrical Characteristics–Clock Input Parameters

T_A = 0 - 70°C; Supply Voltage V_{DD} = 3.3 V +/-5%

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	NOTES
Input High Voltage - DIF_IN	V_{IHDIF}	Differential inputs (single-ended measurement)	600	800	1150	mV	1
Input Low Voltage - DIF_IN	V_{ILDIF}	Differential inputs (single-ended measurement)	V_{SS} - 300	0	300	mV	1
Input Common Mode Voltage - DIF_IN	V_{COM}	Common Mode Input Voltage	300		1000	mV	1
Input Amplitude - DIF_IN	V_{SWING}	Peak to Peak value	300		1450	mV	1
Input Slew Rate - DIF_IN	dv/dt	Measured differentially	0.4		8	V/ns	1,2
Input Leakage Current	I_{IN}	$V_{IN} = V_{DD}$, V_{IN} = GND	-5		5	uA	1
Input Duty Cycle	d_{tin}	Measurement from differential wavefrom	45		55	%	1
Input Jitter - Cycle to Cycle	J_{DIFIn}	Differential Measurement	0		125	ps	1

[1] Guaranteed by design and characterization, not 100% tested in production.

[2]Slew rate measured through Vswing min centered around differential zero

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Electrical Characteristics–Input/Supply/Common Output Parameters

T_A = 0 - 70°C; Supply Voltage V_{DD} = 3.3 V +/-5%

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	NOTES
Input High Voltage	V_{IH}	3.3 V +/-5%	2		V_{DD} + 0.3	V	1
Input Low Voltage	V_{IL}	3.3 V +/-5%	GND - 0.3		0.8	V	1
Input High Current	I_{IH}	V_{IN} = V_{DD}	-5		5	uA	1
Input Low Current	I_{IL1}	V_{IN} = 0 V; Inputs with no pull-up resistors	-5			uA	1
	I_{IL2}	V_{IN} = 0 V; Inputs with pull-up resistors	-200			uA	1
Operating Supply Current	$I_{DD3.3OP}$	Full Active, C_L = Full load;			200	mA	1
Powerdown Current	$I_{DD3.3PD}$	all diff pairs driven			60	mA	1
		all differential pairs tri-stated			6	mA	1
Input Frequency	F_{iPLL}	PCIe Mode (Bypass/133/100= 1)	50	100.00	110	MHz	1
	F_{iPLL}	QPI Mode (Bypass/133/100= M)	67	133.33	140	MHz	1
	$F_{iBYPASS}$	Bypass Mode (Bypass/133/100= 0)	33		400	MHz	1
Pin Inductance	L_{pin}				7	nH	1
Capacitance	C_{IN}	Logic Inputs, except SRC_IN	1.5		5	pF	1
	C_{INSRC_IN}	SRC_IN differential clock inputs	1.5		2.7	pF	1,4
	C_{OUT}	Output pin capacitance			6	pF	1
PLL Bandwidth	BW	-3dB point in High BW Mode	2	3	4	MHz	1
		-3dB point in Low BW Mode	0.7	1	1.4	MHz	1
PLL Jitter Peaking	t_{JPEAK}	Peak Pass band Gain		1.5	2	dB	1
Clk Stabilization	T_{STAB}	From V_{DD} Power-Up and after input clock stabilization or de-assertion of PD# to 1st clock			1	ms	1,2
Input SS Modulation Frequency	f_{MODIN}	Allowable Frequency (Triangular Modulation)	30		33	kHz	1
OE# Latency	$t_{LATOE\#}$	DIF start after OE# assertion DIF stop after OE# deassertion	1		3	cycles	1,3
Tdrive_DIF_Stop#	t_{DRVSTP}	DIF output enable after DIF_Stop# de-assertion			10	ns	1,3
Tdrive_PD#	t_{DRVPD}	DIF output enable after PD# de-assertion			300	us	1,3
Tfall	t_F	Fall time of PD# and DIF_Stop#			5	ns	1
Trise	t_R	Rise time of PD# and DIF_Stop#			5	ns	2
SMBus Voltage	V_{MAX}	Maximum input voltage			5.5	V	1
Low-level Output Voltage	V_{OL}	@ I_{PULLUP}			0.4	V	1
Current sinking at V_{OL}	I_{PULLUP}		4			mA	1
SCLK/SDATA Clock/Data Rise Time	t_{RSMB}	(Max VIL - 0.15) to (Min VIH + 0.15)			1000	ns	1
SCLK/SDATA Clock/Data Fall Time	t_{FSMB}	(Min VIH + 0.15) to (Max VIL - 0.15)			300	ns	1
SMBus Operating Frequency	f_{MAXSMB}	Maximum SMBus operating frequency			100	kHz	1,5

[1]Guaranteed by design and characterization, not 100% tested in production.

[2]See timing diagrams for timing requirements.

[3]Time from deassertion until outputs are >200 mV

[4]SRC_IN input

[5]The differential input clock must be running for the SMBus to be active

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Electrical Characteristics–DIF 0.7V Current Mode Differential Pair

T_A = 0 - 70°C; V_{DD} = 3.3 V +/-5%; C_L =2pF, R_S=33Ω, R_P=49.9Ω, R_{REF}=475Ω

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	NOTES
Current Source Output Impedance	Zo[1]		3000			Ω	1
Voltage High	VHigh	Statistical measurement on single ended signal using oscilloscope math function.	660		850	mV	1,2
Voltage Low	VLow		-150		150		1,2
Max Voltage	Vovs	Measurement on single ended signal using absolute value.			1150	mV	1
Min Voltage	Vuds		-300				1
Crossing Voltage (abs)	Vcross(abs)		250		550	mV	1
Crossing Voltage (var)	d-Vcross	Variation of crossing over all edges			140	mV	1
Rise Time	t_r	V_{OL} = 0.175V, V_{OH} = 0.525V	175		700	ps	1
Fall Time	t_f	V_{OH} = 0.525V V_{OL} = 0.175V	175		700	ps	1
Rise Time Variation	d-t_r				125	ps	1
Fall Time Variation	d-t_f				125	ps	1
Duty Cycle	d_{t3}	Measurement from differential wavefrom	45		55	%	1
Skew, Input to Output	t_{pdBYP}	Bypass Mode, V_T = 50%	2500		4500	ps	1
	t_{pdPLL}	PLL Mode V_T = 50%	-250		250	ps	1
Skew, Output to Output	t_{sk3}	V_T = 50%			50	ps	1
Jitter, Cycle to cycle	$t_{jcyc-cyc}$	PLL mode			50	ps	1,3
		Additive Jitter in Bypass Mode			50	ps	1,3
Jitter, Phase	$t_{jphaseBYP}$	PCIe Gen1 phase jitter (Additive in Bypass Mode)		7	10	ps (pk2pk)	1,4,5
		PCIe Gen 2 Low Band phase jitter (Additive in Bypass Mode)		0	0.1	ps (rms)	1,4,5
		PCIe Gen 2 High Band phase jitter (Additive in Bypass Mode)		0.7	0.9	ps (rms)	1,4,5
		QPI phase jitter (Additive in Bypass Mode)			0.16	ps (rms)	1,5,6
	$t_{jphasePLL}$	PCIe Gen 1 phase jitter		37	86	ps (pk2pk)	1,4,5
		PCIe Gen 2 Low Band phase jitter		1.5	3	ps (rms)	1,4,5
		PCIe Gen 2 High Band phase jitter		2.7/ 2.2	3.1	ps (rms)	1,4,5,7
		QPI phase jitter		0.28	0.5	ps (rms)	1,5,6

[1]Guaranteed by design and characterization, not 100% tested in production.

[2] $I_{REF} = V_{DD}/(3xR_R)$. For R_R = 475Ω (1%), I_{REF} = 2.32mA. I_{OH} = 6 x I_{REF} and V_{OH} = 0.7V @ Z_O=50Ω.

3 Measured from differential waveform

[4] See http://www.pcisig.com for complete specs

[5] Device driven by 932S421C or equivalent.

[6] 6.4Gb 12UI

[7] First number is High Bandwidth Mode, second number is Low Bandwidth Mode

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Clock Periods–Differential Outputs with Spread Spectrum Enabled

Measurement Window		1 Clock	1us	0.1s	0.1s	0.1s	1us	1 Clock		
Symbol		Lg-	-SSC	-ppm error	0ppm	+ ppm error	+SSC	Lg+		
Definition		Absolute Period	Short-term Average	Long-Term Average	Period	Long-Term Average	Short-term Average	Period		
		Minimum Absolute Period	Minimum Absolute Period	Minimum Absolute Period	Nominal	Maximum	Maximum	Maximum	Units	Notes
Signal Name	DIF 100	9.949	9.999	10.024	10.025	10.026	10.051	10.101	ns	1,2,3
	DIF 133	7.449	7.499	7.518	7.519	7.520	7.538	7.588	ns	1,2,4
	DIF 166	5.949	5.999	6.014	6.015	6.016	6.031	6.081	ns	1,2,5
	DIF 200	4.950	5.000	5.012	5.013	5.013	5.026	5.076	ns	1,2,5
	DIF 266	3.700	3.750	3.759	3.759	3.760	3.769	3.819	ns	1,2,5
	DIF 333	2.950	3.000	3.007	3.008	3.008	3.015	3.065	ns	1,2,5
	DIF 400	2.450	2.500	2.506	2.506	2.507	2.513	2.563	ns	1,2,5

Clock Periods–Differential Outputs with Spread Spectrum Disabled

Measurement Window		1 Clock	1us	0.1s	0.1s	0.1s	1us	1 Clock		
Symbol		Lg-	-SSC	-ppm error	0ppm	+ ppm error	+SSC	Lg+		
Definition		Absolute Period	Short-term Average	Long-Term Average	Period	Long-Term Average	Short-term Average	Period		
		Minimum Absolute Period	Minimum Absolute Period	Minimum Absolute Period	Nominal	Maximum	Maximum	Maximum	Units	Notes
Signal Name	DIF 100	9.949		9.999	10.000	10.001		10.051	ns	1,2,3
	DIF 133	7.449		7.499	7.500	7.501		7.551	ns	1,2,4
	DIF 166	5.949		5.999	6.000	6.001		6.051	ns	1,2,5
	DIF 200	4.950		5.000	5.000	5.001		5.051	ns	1,2,5
	DIF 266	3.700		3.750	3.750	3.750		3.800	ns	1,2,5
	DIF 333	2.950		3.000	3.000	3.000		3.050	ns	1,2,5
	DIF 400	2.450		2.500	2.500	2.500		2.550	ns	1,2,5

[1]Guaranteed by design and characterization, not 100% tested in production.

[2] All Long Term Accuracy specifications are guaranteed with the assumption that the input clock complies with CK410B+ accuracy requirements. The 9DB423/823 itself does not contribute to ppm error.

[3] Driven by SRC output of main clock, PCIe PLL Mode or Bypass mode

[4] Driven by CPU output of main clock, QPI PLL Mode or Bypass mode

[5] Driven by CPU output of CK410B+/CK420BQ/CK505 main clock, **Bypass mode only**

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DIF Reference Clock			
Common Recommendations for Differential Routing	Dimension or Value	Unit	Figure
L1 length, route as non-coupled 50ohm trace	0.5 max	inch	1
L2 length, route as non-coupled 50ohm trace	0.2 max	inch	1
L3 length, route as non-coupled 50ohm trace	0.2 max	inch	1
Rs	33	ohm	1
Rt	49.9	ohm	1

Down Device Differential Routing			
L4 length, route as coupled microstrip 100ohm differential trace	2 min to 16 max	inch	1
L4 length, route as coupled stripline 100ohm differential trace	1.8 min to 14.4 max	inch	1

Differential Routing to PCI Express Connector			
L4 length, route as coupled microstrip 100ohm differential trace	0.25 to 14 max	inch	2
L4 length, route as coupled stripline 100ohm differential trace	0.225 min to 12.6 max	inch	2

Figure 1: Down Device Routing

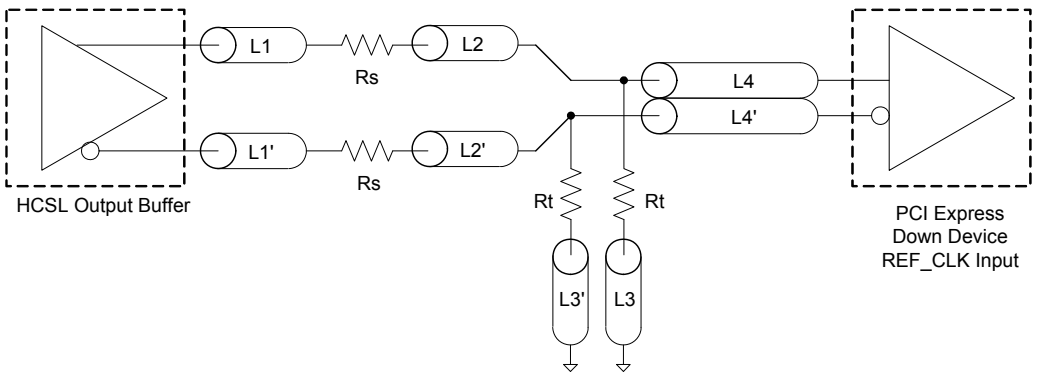
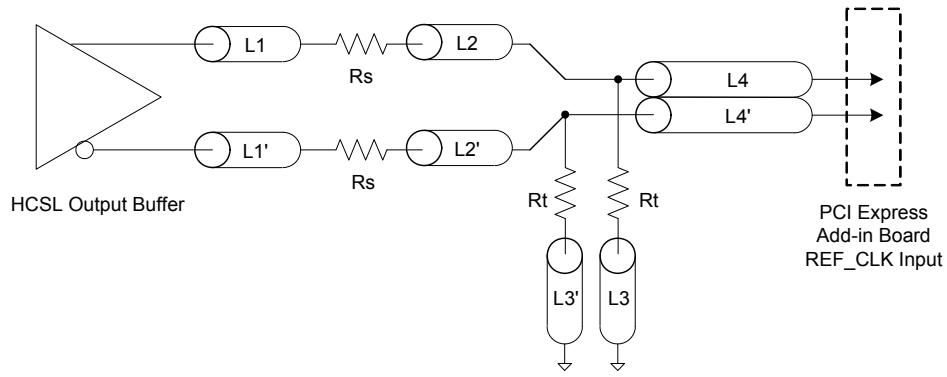


Figure 2: PCI Express Connector Routing

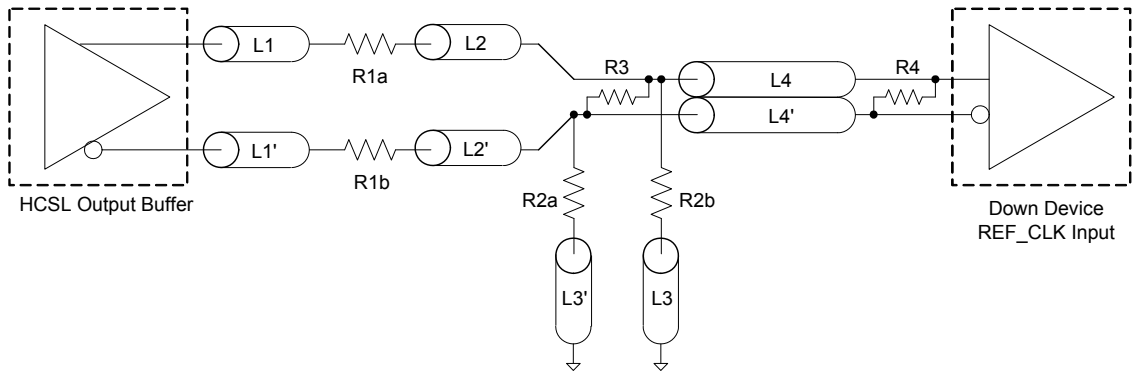


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Alternative Termination for LVDS and other Common Differential Signals (figure 3)							
Vdiff	Vp-p	Vcm	R1	R2	R3	R4	Note
0.45v	0.22v	1.08	33	150	100	100	
0.58	0.28	0.6	33	78.7	137	100	
0.80	0.40	0.6	33	78.7	none	100	ICS874003i-02 input compatible
0.60	0.3	1.2	33	174	140	100	Standard LVDS

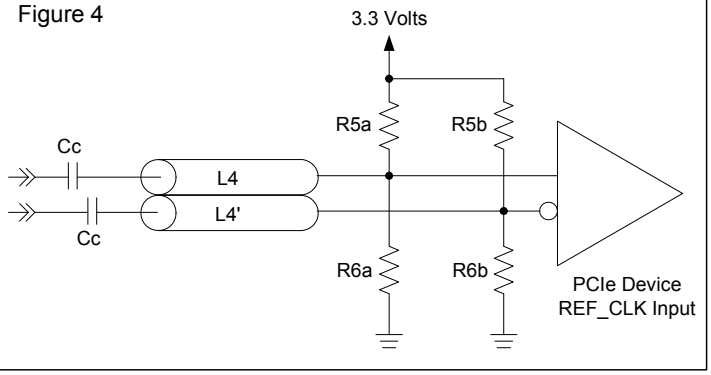
R1a = R1b = R1
R2a = R2b = R2

Figure 3



Cable Connected AC Coupled Application (figure 4)		
Component	Value	Note
R5a, R5b	8.2K 5%	
R6a, R6b	1K 5%	
Cc	0.1 µF	
Vcm	0.350 volts	

Figure 4



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General SMBus Serial Interface Information

How to Write

- Controller (host) sends a start bit
- Controller (host) sends the write address
- IDT clock will **acknowledge**
- Controller (host) sends the beginning byte location = N
- IDT clock will **acknowledge**
- Controller (host) sends the byte count = X
- IDT clock will **acknowledge**
- Controller (host) starts sending Byte **N through Byte N+X-1**
- IDT clock will **acknowledg**e each byte **one at a time**
- Controller (host) sends a Stop bit

Index Block Write Operation			
Controller (Host)			**IDT (Slave/Receiver)**
T	starT bit		
Slave Address			
WR	WRite		
			ACK
Beginning Byte = N			
			ACK
Data Byte Count = X			
			ACK
Beginning Byte N		X Byte	
			ACK
O			
O			O
O			O
			O
Byte N + X - 1			
			ACK
P	stoP bit		

Read Address	Write Address
$DD_{(H)}$	$DC_{(H)}$

How to Read

- Controller (host) will send a start bit
- Controller (host) sends the write address
- IDT clock will **acknowledge**
- Controller (host) sends the beginning byte location = N
- IDT clock will **acknowledge**
- Controller (host) will send a separate start bit
- Controller (host) sends the read address
- IDT clock will **acknowledge**
- IDT clock will send the data byte count = X
- IDT clock sends Byte **N+X-1**
- IDT clock sends **Byte 0 through Byte X (if $X_{(H)}$ was written to Byte 8)**
- Controller (host) will need to acknowledge each byte
- Controller (host) will send a not acknowledge bit
- Controller (host) will send a stop bit

Index Block Read Operation			
Controller (Host)			**IDT (Slave/Receiver)**
T	starT bit		
Slave Address			
WR	WRite		
			ACK
Beginning Byte = N			
			ACK
RT	Repeat starT		
Slave Address			
RD	ReaD		
			ACK
			Data Byte Count=X
ACK			
		X Byte	Beginning Byte N
ACK			
			O
O			O
O			O
O			
			Byte N + X - 1
N	Not acknowledge		
P	stoP bit		

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SMBus Table: Frequency Select Register, READ/WRITE ADDRESS (DC/DD)

Byte 0	Pin #	Name	Control Function	Type	0	1	Default
Bit 7	-	PD_Mode	PD# drive mode	RW	driven	Hi-Z	0
Bit 6	-	STOP_Mode	DIF_Stop# drive mode	RW	driven	Hi-Z	0
Bit 5	-	PD_Polarity	Select PD polarity	RW	Low	High	0
Bit 4	-	Reserved	Reserved	RW	Reserved		X
Bit 3	-	BYPASS#1	BYPASS#/PLL1	RW	See Bypass Readback Table		Input
Bit 2	-	PLL_BW#	Select PLL BW	RW	High BW	Low BW	1
Bit 1	-	BYPASS#0	BYPASS#/PLL0	RW	See Bypass Readback Table		Input
Bit 0	-	SRC_DIV#	SRC Divide by 2 Select	RW	x/2	x/1	1

SMBus Table: Output Control Register

Byte 1	Pin #	Name	Control Function	Type	0	1	Default
Bit 7	42,41	DIF_7	Output Enable	RW	Disable	Enable	1
Bit 6	38,37	DIF_6	Output Enable	RW	Disable	Enable	1
Bit 5	34,33	DIF_5	Output Enable	RW	Disable	Enable	1
Bit 4	30,29	DIF_4	Output Enable	RW	Disable	Enable	1
Bit 3	20,21	DIF_3	Output Enable	RW	Disable	Enable	1
Bit 2	16,17	DIF_2	Output Enable	RW	Disable	Enable	1
Bit 1	12,13	DIF_1	Output Enable	RW	Disable	Enable	1
Bit 0	8,9	DIF_0	Output Enable	RW	Disable	Enable	1

NOTE: The SMBus Output Enable Bit must be '1' AND the respective OE pin must be active for the output to run!

SMBus Table: OE Pin Control Register

Byte 2	Pin #	Name	Control Function	Type	0	1	Default
Bit 7	42,41	DIF_7	DIF_7 Stoppable with DIFSTOP	RW	Free-run	Stoppable	0
Bit 6	38,37	DIF_6	DIF_6 Stoppable with DIFSTOP	RW	Free-run	Stoppable	0
Bit 5	34,33	DIF_5	DIF_5 Stoppable with DIFSTOP	RW	Free-run	Stoppable	0
Bit 4	30,29	DIF_4	DIF_4 Stoppable with DIFSTOP	RW	Free-run	Stoppable	0
Bit 3	20,21	DIF_3	DIF_3 Stoppable with DIFSTOP	RW	Free-run	Stoppable	0
Bit 2	16,17	DIF_2	DIF_2 Stoppable with DIFSTOP	RW	Free-run	Stoppable	0
Bit 1	12,13	DIF_1	DIF_1 Stoppable with DIFSTOP	RW	Free-run	Stoppable	0
Bit 0	8,9	DIF_0	DIF_0 Stoppable with DIFSTOP	RW	Free-run	Stoppable	0

SMBus Table: Reserved Register

Byte 3	Pin #	Name	Control Function	Type	0	1	Default
Bit 7		Reserved					X
Bit 6		Reserved					X
Bit 5		Reserved					X
Bit 4		Reserved					X
Bit 3		Reserved					X
Bit 2		Reserved					X
Bit 1		Reserved					X
Bit 0		Reserved					X

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SMBus Table: Vendor & Revision ID Register

Byte 4	Pin #	Name	Control Function	Type	0	1	Default
Bit 7	-	RID3	REVISION ID	R	-	-	0
Bit 6	-	RID2		R	-	-	0
Bit 5	-	RID1		R	-	-	0
Bit 4	-	RID0		R	-	-	1
Bit 3	-	VID3	VENDOR ID	R	-	-	0
Bit 2	-	VID2		R	-	-	0
Bit 1	-	VID1		R	-	-	0
Bit 0	-	VID0		R	-	-	1

SMBus Table: DEVICE ID

Byte 5	Pin #	Name	Control Function	Type	0	1	Default
Bit 7	-		Device ID 7 (MSB)	RW	Device ID is 82 Hex for 9DB823		1
Bit 6	-		Device ID 6	RW			0
Bit 5	-		Device ID 5	RW			0
Bit 4	-		Device ID 4	RW			0
Bit 3	-		Device ID 3	RW			0
Bit 2	-		Device ID 2	RW			0
Bit 1	-		Device ID 1	RW			1
Bit 0	-		Device ID 0	RW			0

SMBus Table: Byte Count Register

Byte 6	Pin #	Name	Control Function	Type	0	1	Default
Bit 7	-	BC7	Writing to this register configures how many bytes will be read back.	RW	-	-	0
Bit 6	-	BC6		RW	-	-	0
Bit 5	-	BC5		RW	-	-	0
Bit 4	-	BC4		RW	-	-	0
Bit 3	-	BC3		RW	-	-	0
Bit 2	-	BC2		RW	-	-	1
Bit 1	-	BC1		RW	-	-	1
Bit 0	-	BC0		RW	-	-	1

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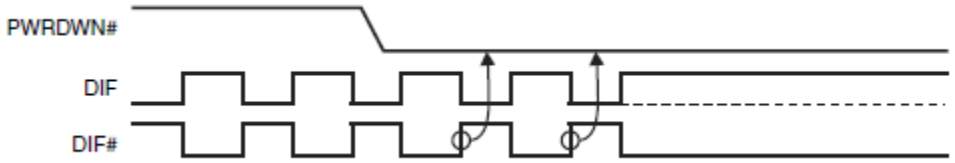
Note: Polarities in timing diagrams are shown OE_INV = 0. They are similar to OE_INV = 1.

PD#, Power Down

The PD# pin cleanly shuts off all clocks and places the device into a power saving mode. PD# must be asserted before shutting off the input clock or power to insure an orderly shutdown. PD is asynchronous active-low input for both powering down the device and powering up the device. When PD# is asserted, all clocks will be driven high, or tri-stated (depending on the PD# drive mode and Output control bits) before the PLL is shut down.

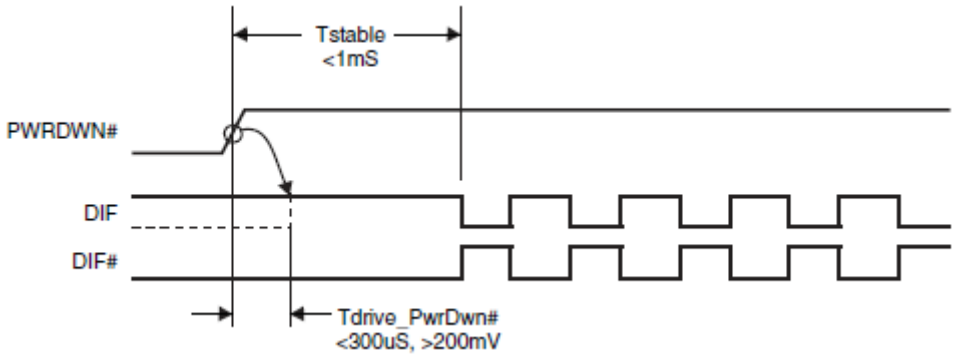
PD# Assertion

When PD# is sampled low by two consecutive rising edges of DIF#, all DIF outputs must be held High, or tri-stated (depending on the PD# drive mode and Output control bits) on the next High-Low transition of the DIF# outputs. When the PD# drive mode bit is set to ‘0’, all clock outputs will be held with DIF driven High with 2 x IREF and DIF# tri-stated. If the PD# drive mode bit is set to ‘1’, both DIF and DIF# are tri-stated.



PD# De-assertion

Power-up latency is less than 1 ms. This is the time from de-assertion of the PD# pin, or VDD reaching 3.3V, or the time from valid SRC_IN clocks until the time that stable clocks are output from the device (PLL Locked). If the PD# drive mode bit is set to ‘1’, all the DIF outputs must driven to a voltage of >200 mV within 300 us of PD# de-assertion.



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DIF_STOP#

The DIF_STOP# signal is an active-low asynchronous input that cleanly stops and starts the DIF outputs. A valid clock must be present on SRC_IN for this input to work properly. The DIF_STOP# signal is de-bounced and must remain stable for two consecutive rising edges of DIF# to be recognized as a valid assertion or de-assertion.

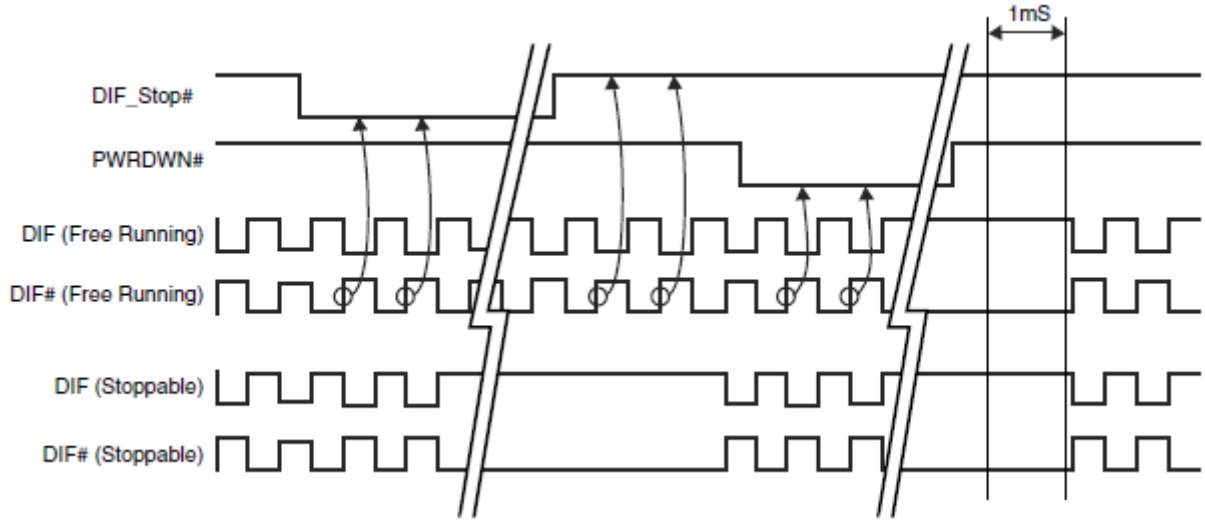
DIF_STOP# - Assertion

Asserting DIF_STOP# causes all DIF outputs to stop after their next transition (if the control register settings allow the output to stop). When the DIF_STOP# drive bit is '0', the final state of all stopped DIF outputs is DIF = High and DIF# = Low. There is no change in output drive current. DIF is driven with 6xIREF. DIF# is not driven, but pulled low by the termination. When the DIF_STOP# drive bit is '1', the final state of all DIF output pins is Low. Both DIF and DIF# are not driven.

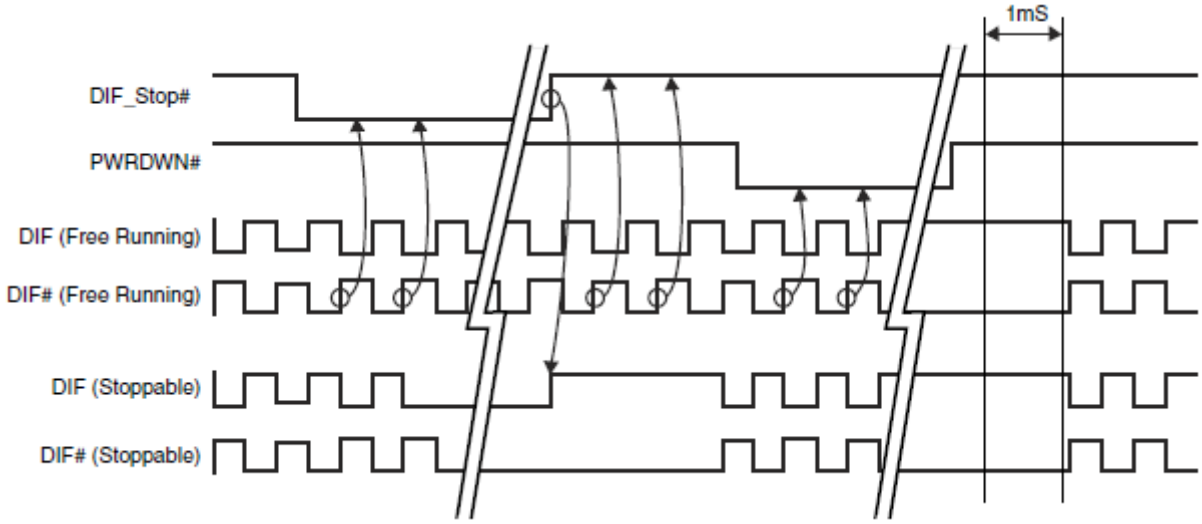
DIF_STOP# - De-assertion (transition from '0' to '1')

All stopped differential outputs resume normal operation in a glitch-free manner. The de-assertion latency to active outputs is 2-6 DIF clock periods, with all DIF outputs resuming simultaneously. If the DIF_STOP# drive control bit is '1' (tri-state), all stopped DIF outputs must be driven High (>200 mV) within 10 ns of de-assertion.

DIF_STOP_1 (Stop_Mode = Driven, PD_Mode = Driven)

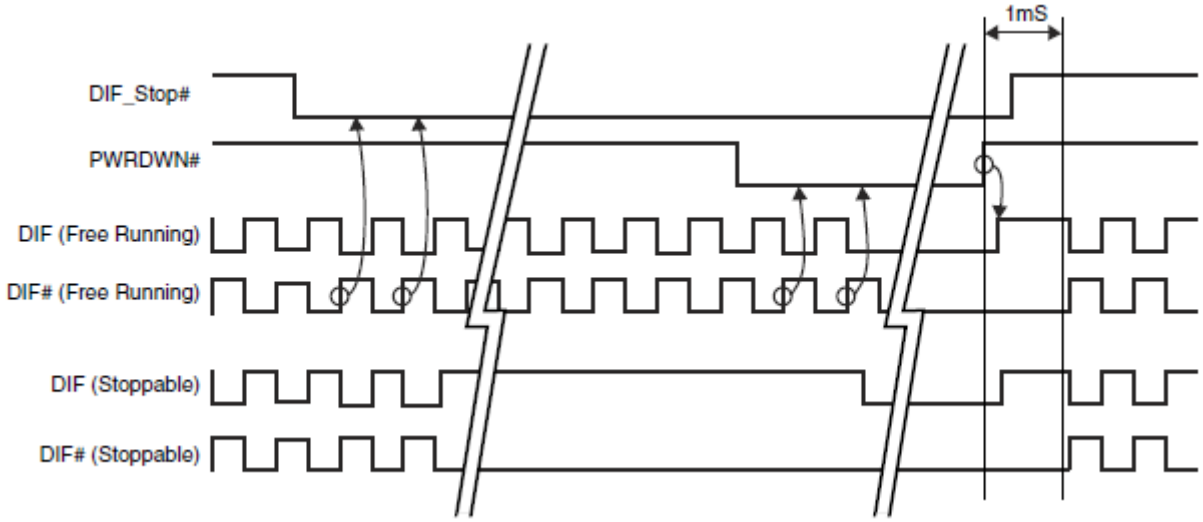


DIF_STOP_2 (Stop_Mode = Tristate, PD_Mode = Driven)

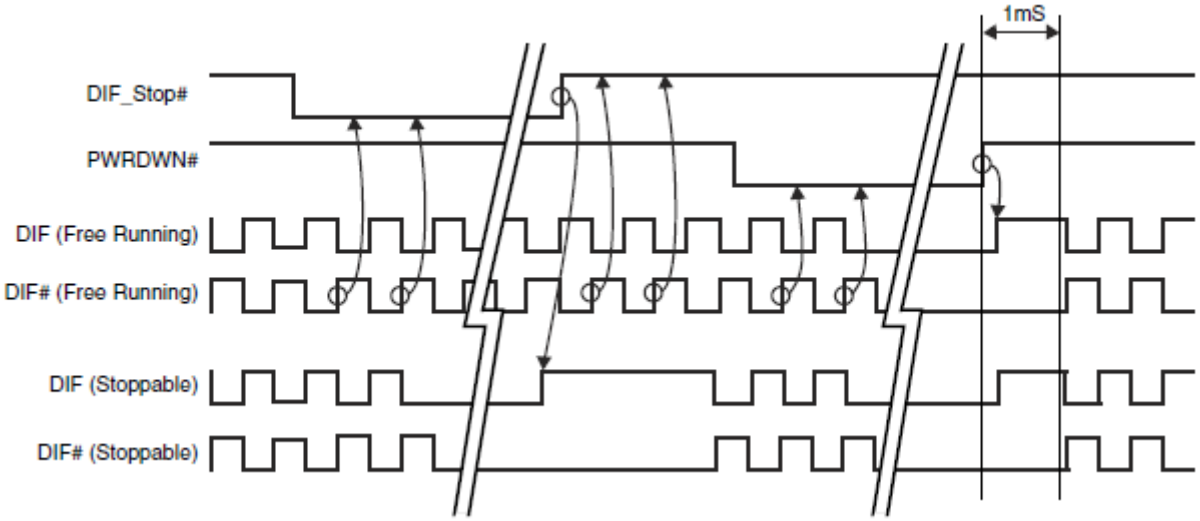


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DIF_STOP_3 (Stop_Mode = Driven, PD_Mode = Tristate)



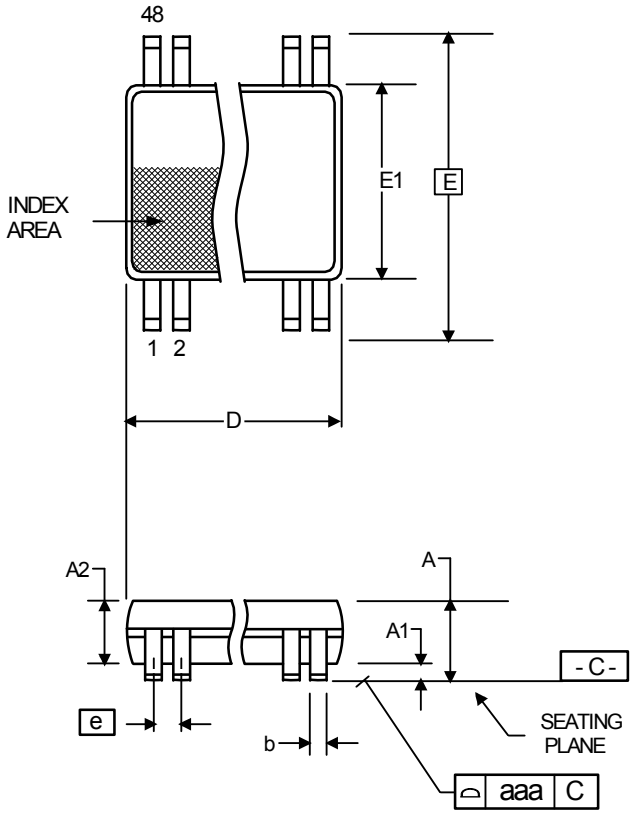
DIF_STOP_4 (Stop_Mode = Tristate, PD_Mode = Tristate)



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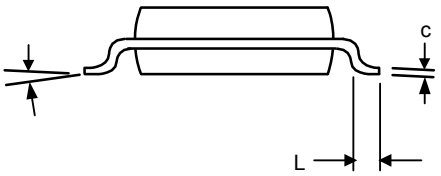
Package Outline and Package Dimensions (48-pin TSSOP, 6.10mm Body, 0.50 Pitch)

Package dimensions are kept current with JEDEC Publication No. 95



	Millimeters		Inches*	
Symbol	**Min**	**Max**	**Min**	**Max**
A	--	1.20	--	0.047
A1	0.05	0.15	0.002	0.006
A2	0.80	1.05	0.032	0.041
b	0.17	0.27	0.007	0.011
c	0.09	0.20	0.0035	0.008
D	12.40	12.60	0.488	0.496
E	8.10 BASIC		0.319 BASIC	
E1	6.00	6.20	0.236	0.244
e	0.50 Basic		0.020 Basic	
L	0.45	0.75	0.018	0.030
α	0°	8°	0°	8°
aaa	--	0.10	--	0.004

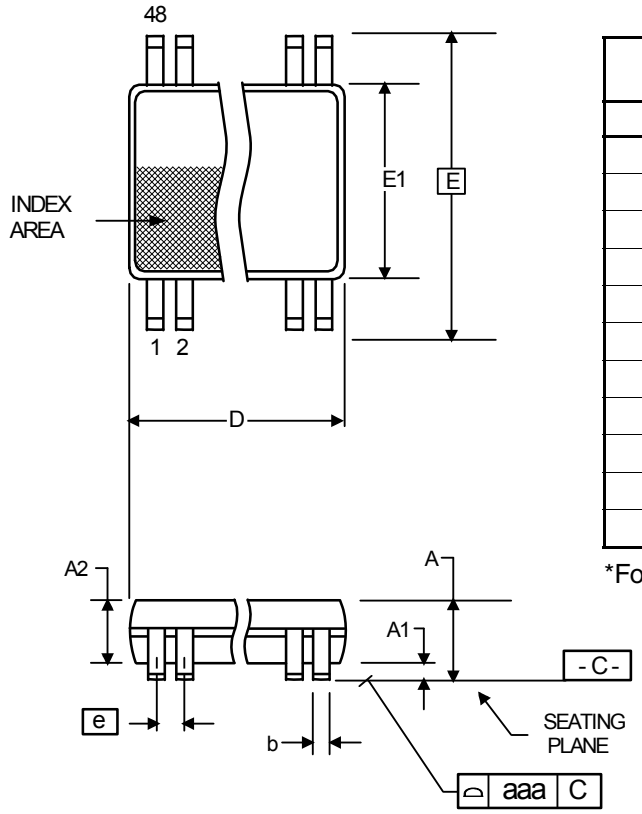
*For reference only. Controlling dimensions in mm.



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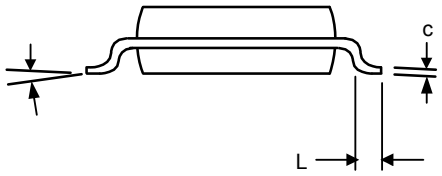
Package Outline and Package Dimensions (48-pin SSOP, 300 mil)

Package dimensions are kept current with JEDEC Publication No. 95



	Millimeters		Inches*	
Symbol	**Min**	**Max**	**Min**	**Max**
A	2.41	2.80	.095	.110
A1	0.20	0.40	.008	.016
b	0.20	0.34	.008	.0135
c	0.13	0.25	.005	.010
D	15.75	16.00	.620	.630
E	10.03	10.68	.395	.420
E1	7.40	7.60	.291	.299
e	0.635 BASIC		0.025 BASIC	
h	0.38	0.64	.015	.025
L	0.50	1.02	.020	.040
α	0°	8°	0°	8°

*For reference only. Controlling dimensions in mm.



Ordering Information

Part / Order Number	Shipping Packaging	Package	Temperature
9DB823BFLF	Tubes	48-pin SSOP	0 to +70°C
9DB823BFLFT	Tape and Reel	48-pin SSOP	0 to +70°C
9DB823BGLF	Tubes	48-pin TSSOP	0 to +70°C
9DB823BGLFT	Tape and Reel	48-pin TSSOP	0 to +70°C

"LF" suffix to the part number are the Pb-Free configuration and are RoHS compliant.

"B" is the device revision designator (will not correlate with the datasheet revision).

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Revision History

Rev.	Issue Date	Description	Page #
A	10/1/2008	1. Updated Electrical Characteristics to add propagation delay and phase noise information. 2. Added SMBus electrical characteristics 3. Added foot note about DIF input running in order for the SMBus interface to work 4. Added foot note to Byte 1 about functionality of OE bits and OE pins 5. Updated clock periods to reflect +/-100ppm input clock tolerance (CK410B+/CK420BQ/CK505). 6. Changed SRC_Stop references to DIF_Stop references for consistency..	Various
B	10/7/2008	Corrected Common Dimensions.	19-20
C	2/4/2010	1. Corrected Polarity of Power Down pin when OE_INV = 1. Power Down is always active low (or PD#). This is a difference from the 9DB803D.	Various
D	8/31/2010	1. Corrected Termination drawings/tables 2. Removed "Polarity Inversion Pin List" table.	Various
E	5/9/2011	1. Update pin 2 pin-name and pin description from VDD to VDDR. This highlights that optimal peformance is obtained by treating VDDR as in analog pin. This is a document update only, there is no silicon change.	Various
F	9/18/2012	Updated Byte 2, bits 0~7 per char review. Outputs can be programmed with Byte 2 to be Stoppable or Free-Run with DIF_Stop pin, not the OE pins.	14

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