9DBL411B

Four Output Low Power Differential Fanout Buffer for PCI Express Gen1, Gen2, Gen3, and QPI

The 9DBL411B is a four output, lower power differential buffer. Each output has its own OE# pin. The device has a maximum operating frequency of 150MHz.

Applications

- PCI-Express Gen1-2-3 or QPI fanout buffer

Key Specifications

- Output cycle-cycle jitter: < 15ps additive
- Output to output skew: < 50ps

Features

- Low power differential outputs for PCI-Express and QPI clocks
- Power down mode when all OE# are high
- Available in commercial (0 to +70°C) and industrial (-40°C to +85°C) temperature ranges
- Available in 20-VFQFPN or 20-TSSOP packages

Output Features

- Four low power differential output pairs
- Individual OE# control of each output pair

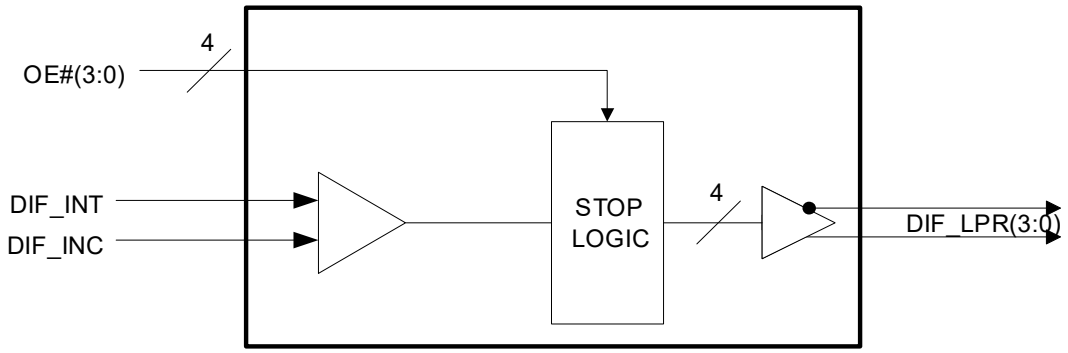


Figure 1. Block Diagram

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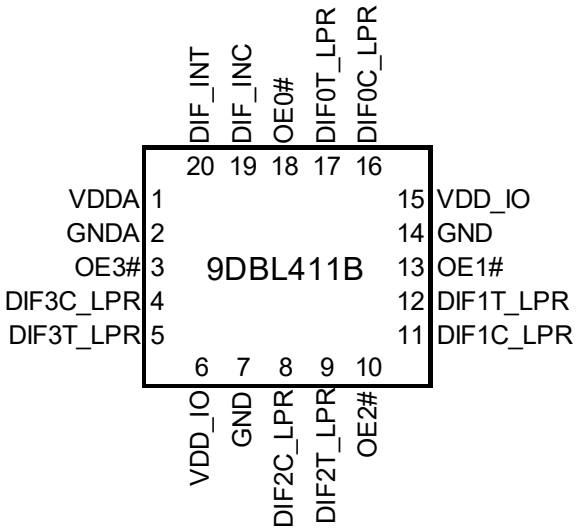
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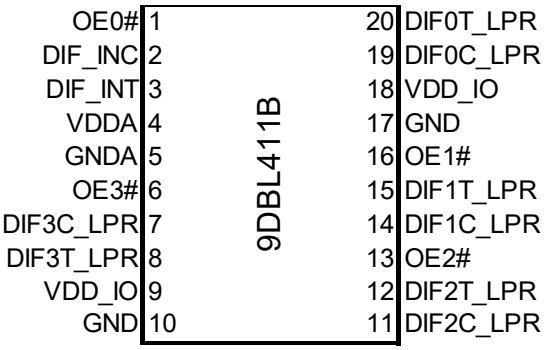
1. Pin Information

1.1 Pin Assignments

1.1.1 20-VFQFPN



1.1.2 20-TSSOP



1.2 Pin Descriptions

1.2.1 20-VFQFPN

Table 1. 20-VFQFPN Pin Descriptions

Pin Number	Pin Name	Pin Type	Description
1	VDDA	Power	3.3V Power for the Analog core.
2	GNDA	GND	Ground for the Analog core.
3	OE3#	Input	Output Enable for DIF3 output. Control is as follows: 0 = enabled, 1 = Low-Low
4	DIF3C_LPR	Output	Complement clock of low power differential clock pair (no 50ohm shunt resistor to GND needed).
5	DIF3T_LPR	Output	True clock of low power differential clock pair (no 50ohm shunt resistor to GND needed).
6	VDD_IO	Power	Power supply for low power differential outputs, nominal 1.05V to 3.3V.

Table 1. 20-VFQFPN Pin Descriptions (Cont.)

Pin Number	Pin Name	Pin Type	Description
7	GND	GND	Ground pin.
8	DIF2C_LPR	Output	Complement clock of low power differential clock pair (no 50ohm shunt resistor to GND needed).
9	DIF2T_LPR	Output	True clock of low power differential clock pair (no 50ohm shunt resistor to GND needed).
10	OE2#	Input	Output Enable for DIF2 output. Control is as follows: 0 = enabled, 1 = Low-Low
11	DIF1C_LPR	Output	Complement clock of low power differential clock pair (no 50ohm shunt resistor to GND needed).
12	DIF1T_LPR	Output	True clock of low power differential clock pair (no 50ohm shunt resistor to GND needed).
13	OE1#	Input	Output Enable for DIF1 output. Control is as follows: 0 = enabled, 1 = Low-Low
14	GND	GND	Ground pin.
15	VDD_IO	Power	Power supply for low power differential outputs, nominal 1.05V to 3.3V.
16	DIF0C_LPR	Output	Complement clock of low power differential clock pair (no 50ohm shunt resistor to GND needed).
17	DIF0T_LPR	Output	True clock of low power differential clock pair (no 50ohm shunt resistor to GND needed).
18	OE0#	Input	Output Enable for DIF0 output. Control is as follows: 0 = enabled, 1 = Low-Low
19	DIF_INC	Input	Complement side of differential input clock.
20	DIF_INT	Input	True side of differential input clock.

1.2.2 20-TSSOP

Table 2. 20-TSSOP Pin Descriptions

Pin Number	Pin Name	Pin Type	Description
1	OE0#	IN	Output Enable for DIF0 output. Control is as follows: 0 = enabled, 1 = Low-Low
2	DIF_INC	IN	Complement side of differential input clock.
3	DIF_INT	IN	True side of differential input clock.
4	VDDA	PWR	3.3V Power for the Analog core.
5	GNDA	GND	Ground for the Analog core.
6	OE3#	IN	Output Enable for DIF3 output. Control is as follows: 0 = enabled, 1 = Low-Low
7	DIF3C_LPR	OUT	Complement clock of low power differential clock pair (no 50ohm shunt resistor to GND needed).
8	DIF3T_LPR	OUT	True clock of low power differential clock pair (no 50ohm shunt resistor to GND needed).
9	VDD_IO	PWR	Power supply for low power differential outputs, nominal 1.05V to 3.3V.
10	GND	GND	Ground pin.

Table 2. 20-TSSOP Pin Descriptions (Cont.)

Pin Number	Pin Name	Pin Type	Description
11	DIF2C_LPR	OUT	Complement clock of low power differential clock pair (no 50ohm shunt resistor to GND needed).
12	DIF2T_LPR	OUT	True clock of low power differential clock pair (no 50ohm shunt resistor to GND needed).
13	OE2#	IN	Output Enable for DIF2 output. Control is as follows: 0 = enabled, 1 = Low-Low
14	DIF1C_LPR	OUT	Complement clock of low power differential clock pair (no 50ohm shunt resistor to GND needed).
15	DIF1T_LPR	OUT	True clock of low power differential clock pair (no 50ohm shunt resistor to GND needed).
16	OE1#	IN	Output Enable for DIF1 output. Control is as follows: 0 = enabled, 1 = Low-Low
17	GND	GND	Ground pin.
18	VDD_IO	PWR	Power supply for low power differential outputs, nominal 1.05V to 3.3V.
19	DIF0C_LPR	OUT	Complement clock of low power differential clock pair (no 50ohm shunt resistor to GND needed).
20	DIF0T_LPR	OUT	True clock of low power differential clock pair (no 50ohm shunt resistor to GND needed).

1.3 Power Groups

Pin Number (VFQFPN)		Description
VDD	GND	
6, 15	7, 14	VDD_IO for DIF(3:0)
1	2	3.3V Analog VDD & GND

Pin Number (TSSOP)		Description
VDD	GND	
9, 18	10, 17	VDD_IO for DIF(3:0)
4	5	3.3V Analog VDD & GND

2. Specifications

2.1 Absolute Maximum Ratings

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions can adversely impact product reliability and result in failures not covered by warranty.

Parameter	Symbol	Test Conditions	Minimum	Maximum	Unit
Maximum Supply Voltage [1][2]	VDDA	Core Supply Voltage	-	4.6	V
Maximum Supply Voltage [1][2]	VDD_IO	Low-Voltage differential I/O supply.	0.99	3.8	V
Maximum Input Voltage [1][2][3]	V_{IH}	3.3V LVCMOS inputs.	-	4.6	V
Minimum Input Voltage [1][2]	V_{IL}	Any input.	Vss - 0.5	-	V
Ambient Operating Temp	TambCOM [1]	Commercial range.	0	70	°C
	TambIND [1]	Industrial range.	-40	85	°C
Storage Temperature [1][2]	Ts	-	-65	150	°C

1. Confirmed by design and characterization, not 100% tested in production.
2. Operation under these conditions is neither implied, nor guaranteed.
3. Maximum input voltage is not to exceed maximum VDD.

2.2 ESD Ratings

ESD Model/Test	Rating	Unit
Input ESD Protection (ESD prot), Human Body Model	2000	V

2.3 Electrical Specifications

All measurements use 9LRS3187B as clock source and R_S = 33ohms, C_L = 2pF test load.

Table 3. Input/Supply/Common Output Parameters

Parameter	Symbol	Test Conditions	Min	Max	Unit
Supply Voltage [1]	VDDA	Supply voltage.	3.000	3.600	V
Supply Voltage [1]	VDDxxx_IO	Low-Voltage differential I/O supply.	0.99	3.600	V
Input High Voltage [1]	V_{IHSE}	Single-ended inputs.	2	V_{DD} + 0.3	V
Input Low Voltage [1]	V_{ILSE}	Single-ended inputs.	V_{SS} - 0.3	0.8	V
Differential Input High Voltage [1]	V_{IHDIF}	Differential inputs (single-ended measurement).	600	1.15	V
Differential Input Low Voltage [1]	V_{ILDIF}	Differential inputs (single-ended measurement).	V_{SS} - 0.3	300	mV
Input Slew Rate–DIF_IN [2]	dv/dt	Measured differentially.	0.4	8	V/ns
Input Leakage Current [1]	I_{IN}	V_{IN} = V_{DD} , V_{IN} = GND.	-5	5	µA
Operating Supply Current [1]	$I_{DD_3.3V}$	VDDA supply current.	-	20	mA
	$I_{DD_IO_133M}$	VDD_IO supply at f_{OP} = 133MHz.	-	20	mA

Table 3. Input/Supply/Common Output Parameters (Cont.)

Parameter	Symbol	Test Conditions	Min	Max	Unit
Power Down Current (All OE# pins High) [1]	$I_{DD_SB_3.3V}$	VDDA supply current, Input stopped, OE# pins all high.	-	750	µA
	I_{DD_SBIO}	VDD_IO supply, Input stopped, OE# pins all high.	-	150	µA
Input Frequency [2]	F_i	V_{DD} = 3.3V.	15	150	MHz
Pin Inductance [1]	L_{pin}	-	-	7	nH
Input Capacitance [1]	C_{IN}	Logic Inputs.	1.5	5	pF
	C_{OUT}	Output pin capacitance.	-	6	pF
OE# Latency (at least one OE# is low) [1]	$T_{OE\#LAT}$	Number of clocks to enable or disable output from assertion/deassertion of OE#.	1	3	periods
Clock Stabilization Time (from all OE# high to first OE# low). [1]	T_{STAB}	Delay from assertion of first OE# to first clock out (assumes input clock running and device in power down state).	-	150	ns
Tdrive_OE# [1]	$T_{DROE\#}$	Output enable after OE# de-assertion.	-	10	ns
Tfall_OE# [1]	T_{FALL}	Fall/rise time of OE# inputs.	-	5	ns
Trise_OE# [1]	T_{RISE}	-	-	5	ns

1. Confirmed by design and characterization, not 100% tested in production.
2. Slew rate measured through Vswing centered around differential zero.

Table 4. AC Electrical Characteristics–DIF Low Power Differential Outputs

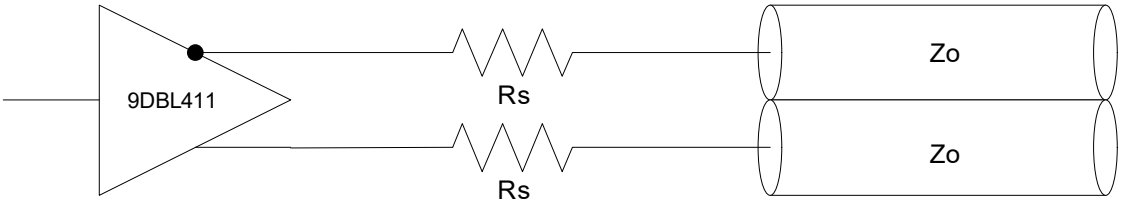
Parameter	Symbol	Test Conditions	Min	Max	Unit
Rising Edge Slew Rate [1][2]	t_{SLR}	Differential measurement.	1.5	4	V/ns
Falling Edge Slew Rate [1][2]	t_{FLR}	Differential measurement.	1.5	4	V/ns
Slew Rate Variation [1]	t_{SLVAR}	Single-ended measurement.	-	20	%
Maximum Output Voltage [1]	V_{HIGH}	Includes overshoot.	-	1150	mV
Minimum Output Voltage [1]	V_{LOW}	Includes undershoot.	-300	-	mV
Differential Voltage Swing [1]	V_{SWING}	Differential measurement.	1200	-	mV
Crossing Point Voltage [1][3][4]	V_{XABS}	Single-ended measurement.	300	550	mV
Crossing Point Variation [1][3][5]	$V_{XABSVAR}$	Single-ended measurement.	-	140	mV
Duty Cycle Distortion [1][6]	$D_{CYCDIS0}$	Differential measurement, f_{IN} < =133.33MHz.	-	3	%
Additive Cycle to Cycle Jitter [1]	$DIFJ_{C2CADD}$	Differential measurement, Additive.	-	15	ps
DIF[3:0] Skew [1]	DIF_{SKEW}	Differential measurement.	-	50	ps
Propagation Delay [1]	t_{PD}	Input to output delay.	2.5	3.5	ns
Additive Phase Jitter–PCIe Gen1 [1][7]	t_{phase_add} PCIG1	1.5MHz < 22MHz.	-	6	ps Pk-Pk
Additive Phase Jitter–PCIe Gen2 High Band [1][7]	t_{phase_add} PCIG2HI	High Band is 1.5MHz to Nyquist (50MHz).	-	0.16	ps RMS
Additive Phase Jitter PCIe Gen2 Low Band [1][7]	t_{phase_add} PCIG2LO	Low Band is 10kHz to 1.5MHz.	-	0.07	ps RMS

Table 4. AC Electrical Characteristics–DIF Low Power Differential Outputs (Cont.)

Parameter	Symbol	Test Conditions	Min	Max	Unit
Additive Phase Jitter PCIe Gen3 [1][7]	t_{phase_add} PCIG2LO	2M–4M, 2M–5M filter.	-	0.2	ps RMS
Additive Phase Jitter QPI 133 (6.4GBs, 12 UI) [1][7]	t_{phase_add} QPI6G4	11MHz to 33MHz.	-	0.04	ps RMS

1. Confirmed by design and characterization, not 100% tested in production.
2. Slew rate measured through Vswing centered around differential zero.
3. Vxabs is defined as the voltage where CLK = CLK#.
4. Only applies to the differential rising edge (CLK rising and CLK# falling).
5. Defined as the total variation of all crossing voltages of CLK rising and CLK# falling. Matching applies to rising edge rate of CLK and falling edge of CLK#. It is measured using a ±75mV window centered on the average cross point where CLK meets CLK#.
6. This figure refers to the maximum distortion of the input wave form.
7. The 9DBL411B has no PLL, so the part itself contributes very little jitter to the input clock. But this also means that the 9DBL411 cannot "de-jitter" a noisy input clock. Values calculated per PCI SIG and per Intel Clock Jitter tool version 1.5.

3. Terminations



Zo – 17 = Rs (ohms), where Zo is the single-ended intrinsic impedance of the board transmission line. Single-ended intrinsic impedance is ½ that of the differential impedance.

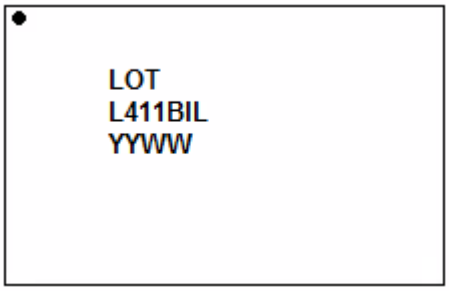
Single-ended Impedance (Z_O)	Rs 5% Tolerance	Rs 2% Tolerance	Notes
50	33	33.2	In general, 5% resistors may be used. All values are in ohms.
45	27	27.4	
42.5	24 or 27	24.9	

4. Package Outline Drawings

The package outline drawings are located at the end of this document and are accessible from the Renesas website (see Ordering Information for POD links). The package information is the most current data available and is subject to change without revision of this document.

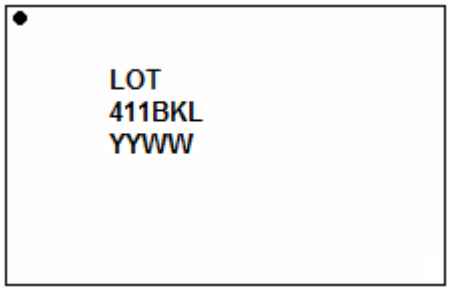
5. Marking Diagrams

5.1 20-VFQFPN



9DBL411BKILF

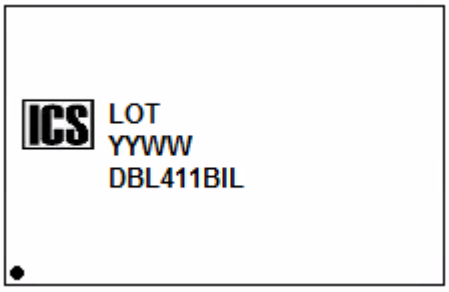
- Line 1: “LOT” designates the lot number.
- Line 2: truncated part number.
  - “I” designates industrial temperature range.
- Line 3: “YYWW” is the last two digits of the year and work week that the part was assembled.



9DBL411BKLF

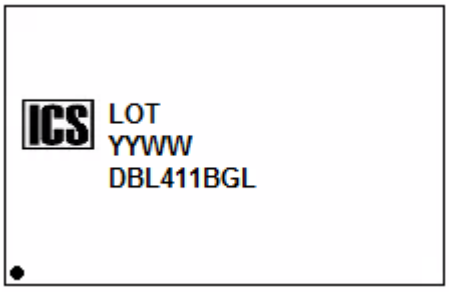
- Line 1: “LOT” designates the lot number.
- Line 2: truncated part number.
- Line 3: “YYWW” is the last two digits of the year and work week that the part was assembled.

5.2 20-TSSOP



9DBL411BGILF

- Line 1: “LOT” designates the lot number.
- Line 2: “YYWW” is the last two digits of the year and work week that the part was assembled.
- Line 3: truncated part number.
  - “I” designates industrial temperature range.



9DBL411BGLF

- Line 1: “LOT” designates the lot number.
- Line 2: “YYWW” is the last two digits of the year and work week that the part was assembled.
- Line 3: truncated part number.

6. Ordering Information

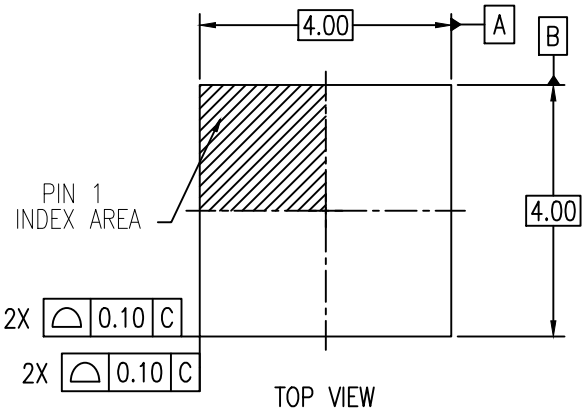
Part Number	Package Description	Carrier Type	Temperature Range
9DBL411BKILF	20-VFQFPN, 4.0 × 4.0 mm	Tubes	-40 to +85°C
9DBL411BKILFT		Tape & Reel	
9DBL411BKLF	20-VFQFPN, 4.0 × 4.0 mm	Tubes	0 to +70°C
9DBL411BKLFT		Tape & Reel	
9DBL411BGILF	20-TSSOP, 4.4mm body, 0.65mm pitch	Tubes	-40 to +85°C
9DBL411BGILFT		Tape & Reel	
9DBL411BGLF	20-TSSOP, 4.4mm body, 0.65mm pitch	Tubes	0 to +70°C
9DBL411BGLFT		Tape & Reel	

“LF” suffix to the part number are the Pb-Free configuration and are RoHS compliant.

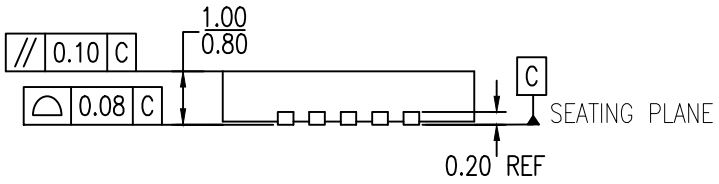
“B” is the device revision designator (will not correlate to the datasheet revision).

7. Revision History

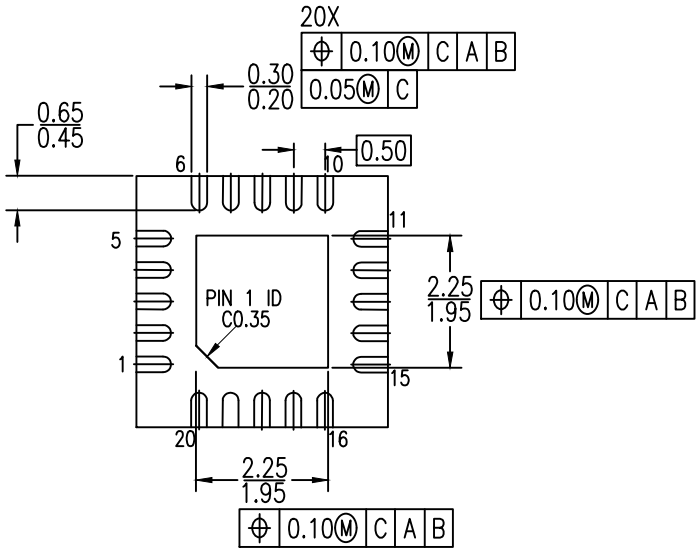
Revision	Date	Description
1.07	Sep 30, 2022	▪ Reformatted to the latest Renesas template. All specifications and characteristics remain unchanged. ▪ Replaced references to MLF with VFQFPN. ▪ Updated Package Outline Drawings section. ▪ Updated Marking Diagrams section. ▪ Updated Ordering Information table with POD links.
-	Sep 25, 2018	Replaced “Trays” with “Tubes” in Ordering Information.
-	Aug 16, 2013	Correct typo on top-side marking for MLF (commercial temp.) from “L411BKL” to “411BKL”.
-	Jun 28, 2012	Typo in “Differential Input Low Voltage” units; changed “V” to “mV”.
-	Mar 22, 2012	Updated phase jitter table for PCIe Gen3.
-	Oct 18, 2010	Updated supply voltage min/max ratings.
-	Apr 23, 2010	Changed input frequency from 33MHz minimum to 15MHz minimum.
-	Jan 8, 2010	Initial release.



TOP VIEW



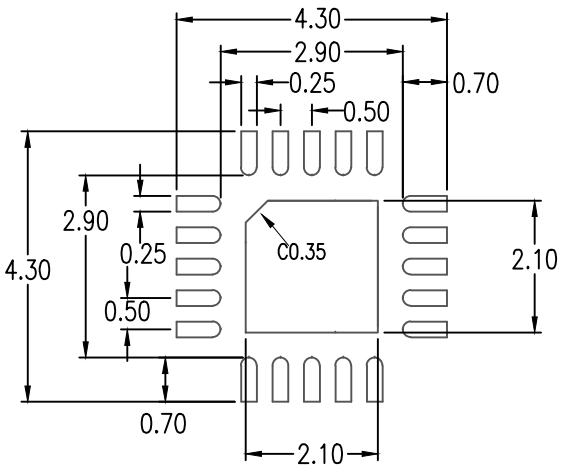
SIDE VIEW



BOTTOM VIEW

NOTES:
1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. ALL DIMENSIONING AND TOLERANCING CONFROM TO ANSI Y14.5M–1982.

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RECOMMENDED LAND PATTERN DIMENSION

NOTES:
1. ALL DIMENSIONING AND TOLERANCING CONFORM TO ANSI Y14.5M–1994
2. ALL DIMENSONS ARE IN MILLIMETERS
3. LAND PATTERN RECOMMENDATION PER IPC–7351B GENERIC REQUIREMENT FOR SURFACE MOUNT DESIGN AND LAND PATTERN

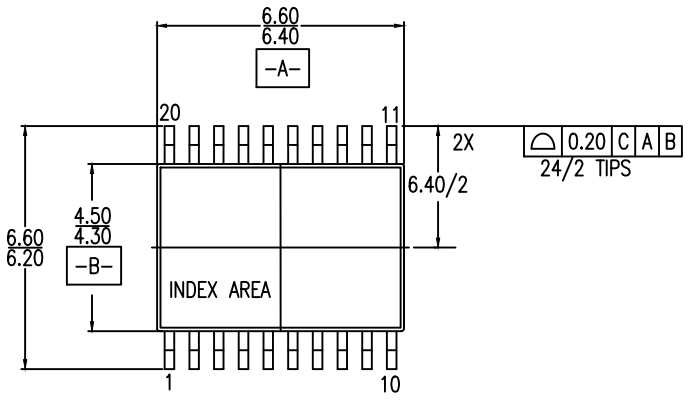
Package Revision History		
Date Created	Rev No.	Description
March 1, 2018	Rev 01	New Format, Add P1, Re-calculate Land Pattern
May 19, 2016	Rev 00	Initial Release

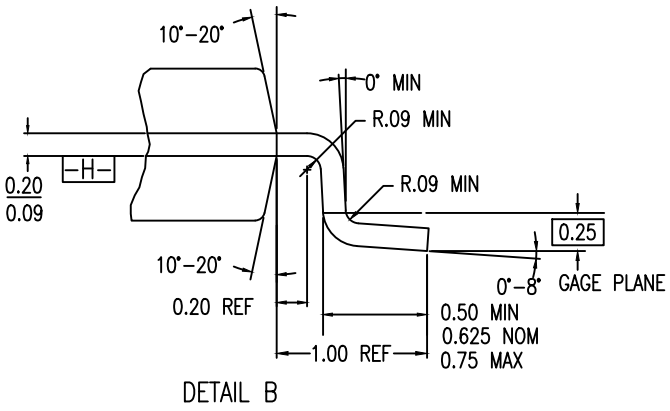
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20-TSSOP Package Outline Drawing

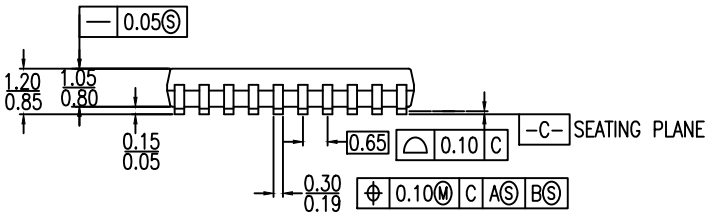
4.4 mm Body 0.65mm Pitch

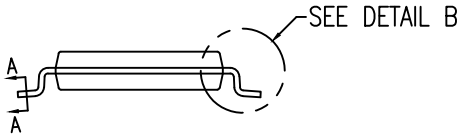
PGG20D1, PSC-4770-01, Rev 00, Page 1

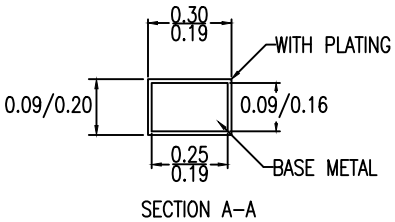




DETAIL B





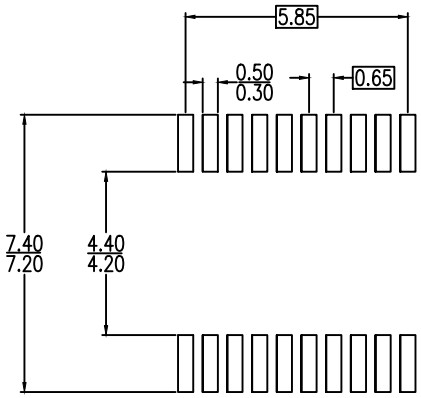


SECTION A-A

NOTES:

1. ALL DIMENSIONING AND TOLERANCING CONFORM TO ANSI Y14.5M-1982
2. ALL DIMENSION ARE IN MM.

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RECOMMENDED LAND PATTERN DIMENSIONS

NOTES:

1. ALL DIMENSIONS ARE IN MILLIMETERS

Package Revision History		
Date Created	Rev No.	Description
July 24, 2018	Rev 00	Initial Release

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Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,
Koto-ku, Tokyo 135-0061, Japan
www.renesas.com

Contact Information

For further information on a product, technology, the most up-to-date version of a document, or your nearest sales office, please visit:
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