Eighteen Output Differential Buffer w/2 input mux for PCIe Gen1/2/3

9EX21831

Recommended Application:

18 Output PCIe G3 Differential Buffer with 2:1 input mux

General Description

The ICS9EX21831 provides 18 output clocks for PCIe Gen1/2/3 applications. The 9EX21831 has 4 selectable SMBus addresses, and dedicated CKPWRGD/PD# and VDDA pins for easy board design. A differential clock from a CK410B+ or CK420BQ main clock generator, such as the ICS932S421, drives the ICS9EX21831. In fanout mode, the 9EX21831 provides outputs up to 166MHz.

Output Features:

- 18 - 0.7V current mode differential HCSL output pairs

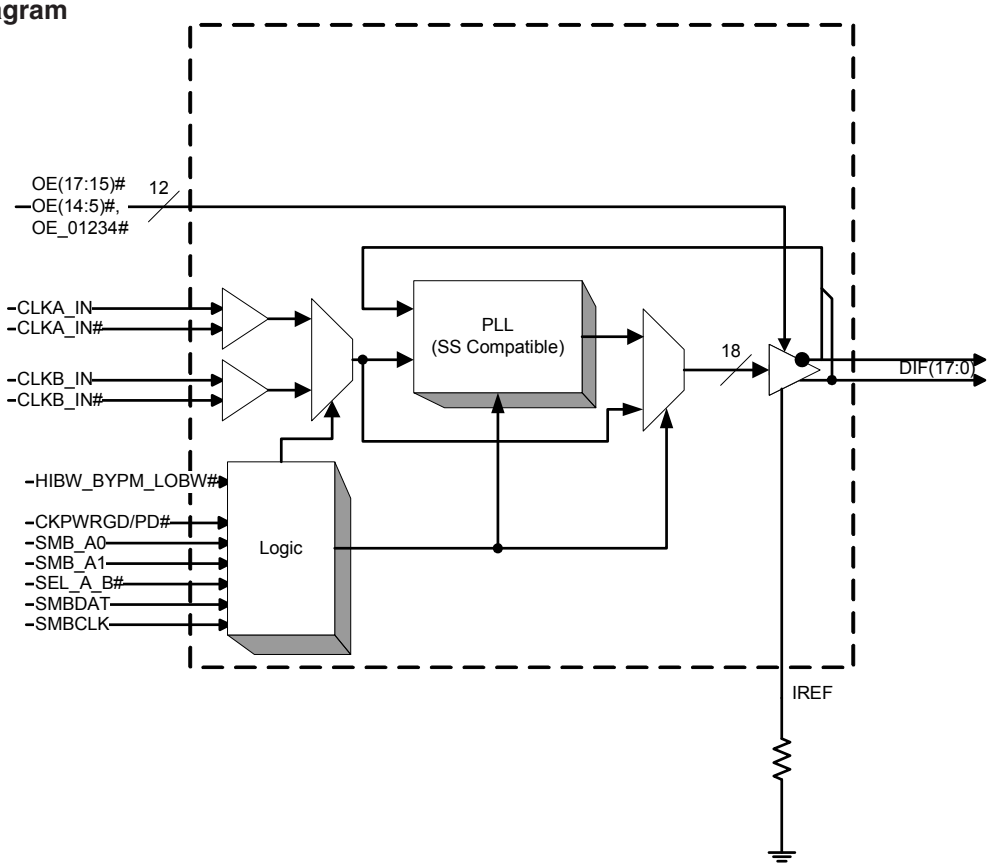
Features/Benefits:

- Pin compatible to 9EX21801/ Easy PCIe Gen3 upgrade
- 4 Selectable SMBus Addresses/Mulitple devices can share the same SMBus Segment
- 10 dedicated and 2 group OE# pins/Hardware control of the outputs
- PLL or bypass mode/PLL can dejitter incoming clock
- Selectable PLL bandwidth/minimizes jitter peaking in downstream PLL's
- Spread Spectrum Compatible/tracks spreading input clock for low EMI
- SMBus Interface/unused outputs can be disabled
- Undriven differential outputs in Power Down mode/ Easy power management

Key Specifications:

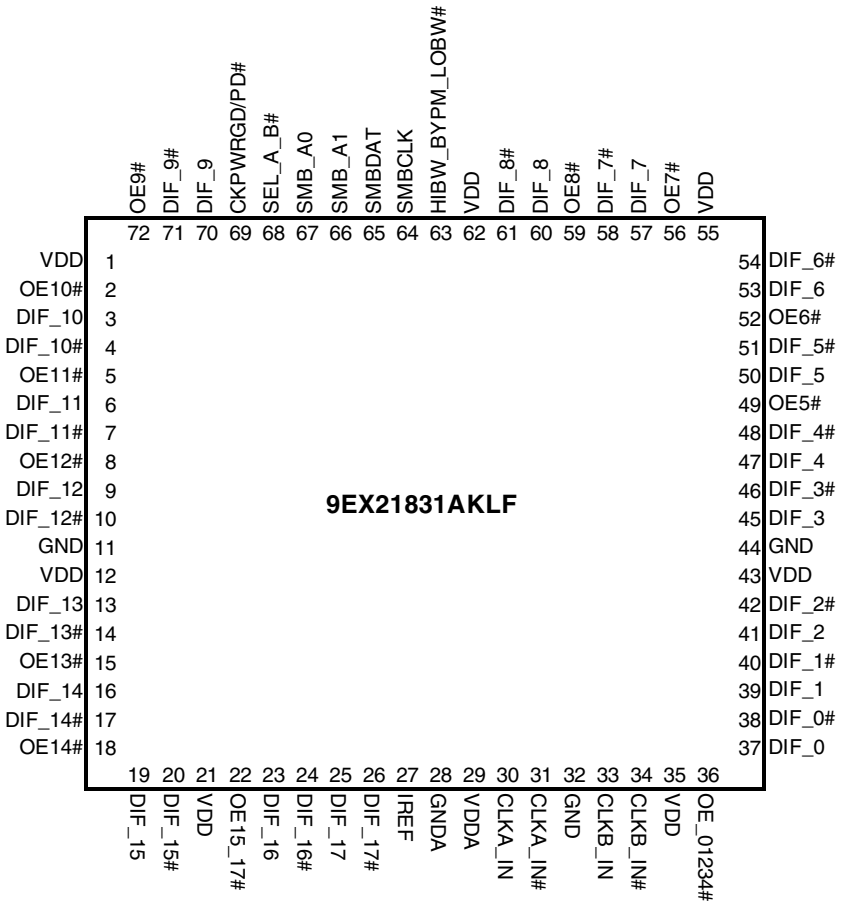
- Cycle-to-cycle jitter <50ps
- Output-to-output skew < 150 ps
- PCIe Gen3 phase jitter < 1.0ps RMS

Functional Block Diagram



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Pin Configuration



Power Groups

Pin Number		Description
VDD	GND	
29	28	Main PLL, Analog
35	32	Input buffers
1,12,21,35,43, 55,62	11,32,44	DIF clocks

HIBW_BYPM_LOBW# Selection (Pin 63)

State	Voltage	Mode
Low	<0.8V	Low BW
Mid	1.2<Vin<1.8V	Bypass
High	Vin > 2.0V	High BW

SMBus Address Selection (pins 66, 67)

SMB_A1	SMB_A0	Address
0	0	D4
0	1	D6
1	0	D8
1	1	DA

Power Down Functionality

INPUTS		OUTPUTS	PLL State
CKPWRGD/PD#	Input	DIF_x	
1	Running	Running	ON
0	X	Hi-Z	OFF

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Pin Description

PIN #	PIN NAME	PIN TYPE	DESCRIPTION
1	VDD	PWR	Power supply, nominal 3.3V
2	OE10#	IN	Active low input for enabling DIF pair 10. 1 = tri-state outputs, 0 = enable outputs
3	DIF_10	OUT	0.7V differential true clock output
4	DIF_10#	OUT	0.7V differential complement clock output
5	OE11#	IN	Active low input for enabling DIF pair 11. 1 = tri-state outputs, 0 = enable outputs
6	DIF_11	OUT	0.7V differential true clock output
7	DIF_11#	OUT	0.7V differential complement clock output
8	OE12#	IN	Active low input for enabling DIF pair 12. 1 = tri-state outputs, 0 = enable outputs
9	DIF_12	OUT	0.7V differential true clock output
10	DIF_12#	OUT	0.7V differential complement clock output
11	GND	PWR	Ground pin.
12	VDD	PWR	Power supply, nominal 3.3V
13	DIF_13	OUT	0.7V differential true clock output
14	DIF_13#	OUT	0.7V differential complement clock output
15	OE13#	IN	Active low input for enabling DIF pair 13. 1 = tri-state outputs, 0 = enable outputs
16	DIF_14	OUT	0.7V differential true clock output
17	DIF_14#	OUT	0.7V differential complement clock output
18	OE14#	IN	Active low input for enabling DIF pair 14. 1 = tri-state outputs, 0 = enable outputs
19	DIF_15	OUT	0.7V differential true clock output
20	DIF_15#	OUT	0.7V differential complement clock output
21	VDD	PWR	Power supply, nominal 3.3V
22	OE15_17#	IN	Active low input for enabling DIF pairs 15, 16 and 17 1 = tri-state outputs, 0 = enable outputs
23	DIF_16	OUT	0.7V differential true clock output
24	DIF_16#	OUT	0.7V differential complement clock output
25	DIF_17	OUT	0.7V differential true clock output
26	DIF_17#	OUT	0.7V differential complement clock output
27	IREF	OUT	This pin establishes the reference current for the differential current-mode output pairs. This pin requires a fixed precision resistor tied to ground in order to establish the appropriate current. 475 ohms is the standard value.
28	GNDA	PWR	Ground pin for the PLL core.
29	VDDA	PWR	3.3V power for the PLL core.
30	CLKA_IN	IN	True Input for differential reference clock.
31	CLKA_IN#	IN	Complement Input for differential reference clock.
32	GND	PWR	Ground pin.
33	CLKB_IN	IN	True Input for differential reference clock.
34	CLKB_IN#	IN	Complement Input for differential reference clock.
35	VDD	PWR	Power supply, nominal 3.3V
36	OE_01234#	IN	Active low input for enabling DIF pairs 0, 1, 2, 3 and 4. 1 = tri-state outputs, 0 = enable outputs

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Pin Description (Continued)

37	DIF_0	OUT	0.7V differential true clock output
38	DIF_0#	OUT	0.7V differential complement clock output
39	DIF_1	OUT	0.7V differential true clock output
40	DIF_1#	OUT	0.7V differential complement clock output
41	DIF_2	OUT	0.7V differential true clock output
42	DIF_2#	OUT	0.7V differential complement clock output
43	VDD	PWR	Power supply, nominal 3.3V
44	GND	PWR	Ground pin.
45	DIF_3	OUT	0.7V differential true clock output
46	DIF_3#	OUT	0.7V differential complement clock output
47	DIF_4	OUT	0.7V differential true clock output
48	DIF_4#	OUT	0.7V differential complement clock output
49	OE5#	IN	Active low input for enabling DIF pair 5. 1 = tri-state outputs, 0 = enable outputs
50	DIF_5	OUT	0.7V differential true clock output
51	DIF_5#	OUT	0.7V differential complement clock output
52	OE6#	IN	Active low input for enabling DIF pair 6. 1 = tri-state outputs, 0 = enable outputs
53	DIF_6	OUT	0.7V differential true clock output
54	DIF_6#	OUT	0.7V differential complement clock output
55	VDD	PWR	Power supply, nominal 3.3V
56	OE7#	IN	Active low input for enabling DIF pair 7. 1 = tri-state outputs, 0 = enable outputs
57	DIF_7	OUT	0.7V differential true clock output
58	DIF_7#	OUT	0.7V differential complement clock output
59	OE8#	IN	Active low input for enabling DIF pair 8. 1 = tri-state outputs, 0 = enable outputs
60	DIF_8	OUT	0.7V differential true clock output
61	DIF_8#	OUT	0.7V differential complement clock output
62	VDD	PWR	Power supply, nominal 3.3V
63	HIBW_BYPM_LOBW#	IN	Trilevel input to select High BW, Bypass Mode or Low BW. 0 = Low BW Mode, Mid= Bypass Mode, 1 = High Bandwidth
64	SMBCLK	IN	Clock pin of SMBUS circuitry, 5V tolerant
65	SMBDAT	I/O	Data pin of SMBUS circuitry, 5V tolerant
66	SMB_A1	IN	SMBus address bit 1
67	SMB_A0	IN	SMBus address bit 0 (LSB)
68	SEL_A_B#	IN	Input to select differential input clock A or differential input clock B. 0 = Input B selected, 1 = Input A selected.
69	CKPWRGD/PD#	IN	Notifies the clock to sample latched inputs on the rising edge, and to power down on the falling edge.
70	DIF_9	OUT	0.7V differential true clock output
71	DIF_9#	OUT	0.7V differential complement clock output
72	OE9#	IN	Active low input for enabling DIF pair 9. 1 = tri-state outputs, 0 = enable outputs

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Electrical Characteristics - Absolute Maximum Ratings

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	NOTES
3.3V Core Supply Voltage	VDDA				4.6	V	1,2
3.3V Logic Supply Voltage	VDD				4.6	V	1,2
Input Low Voltage	V_{IL}		GND-0.5			V	1
Input High Voltage	V_{IH}	Except for SMBus interface			V_{DD}+0.5	V	1
Input High Voltage	V_{IHSMB}	SMBus clock and data pins			5.5V	V	1
Storage Temperature	Ts		-65		150	°C	1
Junction Temperature	Tj				125	°C	1
Input ESD protection	ESD prot	Human Body Model	2000			V	1

[1]Guaranteed by design and characterization, not 100% tested in production.

[2] Operation under these conditions is neither implied nor guaranteed.

Electrical Characteristics - Input/Supply/Common Parameters

TA = T_{COM}; Supply Voltage VDD/VDDA = 3.3 V +/-5%

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	NOTES
Operating Supply Voltage	V_{DDX}	VDD and VDDA	3.135	3.3	3.465	V	1,6
Ambient Operating	T_{COM}	Commmercial range	0	25	70	°C	1
Input High Voltage	V_{IH}	Single-ended inputs, except SMBus, low threshold and tri-level inputs	2		V_{DD}+0.3	V	1,6
Input Low Voltage	V_{IL}	Single-ended inputs, except SMBus, low threshold and tri-level inputs	GND-0.3		0.8	V	1,6
Input High Voltage	V_{IHtri}	HIBW_BYPM_LOBW# pin	2		V_{DD}+0.3	V	1,6
Input Mid-level Voltage	V_{IMtri}	HIBW_BYPM_LOBW# pin	1.2		1.8	V	1,6
Input Low Voltage	V_{ILtri}	HIBW_BYPM_LOBW# pin	GND-0.3		0.8	V	1,6
Input Current	I_{IN}	Single-ended inputs, V_{IN} = GND, V_{IN} = VDD	-5		5	uA	1
	I_{INP}	Single-ended inputs V_{IN} = 0 V; Inputs with internal pull-up resistors V_{IN} = VDD; Inputs with internal pull-down resistors	-200		200	uA	1
Input Frequency	F_{ibyp}	V_{DD} = 3.3 V, Bypass mode	33		167	MHz	2
	F_{ipll}	V_{DD} = 3.3 V, 100MHz PLL mode	80	100	110	MHz	2
Pin Inductance	L_{pin}				7	nH	1
Capacitance	C_{IN}	Logic Inputs, except DIF_IN	1.5		5	pF	1
	C_{INDIF_IN}	DIF_IN differential clock inputs	1.5		2.7	pF	1,4
	C_{OUT}	Output pin capacitance			6	pF	1
Clk Stabilization	T_{STAB}	From V_{DD} Power-Up and after input clock stabilization or de-assertion of PD# to 1st clock		0.50	1	ms	1,2
Input SS Modulation Frequency	f_{MODIN}	Allowable Frequency (Triangular Modulation)	30	31.5	33	kHz	1
OE# Latency	$t_{LATOE\#}$	DIF start after OE# assertion DIF stop after OE# deassertion	4		12	cycles	1,3
Tdrive_PD#	t_{DRVPD}	DIF output enable after PD# de-assertion			300	us	1,3
Tfall	t_F	Fall time of control inputs			5	ns	1,2
Trise	t_R	Rise time of control inputs			5	ns	1,2
SMBus Input Low Voltage	V_{ILSMB}				0.8	V	1
SMBus Input High Voltage	V_{IHSMB}		2.1		V_{DDSMB}	V	1
SMBus Output Low Voltage	V_{OLSMB}	@ I_{PULLUP}			0.4	V	1
SMBus Sink Current	I_{PULLUP}	@ V_{OL}	4			mA	1
Nominal Bus Voltage	V_{DDSMB}	3V to 5V +/- 10%	2.7		5.5	V	1
SCLK/SDATA Rise Time	t_{RSMB}	(Max VIL - 0.15) to (Min VIH + 0.15)			1000	ns	1
SCLK/SDATA Fall Time	t_{FSMB}	(Min VIH + 0.15) to (Max VIL - 0.15)			300	ns	1
SMBus Operating Frequency	f_{MAXSMB}	Maximum SMBus operating frequency			100	kHz	1,5

[1]Guaranteed by design and characterization, not 100% tested in production.

[2]Control input must be monotonic from 20% to 80% of input swing.

[3]Time from deassertion until outputs are >200 mV

[4]DIF_IN input

[5]The differential input clock must be running for the SMBus to be active

[6] See the functionality tables for the thresholds for the tri-level and low threshold inputs.

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Electrical Characteristics - Clock Input Parameters

TA = $T_{COM;}$ Supply Voltage VDD/VDDA = 3.3 V +/-5%

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	NOTES
Input High Voltage - DIF_IN	V_{IHDIF}	Differential inputs (single-ended measurement)	300	750	1150	mV	1
Input Low Voltage - DIF_IN	V_{ILDIF}	Differential inputs (single-ended measurement)	V_{SS} - 300	0	300	mV	1
Input Common Mode Voltage - DIF_IN	V_{COM}	Common Mode Input Voltage	150	350	1000	mV	1,3
Input Amplitude - DIF_IN	V_{SWING}	Peak to Peak value	300			mV	1
Input Slew Rate - DIF_IN	dv/dt	Measured differentially	0.4		8	V/ns	1,2
Input Duty Cycle	d_{tin}	Measurement from differential wavefrom	45		55	%	1,4
Input Jitter - Cycle to Cycle	J_{DIFIn}	Differential Measurement	0		125	ps	1

[1] Guaranteed by design and characterization, not 100% tested in production.

[2]Slew rate measured through +/-75mV window centered around differential zero

[3]Any combination of V_{SWING} and V_{COM} is acceptable as long as V_{SWING} >300mV and V_{IH} is <1150mV.

[4]The device works over a wider range, but the user must take into account duty cycle distortion and required output duty cycle, if using the part in bypass mode.

Electrical Characteristics - DIF 0.7V Current Mode Differential Outputs

TA = $T_{COM;}$ Supply Voltage VDD/VDDA = 3.3 V +/-5%

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	NOTES
Slew rate	Trf	Scope averaging on	1	2.1	4	V/ns	1, 2, 3
Slew rate matching	DTrf	Slew rate matching, Scope averaging on		12.5	20	%	1, 2, 4
Voltage High	VHigh	Statistical measurement on single-ended signal using oscilloscope math function. (Scope averaging on)	660	749	850	mV	1
Voltage Low	VLow		-150	4	150		1
Max Voltage	Vmax	Measurement on single ended signal using absolute value. (Scope averaging off)			1150	mV	1
Min Voltage	Vmin		-300				1
Vswing	Vswing	Scope averaging off	300			mV	1, 2
Crossing Voltage (abs)	Vcross_abs	Scope averaging off	250	333	550	mV	1, 5
Crossing Voltage (var)	D-Vcross	Scope averaging off			140	mV	1, 6

[1]Guaranteed by design and characterization, not 100% tested in production. IREF = VDD/(3xR_R). For R_R = 475Ω (1%), I_{REF} = 2.32mA. I_{OH} = 6 x I_{REF} and V_{OH} = 0.7V @ Z_O=50Ω (100Ω differential impedance).

[2] Measured from differential waveform

[3] Slew rate is measured through the Vswing voltage range centered around differential 0V. This results in a +/-150mV window around differential 0V.

[4] Matching applies to rising edge rate of Clock / falling edge rate of Clock#. It is measured in a +/-75mV window centered on the average cross point where Clock rising meets Clock# falling. The median cross point is used to calculate the voltage thresholds the oscilloscope uses for the edge rate calculations.

[5] Vcross is defined as voltage where Clock = Clock# measured on a component test board and only applies to the differential rising edge (i.e. Clock rising and Clock# falling).

[6] The total variation of all Vcross measurements in any particular system. Note that this is a subset of V_cross_min/max (V_cross absolute) allowed. The intent is to limit Vcross induced modulation by setting V_cross_delta to be smaller than V_cross absolute.

Electrical Characteristics - Current Consumption

TA = $T_{COM;}$ Supply Voltage VDD/VDDA = 3.3 V +/-5%

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	NOTES
Operating Supply Current	$I_{DD3.3OP}$	VDD. All outputs active @100MHz, CL=2pF		340	425	mA	1
	$I_{DD3.3AOP}$	VDDA. All outputs active @100MHz, C_L=2pF		30	40	mA	1
Powerdown Current	$I_{DD3.3PDZ}$	VDD, All differential pairs tri-stated		12	15	mA	1
	$I_{DD3.3APDZ}$	VDDA, All differential pairs tri-stated		13	20	mA	1

[1]Guaranteed by design and characterization, not 100% tested in production.

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Electrical Characteristics - Skew and Differential Jitter Parameters

TA = $T_{COM;}$ Supply Voltage VDD/VDDA = 3.3 V +/-5%

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	NOTES
CLK_IN, DIF[x:0]	t_{SPO_PLL}	Input-to-Output Skew in PLL mode nominal value @ 25°C, 3.3V	900	1000	1125	ps	1,2,4,5,8
CLK_IN, DIF[x:0]	t_{PD_BYP}	Input-to-Output Skew in Bypass mode nominal value @ 25°C, 3.3V	4000	4700	5200	ns	1,2,3,5,8
CLK_IN, DIF[x:0]	t_{DSPO_PLL}	Input-to-Output Skew Varation in PLL mode across voltage and temperature		|250|	|350|	ps	1,2,3,5,8
CLK_IN, DIF[x:0]	t_{DSPO_BYP}	Input-to-Output Skew Varation in Bypass mode across voltage and temperature		|800|	|900|	ps	1,2,3,5,8
CLK_IN, DIF[x:0]	t_{DTE}	Random Differential Tracking error beween two 9EX devices in Hi BW Mode		2	5	ps (rms)	1,2,3,5,8
CLK_IN, DIF[x:0]	t_{DSSTE}	Random Differential Spread Spectrum Tracking error beween two 9EX devices in Hi BW Mode		20	75	ps	1,2,3,5,8
DIF{x:0]	t_{SKEW_ALL}	Output-to-Output Skew across all outputs (Common to Bypass and PLL mode)		100	150	ps	1,2,3,8
PLL Jitter Peaking	$j_{peak-hibw}$	LOBW#_BYPASS_HIBW = 1	0	2	2.5	dB	7,8
PLL Jitter Peaking	$j_{peak-lobw}$	LOBW#_BYPASS_HIBW = 0	0	2.3	3	dB	7,8
PLL Bandwidth	pll_{HIBW}	LOBW#_BYPASS_HIBW = 1	2	2.3	4	MHz	8,9
PLL Bandwidth	pll_{LOBW}	LOBW#_BYPASS_HIBW = 0	0.7	0.8	1.4	MHz	8,9
Duty Cycle	t_{DC}	Measured differentially, PLL Mode	45	50	55	%	1
Duty Cycle Distortion	t_{DCD}	Measured differentially, Bypass Mode @100MHz	-1	0	1	%	1,10
Jitter, Cycle to cycle	$t_{jcyc-cyc}$	PLL mode		27	50	ps	1,11
		Additive Jitter in Bypass Mode		12	50	ps	1,11

Notes for preceding table:

[1] Measured into fixed 2 pF load cap. Input to output skew is measured at the first output edge following the corresponding input.

[2] Measured from differential cross-point to differential cross-point.

[3] All Bypass Mode Input-to-Output specs refer to the timing between an input edge and the specific output edge created by it.

[4] This parameter is deterministic for a given device

[5] Measured with scope averaging on to find mean value.

[6] t is the period of the input clock

[7] Measured as maximum pass band gain. At frequencies within the loop BW, highest point of magnification is called PLL jitter peaking.

[8] Guaranteed by design and characterization, not 100% tested in production.

[9] Measured at 3 db down or half power point.

[10] Duty cycle distortion is the difference in duty cycle between the output and the input clock when the device is operated in bypass mode.

[11] Measured from differential waveform

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Electrical Characteristics - Phase Jitter Parameters

TA = $T_{COM;}$ Supply Voltage VDD/VDDA = 3.3 V +/-5%

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	Notes
Phase Jitter, PLL Mode	$t_{jphPCIeG1}$	PCIe Gen 1		30	86	ps (p-p)	1,2,3
	$t_{jphPCIeG2}$	PCIe Gen 2 Lo Band 10kHz < f < 1.5MHz		1.2	3	ps (rms)	1,2
		PCIe Gen 2 High Band 1.5MHz < f < Nyquist (50MHz)		2.0	3.1	ps (rms)	1,2
	$t_{jphPCIeG3}$	PCIe Gen 3 (PLL BW of 2-4MHz, CDR = 10MHz)		0.5	1	ps (rms)	1,2,4
Additive Phase Jitter, Bypass Mode	$t_{jphPCIeG1}$	PCIe Gen 1		1.4	10	ps (p-p)	1,2,3
	$t_{jphPCIeG2}$	PCIe Gen 2 Lo Band 10kHz < f < 1.5MHz		0.30	0.4	ps (rms)	1,2,6
		PCIe Gen 2 High Band 1.5MHz < f < Nyquist (50MHz)		0.24	0.5	ps (rms)	1,2,6
	$t_{jphPCIeG3}$	PCIe Gen 3 (PLL BW of 2-4MHz, CDR = 10MHz)		0.07	0.3	ps (rms)	1,2,4,5,6

[1] Applies to all outputs.

[2] See http://www.pcisig.com for complete specs

[3] Sample size of at least 100K cycles. This figures extrapolates to 108ps pk-pk @ 1M cycles for a BER of 1-12.

[4] Subject to final radification by PCI SIG.

[5] Calculated from Intel-supplied Clock Jitter Tool v 1.6.3

[6] For RMS figures, additive jitter is calculated by solving the following equation: (Additive jitter)^2 = (total jittter)^2 - (input jitter)^2

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Clock Periods Differential Outputs with Spread Spectrum Enabled

Measurement Window		1 Clock	1us	0.1s	0.1s	0.1s	1us	1 Clock		
Symbol		Lg-	-SSC	-ppm error	0ppm	+ ppm error	+SSC	Lg+		
Definition		Absolute Period	Short-term Average	Long-Term Average	Period	Long-Term Average	Short-term Average	Period		
		Minimum Absolute Period	Minimum Absolute Period	Minimum Absolute Period	Nominal	Maximum	Maximum	Maximum	Units	Notes
DIF	DIF 100	9.87400	9.99900	9.99900	10.00000	10.00100	10.05130	10.17630	ns	1,2,3

Clock Periods Differential Outputs with Spread Spectrum Disabled

Measurement Window		1 Clock	1us	0.1s	0.1s	0.1s	1us	1 Clock		
Symbol		Lg-	-SSC	-ppm error	0ppm	+ ppm error	+SSC	Lg+		
Definition		Absolute Period	Short-term Average	Long-Term Average	Period	Long-Term Average	Short-term Average	Period		
		Minimum Absolute Period	Minimum Absolute Period	Minimum Absolute Period	Nominal	Maximum	Maximum	Maximum	Units	Notes
DIF	DIF 100	9.87400		9.99900	10.00000	10.00100		10.17630	ns	1,2,3

[1]Guaranteed by design and characterization, not 100% tested in production.

[2] All Long Term Accuracy specifications are guaranteed with the assumption that the input clock complies with CK410B+/CK420BQ accuracy requirements. The 9EX21831 itself does not contribute to ppm error.

[3] Driven by SRC output of main clock, PLL or Bypass mode

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DIF Reference Clock			
Common Recommendations for Differential Routing	Dimension or Value	Unit	Figure
L1 length, route as non-coupled 50ohm trace	0.5 max	inch	1
L2 length, route as non-coupled 50ohm trace	0.2 max	inch	1
L3 length, route as non-coupled 50ohm trace	0.2 max	inch	1
Rs	33	ohm	1
Rt	49.9	ohm	1

Down Device Differential Routing			
L4 length, route as coupled microstrip 100ohm differential trace	2 min to 16 max	inch	1
L4 length, route as coupled stripline 100ohm differential trace	1.8 min to 14.4 max	inch	1

Differential Routing to PCI Express Connector			
L4 length, route as coupled microstrip 100ohm differential trace	0.25 to 14 max	inch	2
L4 length, route as coupled stripline 100ohm differential trace	0.225 min to 12.6 max	inch	2

Figure 1: Down Device Routing

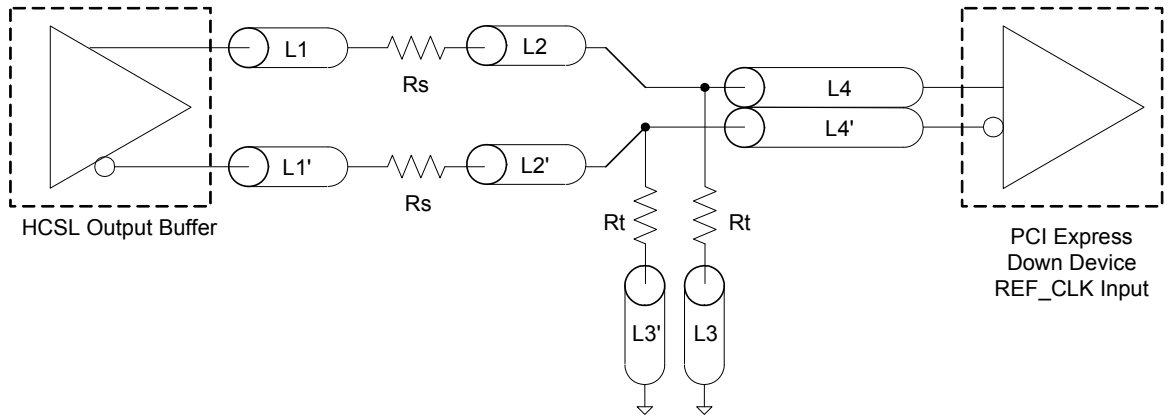
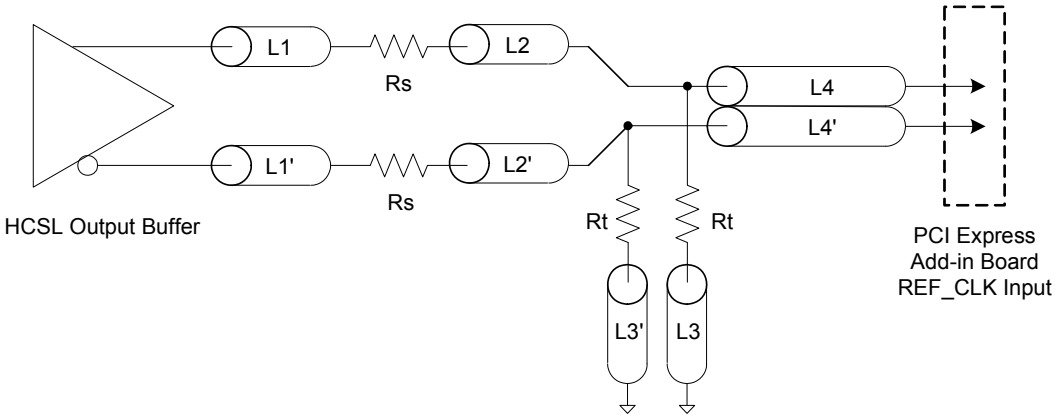


Figure 2: PCI Express Connector Routing

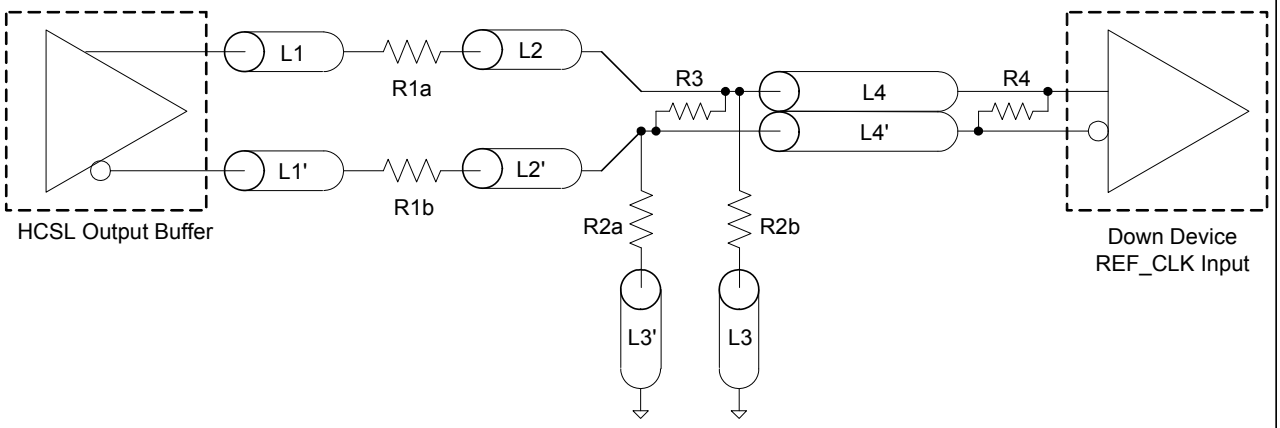


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Alternative Termination for LVDS and other Common Differential Signals (figure 3)							
Vdiff	Vp-p	Vcm	R1	R2	R3	R4	Note
0.45v	0.22v	1.08	33	150	100	100	
0.58	0.28	0.6	33	78.7	137	100	
0.80	0.40	0.6	33	78.7	none	100	ICS874003i-02 input compatible
0.60	0.3	1.2	33	174	140	100	Standard LVDS

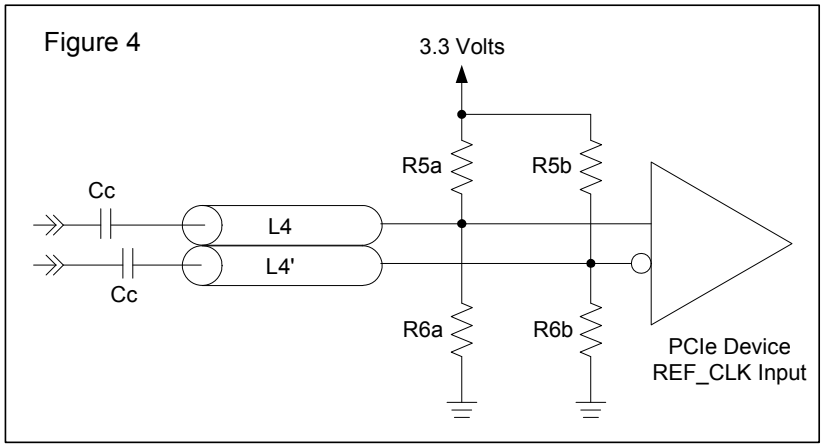
R1a = R1b = R1
R2a = R2b = R2

Figure 3



Cable Connected AC Coupled Application (figure 4)		
Component	Value	Note
R5a, R5b	8.2K 5%	
R6a, R6b	1K 5%	
Cc	0.1 µF	
Vcm	0.350 volts	

Figure 4



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General SMBus serial interface information for the 9EX21831

How to Write:

- Controller (host) sends a start bit.
- Controller (host) sends the write address D4 $_{(H)}$
- ICS clock will ***acknowledge***
- Controller (host) sends the begining byte location = N
- ICS clock will ***acknowledge***
- Controller (host) sends the data byte count = X
- ICS clock will ***acknowledge***
- Controller (host) starts sending ***Byte N through Byte N + X -1***
  (see Note 2)
- ICS clock will ***acknowledge*** each byte ***one at a time***
- Controller (host) sends a Stop bit

How to Read:

- Controller (host) will send start bit.
- Controller (host) sends the write address D4 $_{(H)}$
- ICS clock will ***acknowledge***
- Controller (host) sends the begining byte location = N
- ICS clock will ***acknowledge***
- Controller (host) will send a separate start bit.
- Controller (host) sends the read address D5 $_{(H)}$
- ICS clock will ***acknowledge***
- ICS clock will send the data byte count = X
- ICS clock sends ***Byte N + X -1***
- ICS clock sends ***Byte 0 through byte X (if X$_{(H)}$ was written to byte 8)***.
- Controller (host) will need to acknowledge each byte
- Controllor (host) will send a not acknowledge bit
- Controller (host) will send a stop bit

Index Block Write Operation

Controller (Host)			ICS (Slave/Receiver)
T	starT bit		
Slave Address D4$_{(H)}$			
WR	WRite		
			ACK
Beginning Byte = N			
			ACK
Data Byte Count = X			
			ACK
Beginning Byte N		X Byte	
			ACK
◇			
◇			◇
◇			◇
			◇
Byte N + X - 1			
			ACK
P	stoP bit		

Note: The SMBus addresses assume that the select pins are '00'

Index Block Read Operation

Controller (Host)		ICS (Slave/Receiver)	
T	starT bit		
Slave Address D4$_{(H)}$			
WR	WRite		
		ACK	
Beginning Byte = N			
		ACK	
RT	Repeat starT		
Slave Address D5$_{(H)}$			
RD	ReaD		
		ACK	
		Data Byte Count = X	
ACK			
			Beginning Byte N
ACK			
			◇
◇			◇
◇			◇
◇			
			Byte N + X - 1
N	Not acknowledge		
P	stoP bit		

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SMBusTable: Output, and PLL BW Control Register

Byte 0	Pin #	Name	Control Function	Type	0	1	Default
Bit 7	4	PLL_BW# adjust		RW	00 = Low BW (1MHz) 10 = Bypass 11 = High BW (3MHz)		Latch
Bit 6		BYPASS# test mode / PLL		RW			Latch
Bit 5		DIF_17	Output Control	RW	Hi-Z	Enable	1
Bit 4		DIF_16	Output Control	RW	Hi-Z	Enable	1
Bit 3		RESERVED					0
Bit 2		RESERVED					1
Bit 1		RESERVED					0
Bit 0		RESERVED					1

SMBusTable: Output Control Register

Byte 1	Pin #	Name	Control Function	Type	0	1	Default
Bit 7		DIF_7	Output Control	RW	Hi-Z	Enable	1
Bit 6		DIF_6	Output Control	RW	Hi-Z	Enable	1
Bit 5		DIF_5	Output Control	RW	Hi-Z	Enable	1
Bit 4		DIF_4	Output Control	RW	Hi-Z	Enable	1
Bit 3		DIF_3	Output Control	RW	Hi-Z	Enable	1
Bit 2		DIF_2	Output Control	RW	Hi-Z	Enable	1
Bit 1		DIF_1	Output Control	RW	Hi-Z	Enable	1
Bit 0		DIF_0	Output Control	RW	Hi-Z	Enable	1

SMBusTable: Output Control Register

Byte 2	Pin #	Name	Control Function	Type	0	1	Default
Bit 7		DIF_15	Output Control	RW	Hi-Z	Enable	1
Bit 6		DIF_14	Output Control	RW	Hi-Z	Enable	1
Bit 5		DIF_13	Output Control	RW	Hi-Z	Enable	1
Bit 4		DIF_12	Output Control	RW	Hi-Z	Enable	1
Bit 3		DIF_11	Output Control	RW	Hi-Z	Enable	1
Bit 2		DIF_10	Output Control	RW	Hi-Z	Enable	1
Bit 1		DIF_9	Output Control	RW	Hi-Z	Enable	1
Bit 0		DIF_8	Output Control	RW	Hi-Z	Enable	1

SMBusTable: Output Enable Readback Register

Byte 3	Pin #	Name	Control Function	Type	0	1	Default
Bit 7	5	OE11# Input	Pin Readback	R	Pin Low	Pin Hi	X
Bit 6	2	OE10# Input	Pin Readback	R	Pin Low	Pin Hi	X
Bit 5	72	OE9# Input	Pin Readback	R	Pin Low	Pin Hi	X
Bit 4	59	OE8# Input	Pin Readback	R	Pin Low	Pin Hi	X
Bit 3	56	OE7# Input	Pin Readback	R	Pin Low	Pin Hi	X
Bit 2	52	OE6# Input	Pin Readback	R	Pin Low	Pin Hi	X
Bit 1	49	OE5# Input	Pin Readback	R	Pin Low	Pin Hi	X
Bit 0	36	OE_01234# Input	Pin Readback	R	Pin Low	Pin Hi	X

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SMBusTable: Output Enable Readback Register

Byte 4	Pin #	Name	Control Function	Type	0	1	Default
Bit 7		RESERVED					0
Bit 6		RESERVED					0
Bit 5		RESERVED					1
Bit 4	68	SEL_A_B# Input	Pin Readback	R	Input B	Input A	X
Bit 3	22	OE15_17# Input	Pin Readback	R	Pin Low	Pin Hi	X
Bit 2	18	OE14# Input	Pin Readback	R	Pin Low	Pin Hi	X
Bit 1	15	OE13# Input	Pin Readback	R	Pin Low	Pin Hi	X
Bit 0	8	OE12# Input	Pin Readback	R	Pin Low	Pin Hi	X

Note: For an output to be enabled, BOTH the Output Enable Bit and the OE# pin must be enabled. This means that the Output Enable Bit must be '1' and the corresponding OE# pin must be '0'.

SMBusTable: Vendor & Revision ID Register

Byte 5	Pin #	Name	Control Function	Type	0	1	Default
Bit 7	-	RID3	REVISION ID	R	-	-	0
Bit 6	-	RID2		R	-	-	0
Bit 5	-	RID1		R	-	-	0
Bit 4	-	RID0		R	-	-	1
Bit 3	-	VID3	VENDOR ID	R	-	-	0
Bit 2	-	VID2		R	-	-	0
Bit 1	-	VID1		R	-	-	0
Bit 0	-	VID0		R	-	-	1

SMBusTable: DEVICE ID

Byte 6	Pin #	Name	Control Function	Type	0	1	Default
Bit 7	-	Device ID 7 (MSB)		R	Device ID is 18 hex		0
Bit 6	-	Device ID 6		R			0
Bit 5	-	Device ID 5		R			0
Bit 4	-	Device ID 4		R			1
Bit 3	-	Device ID 3		R			1
Bit 2	-	Device ID 2		R			0
Bit 1	-	Device ID 1		R			0
Bit 0	-	Device ID 0		R			0

SMBusTable: Byte Count Register

Byte 7	Pin #	Name	Control Function	Type	0	1	Default
Bit 7	-	BC7	Writing to this register configures how many bytes will be read back.	RW	-	-	0
Bit 6	-	BC6		RW	-	-	0
Bit 5	-	BC5		RW	-	-	0
Bit 4	-	BC4		RW	-	-	0
Bit 3	-	BC3		RW	-	-	0
Bit 2	-	BC2		RW	-	-	1
Bit 1	-	BC1		RW	-	-	1
Bit 0	-	BC0		RW	-	-	1

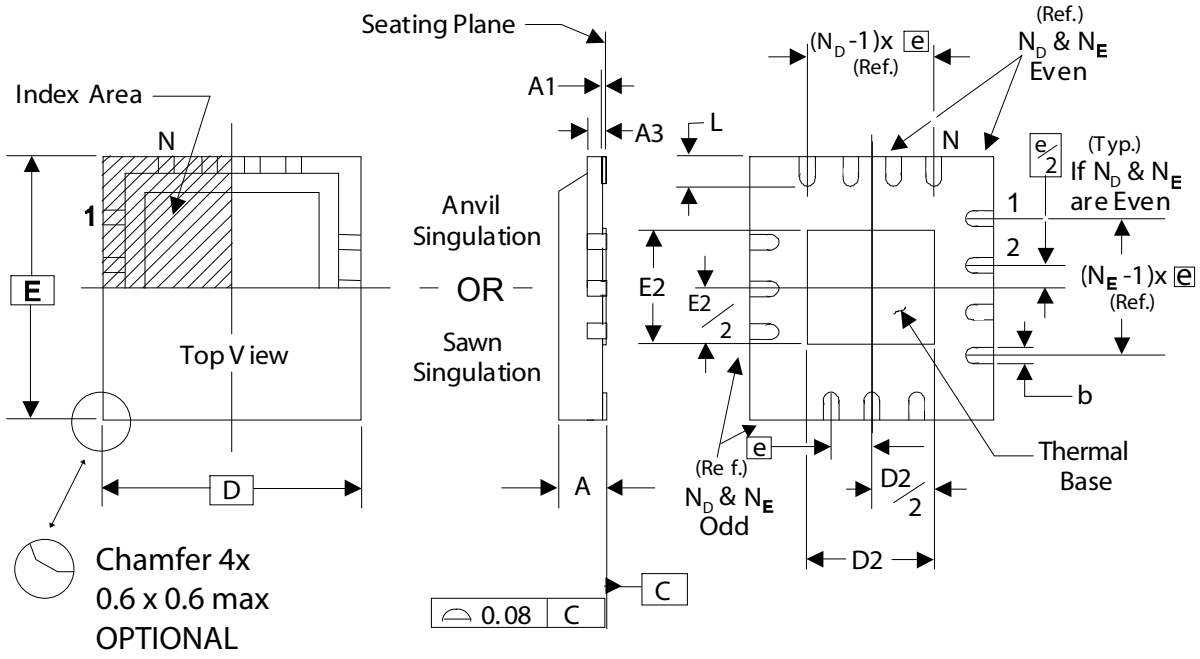
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SMBus Address Mapping

SMBus Address (Hex)	Main Clock (CKxxx)	9DB233	9DB433	9DB633	9DB833	9DB1233	9DB1933	9EX21531	9EX21831
D0							✓		
D2	✓						✓		
D4		✓		✓		✓	✓	✓	✓
D6						✓	✓	✓	✓
D8			✓		✓		✓	✓	✓
DA			✓		✓		✓	✓	✓
DC			✓		✓	✓	✓		
DE							✓		

Note: ✓ Indicates Bypass Mode. PLL is OFF.

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THERMALLY ENHANCED, VERY THIN, FINE PITCH
QUAD FLAT / NO LEAD PLASTIC PACKAGE

DIMENSIONS

SYMBOL	72L
N	72
N_D	18
N_E	18

DIMENSIONS (mm)

SYMBOL	MIN.	MAX.
A	0.8	1.0
A1	0	0.05
A3	0.25 Reference	
b	0.18	0.3
e	0.50 BASIC	
D x E BASIC	10.00 x 10.00	
D2 MIN. / MAX.	5.75	6.15
E2 MIN. / MAX.	5.75	6.15
L MIN. / MAX.	0.3	0.5

Marking Diagram



Notes:
1. Line 1: Company name
2. Line 2: Part number
3. Line 3: '######' denotes lot number
4. Line 4: Origin, date code, 'P' for punch

Ordering Information

Part / Order Number	Shipping Packaging	Package	Temperature
9EX21831AKLF	Tubes	72-pin MLF	0 to +70°C
9EX21831AKLFT	Tape and Reel	72-pin MLF	0 to +70°C

"LF" suffix to the part number are the Pb-Free configuration and are RoHS compliant.
"A" is the device revision designator (will not correlate to the datasheet revision).

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Revision History

Rev.	Who	Issue Date	Description	Page #
0.1	RDW	7/12/2010	Initial Release	-
A	RDW	7/13/2010	Move to final	
B	RDW	10/5/2011	Added top-side marking diagram	
C	RDW	11/29/2011	1. Minor updates/additions to typical values in the Electrical Tables. In all cases typical values have improved. 2. Widened input common mode voltage range from 300mV-1000mV to 150mV-1000mV (wider range).	5-8
D	RDW	3/22/2012	1. Updated Datasheet Title and General Description to Highlight PCIe Gen1/2/3 instead of PCIe Gen3. 2. Updated max additive phase jitter for PCIe Gen2 Lo band from 0.1ps rms to 0.4ps rms.	1,8

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