Description

The ICS9FG108E is a Frequency Generator that provides 8 differential HCSL output pairs. It can be used to drive PCe Gen1/2, SATA and USB3.0 devices. The part can use either a 14.31818 Mhz or 25 MHz crystal. The ICS9FG108E can also be driven by a reference input clock instead of a crystal. It provides outputs with cycle-to-cycle jitter of less than 50 ps and output-to-output skew of less than 65 ps.

Recommended Application

Frequency Generator for CPU, PCIe Gen1/2, SATA and USB3.0

Output Features

- 8 - HCSL differential outputs
- 1 - 3.3V REF output (either 14.318M or 25M depending on XTAL)

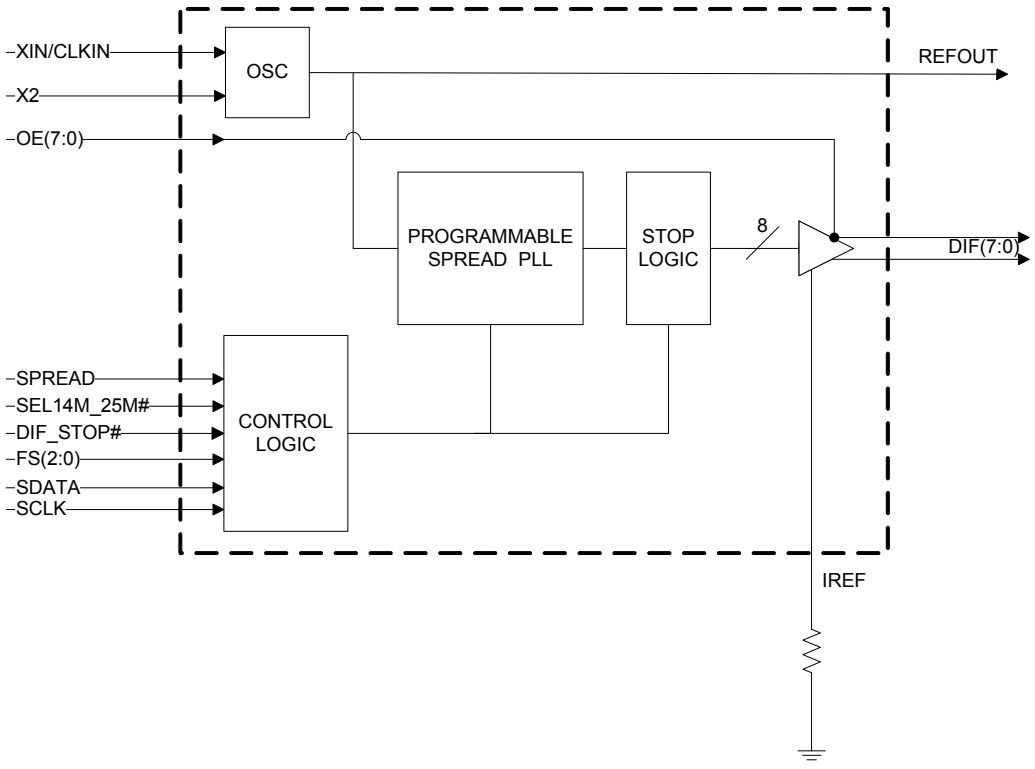
Features/Benefits

- Generates common frequencies from 14.318MHz or 25MHz
- Crystal or reference input
- 8 - 0.7V current-mode HCSL output pairs
- Supports Serial-ATA at 100MHz
- Two spread spectrum modes: -0.5% down spread and +/-0.25% center spread; Lower EMI
- 31.5KHz spread modulation rate; passes USB3 compliance testing
- Unused outputs may be disabled in either driven or Hi-Z state for power manangement
- I-temp version available; supports embedded applications

Key Specifications

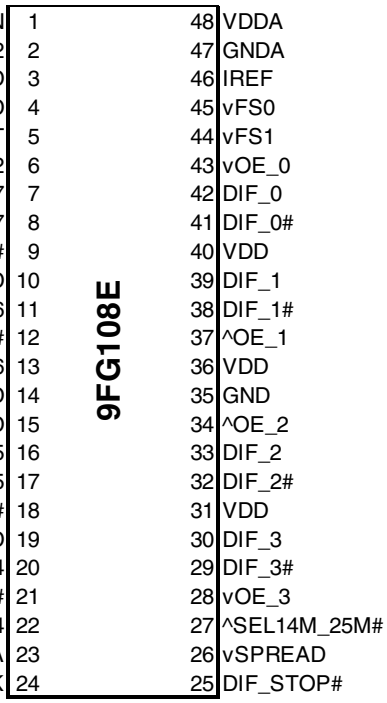
- Cycle to cycle jitter: < 50ps
- Phase jitter: PCIe Gen1/2 <3ps rms
- Output to output skew <65ps
- +/-300 ppm frequency accuracy on output clocks
- +/-50ppm on all output frequencies with Spread Off

Block Diagram



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Pin Configuration



^ indicates internal 120K pull up
v indicates internal 120K pull down

Power Groups

Pin Number		
VDD	**GND**	**Description**
3	4	REFOUT, Digital Inputs, SMBus
10,14,19,31,36,40	15,35	DIF Outputs
N/A	47	IREF
48	47	Analog VDD & GND for PLL Core

Frequency Select Table

SEL14M_25M# (FS3)	FS2	FS1	FS0	OUTPUT(MHz)
0	0	0	0	100.00
0	0	0	1	125.00
0	0	1	0	133.33
0	0	1	1	166.67
0	1	0	0	200.00
0	1	0	1	266.66
0	1	1	0	333.33
0	1	1	1	400.00
1	0	0	0	100.00
1	0	0	1	125.00
1	0	1	0	133.33
1	0	1	1	166.67
1	1	0	0	200.00
1	1	0	1	266.66
1	1	1	0	333.33
1	1	1	1	400.00

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Pin Descriptions

PIN #	PIN NAME	PIN TYPE	DESCRIPTION
1	XIN/CLKIN	IN	Crystal input or Reference Clock input
2	X2	OUT	Crystal output, Nominally 14.318MHz
3	VDD	PWR	Power supply, nominal 3.3V
4	GND	PWR	Ground pin.
5	REFOUT	OUT	Reference Clock output
6	vFS2	IN	Frequency select pin. This pin has an internal 120k pull down resistor
7	vOE_7	IN	Active high input for enabling output 7. This pin has a 120kohm pull down. 0 = tri-state outputs, 1= enable outputs
8	DIF_7	OUT	0.7V differential true clock output
9	DIF_7#	OUT	0.7V differential Complementary clock output
10	VDD	PWR	Power supply, nominal 3.3V
11	DIF_6	OUT	0.7V differential true clock output
12	DIF_6#	OUT	0.7V differential Complementary clock output
13	^OE_6	IN	Active high input for enabling output 6. This pin has an internal 120kohm pull up. 0 = tri-state outputs, 1= enable outputs
14	VDD	PWR	Power supply, nominal 3.3V
15	GND	PWR	Ground pin.
16	^OE_5	IN	Active high input for enabling output 5. This pin has an internal 120kohm pull up. 0 = tri-state outputs, 1= enable outputs
17	DIF_5	OUT	0.7V differential true clock output
18	DIF_5#	OUT	0.7V differential Complementary clock output
19	VDD	PWR	Power supply, nominal 3.3V
20	DIF_4	OUT	0.7V differential true clock output
21	DIF_4#	OUT	0.7V differential Complementary clock output
22	vOE_4	IN	Active high input for enabling output 4. This pin as an internal 120kohm pull down. 0 = tri-state outputs, 1= enable outputs
23	SDATA	I/O	Data pin for SMBus circuitry, 3.3V tolerant.
24	SCLK	IN	Clock pin of SMBus circuitry, 5V tolerant.

Note:
^ indicates internal 120K pull up
v indicates internal 120K pull down

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Pin Descriptions (cont.)

PIN #	PIN NAME	PIN TYPE	DESCRIPTION
25	DIF_STOP#	IN	Active low input to stop differential output clocks.
26	vSPREAD	IN	Asynchronous, active high input to enable spread spectrum functionality. This pin has a 120Kohm pull down resistor.
27	^SEL14M_25M#	IN	Select 14.31818 MHz or 25 Mhz input frequency. This pin has an internal 120kohm pull up resistor. 1 = 14.31818 MHz, 0 = 25 MHz
28	vOE_3	IN	Active high input for enabling output 3. This pin has an internal 120kohm pull down resistor. 0 = tri-state outputs, 1= enable outputs
29	DIF_3#	OUT	0.7V differential Complementary clock output
30	DIF_3	OUT	0.7V differential true clock output
31	VDD	PWR	Power supply, nominal 3.3V
32	DIF_2#	OUT	0.7V differential Complementary clock output
33	DIF_2	OUT	0.7V differential true clock output
34	^OE_2	IN	Active high input for enabling output 2. This pin has in internal 120kohm pull up resistor. 0 = tri-state outputs, 1= enable outputs
35	GND	PWR	Ground pin.
36	VDD	PWR	Power supply, nominal 3.3V
37	^OE_1	IN	Active high input for enabling output 1. This pin has an internal 120kohm pull up resistor. 0 = tri-state outputs, 1= enable outputs
38	DIF_1#	OUT	0.7V differential Complementary clock output
39	DIF_1	OUT	0.7V differential true clock output
40	VDD	PWR	Power supply, nominal 3.3V
41	DIF_0#	OUT	0.7V differential Complementary clock output
42	DIF_0	OUT	0.7V differential true clock output
43	vOE_0	IN	Active high input for enabling output 0. This pin has an internal 120kohm pull down resistor. 0 = tri-state outputs, 1= enable outputs
44	vFS1	IN	3.3V Frequency select latched input pin with internal 120kohm pull down resistor.
45	vFS0	IN	3.3V Frequency select latched input pin with internal 120kohm pull down resistor.
46	IREF	OUT	This pin establishes the reference current for the differential current-mode output pairs. This pin requires a fixed precision resistor tied to ground in order to establish the appropriate current. 475 ohms is the standard value.
47	GNDA	PWR	Ground pin for the PLL core.
48	VDDA	PWR	3.3V power for the PLL core.

Note:
^ indicates internal 120K pull up
v indicates internal 120K pull down

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Absolute Maximum Ratings

Stresses above the ratings listed below can cause permanent damage to the ICS9FG108E. These ratings, which are standard values for IDT commercially rated parts, are stress ratings only. Functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods can affect product reliability. Electrical parameters are guaranteed only over the recommended operating temperature range.

Symbol	Parameter	Min	Max	Units
VDD_A	3.3V Core Supply Voltage		4.6	V
VDD	3.3V Logic Supply Voltage		4.6	V
Ts	Storage Temperature	-65	150	°C
Tambient	Ambient Operating Temp•(Commerical Grade)	0	+70	°C
Tambient	Ambient Operating Temp•(Industrial Grade)	-40	+85	°C
Tcase	Case Temperature		115	°C
ESD prot	Input ESD protection•human body model	2000		V

Electrical Characteristics–REF-14.318/25 MHz

$T_A = T_{AMBIENT}$; V_{DD} = 3.3 V +/-5%;R_S=33Ω, C_L = 5 pF (unless otherwise specified)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	Notes
Output High Voltage	V_{OH}	I_{OH} = -1 mA	2.4			V	1
Output Low Voltage	V_{OL}	I_{OL} = 1 mA			0.4	V	1
Rise	t_{r1}	V_{OL} = 0.4 V, V_{OH} = 2.4 V	1	1.4	2.5	ns	1
Fall Time	t_{f1}	V_{OH} = 2.4 V, V_{OL} = 0.4 V	1	1.4	2.5	ns	1
Duty Cycle	d_{t1}	V_T = 1.5 V	45	53	55	%	1
Jitter	$t_{jcyc-cycCOM}$	VT = 1.5 V (commercial)		87	200	ps	1
Jitter	$t_{jcyc-cycIND}$	VT = 1.5 V (industrial)		87	250	ps	1

[1]Guaranteed by design and characterization, not 100% tested in production.

[2] Trim capacitors must be used to tune the REF to the exact Crystal Frequency.

Electrical Characteristics–Differential Phase Jitter Parameters

T_A = Commercial and Industrial, Supply Voltage VDD = 3.3 V +/-5%

PARAMETER	Symbol	Conditions	Min	Typ	Max	Units	Notes
Jitter, Phase	$t_{jphasePLL}$	PCIe Gen 1		25.2	86	ps (p-p)	1,2
	$t_{jphaseLo}$	PCIe Gen1/2 10kHz < f < 1.5MHz		0.8	3	ps (RMS)	1,2
	$t_{jphaseHigh}$	PCIe Gen1/2 1.5MHz < f < Nyquist (50MHz)		1.8	3.1	ps (RMS)	1,2
	t_{jphQPI}	QPI 133MHz 4.8G/6.4Gb,12UI		0.2	0.5	ps (RMS)	1,3
	$t_{jphFBD3.2G}$	FBD specs (11 to 33MHz)		1.4	3	ps (RMS)	1
	$t_{jphFBD4.8G}$	FBD specs		1.1	2.5	ps	1

[1]Guaranteed by design and characterization, not 100% tested in production.

[2]See http://www.pcisig.com for complete specs

[3]First number is 4.8G link speed, second number is 6.4G link speed. From Intel Clock Jit tool

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Electrical Characteristics–Input/Supply/Common Output Parameters

T_A = $T_{AMBIENT}$; Supply Voltage V_{DD} = 3.3 V +/-5%

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	NOTES
Tambient	T_{COM}	Commericial Temperature	0		70	°C	
Tambient	T_{IND}	Industrial Temperature	-40		85	°C	
Input High Voltage	V_{IH}	3.3 V +/-5%	2		V_{DD} + 0.3	V	1
Input Low Voltage	V_{IL}	3.3 V +/-5%	V_{SS} - 0.3		0.8	V	1
Input High Current	I_{IH}	V_{IN} = V_{DD}	-5		5	uA	1
Input Low Current	I_{IL1}	V_{IN} = 0 V; Inputs with no pull-up resistors	-5			uA	1
	I_{IL2}	V_{IN} = 0 V; Inputs with pull-up resistors	-200			uA	1
Operating Supply Current (T_A = Commercial)	IDD_{VDD}	C_L=Full load; fout = 400 MHz		182	205	mA	1
	IDD_{VDDA}			20	25	mA	1
	IDD_{VDD}	C_L=Full load; fout = 100 MHz		153	175	mA	1
	IDD_{VDDA}			19	25	mA	1
DIF_STOP# Current (T_A = Commercial)	IDD_{VDDPD}	All DIF pairs stopped in driven mode		146	165	mA	1
	IDD_{VDDAPD}			19	25	mA	1
	IDD_{VDDPD}	All DIF pairs stopped in Hi-Z mode		26	35	mA	1
	IDD_{VDDAPD}			19	25	mA	1
Operating Supply Current (T_A = Industrial)	IDD_{VDD}	C_L=Full load; fout = 400 MHz		181	225	mA	1
	IDD_{VDDA}			21	28	mA	1
	IDD_{VDD}	C_L=Full load; fout = 100 MHz		152	180	mA	1
	IDD_{VDDA}			20	28	mA	1
DIF_STOP# Current (T_A = Industrial)	IDD_{VDDPD}	All DIF pairs stopped in driven mode		145	175	mA	1
	IDD_{VDDAPD}			20	28	mA	1
	IDD_{VDDPD}	All DIF pairs stopped in Hi-Z mode		26	38	mA	1
	IDD_{VDDAPD}			20	28	mA	1
Input Frequency[3]	F_i	SEL14M_25M# = 0	22.50	25	28.00	MHz	3
		SEL14M_25M# = 1	12.89	14.318	15.75	MHz	3
Pin Inductance[1]	L_{pin}				7	nH	1
Input/Output Capacitance[1]	C_{IN}	Logic Inputs	1.5		5	pF	1
	C_{OUT}	Output pin capacitance			6	pF	1
Clk Stabilization[1,2]	$T_{STABcom}$	From V_{DD} Power-Up to 1st clock		1.2	1.8	ms	1,2
	$T_{STABind}$	From V_{DD} Power-Up to 1st clock		1.8	3	ms	1,2
Spread Modulation Frequency	f_{MOD}	SEL14M_25M# = 0	30	31.5	33	kHz	1,3,4
		SEL14M_25M# = 1	30	31.5	33	kHz	1,3,4
Spread Modulation %	$f_{MOD\%DWN}$	Down Spread Selected			-0.5	%	1,3,4
Spread Modulation %	$f_{MOD\%CTR}$	Center Spread Selected			+/-0.25	%	1,3,4
DIF output enable	t_{DIFOE}	DIF output enable after			15	ns	1
Input Rise and Fall times	t_R/t_F	20% to 80% of VDD			5	ns	1

[1]Guaranteed by design and characterization, not 100% tested in production.

[2]See timing diagrams for timing requirements.

[3] Input frequency should be measured at the REF pin and tuned to 0 PPM to meet ppm frequency accuracy on PLL outputs.

[4] These values assume 25MHz or 14.31818MHz inputs respectively. Using a higher or lower frequency will scale these frequencies accordingly. The output frequecy selected by the FS inputs will also scale. For example, 27MHz input with an FS selection of 100MHz will yield an output frequency of 27/25 x 100 = 108MHz.

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Electrical Characteristics–DIF 0.7V Current Mode Differential Pair

$T_A = T_{AMBIENT}$; V_{DD} = 3.3 V +/-5%; C_L =2pF, R_S=33.2Ω, R_P=49.9Ω, I_{REF} = 475Ω

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	NOTES
Current Source Output Impedance	Zo[1]	$V_O = V_x$	3000			Ω	1
Voltage High	VHigh	Statistical measurement on single ended signal using oscilloscope math function.	660	750	850	mV	1
Voltage Low	VLow		-150	3	150		1
Max Voltage	Vovs	Measurement on single ended signal using absolute value.			1150	mV	1
Min Voltage	Vuds		-300				1
Crossing Voltage (abs)	Vcross(abs)		250	336	550	mV	1
Crossing Voltage (var)	d-Vcross	Crossing variation over all edges		40	140	mV	1
Long Accuracy	ppm	14.3M input, SS OFF	-300		300	ppm	1,2,5
		14.3M input, SS ON	-300		300	ppm	1,2,5
		25M input SS OFF	-50		50	ppm	1,2,5
		25M input, SS ON	-300		300	ppm	1,2,5
Average period	Tperiod	400MHz nominal	2.4993		2.5008	ns	2
		400MHz spread	2.4993		2.5133	ns	2,3
		333.33MHz nominal	2.9991		3.0009	ns	2
		333.33MHz spread	2.9991		3.016	ns	2,3
		266.66MHz nominal	3.7489		3.7511	ns	2
		266.66MHz spread	3.7489		3.77	ns	2,3
		200MHz nominal	4.9985		5.0015	ns	2
		200MHz spread	4.9985		5.0266	ns	2,3
		166.66MHz nominal	5.9982		6.0018	ns	2
		166.66MHz spread	5.9982		6.0320	ns	2,3
		133.33MHz nominal	7.4978		7.5023	ns	2
		133.33MHz spread	7.4978		5.4000	ns	2,3
		100.00MHz nominal	9.9970		10.0030	ns	2
		100.00MHz spread	9.9970		10.0533	ns	2,3
Absolute min period	T_{absmin}	400MHz nominal/spread	2.4143			ns	1,2
		333.33MHz nominal/spread	2.9141			ns	1,2
		266.66MHz nominal/spread	3.6639			ns	1,2
		200MHz nominal/spread	4.8735			ns	1,2
		166.66MHz nominal/spread	5.8732			ns	1,2
		133.33MHz nominal/spread	7.3728			ns	1,2
		100.00MHz nominal/spread	9.8720			ns	1,2
Rise Time	t_r	V_{OL} = 0.175V, V_{OH} = 0.525V	175	241	700	ps	1
Fall Time	t_f	V_{OH} = 0.525V V_{OL} = 0.175V	175	260	700	ps	1
Rise Time Variation	d-t_r		0	18	125	ps	1
Fall Time Variation	d-t_f		0	19	125	ps	1
Duty Cycle	d_{t3}	Measured Differentially	45	50	55	%	1
Skew, output to output	t_{sk3COM}	T_A = Commercial, V_T=50%		30	50	ps	1
	t_{sk3IND}	T_A = Industrial, V_T=50%		35	65	ps	1
Jitter, Cycle to cycle	$t_{jcyc-cyc}$	Measurement from differential wavefrom		17	50	ps	1

[1]Guaranteed by design and characterization, not 100% tested in production.

[2] All Long Term Accuracy

[3] Figures are for down spread.

[4] This figure is the peak-to-peak phase jitter as defined by PCI-SIG for a PCI Express reference clock. Please visit http://www.pcisig.com for additional details

[5] +/- 50 ppm at any frequency with spread off

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General SMBus Serial Interface Information for ICS9FG108E

How to Write

- Controller (host) sends a start bit
- Controller (host) sends the write address
- IDT clock will **acknowledge**
- Controller (host) sends the beginning byte location = N
- IDT clock will **acknowledge**
- Controller (host) sends the byte count = X
- IDT clock will **acknowledge**
- Controller (host) starts sending Byte **N through Byte N+X-1**
- IDT clock will **acknowledg**e each byte **one at a time**
- Controller (host) sends a Stop bit

Index Block Write Operation			
Controller (Host)			**IDT (Slave/Receiver)**
T	starT bit		
Slave Address			
WR	WRite		
			ACK
Beginning Byte = N			
			ACK
Data Byte Count = X			
			ACK
Beginning Byte N		X Byte	
			ACK
O			
O			O
O			O
			O
Byte N + X - 1			
			ACK
P	stoP bit		

Read Address	Write Address
$DD_{(H)}$	$DC_{(H)}$

How to Read

- Controller (host) will send a start bit
- Controller (host) sends the write address
- IDT clock will **acknowledge**
- Controller (host) sends the beginning byte location = N
- IDT clock will **acknowledge**
- Controller (host) will send a separate start bit
- Controller (host) sends the read address
- IDT clock will **acknowledge**
- IDT clock will send the data byte count = X
- IDT clock sends Byte **N+X-1**
- IDT clock sends **Byte 0 through Byte X (if $X_{(H)}$ was written to Byte 8)**
- Controller (host) will need to acknowledge each byte
- Controller (host) will send a not acknowledge bit
- Controller (host) will send a stop bit

Index Block Read Operation			
Controller (Host)			**IDT (Slave/Receiver)**
T	starT bit		
Slave Address			
WR	WRite		
			ACK
Beginning Byte = N			
			ACK
RT	Repeat starT		
Slave Address			
RD	ReaD		
			ACK
			Data Byte Count=X
ACK			
		X Byte	Beginning Byte N
ACK			
			O
O			O
O			O
O			
			Byte N + X - 1
N	Not acknowledge		
P	stoP bit		

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SMBus Table: Device Control Register, READ/WRITE ADDRESS (DC/DD)

Byte 0	Pin #	Name	Control Function	Type	0	1	Default
Bit 7	27		FS3[1]	RW	See Frequency Selection Table, Page 1		Pin 27
Bit 6	5		FS2[1]	RW			Pin 5
Bit 5	44		FS1[1]	RW			Pin 44
Bit 4	7		FS0[1]	RW			Pin 7
Bit 3	26		Spread Enable[1]	RW	Off	On	Pin 26
Bit 2	-		Enable Software Control of Frequency, Spread Enable (Spread Type always Software Control)	RW	Hardware Select	Software Select	0
Bit 1	-		DIF_STOP# drive mode	RW	Driven	Hi-Z	0
Bit 0	-		Spread Type	RW	Down	Center	0

Notes:
1. These bits reflect the state of the corresponding pins at power up, but may be written to if Byte 0, bit 2 is set to '1'. FS3 is the SEL14M_25M# pin.

SMBus Table: Output Enable Register

Byte 1	Pin #	Name	Control Function	Type	0	1	Default
Bit 7	-	DIF_7 EN	Output Enable	RW	Disable	Enable	1
Bit 6	-	DIF_6 EN	Output Enable	RW	Disable	Enable	1
Bit 5	-	DIF_5 EN	Output Enable	RW	Disable	Enable	1
Bit 4	-	DIF_4 EN	Output Enable	RW	Disable	Enable	1
Bit 3	-	DIF_3 EN	Output Enable	RW	Disable	Enable	1
Bit 2	-	DIF_2 EN	Output Enable	RW	Disable	Enable	1
Bit 1	-	DIF_1 EN	Output Enable	RW	Disable	Enable	1
Bit 0	-	DIF_0 EN	Output Enable	RW	Disable	Enable	1

Note: Byte 1 sets outputs active or inactive, not the conditons set by the OE inputs.

SMBus Table: Output Stop Mode Register

Byte 2	Pin #	Name	Control Function	Type	0	1	Default
Bit 7	-	DIF_7 STOP EN	Free Run/ Stop Enable	RW	Free-run	Stop-able	0
Bit 6	-	DIF_6 STOP EN	Free Run/ Stop Enable	RW	Free-run	Stop-able	0
Bit 5	-	DIF_5 STOP EN	Free Run/ Stop Enable	RW	Free-run	Stop-able	0
Bit 4	-	DIF_4 STOP EN	Free Run/ Stop Enable	RW	Free-run	Stop-able	0
Bit 3	-	DIF_3 STOP EN	Free Run/ Stop Enable	RW	Free-run	Stop-able	0
Bit 2	-	DIF_2 STOP EN	Free Run/ Stop Enable	RW	Free-run	Stop-able	0
Bit 1	-	DIF_1 STOP EN	Free Run/ Stop Enable	RW	Free-run	Stop-able	0
Bit 0	-	DIF_0 STOP EN	Free Run/ Stop Enable	RW	Free-run	Stop-able	0

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SMBus Table: Frequency Select Readback Register

Byte 3	Pin #	Name	Control Function	Type	0	1	Default
Bit 7	27	SEL14M_25M#[1] (FS3)	State of pin 27	R	See Frequency Selection Table, Page 1		Pin 27
Bit 6	6	FS2[1]	State of pin 6	R			Pin 6
Bit 5	44	FS1[1]	State of pin 44	R			Pin 44
Bit 4	45	FS0[1]	State of pin 45	R			Pin 45
Bit 3	26	SPREAD[1]	State of pin 26	R	Off	On	Pin 26
Bit 2		Reserved		R	Reserved		X
Bit 1		Reserved		R	Reserved		X
Bit 0		Reserved		R	Reserved		X

Notes:
1. These bits reflect the state of the corresponding pins, regardless of whether software programming is enabled or not.

SMBus Table: Vendor & Revision ID Register

Byte 4	Pin #	Name	Control Function	Type	0	1	Default
Bit 7	-	RID3	REVISION ID	R	Rev E = 1000		X
Bit 6	-	RID2		R			X
Bit 5	-	RID1		R			X
Bit 4	-	RID0		R			X
Bit 3	-	VID3	VENDOR ID	R	-	-	0
Bit 2	-	VID2		R	-	-	0
Bit 1	-	VID1		R	-	-	0
Bit 0	-	VID0		R	-	-	1

SMBus Table: DEVICE ID

Byte 5	Pin #	Name	Control Function	Type	0	1	Default
Bit 7	-	DEVID7	Device ID = 08 hex	R	Reserved		0
Bit 6	-	DEVID6		R	Reserved		0
Bit 5	-	DEVID5		R	Reserved		0
Bit 4	-	DEVID4		R	Reserved		0
Bit 3	-	DEVID3		R	Reserved		1
Bit 2	-	DEVID2		R	Reserved		0
Bit 1	-	DEVID1		R	Reserved		0
Bit 0	-	DEVID0		R	Reserved		0

SMBus Table: Byte Count Register

Byte 6	Pin #	Name	Control Function	Type	0	1	Default
Bit 7	-	BC7	Writing to this register will configure how many bytes will be read back, default is 07 = 7 bytes.	RW	-	-	0
Bit 6	-	BC6		RW	-	-	0
Bit 5	-	BC5		RW	-	-	0
Bit 4	-	BC4		RW	-	-	0
Bit 3	-	BC3		RW	-	-	0
Bit 2	-	BC2		RW	-	-	1
Bit 1	-	BC1		RW	-	-	1
Bit 0	-	BC0		RW	-	-	1

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SMBus Table: Reserved Register

Byte 7	Pin #	Name	Control Function	Type	0	1	Default
Bit 7		Reserved					X
Bit 6		Reserved					X
Bit 5		Reserved					X
Bit 4		Reserved					X
Bit 3		Reserved					X
Bit 2		Reserved					X
Bit 1		Reserved					X
Bit 0		Reserved					X

SMBus Table: Reserved Register

Byte 8	Pin #	Name	Control Function	Type	0	1	Default
Bit 7		Reserved					X
Bit 6		Reserved					X
Bit 5		Reserved					X
Bit 4		Reserved					X
Bit 3		Reserved					X
Bit 2		Reserved					X
Bit 1		Reserved					X
Bit 0		Reserved					X

SMBus Table: M/N Programming Enable

Byte 9	Pin #	Name	Control Function	Type	0	1	Default
Bit 7	-	M/N_EN	PLL M/N Programming Enable	RW	Disable	Enable	0
Bit 6	-	OE_Polarity	Select Polarity of OE inputs	RW	OE#	OE	1
Bit 5	5	REFOUT_En	Enables/Disables REF	RW	Disable	Enable	1
Bit 4		Reserved					0
Bit 3		Reserved					0
Bit 2		Reserved					0
Bit 1		Reserved					0
Bit 0		Reserved					0

SMBus Table: PLL Frequency Control Register

Byte 10	Pin #	Name	Control Function	Type	0	1	Default
Bit 7	-	PLL N Div8	N Divider Prog bit 8	RW	The decimal representation of M and N Divider in Byte 11 and 12 will configure the PLL VCO frequency. Default at power up = latch-in or Byte 0 Rom table. VCO Frequency = fXTAL x [NDiv(9:0)+8] / [MDiv(5:0)+2]		X
Bit 6	-	PLL N Div9	N Divider Prog bit 9	RW			X
Bit 5	-	PLL M Div5	M Divider Programming bit (5:0)	RW			X
Bit 4	-	PLL M Div4		RW			X
Bit 3	-	PLL M Div3		RW			X
Bit 2	-	PLL M Div2		RW			X
Bit 1	-	PLL M Div1		RW			X
Bit 0	-	PLL M Div0		RW			X

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SMBus Table: PLL Frequency Control Register

Byte 11	Pin #	Name	Control Function	Type	0	1	Default
Bit 7	-	PLL N Div7	N Divider Programming Byte11 bit(7:0) and Byte10 bit(7:6)	RW	The decimal representation of M and N Divider in Byte 11 and 12 will configure the PLL VCO frequency. Default at power up = latch-in or Byte 0 Rom table. VCO Frequency = fXTAL x [NDiv(9:0)+8] / [MDiv(5:0)+2]		X
Bit 6	-	PLL N Div6		RW			X
Bit 5	-	PLL N Div5		RW			X
Bit 4	-	PLL N Div4		RW			X
Bit 3	-	PLL N Div3		RW			X
Bit 2	-	PLL N Div2		RW			X
Bit 1	-	PLL N Div1		RW			X
Bit 0	-	PLL N Div0		RW			X

SMBus Table: PLL Spread Spectrum Control Register

Byte 12	Pin #	Name	Control Function	Type	0	1	Default
Bit 7	-	PLL SSP7	Spread Spectrum Programming bit(7:0)	RW	These Spread Spectrum bits in Byte 13 and 14 will program the spread pecentage of PLL		X
Bit 6	-	PLL SSP6		RW			X
Bit 5	-	PLL SSP5		RW			X
Bit 4	-	PLL SSP4		RW			X
Bit 3	-	PLL SSP3		RW			X
Bit 2	-	PLL SSP2		RW			X
Bit 1	-	PLL SSP1		RW			X
Bit 0	-	PLL SSP0		RW			X

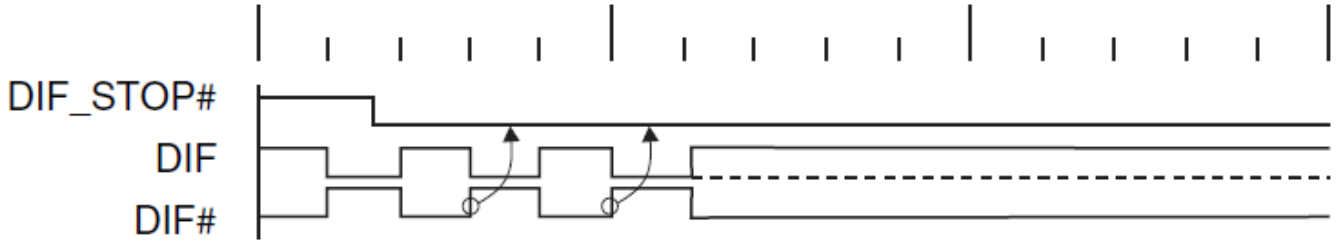
SMBus Table: PLL Spread Spectrum Control Register

Byte 13	Pin #	Name	Control Function	Type	0	1	Default
Bit 7	-	Reserved					0
Bit 6	-	PLL SSP14	Spread Spectrum Programming bit(14:8)	RW	These Spread Spectrum bits in Byte 13 and 14 will program the spread pecentage of PLL		X
Bit 5	-	PLL SSP13		RW			X
Bit 4	-	PLL SSP12		RW			X
Bit 3	-	PLL SSP11		RW			X
Bit 2	-	PLL SSP10		RW			X
Bit 1	-	PLL SSP9		RW			X
Bit 0	-	PLL SSP8		RW			X

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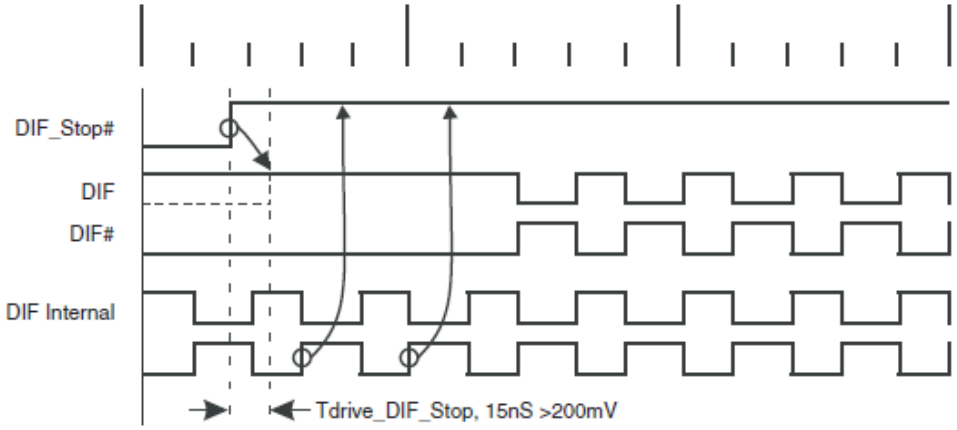
DIF_STOP# - Assertion (transition from '1' to '0')

Asserting DIF_STOP# pin stops all DIF outputs that are set to be stoppable after their next transition. When the SMBus DIF_STOP tri-state bit corresponding to the DIF output of interest is programmed to a '0', DIF output will stop DIF_True = HIGH and DIF_Complement = LOW. When the SMBus DIF_STOP tri-state bit corresponding to the DIF output of interest is programmed to a '1', DIF outputs will be tri-stated.



DIF_STOP# - De-assertion (transition from '0' to '1')

With the de-assertion of DIF_STOP# all stopped DIF outputs will resume without a glitch. The maximum latency from the de-assertion to active outputs is 2 - 6 DIF clock periods. If the control register tristate bit corresponding to the output of interest is programmed to '1', then the stopped DIF outputs will be driven High within 15nS of DIF_Stop# de-assertion to a voltage greater than 200mV.



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DIF Reference Clock			
Common Recommendations for Differential Routing	Dimension or Value	Unit	Figure
L1 length, route as non-coupled 50ohm trace	0.5 max	inch	1
L2 length, route as non-coupled 50ohm trace	0.2 max	inch	1
L3 length, route as non-coupled 50ohm trace	0.2 max	inch	1
Rs	33	ohm	1
Rt	49.9	ohm	1

Down Device Differential Routing			
L4 length, route as coupled microstrip 100ohm differential trace	2 min to 16 max	inch	1
L4 length, route as coupled stripline 100ohm differential trace	1.8 min to 14.4 max	inch	1

Differential Routing to PCI Express Connector			
L4 length, route as coupled microstrip 100ohm differential trace	0.25 to 14 max	inch	2
L4 length, route as coupled stripline 100ohm differential trace	0.225 min to 12.6 max	inch	2

Figure 1: Down Device Routing

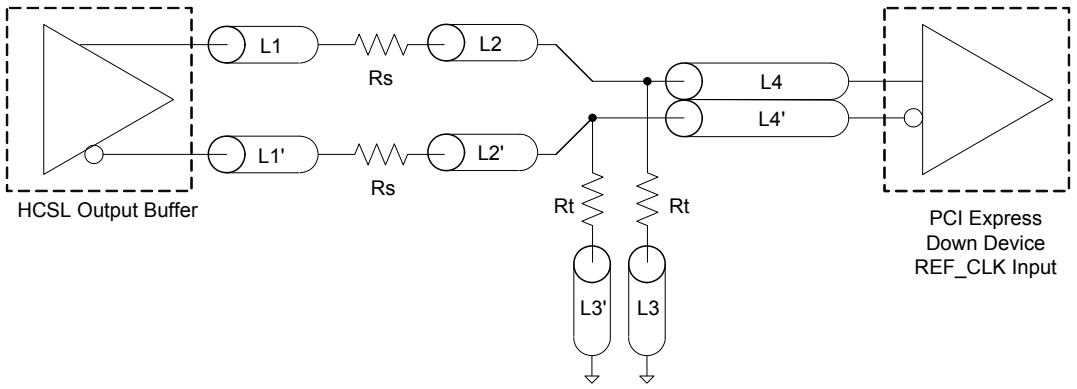
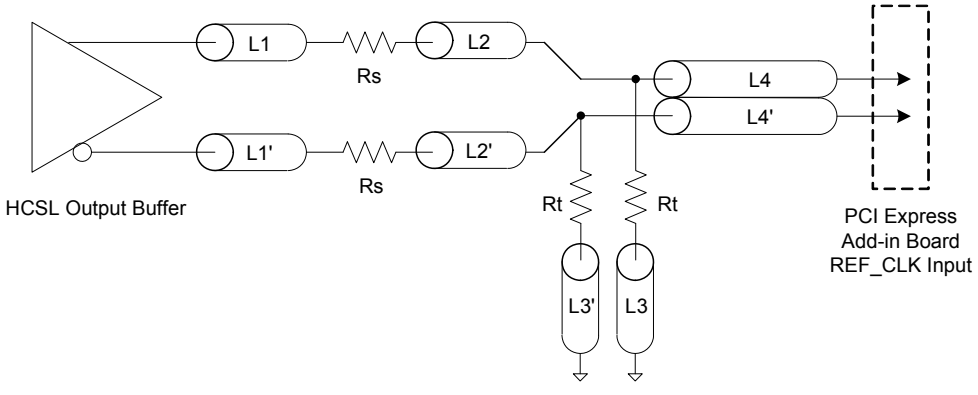


Figure 2: PCI Express Connector Routing

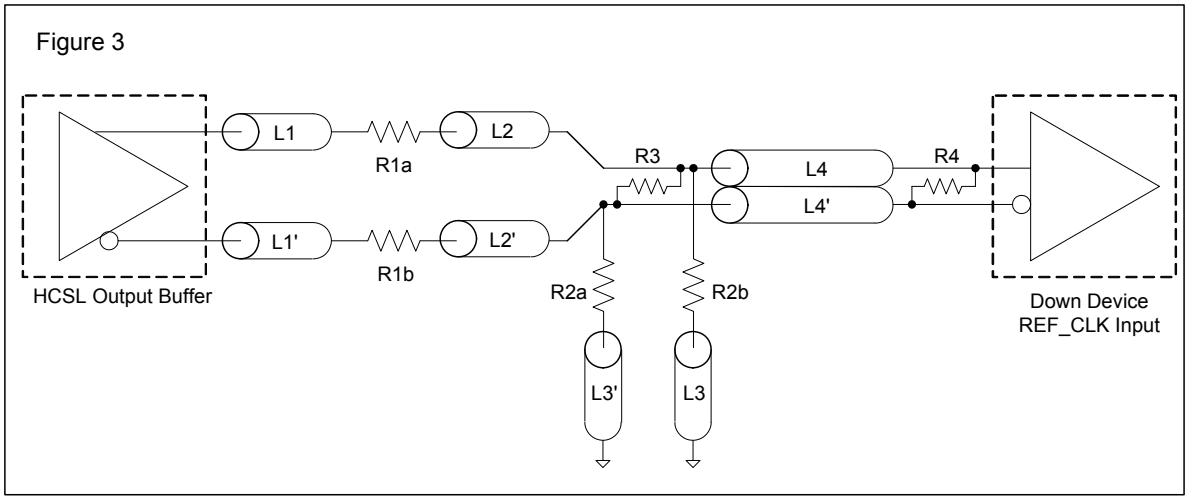


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Alternative Termination for LVDS and other Common Differential Signals (figure 3)							
Vdiff	Vp-p	Vcm	R1	R2	R3	R4	Note
0.45v	0.22v	1.08	33	150	100	100	
0.58	0.28	0.6	33	78.7	137	100	
0.80	0.40	0.6	33	78.7	none	100	ICS874003i-02 input compatible
0.60	0.3	1.2	33	174	140	100	Standard LVDS

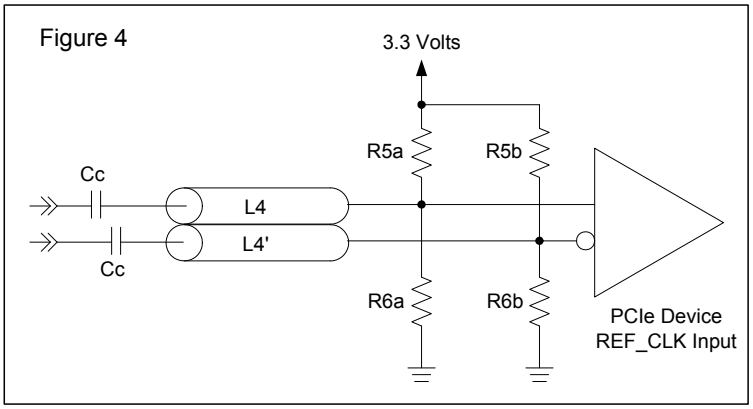
R1a = R1b = R1
R2a = R2b = R2

Figure 3



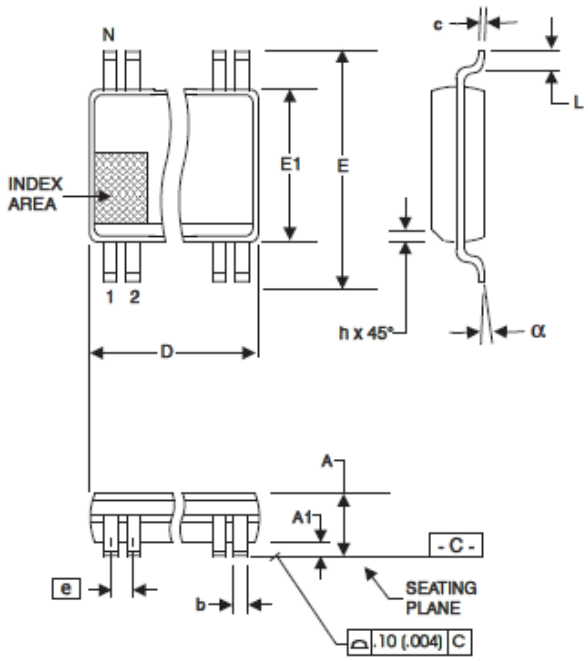
Cable Connected AC Coupled Application (figure 4)		
Component	Value	Note
R5a, R5b	8.2K 5%	
R6a, R6b	1K 5%	
Cc	0.1 µF	
Vcm	0.350 volts	

Figure 4



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Package Outline and Package Dimensions (48-SSOP)



48-Lead 300 mil SSOP

SYMBOL	In Millimeters COMMON DIMENSIONS		In Inches COMMON DIMENSIONS	
	MIN	MAX	MIN	MAX
A	2.41	2.80	.095	.110
A1	0.20	0.40	.008	.016
b	0.20	0.34	.008	.0135
c	0.13	0.25	.005	.010
D	SEE VARIATIONS		SEE VARIATIONS	
E	10.03	10.68	.395	.420
E1	7.40	7.60	.291	.299
e	0.635 BASIC		0.025 BASIC	
h	0.38	0.64	.015	.025
L	0.50	1.02	.020	.040
N	SEE VARIATIONS		SEE VARIATIONS	
α	0°	8°	0°	8°

VARIATIONS

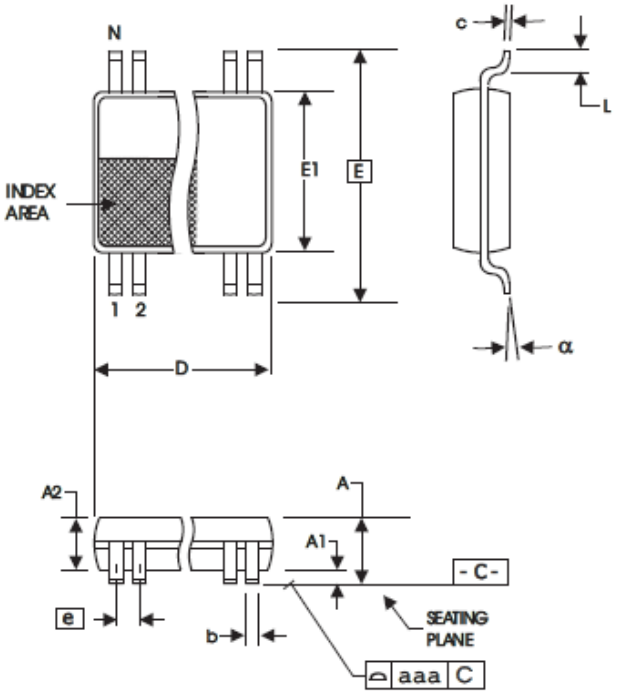
N	D mm.		D (inch)	
	MIN	MAX	MIN	MAX
48	15.75	16.00	.620	.630

Reference Doc.: JEDEC Publication 95, MO-118

10-0034

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Package Outline and Package Dimensions (48-TSSOP)



48-Lead, 6.10 mm. Body, 0.50 mm. Pitch TSSOP
(240 mil) (20 mil)

SYMBOL	In Millimeters COMMON DIMENSIONS		In Inches COMMON DIMENSIONS	
	MIN	MAX	MIN	MAX
A	--	1.20	--	.047
A1	0.05	0.15	.002	.006
A2	0.80	1.05	.032	.041
b	0.17	0.27	.007	.011
c	0.09	0.20	.0035	.008
D	SEE VARIATIONS		SEE VARIATIONS	
E	8.10 BASIC		0.319 BASIC	
E1	6.00	6.20	.236	.244
e	0.50 BASIC		0.020 BASIC	
L	0.45	0.75	.018	.030
N	SEE VARIATIONS		SEE VARIATIONS	
α	0°	8°	0°	8°
aaa	--	0.10	--	.004

VARIATIONS

N	D mm.		D (inch)	
	MIN	MAX	MIN	MAX
48	12.40	12.60	.488	.496

Reference Doc.: JEDEC Publication 95, MO-153

10-0039

Ordering Information

Part / Order Number	Shipping Packaging	Package	Temperature
9FG108EFLF	Tubes	48-pin SSOP	0 to +70°C
9FG108EFLFT	Tape and Reel	48-pin SSOP	0 to +70°C
9FG108EFILF	Tubes	48-pin SSOP	-40 to +85°C
9FG108EFILFT	Tape and Reel	48-pin SSOP	-40 to +85°C
9FG108EGLF	Tubes	48-pin TSSOP	0 to +70°C
9FG108EGLFT	Tape and Reel	48-pin TSSOP	0 to +70°C
9FG108EGILF	Tubes	48-pin TSSOP	-40 to +85°C
9FG108EGILFT	Tape and Reel	48-pin TSSOP	-40 to +85°C

"LF" suffix to the part number are the Pb-Free configuration and are RoHS compliant.

"E" is the device revision designator (will not correlate with the datasheet revision).

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Revision History

Rev.	Issue Date	Issuer	Description	Page #
A	6/21/2012	RDW	Moved from Advance to Final	
B	10/11/2012	RDW	Harmonized the Elecrical Tables with the 9FG104E	
C	10/29/2012	AT	Update the Jitter parameters in the table “Electrical Characteristics – REF 14.318/25MHz” to distinguish between commercial and industrial conditions. Added a separate line for each condition. For commercial, values were changed from 87ps Min & 250ps Max to 87ps Min & 200ps Max. For industrial, values are kept the same – 87ps Min & 250ps Max.	5

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(Rev.1.0 Mar 2020)

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