Frequency Gearing Clock for CPU, PCIe Gen1, Gen2 & FBD

ICS9FG1200D-1

Description

ICS9FG1200D-1 follows the Intel DB1200GS Differential Buffer Specification. This buffer provides 12 output clocks for CPU Host Bus, PCIe Gen2, or Fully Buffered DIMM applications. The outputs are configured with two groups. Both groups (DIF 9:0) and (DIF 11:10) can be equal to or have a gear ratio to the input clock. A differential CPU clock from a CK410B+ main clock generator, such as the ICS932S421, drives the . The can provide outputs up to 400MHz.

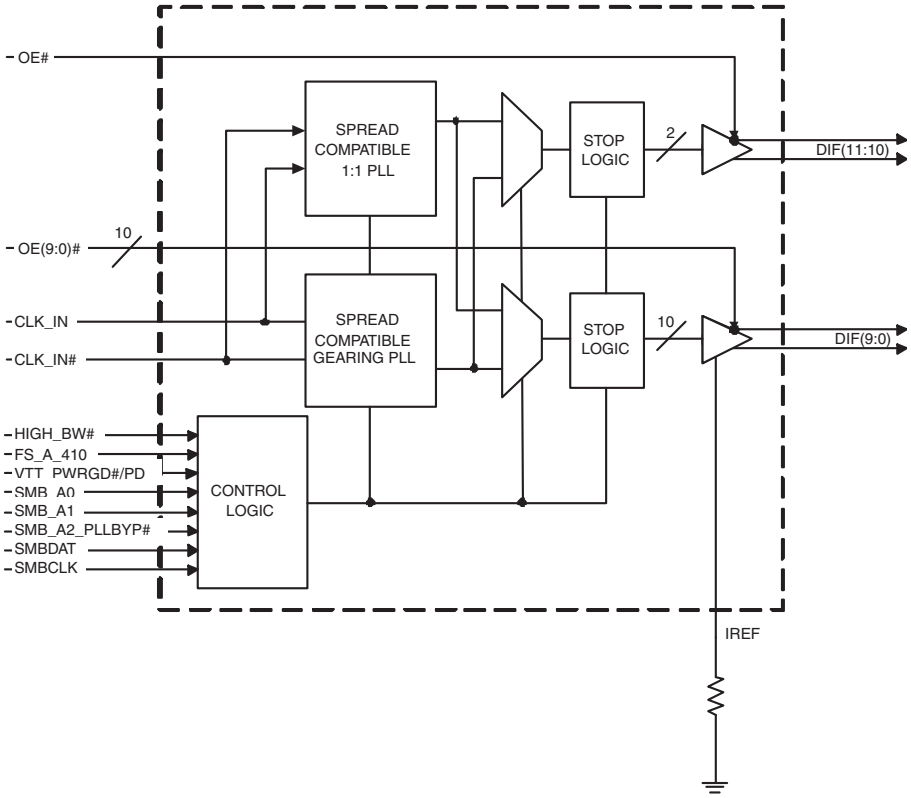
Features/Benefits

- Drives 2 channels of 4 FBDIMMs (total of 8 FBDIMMs)
- Power up default is all outputs in 1:1 mode
- DIF_(9:0) can be “gear-shifted” from the input CPU Host Clock
- DIF_(11:10) can be “gear-shifted” from the input CPU Host Clock
- Spread spectrum compatible
- Supports output clock frequencies up to 400 MHz
- 8 Selectable SMBus addresses
- SMBus address determines PLL or Bypass mode

Key Specifications

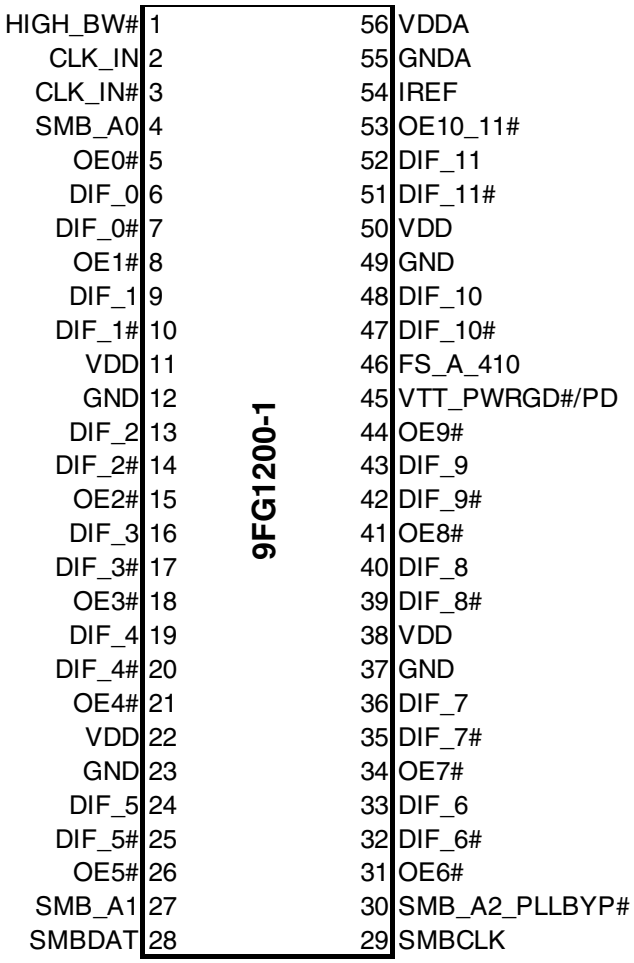
- DIF output cycle-to-cycle jitter < 50ps
- DIF output-to-output skew < 100ps across all outputs in 1:1 mode
- 56-pin SSOP/TSSOP package
- RoHS compliant packaging

Functional Block Diagram



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Pin Configuration



56-pin SSOP & TSSOP

Power Groups

Pin Number		Description
VDD	GND	
56	55	Main PLL, Analog
11,22,38,50	12,23,37,49	DIF clocks

Functionality at Power Up (PLL Mode)

FS_A_410[1]	CLK_IN (CPU FSB) MHz	DIF_(11:0) MHz
1	100 <= CLK_IN < 200	CLK_IN
0	200<= CLK_IN <= 400	CLK_IN

1. FS_A_410 is a low-threshold input. Please see the V_{IL_FS} and V_{IH_FS} specifications in the Input/Supply/Common Output Parameters Table for correct values.

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Pin Description

PIN #	PIN NAME	PIN TYPE	DESCRIPTION
1	HIGH_BW#	IN	3.3V input for selecting PLL Band Width 0 = High, 1= Low
2	CLK_IN	IN	Input for reference clock.
3	CLK_IN#	IN	"Complementary" reference clock input.
4	SMB_A0	IN	SMBus address bit 0 (LSB)
5	OE0#	IN	Active low input for enabling DIF pair 0. 1 = tri-state outputs, 0 = enable outputs
6	DIF_0	OUT	0.7V differential true clock output
7	DIF_0#	OUT	0.7V differential complement clock output
8	OE1#	IN	Active low input for enabling DIF pair 1. 1 = tri-state outputs, 0 = enable outputs
9	DIF_1	OUT	0.7V differential true clock output
10	DIF_1#	OUT	0.7V differential complement clock output
11	VDD	PWR	Power supply, nominal 3.3V
12	GND	PWR	Ground pin.
13	DIF_2	OUT	0.7V differential true clock output
14	DIF_2#	OUT	0.7V differential complement clock output
15	OE2#	IN	Active low input for enabling DIF pair 2. 1 = tri-state outputs, 0 = enable outputs
16	DIF_3	OUT	0.7V differential true clock output
17	DIF_3#	OUT	0.7V differential complement clock output
18	OE3#	IN	Active low input for enabling DIF pair 3. 1 = tri-state outputs, 0 = enable outputs
19	DIF_4	OUT	0.7V differential true clock output
20	DIF_4#	OUT	0.7V differential complement clock output
21	OE4#	IN	Active low input for enabling DIF pair 4 1 = tri-state outputs, 0 = enable outputs
22	VDD	PWR	Power supply, nominal 3.3V
23	GND	PWR	Ground pin.
24	DIF_5	OUT	0.7V differential true clock output
25	DIF_5#	OUT	0.7V differential complement clock output
26	OE5#	IN	Active low input for enabling DIF pair 5. 1 = tri-state outputs, 0 = enable outputs
27	SMB_A1	IN	SMBus address bit 1
28	SMBDAT	I/O	Data pin of SMBUS circuitry, 5V tolerant

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Pin Description (continued)

PIN #	PIN NAME	Type	Pin Description
29	SMBCLK	IN	Clock pin of SMBUS circuitry, 5V tolerant
30	SMB_A2_PLLBYP#	IN	SMBus address bit 2. When Low, the part operates as a fanout buffer with the PLL bypassed. When High, the part operates as a zero-delay buffer (ZDB) with the PLL operating. 0 = fanout mode (PLL bypassed), 1 = ZDB mode (PLL used)
31	OE6#	IN	Active low input for enabling DIF pair 6. 1 = tri-state outputs, 0 = enable outputs
32	DIF_6#	OUT	0.7V differential complement clock output
33	DIF_6	OUT	0.7V differential true clock output
34	OE7#	IN	Active low input for enabling DIF pair 7. 1 = tri-state outputs, 0 = enable outputs
35	DIF_7#	OUT	0.7V differential complement clock output
36	DIF_7	OUT	0.7V differential true clock output
37	GND	PWR	Ground pin.
38	VDD	PWR	Power supply, nominal 3.3V
39	DIF_8#	OUT	0.7V differential complement clock output
40	DIF_8	OUT	0.7V differential true clock output
41	OE8#	IN	Active low input for enabling DIF pair 8. 1 = tri-state outputs, 0 = enable outputs
42	DIF_9#	OUT	0.7V differential complement clock output
43	DIF_9	OUT	0.7V differential true clock output
44	OE9#	IN	Active low input for enabling DIF pair 9. 1 = tri-state outputs, 0 = enable outputs
45	VTT_PWRGD#/PD	IN	Vtt_PwrGd# is an active low input used to determine when latched inputs are ready to be sampled. PD is an asynchronous active high input pin used to put the device into a low power state. The internal clocks, PLLs and the crystal oscillator are stopped.
46	FS_A_410	IN	3.3V tolerant low threshold input for CPU frequency selection. This pin requires CK410 FSA. Refer to input electrical characteristics for Vil_FS and Vih_FS threshold values.
47	DIF_10#	OUT	0.7V differential complement clock output
48	DIF_10	OUT	0.7V differential true clock output
49	GND	PWR	Ground pin.
50	VDD	PWR	Power supply, nominal 3.3V
51	DIF_11#	OUT	0.7V differential complement clock output
52	DIF_11	OUT	0.7V differential true clock output
53	OE10_11#	IN	Active low input for enabling output pairs 10 and 11. 1 = tri-state outputs, 0 = enable outputs
54	IREF	OUT	This pin establishes the reference current for the differential current-mode output pairs. This pin requires a fixed precision resistor tied to ground in order to establish the appropriate current. 475 ohms is the standard value.
55	GNDA	PWR	Ground pin for the PLL core.
56	VDDA	PWR	3.3V power for the PLL core.

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9FG1200-1 Programmable Gear Ratios

CLK_IN (CPU FSB) MHz	Geared DIF Outputs MHz	M	n	Gear Ratio n/M	(FS_A#) Byte 0, bit 4 FS4	Byte 0, bit 3 FS3	Byte 0, bit 2 FS2	Byte 0, bit 1 FS1	Byte 0, bit 0 FS0	Notes
100.00	133.33	3	4	1.333	0	0	0	0	0	
100.00	166.67	3	5	1.667	0	0	0	0	1	
100.00	200.00	1	2	2.000	0	0	0	1	0	
100.00	266.67	3	8	2.667	0	0	0	1	1	
100.00	333.33	3	10	3.333	0	0	1	0	0	
100.00	400.00	1	4	4.000	0	0	1	0	1	
133.33	166.67	4	5	1.250	0	0	1	1	0	1
133.33	200.00	2	3	1.500	0	0	1	1	1	1
133.33	266.67	1	2	1.250	0	1	0	0	0	
133.33	333.33	2	5	1.500	0	1	0	0	1	
133.33	400.00	1	3	3.000	0	1	0	1	0	
166.67	**133.33**	**5**	**4**	**0.800**	**0**	**1**	**0**	**1**	**1**	1,3
166.67	200.00	5	6	1.200	0	1	1	0	0	1
166.67	266.67	5	8	1.600	0	1	1	0	1	
160.00	320.00	1	2	2.000	0	1	1	1	0	1,2
166.67	333.33									
166.67	400.00	5	12	2.400	0	1	1	1	1	
200.00	133.33	3	2	0.667	1	0	0	0	0	1
200.00	166.67	6	5	0.833	1	0	0	0	1	1
200.00	266.67	3	4	1.333	1	0	0	1	0	1
200.00	333.33	3	5	1.667	1	0	0	1	1	1
200.00	400.00	1	2	2.000	1	0	1	0	0	1
266.67	133.33	2	1	0.500	1	0	1	0	1	1
266.67	166.67	8	5	0.625	1	0	1	1	0	1, 6
320.00	200.00									
266.67	200.00	4	3	0.750	1	0	1	1	1	1
333.33	133.33	5	2	0.400	1	1	0	0	0	1
320.00	160.00	2	1	0.500	1	1	0	0	1	1,5
333.33	166.67									
333.33	200.00	5	3	0.600	1	1	0	1	0	1
400.00	**133.33**	**3**	**1**	**0.333**	**1**	**1**	**0**	**1**	**1**	1,4
400.00	160.00	5	2	0.400	1	1	1	0	0	1
400.00	166.67	12	5	0.417	1	1	1	0	1	1
400.00	320.00	5	4	0.800	1	1	1	1	0	1
400.00	333.33	6	5	0.833	1	1	1	1	1	1

Notes:
1. Targetted input/output frequency pairs
2. This Gear is also used for 160MHz/320 MHz.
3. Gear Ratio 5/4 is power up default for FS_A_410 = 1
4. Gear Ratio 3/1 is power up default for FS_A_410 = 0
5. This Gear is also used for 400MHz/200MHz
6. This Gear is also used for 320MHz/200MHz

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9FG1200-1 1:1 PLL Programming

Byte 8, bit 2 FSC	Byte 8, bit 1 FSB	Byte 8, bit 0 FS_A_410	CLK_IN (CPU FSB) MHz	1:1 DIF Outputs MHz	Notes
1	0	1	100.00	100.00	3
0	0	1	133.33	133.33	3
0	**1**	**1**	**166.67**	**166.67**	1
0	1	0	200.00	200.00	3
0	0	0	266.67	266.67	3
1	0	0	333.33	333.33	3
1	**1**	**0**	**400.00**	**400.00**	2
1	1	1	Reserved		

Notes:FS_A_410 = 1

1. Powerup Default for FS_A_410 = 1
2. Powerup Default for FS_A_410 = 0
3. Setting the exact FSB frequency after Power up is required for best phase noise performance.

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Absolute Maximum Ratings

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	Notes
3.3V Core Supply Voltage	VDD_A		GND - 0.5		V_{DD} + 0.5V	V	1
3.3V Logic Supply Voltage	VDD_In		GND - 0.5		V_{DD} + 0.5V	V	1
Storage Temperature	Ts		-65		150	°C	1
Ambient Operating Temp	Tambient		0		70	°C	1
Case Temperature	Tcase				115	°C	1
Input ESD protection	ESD prot	Human Body Model	2000			V	1

Electrical Characteristics - Input/Supply/Common Output Parameters

T_A = 0 - 70°C; Supply Voltage V_{DD} = 3.3 V +/-5%

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	Notes
Input High Voltage	V_{IH}	3.3 V +/-5%, except CLK_IN	2		V_{DD} + 0.3	V	1
Input Low Voltage	V_{IL}	3.3 V +/-5%, except CLK_IN	V_{SS} - 0.3		0.8	V	1
Input High Current	I_{IH}	$V_{IN} = V_{DD}$	-5		5	uA	
Input Low Current	I_{IL1}	V_{IN} = 0 V; Inputs with no pull-up resistors	-5			uA	
Low Threshold Input-High Voltage	V_{IH_FS}	3.3 V +/-5%, Applies to FS_A_410 pin	0.7		V_{DD} + 0.3	V	1
Low Threshold Input-Low Voltage	V_{IL_FS}	3.3 V +/-5%, Applies to FS_A_410 pin	V_{SS} - 0.3		0.35	V	1
Operating Current	$I_{DD3.3OP}$	all outputs driven			375	mA	1
Powerdown Current	$I_{DD3.3PD}$	all differential pairs tri-stated			24	mA	1
Input Frequency	F_i	V_{DD} = 3.3 V	100		400	MHz	3
Pin Inductance	L_{pin}				7	nH	1
Input Capacitance	C_{IN}	Logic Inputs			6	pF	1
	C_{OUT}	Output pin capacitance			5	pF	1
Clk Stabilization	T_{STAB}	From V_{DD} Power-Up or de-assertion of PD# to 1st clock			1.8	ms	1
Modulation Frequency		Triangular Modulation	30		33	kHz	1
Tdrive_PD#		DIF output enable after PD# de-assertion			300	us	1
Tfall_Pd#		PD# fall time of			5	ns	1
Trise_Pd#		PD# rise time of			5	ns	2
SMBus Voltage	V_{MAX}	Maximum input voltage			5.5	V	1
Low-level Output Voltage	V_{OL}	@ I_{PULLUP}			0.4	V	1
Current sinking at V_{OL} = 0.4 V	I_{PULLUP}		4			mA	1
SCLK/SDATA Clock/Data Rise Time	T_{RI2C}	(Max VIL - 0.15) to (Min VIH + 0.15)			1000	ns	1
SCLK/SDATA Clock/Data Fall Time	T_{FI2C}	(Min VIH + 0.15) to (Max VIL - 0.15)			300	ns	1

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Electrical Characteristics - DIF 0.7V Current Mode Differential Pair

T_A = 0 - 70°C; V_{DD} = 3.3 V +/-5%; C_L =2pF, R_S=33.2Ω, R_P=49.9Ω, I_{REF} = 475Ω

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	NOTES
Current Source Output Impedance	Zo^1	$V_O = V_x$	3000			Ω	1
Voltage High	VHigh	Statistical measurement on single ended signal using oscilloscope math function.	660		850	mV	1,3
Voltage Low	VLow		-150		150		1,3
Max Voltage	Vovs	Measurement on single ended signal using absolute value.			1150	mV	1
Min Voltage	Vuds		-300				1
Crossing Voltage (abs)	Vcross(abs)		250		550	mV	1
Crossing Voltage (var)	d-Vcross	Variation of crossing over all edges			140	mV	1
Long Accuracy	ppm	see Tperiod min-max values	-300		300	ppm	1,2
Average period	Tperiod	400MHz nominal	2.4993		2.5008	ns	2
		400MHz spread	2.4993		2.5133	ns	2
		333.33MHz nominal	2.9991		3.0009	ns	2
		333.33MHz spread	2.9991		3.016	ns	2
		266.66MHz nominal	3.7489		3.7511	ns	2
		266.66MHz spread	3.7489		3.77	ns	2
		200MHz nominal	4.9985		5.0015	ns	2
		200MHz spread	4.9985		5.0266	ns	2
		166.66MHz nominal	5.9982		6.0018	ns	2
		166.66MHz spread	5.9982		6.0320	ns	2
		133.33MHz nominal	7.4978		7.5023	ns	2
		133.33MHz spread	7.4978		7.5400	ns	2
		100.00MHz nominal	9.9970		10.0030	ns	2
		100.00MHz spread	9.9970		10.0533	ns	2
Absolute min period	T_{absmin}	400MHz nominal/spread	2.4143			ns	1,2
		333.33MHz nominal/spread	2.9141			ns	1,2
		266.66MHz nominal/spread	3.6639			ns	1,2
		200MHz nominal/spread	4.8735			ns	1,2
		166.66MHz nominal/spread	5.8732			ns	1,2
		133.33MHz nominal/spread	7.3728			ns	1,2
		100.00MHz nominal/spread	9.8720			ns	1,2
Rise Time	t_r	V_{OL} = 0.175V, V_{OH} = 0.525V	175		700	ps	1
Fall Time	t_f	V_{OH} = 0.525V V_{OL} = 0.175V	175		700	ps	1
Rise Time Variation	d-t_r				125	ps	1
Fall Time Variation	d-t_f				125	ps	1
Duty Cycle	d_{t3}	Measurement from differential wavefrom	45		55	%	1
Jitter, Cycle to cycle	$t_{JCYC-CYC}$	PLL mode, from differential wavefrom			50	ps	1,4,5
	t_{JBYP}	Bypass mode as additive jitter			50	ps	1,4

Notes:

1.Guaranteed by design and characterization, not 100% tested in production.

2. All Long Term Accuracy and Clock Period specifications are guaranteed assuming that the input frequency meets CK410B+ accuracy requirements

3.IREF = VDD/(3xRR). For RR = 475Ω (1%), IREF = 2.32mA. IOH = 6 x IREF and VOH = 0.7V @ ZO=50Ω.

4. Measured into fixed 2 pF load cap. Input to output skew is measured at the first output edge following the corresponding input.

5. Measured from differential cross-point to differential cross-point

6. All Bypass Mode Input-to-Output specs refer to the timing between an input edge and the specific output edge created by it.

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Electrical Characteristics - Skew and Differential Jitter Parameters

T_A = 0 - 70°C; Supply Voltage V_{DD} = 3.3 V +/-5%

Group	Parameter	Description	Min	Typ	Max	Units	Notes
CLK_IN, DIF[x:0]	t_{SPO_PLL}	Input-to-Output Skew in PLL mode (1:1 only), nominal value @ 25°C, 3.3V	-500	140	500	ps	1,2,4,5,8, 12
CLK_IN, DIF[x:0]	t_{PD_BYP}	Input-to-Output Skew in Bypass mode (1:1 only), nominal value @ 25°C, 3.3V	2.5	3.1	4.5	ns	1,2,3,5, 12
CLK_IN, DIF [x:0]	Δt_{SPO_PLL}	Input-to-Output Skew Variation in PLL mode (over specified voltage / temperature operating ranges)		270	|350|	ps	1,2,4,5,6, 10,12
CLK_IN, DIF [x:0]	Δt_{PD_BYP}	Input-to-Output Skew Variation in Bypass mode (over specified voltage / temperature operating ranges)		470	|500|	ps	1,2,3,4,5, 6,10,12
DIF[11:10]	t_{SKEW_G2}	Output-to-Output Skew Group of 2 (Common to Bypass and PLL mode)		10	25	ps	1,2,12
DIF[9:0]	t_{SKEW_G10}	Output-to-Output Skew Group of 10 (Common to Bypass and PLL mode)		40	50	ps	1,2,12
DIF[11:0]	t_{SKEW_A12}	Output-to-Output Skew across all 12 outputs (Common to Bypass and PLL mode - all outputs at same gear)		80	100	ps	1,2,3,12
DIF[11:0]	t_{JPH}	Differential Phase Jitter (RMS Value)		5	10	ps	1,4,7,12
DIF[11:0]	$t_{SSTERROR}$	Differential Spread Spectrum Tracking Error (peak to peak)		40	80	ps	1,4,9,12
PLL Jitter Peaking	$j_{peak\text{-}hibw}$	(HIGH_BW# = 0)	0	2.15	2.5	dB	11,12
PLL Jitter Peaking	$j_{peak\text{-}lobw}$	(HIGH_BW# = 1)	0	1.2	2	dB	11,12
PLL Bandwidth	pll_{HIBW}	(HIGH_BW# = 0)	2	3.6	4	MHz	12,13
PLL Bandwidth	pll_{LOBW}	(HIGH_BW# = 1)	0.7	1.2	1.4	MHz	12,13

NOTES on Skew and Differential Jitter Parameters:

1. Measured into fixed 2 pF load cap. Input to output skew is measured at the first output edge following the corresponding input.
2. Measured from differential cross-point to differential cross-point
3. All Bypass Mode Input-to-Output specs refer to the timing between an input edge and the specific output edge created by it.
4. This parameter is deterministic for a given device
5. Measured with scope averaging on to find mean value.
6. Long-term variation from nominal of input-to-output skew over temperature and voltage for a single device.
7. This parameter is measured at the outputs of two separate 9FG1200D-1 devices driven by a single CK410B+. The 9FG1200D-1 must be set to high bandwidth. Differential phase jitter is the accumulation of the phase jitter not shared by the outputs (eg. not including the affects of spread spectrum). Target ranges of consideration are agents with BW of 1-22MHz and 11-33MHz.
8. t is the period of the input clock
9. Differential spread spectrum tracking error is the difference in spread spectrum tracking between two 9FG1200D-1 devices This parameter is measured at the outputs of two separate 9FG1200D-1 devices driven by a single CK410B+ in Spread Spectrum mode. The 9FG1200D-1 must set to high bandwidth. The spread spectrum characterisitics are : maximum of 0.5%, 30 to 33KHz modulation frequency, linear profile.
10. This parameter is an absolute value. It is not a double-sided figure.
11. Measured as maximum pass band gain. At frequencies within the loop BW, highest point of magnification is called PLL jitter peaking.
12. Guaranteed by design and characterization, not 100% tested in production.
13. Measured at 3 db down or half power point.

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Electrical Characteristics - Phase Jitter

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP.	MAX	UNITS	NOTES
Jitter, Phase	$t_{jphPCIe1}$	PCIe Gen 1 REFCLK phase jitter (including PLL BW 8 - 16 MHz, ζ = 0.54, Td=10 ns, Ftrk=1.5 MHz)		43/37	86	ps	1,2,3
	$t_{jphPCIe2Lo}$	PCIe Gen 2 REFCLK phase jitter (including PLL BW 8 - 16 MHz, ζ = 0.54, Td=12 ns) Lo-band content (10kHz to 1.5MHz)		1.2/1.3	3	ps rms	1,2
	$t_{jphPCIe2Hi}$	PCIe Gen 2 REFCLK phase jitter (including PLL BW 8 - 16 MHz, ζ = 0.54, Td=12 ns) Hi-band content (1.5MHz to Nyquist)		3.0/2.4	3.1	ps rms	1,2
	$t_{jphFBD1_3.2G}$	FBD REFCLK phase jitter (including PLL BW 11 - 33 MHz, ζ = 0.54, Td=12 ns Ftrl=0.2MHz)		2.5/2.1	3	ps (RMS)	1,2
	$t_{jphFBD1_4.8G}$	FBD REFCLK phase jitter (including PLL BW 11 - 33 MHz, ζ = 0.54, Td=12 ns Ftrl=0.2MHz)		2.0/1.6	2.5	ps (RMS)	1,2

Notes on Phase Jitter:

[1] See http://www.pcisig.com for complete specs. Guaranteed by design and characterization, not tested in production.

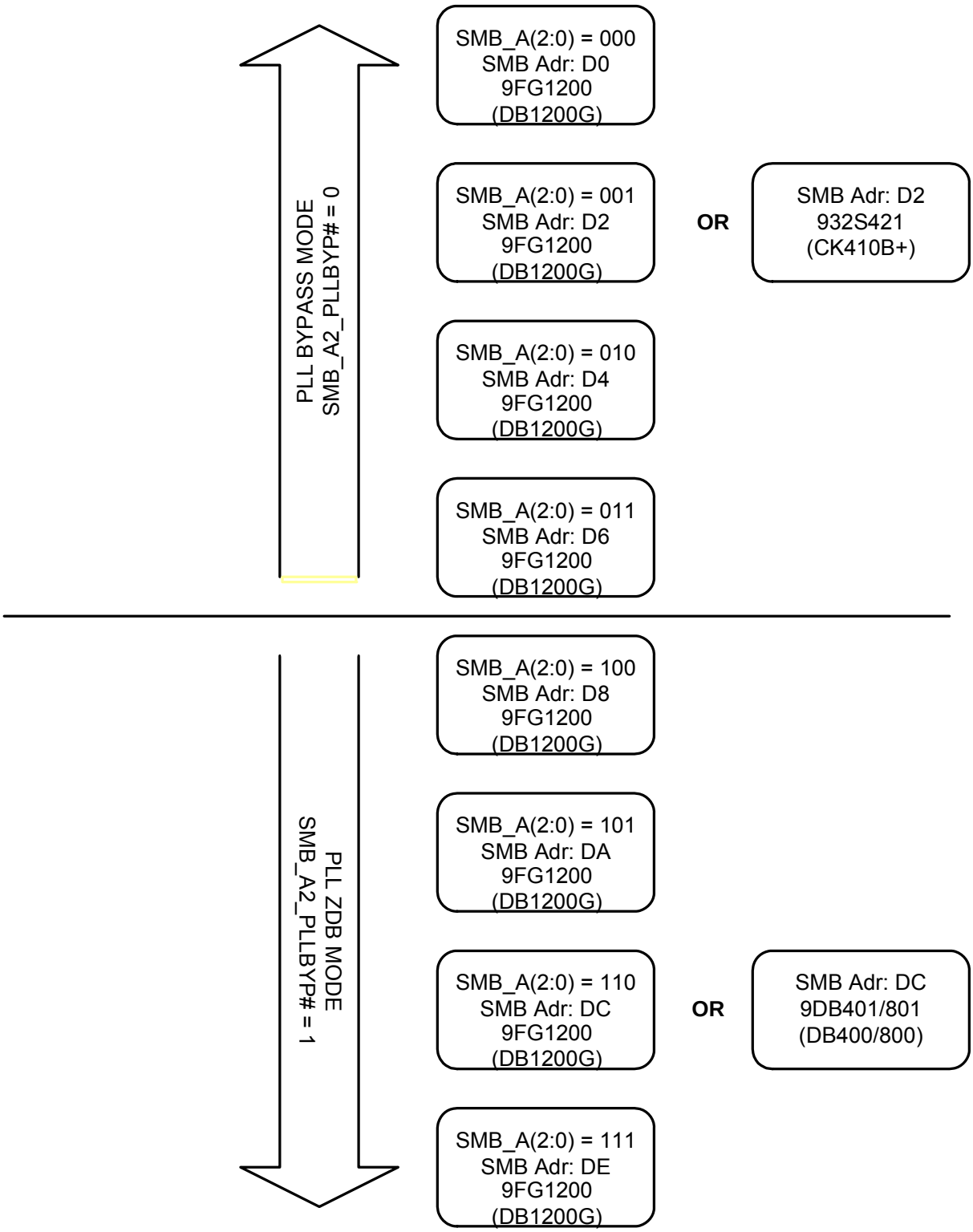
[2] Device driven by 932S421BGLF or equivalent

[3] Sample size of at least 100K cycles. This figures extrapolates to 108ps pk-pk @ 1M cycles for a BER of 1^{-12}

[4] Hi-Bandwidth Number/Low Bandwidth Number with Spread On. Spread Off gives lower numbers.

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9FG1200 SMBus Address Mapping
when using CK410B+ and DB400/800



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General SMBus serial interface information for the 9FG1200D-1

How to Write:

- Controller (host) sends a start bit.
- Controller (host) sends the write address D0 (h)
- ICS clock will ***acknowledge***
- Controller (host) sends the begining byte location = N
- ICS clock will ***acknowledge***
- Controller (host) sends the data byte count = X
- ICS clock will ***acknowledge***
- Controller (host) starts sending ***Byte N through Byte N + X -1***
- ICS clock will ***acknowledge*** each byte ***one at a time***
- Controller (host) sends a Stop bit

How to Read:

- Controller (host) will send start bit.
- Controller (host) sends the write address D0 (h)
- ICS clock will ***acknowledge***
- Controller (host) sends the begining byte location = N
- ICS clock will ***acknowledge***
- Controller (host) will send a separate start bit.
- Controller (host) sends the read address D1 (h)
- ICS clock will ***acknowledge***
- ICS clock will send the data byte count = X
- ICS clock sends ***Byte N + X -1***
- ICS clock sends ***Byte 0 through byte X (if $X_{(h)}$ was written to byte 8)***.
- Controller (host) will need to acknowledge each byte
- Controllor (host) will send a not acknowledge bit
- Controller (host) will send a stop bit

Index Block Write Operation

Controller (Host)			ICS (Slave/Receiver)
T	starT bit		
Slave Address $D0_{(h)}$*			
WR	WRite		
			ACK
Beginning Byte = N			
			ACK
Data Byte Count = X			
			ACK
Beginning Byte N		X Byte	
			ACK
◇			
◇			◇
◇			◇
			◇
Byte N + X - 1			
			ACK
P	stoP bit		

Index Block Read Operation

Controller (Host)		ICS (Slave/Receiver)	
T	starT bit		
Slave Address $D0_{(h)}$*			
WR	WRite		
		ACK	
Beginning Byte = N			
		ACK	
RT	Repeat starT		
Slave Address $D1_{(h)}$*			
RD	ReaD		
		ACK	
		Data Byte Count = X	
ACK			
		X Byte	Beginning Byte N
ACK			
			◇
◇			◇
◇			◇
◇			
			Byte N + X - 1
N	Not acknowledge		
P	stoP bit		

* Note: See SMBus Address Mapping (page 10), for programming SMBus Read/Write Address

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SMBusTable: Gear Ratio Select Register

Byte 0	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	DIF(9:0)	Group of 10 gear ratio enable		RW	Gear Ratio	1:1	**1**
Bit 6	DIF(11:10)	Group of 2 gear ratio enable		RW	Gear Ratio	1:1	**1**
Bit 5	-	Reserved		RW			1
Bit 4	-	Gear Ratio FS4 (FS_A_410#)		RW	See 9FG1200-1 Programmable Gear Ratios Table		Latch
Bit 3	-	Gear Ratio FS3		RW			1
Bit 2	-	Gear Ratio FS2		RW			0
Bit 1	-	Gear Ratio FS1		RW			1
Bit 0	-	Gear Ratio FS0		RW			1

SMBusTable: Output Control Register

Byte 1	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	35, 36	DIF_7	Output Control	RW	Hi-Z	Enable	1
Bit 6	32, 33	DIF_6	Output Control	RW	Hi-Z	Enable	1
Bit 5	24, 25	DIF_5	Output Control	RW	Hi-Z	Enable	1
Bit 4	19,20	DIF_4	Output Control	RW	Hi-Z	Enable	1
Bit 3	16,17	DIF_3	Output Control	RW	Hi-Z	Enable	1
Bit 2	13,14	DIF_2	Output Control	RW	Hi-Z	Enable	1
Bit 1	9,10	DIF_1	Output Control	RW	Hi-Z	Enable	1
Bit 0	6,7	DIF_0	Output Control	RW	Hi-Z	Enable	1

SMBusTable: Output and PLL BW Control Register

Byte 2	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7		Reserved					1
Bit 6	see note	PLL_BW# adjust		RW	High BW	Low BW	**1**
Bit 5	see note	BYPASS# test mode / PLL		RW	Bypass	PLL	**1**
Bit 4		Reserved					1
Bit 3	51,52	DIF_11	Output Control	RW	Hi-Z	Enable	1
Bit 2	47,48	DIF_10	Output Control	RW	Hi-Z	Enable	1
Bit 1	42,43	DIF_9	Output Control	RW	Hi-Z	Enable	1
Bit 0	39,40	DIF_8	Output Control	RW	Hi-Z	Enable	1

Note: Bit 6 is wired OR to the pin 1 input, any 0 selects High BW

Note: Bit 5 is wired OR to the pin 30 input, any 0 selects Fanout Bypass mode

SMBusTable: Output Enable Readback Register

Byte 3	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	34	Readback - OE7# Input		R	Readback		X
Bit 6	31	Readback - OE6# Input		R	Readback		X
Bit 5	26	Readback - OE5# Input		R	Readback		X
Bit 4	21	Readback - OE4# Input		R	Readback		X
Bit 3	18	Readback - OE3# Input		R	Readback		X
Bit 2	15	Readback - OE2# Input		R	Readback		X
Bit 1	8	Readback - OE1# Input		R	Readback		X
Bit 0	5	Readback - OE0# Input		R	Readback		X

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SMBusTable: Output Enable Readback Register

Byte 4	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	46	Readback - FS_A_410		R	Readback		X
Bit 6	1	Readback - HIGH_BW# In		R	Readback		X
Bit 5	30	Readback - SMB_A2_PLLBYP# In		R	Readback		X
Bit 4		Reserved		R	Readback		X
Bit 3		Reserved		R	Readback		X
Bit 2	53	Readback - OE10_11# Input		R	Readback		X
Bit 1	44	Readback - OE9# Input		R	Readback		X
Bit 0	41	Readback - OE8# Input		R	Readback		X

SMBusTable: Vendor & Revision ID Register

Byte 5	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	-	RID3	REVISION ID	R	-	-	X
Bit 6	-	RID2		R	-	-	X
Bit 5	-	RID1		R	-	-	X
Bit 4	-	RID0		R	-	-	X
Bit 3	-	VID3	VENDOR ID	R	-	-	0
Bit 2	-	VID2		R	-	-	0
Bit 1	-	VID1		R	-	-	0
Bit 0	-	VID0		R	-	-	1

SMBusTable: DEVICE ID

Byte 6	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	-	Device ID 7 (MSB)		RW	Reserved		1
Bit 6	-	Device ID 6		RW	Reserved		1
Bit 5	-	Device ID 5		RW	Reserved		0
Bit 4	-	Device ID 4		RW	Reserved		0
Bit 3	-	Device ID 3		RW	Reserved		0
Bit 2	-	Device ID 2		RW	Reserved		0
Bit 1	-	Device ID 1		RW	Reserved		0
Bit 0	-	Device ID 0		RW	Reserved		0

SMBusTable: Byte Count Register

Byte 7	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	-	BC7	Writing to this register configures how many bytes will be read back.	RW	-	-	0
Bit 6	-	BC6		RW	-	-	0
Bit 5	-	BC5		RW	-	-	0
Bit 4	-	BC4		RW	-	-	0
Bit 3	-	BC3		RW	-	-	1
Bit 2	-	BC2		RW	-	-	0
Bit 1	-	BC1		RW	-	-	0
Bit 0	-	BC0		RW	-	-	1

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SMBusTable: 1:1 PLL Frequency Selection

Byte 8	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7		RESERVED					0
Bit 6		RESERVED					0
Bit 5		RESERVED					0
Bit 4		RESERVED					0
Bit 3		RESERVED					0
Bit 2	-	Frequency Select C		RW	See 9FG1200-1 1:1 PLL Programming Table		x
Bit 1	-	Frequency Select B		RW			1
Bit 0	-	FS_A_410		RW			Latch

SMBusTable: Reserved Register

Byte 9	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7		RESERVED					0
Bit 6		RESERVED					0
Bit 5		RESERVED					0
Bit 4		RESERVED					0
Bit 3		RESERVED					0
Bit 2		RESERVED					0
Bit 1		RESERVED					0
Bit 0		RESERVED					0

SMBus Table: M/N Programming Enable

Byte 10	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	-	M/N_EN	Gear PLL and 1:1 PLL M/N Programming Enable	RW	Disable	Enable	0
Bit 6		RESERVED					X
Bit 5		RESERVED					X
Bit 4		RESERVED					X
Bit 3		RESERVED					X
Bit 2		RESERVED					X
Bit 1		RESERVED					X
Bit 0		RESERVED					X

SMBus Table: Gear PLL Frequency Control Register

Byte 11	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7		RESERVED					X
Bit 6		RESERVED					X
Bit 5	-	Gear PLL M Div5	M Divider Programming bits	RW	Contact IDT for 9FG1200-1 M/N programming Table		X
Bit 4	-	Gear PLL M Div4		RW			X
Bit 3	-	Gear PLL M Div3		RW			X
Bit 2	-	Gear PLL M Div2		RW			X
Bit 1	-	Gear PLL M Div1		RW			X
Bit 0	-	Gear PLL M Div0		RW			X

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SMBus Table: Gear PLL Frequency Control Register

Byte 12	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	-	Gear PLL N Div7	N Divider Programming bits	RW	Contact IDT for 9FG1200-1 M/N programming Table		X
Bit 6	-	Gear PLL N Div6		RW			X
Bit 5	-	Gear PLL N Div5		RW			X
Bit 4	-	Gear PLL N Div4		RW			X
Bit 3	-	Gear PLL N Div3		RW			X
Bit 2	-	Gear PLL N Div2		RW			X
Bit 1	-	Gear PLL N Div1		RW			X
Bit 0	-	Gear PLL N Div0		RW			X

SMBusTable: Gear PLL Output Divider Register

Byte 13	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7		RESERVED					0
Bit 6		RESERVED					0
Bit 5		RESERVED					0
Bit 4		RESERVED					0
Bit 3		GoutDiv 3	Gear Output Divider	RW	Contact IDT for Output Divider Table		X
Bit 2		GoutDiv 2		RW			X
Bit 1		GoutDiv 1		RW			X
Bit 0		GoutDiv 1		RW			X

SMBusTable: Reserved Register

Byte 14	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7		RESERVED					0
Bit 6		RESERVED					0
Bit 5		RESERVED					0
Bit 4		RESERVED					0
Bit 3		RESERVED					0
Bit 2		RESERVED					0
Bit 1		RESERVED					0
Bit 0		RESERVED					0

SMBusTable: Reserved Register

Byte 15	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7		RESERVED					0
Bit 6		RESERVED					0
Bit 5		RESERVED					0
Bit 4		RESERVED					0
Bit 3		RESERVED					0
Bit 2		RESERVED					0
Bit 1		RESERVED					0
Bit 0		RESERVED					0

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SMBusTable: Reserved Register

Byte 16	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7		RESERVED					0
Bit 6		RESERVED					0
Bit 5		RESERVED					0
Bit 4		RESERVED					0
Bit 3		RESERVED					0
Bit 2		RESERVED					0
Bit 1		RESERVED					0
Bit 0		RESERVED					0

SMBus Table: 1:1 PLL Frequency Control Register

Byte 17	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7		RESERVED					0
Bit 6		RESERVED					0
Bit 5	-	1:1 PLL M Div5	M Divider Programming bits	RW	Contact IDT for 9FG1200-1 M/N programming Table		X
Bit 4	-	1:1 PLL M Div4		RW			X
Bit 3	-	1:1 PLL M Div3		RW			X
Bit 2	-	1:1 PLL M Div2		RW			X
Bit 1	-	1:1 PLL M Div1		RW			X
Bit 0	-	1:1 PLL M Div0		RW			X

SMBus Table: 1:1 PLL Frequency Control Register

Byte 18	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	-	1:1 PLL N Div7	N Divider Programming bits	RW	Contact IDT for 9FG1200-1 M/N programming Table		X
Bit 6	-	1:1 PLL N Div6		RW			X
Bit 5	-	1:1 PLL N Div5		RW			X
Bit 4	-	1:1 PLL N Div4		RW			X
Bit 3	-	1:1 PLL N Div3		RW			X
Bit 2	-	1:1 PLL N Div2		RW			X
Bit 1	-	1:1 PLL N Div1		RW			X
Bit 0	-	1:1 PLL N Div0		RW			X

SMBusTable: 1:1 PLL Output Divider Register

Byte 19	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7		RESERVED					0
Bit 6		RESERVED					0
Bit 5		RESERVED					0
Bit 4		RESERVED					0
Bit 3		1outDiv 3	1:1 Output Divider	RW	Contact IDT for Output Divider Table		X
Bit 2		1outDiv 2		RW			X
Bit 1		1outDiv 1		RW			X
Bit 0		1outDiv 1		RW			X

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SMBusTable: Reserved Register

Byte 20	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7		RESERVED					0
Bit 6		RESERVED					0
Bit 5		RESERVED					0
Bit 4		RESERVED					0
Bit 3		RESERVED					0
Bit 2		RESERVED					0
Bit 1		RESERVED					0
Bit 0		RESERVED					0

SMBusTable: Test Byte Register

Byte 21	Test	Test Function	Type	Test Result	PWD
Bit 7	`	ICS ONLY TEST	RW	Reserved	0
Bit 6		ICS ONLY TEST	RW	Reserved	0
Bit 5		ICS ONLY TEST	RW	Reserved	0
Bit 4		ICS ONLY TEST	RW	Reserved	0
Bit 3		ICS ONLY TEST	RW	Reserved	0
Bit 2		ICS ONLY TEST	RW	Reserved	0
Bit 1		ICS ONLY TEST	RW	Reserved	0
Bit 0		ICS ONLY TEST	RW	Reserved	0

Note: Do NOT write to Bit 21. Erratic device operation will result!

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SRC Reference Clock			
Common Recommendations for Differential Routing	Dimension or Value	Unit	Figure
L1 length, route as non-coupled 50ohm trace	0.5 max	inch	1
L2 length, route as non-coupled 50ohm trace	0.2 max	inch	1
L3 length, route as non-coupled 50ohm trace	0.2 max	inch	1
Rs	33	ohm	1
Rt	49.9	ohm	1

Down Device Differential Routing			
L4 length, route as coupled microstrip 100ohm differential trace	2 min to 16 max	inch	1
L4 length, route as coupled stripline 100ohm differential trace	1.8 min to 14.4 max	inch	1

Differential Routing to PCI Express Connector			
L4 length, route as coupled microstrip 100ohm differential trace	0.25 to 14 max	inch	2
L4 length, route as coupled stripline 100ohm differential trace	0.225 min to 12.6 max	inch	2

Figure 1: Down Device Routing

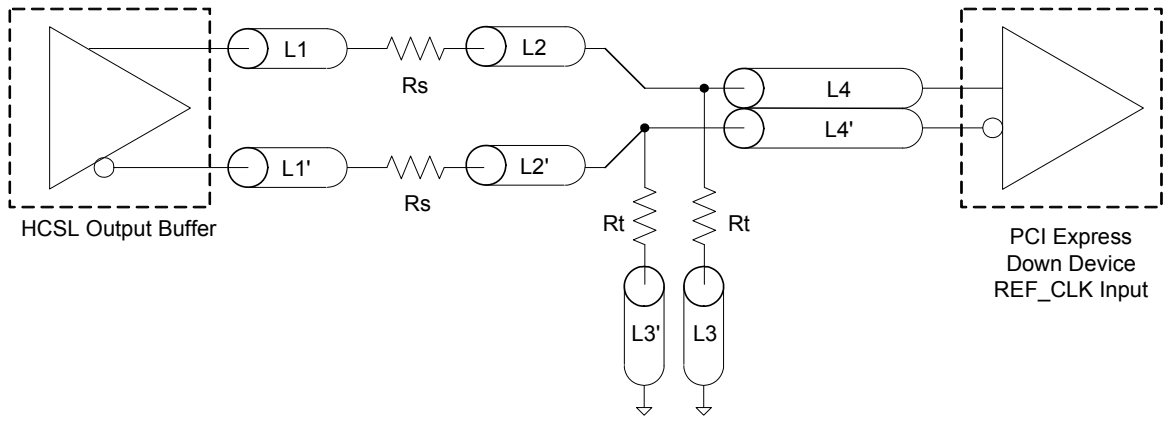
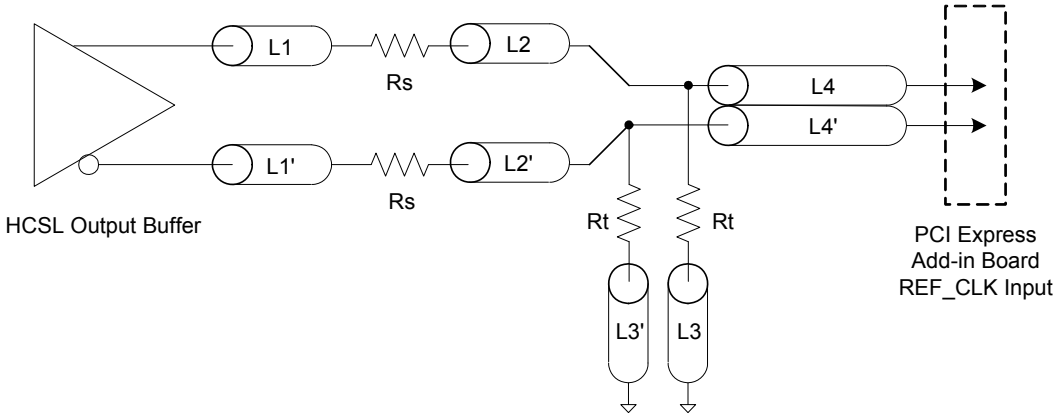


Figure 2: PCI Express Connector Routing

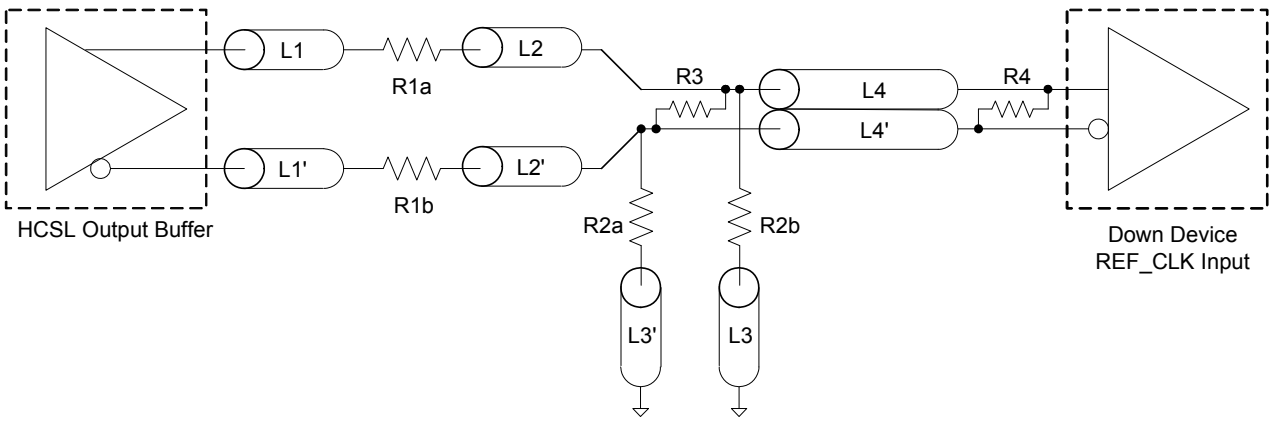


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Alternative Termination for LVDS and other Common Differential Signals (figure 3)							
Vdiff	Vp-p	Vcm	R1	R2	R3	R4	Note
0.45v	0.22v	1.08	33	150	100	100	
0.58	0.28	0.6	33	78.7	137	100	
0.80	0.40	0.6	33	78.7	none	100	ICS874003i-02 input compatible
0.60	0.3	1.2	33	174	140	100	Standard LVDS

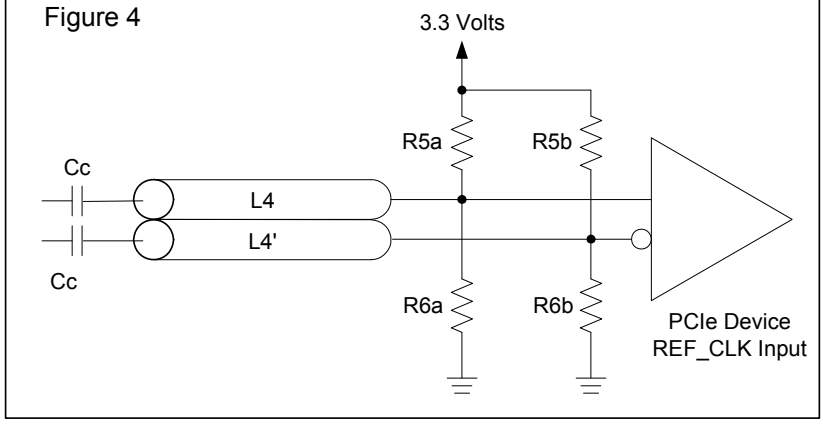
R1a = R1b = R1
R2a = R2b = R2

Figure 3

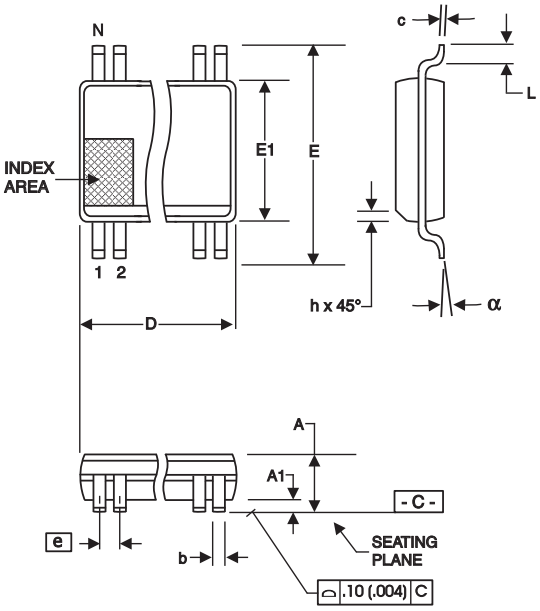


Cable Connected AC Coupled Application (figure 4)		
Component	Value	Note
R5a, R5b	8.2K 5%	
R6a, R6b	1K 5%	
Cc	0.1 µF	
Vcm	0.350 volts	

Figure 4



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56-Lead, 300 mil Body, 25 mil, SSOP

SYMBOL	In Millimeters COMMON DIMENSIONS		In Inches COMMON DIMENSIONS	
	MIN	MAX	MIN	MAX
A	2.41	2.80	.095	.110
A1	0.20	0.40	.008	.016
b	0.20	0.34	.008	.0135
c	0.13	0.25	.005	.010
D	SEE VARIATIONS		SEE VARIATIONS	
E	10.03	10.68	.395	.420
E1	7.40	7.60	.291	.299
e	0.635 BASIC		0.025 BASIC	
h	0.38	0.64	.015	.025
L	0.50	1.02	.020	.040
N	SEE VARIATIONS		SEE VARIATIONS	
a	0°	8°	0°	8°

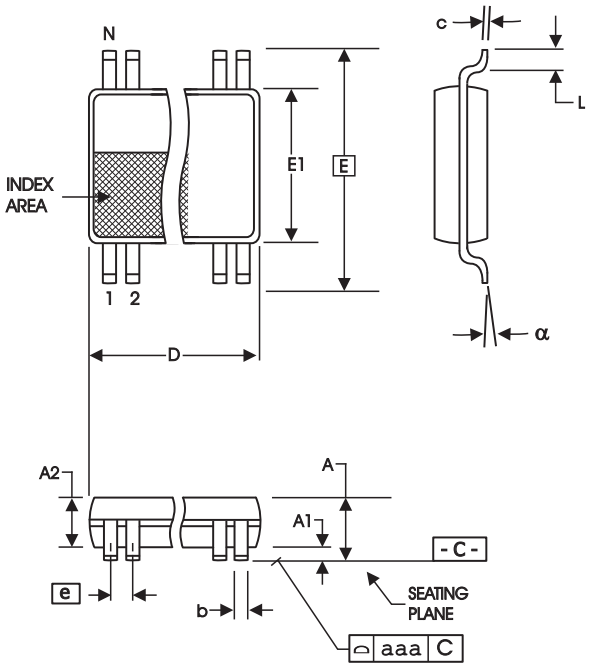
VARIATIONS

N	D mm.		D (inch)	
	MIN	MAX	MIN	MAX
56	18.31	18.55	.720	.730

Reference Doc.: JEDEC Publication 95, MO-118

10-0034

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56-Lead 6.10 mm. Body, 0.50 mm. Pitch TSSOP
(240 mil) (20 mil)

SYMBOL	In Millimeters COMMON DIMENSIONS		In Inches COMMON DIMENSIONS	
	MIN	MAX	MIN	MAX
A	--	1.20	--	.047
A1	0.05	0.15	.002	.006
A2	0.80	1.05	.032	.041
b	0.17	0.27	.007	.011
c	0.09	0.20	.0035	.008
D	SEE VARIATIONS		SEE VARIATIONS	
E	8.10 BASIC		0.319 BASIC	
E1	6.00	6.20	.236	.244
e	0.50 BASIC		0.020 BASIC	
L	0.45	0.75	.018	.030
N	SEE VARIATIONS		SEE VARIATIONS	
a	0°	8°	0°	8°
aaa	--	0.10	--	.004

VARIATIONS

N	D mm.		D (inch)	
	MIN	MAX	MIN	MAX
56	13.90	14.10	.547	.555

Reference Doc.: JEDEC Publication 95, MO-153

10-0039

Ordering Information

Part / Order Number	Shipping Packaging	Package	Temperature
9FG1200DF-1LF	Tubes	56-pin SSOP	0 to +70°C
9FG1200DF-1LFT	Tape and Reel	56-pin SSOP	0 to +70°C
9FG1200DG-1LF	Tubes	56-pin TSSOP	0 to +70°C
9FG1200DG-1LFT	Tape and Reel	56-pin TSSOP	0 to +70°C

"LF" suffix to the part numbers denotes Pb-Free configuration, RoHS compliant.
"D" is the device revision designator (will not correlate with the datasheet revision).

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Revision History

A	12/11/2007	Final Release.	-
B	1/21/2009	Update Skew and Phase Jitter tables.	10,11
C	2/8/2010	Updated part ordering information	

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(Rev.1.0 Mar 2020)

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