Frequency Gearing Clock for CPU, PCIe Gen1 & FBD

9FG1901H

Description

The **9FG1901H** follows the Intel DB1900G Differential Buffer Specification. This buffer provides 19 output clocks for CPU Host Bus, PCI-Express, or Fully Buffered DIMM applications. The outputs are configured with two groups. Both groups, DIF_(16:0) and DIF_(18:17) can be equal to or have a gear ratio to the input clock. A differential CPU clock from a CK410B+ main clock generator, such as the ICS932S421, drives the ICS9FG1901. The **9FG1901H** can provide outputs up to 400MHz.

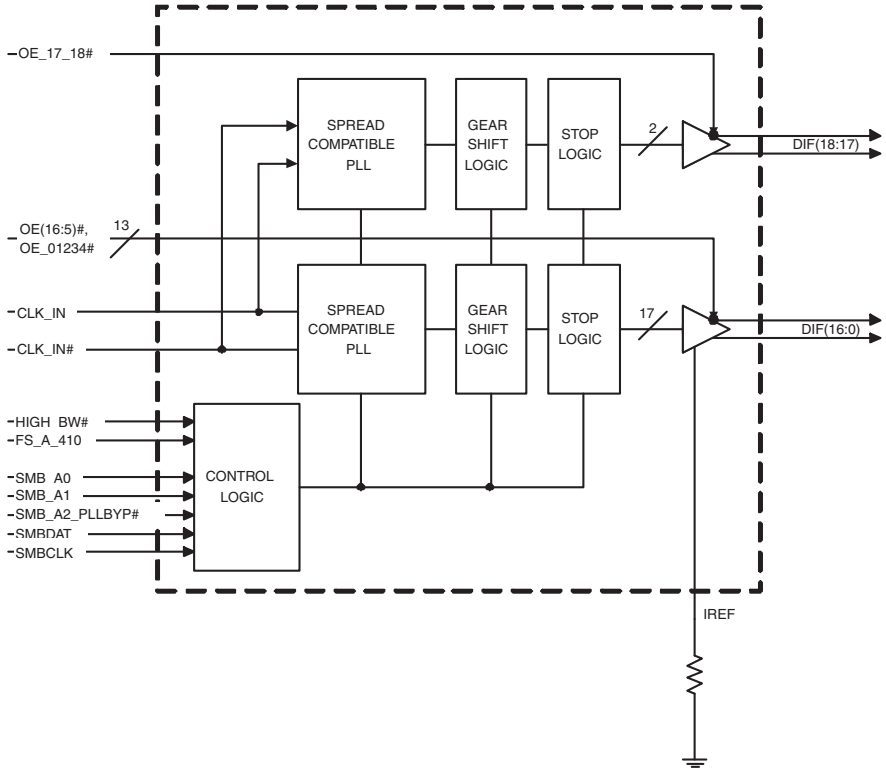
Features/Benefits

- Power up default is all outputs in 1:1 mode
- DIF_(16:0) can be “gear-shifted” from the input CPU Host Clock
- DIF_(18:17) can be “gear-shifted” from the input CPU Host Clock
- Spread spectrum compatible
- Supports output clock frequencies up to 400 MHz
- 8 Selectable SMBus addresses
- SMBus address determines PLL or Bypass mode
- VDDA controlled power down mode

Key Specifications

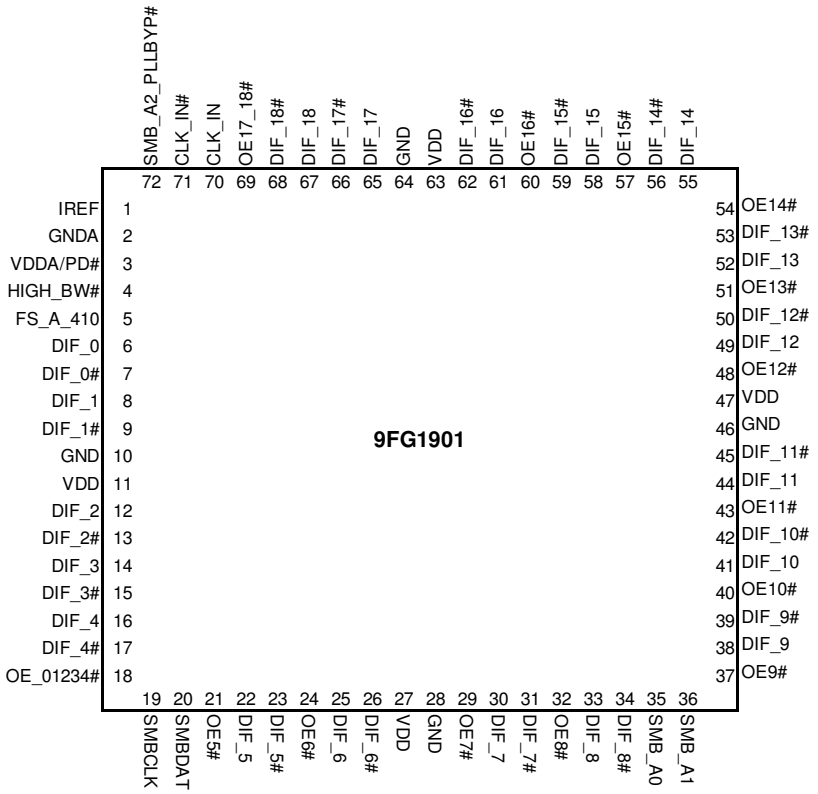
- DIF output cycle-to-cycle jitter < 50ps
- DIF output-to-output skew across all outputs in 1:1 mode < 150ps

Functional Block Diagram



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Pin Configuration



72-pin MLF

Functionality at Power Up (PLL Mode)

FS_A_410[1]	CLK_IN (CPU FSB) MHz	DIF(18:0) MHz
1	100 <= CLK_IN < 200	CLK_IN
0	200<= CLK_IN <= 400	CLK_IN

1. FS_A_410 is a low-threshold input. Please see the V_{IL_FS} and V_{IH_FS} specifications in the Input/Supply/Common Output Parameters Table for correct values.

Power Groups

Pin Number		Description
VDD	GND	
3	2	Main PLL, Analog
11,27,47,63	10,28,46,64	DIF clocks

Power Down Functionality

INPUTS		OUTPUTS		PLL State
VDDA/PD#	CLK_IN/CLK_IN#	DIF	DIF#	
3.3V (NOM)	Running	Running		ON
GND	X	Hi-Z		OFF

Functionality Note

It is recommended that Byte 2, bit 6 be toggled from 1 to 0 and back to 1, the first time VDDA is applied. This ensures proper initialization of the device.

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Pin Description

PIN #	PIN NAME	PIN TYPE	DESCRIPTION
1	IREF	OUT	This pin establishes the reference current for the differential current-mode output pairs. This pin requires a fixed precision resistor tied to ground in order to establish the appropriate current. 475 ohms is the standard value.
2	GNDA	PWR	Ground pin for the PLL core.
3	VDDA/PD#	PWR	3.3V power for the PLL core that also functions as Power Down. Collapsing this power supply places the device in Power Down mode.
4	HIGH_BW#	IN	3.3V input for selecting PLL Band Width 0 = High, 1= Low
5	FS_A_410	IN	3.3V tolerant low threshold input for CPU frequency selection. This pin requires CK410 FSA. Refer to input electrical characteristics for Vil_FS and Vih_FS threshold values.
6	DIF_0	OUT	0.7V differential true clock output
7	DIF_0#	OUT	0.7V differential complement clock output
8	DIF_1	OUT	0.7V differential true clock output
9	DIF_1#	OUT	0.7V differential complement clock output
10	GND	PWR	Ground pin.
11	VDD	PWR	Power supply, nominal 3.3V
12	DIF_2	OUT	0.7V differential true clock output
13	DIF_2#	OUT	0.7V differential complement clock output
14	DIF_3	OUT	0.7V differential true clock output
15	DIF_3#	OUT	0.7V differential complement clock output
16	DIF_4	OUT	0.7V differential true clock output
17	DIF_4#	OUT	0.7V differential complement clock output
18	OE_01234#	IN	Active low input for enabling DIF pairs 0, 1, 2, 3 and 4. 1 = tri-state outputs, 0 = enable outputs
19	SMBCLK	IN	Clock pin of SMBUS circuitry, 5V tolerant
20	SMBDAT	I/O	Data pin of SMBUS circuitry, 5V tolerant
21	OE5#	IN	Active low input for enabling DIF pair 5. 1 = tri-state outputs, 0 = enable outputs
22	DIF_5	OUT	0.7V differential true clock output
23	DIF_5#	OUT	0.7V differential complement clock output
24	OE6#	IN	Active low input for enabling DIF pair 6. 1 = tri-state outputs, 0 = enable outputs
25	DIF_6	OUT	0.7V differential true clock output
26	DIF_6#	OUT	0.7V differential complement clock output
27	VDD	PWR	Power supply, nominal 3.3V
28	GND	PWR	Ground pin.
29	OE7#	IN	Active low input for enabling DIF pair 7. 1 = tri-state outputs, 0 = enable outputs
30	DIF_7	OUT	0.7V differential true clock output
31	DIF_7#	OUT	0.7V differential complement clock output
32	OE8#	IN	Active low input for enabling DIF pair 8. 1 = tri-state outputs, 0 = enable outputs
33	DIF_8	OUT	0.7V differential true clock output
34	DIF_8#	OUT	0.7V differential complement clock output
35	SMB_A0	IN	SMBus address bit 0 (LSB)
36	SMB_A1	IN	SMBus address bit 1

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Pin Description (continued)

PIN #	PIN NAME	PIN TYPE	DESCRIPTION
37	OE9#	IN	Active low input for enabling DIF pair 9. 1 = tri-state outputs, 0 = enable outputs
38	DIF_9	OUT	0.7V differential true clock output
39	DIF_9#	OUT	0.7V differential complement clock output
40	OE10#	IN	Active low input for enabling DIF pair 10. 1 = tri-state outputs, 0 = enable outputs
41	DIF_10	OUT	0.7V differential true clock output
42	DIF_10#	OUT	0.7V differential complement clock output
43	OE11#	IN	Active low input for enabling DIF pair 11. 1 = tri-state outputs, 0 = enable outputs
44	DIF_11	OUT	0.7V differential true clock output
45	DIF_11#	OUT	0.7V differential complement clock output
46	GND	PWR	Ground pin.
47	VDD	PWR	Power supply, nominal 3.3V
48	OE12#	IN	Active low input for enabling DIF pair 12. 1 = tri-state outputs, 0 = enable outputs
49	DIF_12	OUT	0.7V differential true clock output
50	DIF_12#	OUT	0.7V differential complement clock output
51	OE13#	IN	Active low input for enabling DIF pair 13. 1 = tri-state outputs, 0 = enable outputs
52	DIF_13	OUT	0.7V differential true clock output
53	DIF_13#	OUT	0.7V differential complement clock output
54	OE14#	IN	Active low input for enabling DIF pair 14. 1 = tri-state outputs, 0 = enable outputs
55	DIF_14	OUT	0.7V differential true clock output
56	DIF_14#	OUT	0.7V differential complement clock output
57	OE15#	IN	Active low input for enabling DIF pair 15. 1 = tri-state outputs, 0 = enable outputs
58	DIF_15	OUT	0.7V differential true clock output
59	DIF_15#	OUT	0.7V differential complement clock output
60	OE16#	IN	Active low input for enabling DIF pair 16. 1 = tri-state outputs, 0 = enable outputs
61	DIF_16	OUT	0.7V differential true clock output
62	DIF_16#	OUT	0.7V differential complement clock output
63	VDD	PWR	Power supply, nominal 3.3V
64	GND	PWR	Ground pin.
65	DIF_17	OUT	0.7V differential true clock output
66	DIF_17#	OUT	0.7V differential complement clock output
67	DIF_18	OUT	0.7V differential true clock output
68	DIF_18#	OUT	0.7V differential complement clock output
69	OE17_18#	IN	Active low input for enabling DIF pairs 17 and 18. 1 = tri-state outputs, 0 = enable outputs
70	CLK_IN	IN	True Input for differential reference clock.
71	CLK_IN#	IN	Complement Input for differential reference clock.
72	SMB_A2_PLLBYP#	IN	SMBus address bit 2. When Low, the part operates as a fanout buffer with the PLL bypassed. When High, the part operates as a zero-delay buffer (ZDB) with the PLL operating. 0 = fanout mode (PLL bypassed), 1 = ZDB mode (PLL used)

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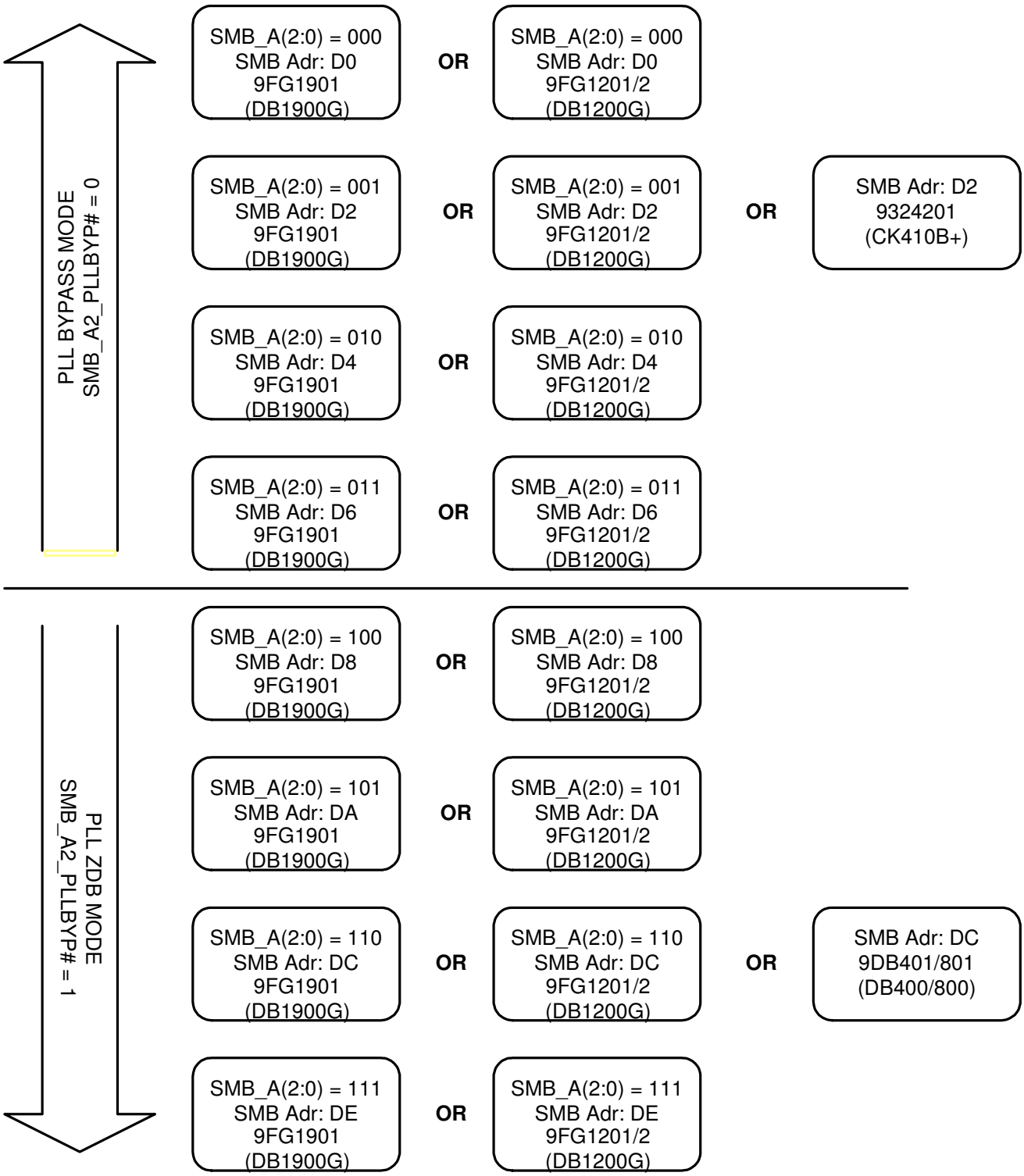
9FG1901 Programmable Gear Ratios

FS_A_410	SMBus Byte 0				Input (m)	Output (n)	Gear Ratio (n/m)	Input (CPU FSB) and Output Frequencies (MHz)				
	Bit 3	Bit 2	Bit 1	Bit 0				200.0	266.7	320.0	333.3	400.0
0	0	0	0	0	3	1	0.333	66.7	88.9	106.7	111.1	133.3
0	0	0	0	1	5	2	0.400	80.0	106.7	128.0	133.3	160.0
0	0	0	1	0	12	5	0.417	83.3	111.1	133.3	138.9	166.7
0	0	0	1	1	2	1	0.500	100.0	133.3	160.0	166.7	200.0
0	0	1	0	0	5	3	0.600	120.0	160.0	192.0	200.0	240.0
0	0	1	0	1	8	5	0.625	125.0	166.7	200.0	208.3	250.0
0	0	1	1	0	3	2	0.667	133.3	177.8	213.3	222.2	266.7
0	0	1	1	1	4	3	0.750	150.0	200.0	240.0	250.0	300.0
0	1	0	0	0	6	5	0.833	166.7	222.2	266.7	277.8	333.3
0	**1**	**0**	**0**	**1**	**1**	**1**	**1.000**	**200.0**	**266.7**	**320.0**	**333.3**	**400.0**
0	1	0	1	0	5	6	1.200	240.0	320.0	384.0	400.0	NA
0	1	0	1	1	4	5	1.250	250.0	333.3	400.0	NA	NA
0	1	1	0	0	3	4	1.333	266.7	355.6	NA	NA	NA
0	1	1	0	1	2	3	1.500	300.0	400.0	NA	NA	NA
0	1	1	1	0	3	5	1.667	333.3	NA	NA	NA	NA
0	1	1	1	1	1	2	2.000	400.0	NA	NA	NA	NA
								CLK IN (CPU FSB) Frequency (MHz)				
								100	**133.33**	**160**	**166.67**	
1	0	0	0	0	3	1	0.333					
1	0	0	0	1	5	2	0.400	NA	53.3	64.0	66.7	
1	0	0	1	0	12	5	0.417	NA	55.6	66.7	69.4	
1	0	0	1	1	2	1	0.500	50.0	66.7	80.0	83.3	
1	0	1	0	0	5	3	0.600	60.0	80.0	96.0	100.0	
1	0	1	0	1	8	5	0.625	62.5	83.3	100.0	104.2	
1	0	1	1	0	3	2	0.667	66.7	88.9	106.7	111.1	
1	0	1	1	1	5	4	0.800	80.0	106.7	128.0	133.3	
1	1	0	0	0	6	5	0.833	NA	111.1	133.3	138.9	
1	**1**	**0**	**0**	**1**	**1**	**1**	**1.000**	**100.0**	**133.3**	**160.0**	**166.7**	
1	1	0	1	0	5	6	1.200	120.0	160.0	192.0	200.0	
1	1	0	1	1	4	5	1.250	125.0	166.7	200.0	208.3	
1	1	1	0	0	3	4	1.333	133.3	177.8	213.3	222.2	
1	1	1	0	1	2	3	1.500	150.0	200.0			
1	1	1	1	0	3	5	1.667	166.7	222.2	266.7	277.8	
1	1	1	1	1	1	2	2.000	200.0	266.7	320.0	333.3	

Note: Lines in **BOLD** are Power-up defaults for FS_A_410 = 0 and 1 respectively.
Shaded areas are shown for reference only and device operation is not guaranteed

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9FG1901 SMBus Address Mapping
when using CK410B+, 9FG1201, and 9DB401/801



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General SMBus serial interface information for the 9FG1901H

How to Write:

- Controller (host) sends a start bit.
- Controller (host) sends the write address D0 (h)
- ICS clock will ***acknowledge***
- Controller (host) sends the begining byte location = N
- ICS clock will ***acknowledge***
- Controller (host) sends the data byte count = X
- ICS clock will ***acknowledge***
- Controller (host) starts sending ***Byte N through Byte N + X -1***
- ICS clock will ***acknowledge*** each byte ***one at a time***
- Controller (host) sends a Stop bit

How to Read:

- Controller (host) will send start bit.
- Controller (host) sends the write address D0 (h)
- ICS clock will ***acknowledge***
- Controller (host) sends the begining byte location = N
- ICS clock will ***acknowledge***
- Controller (host) will send a separate start bit.
- Controller (host) sends the read address D1 (h)
- ICS clock will ***acknowledge***
- ICS clock will send the data byte count = X
- ICS clock sends ***Byte N + X -1***
- ICS clock sends ***Byte 0 through byte X (if X(h) was written to byte 8)***.
- Controller (host) will need to acknowledge each byte
- Controllor (host) will send a not acknowledge bit
- Controller (host) will send a stop bit

Index Block Write Operation

Controller (Host)			ICS (Slave/Receiver)
T	starT bit		
Slave Address D0(h)*			
WR	WRite		
			ACK
Beginning Byte = N			
			ACK
Data Byte Count = X			
			ACK
Beginning Byte N		X Byte	
			ACK
◇			
◇			◇
◇			◇
			◇
Byte N + X - 1			
			ACK
P	stoP bit		

Index Block Read Operation

Controller (Host)		ICS (Slave/Receiver)	
T	starT bit		
Slave Address D0(h)*			
WR	WRite		
		ACK	
Beginning Byte = N			
		ACK	
RT	Repeat starT		
Slave Address D1(h)*			
RD	ReaD		
		ACK	
		Data Byte Count = X	
ACK			
		X Byte	Beginning Byte N
ACK			
			◇
◇			◇
◇			◇
◇			
			Byte N + X - 1
N	Not acknowledge		
P	stoP bit		

* Note: See SMBus Address Mapping (page 6), for programming SMBus Read/Write Address

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SMBusTable: FSB Frequency Select Register

Byte 0	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	DIF(16:0)	GRSEL_17	Group of 17 gear ratio select	RW	Gear Ratio	1:1	**1**
Bit 6	DIF(18:17)	GRSEL_2	Group of 2 gear ratio select	RW	Gear Ratio	1:1	**1**
Bit 5		Reserved					X
Bit 4	-	FS_A_410 Latched Input		RW	See ICS9FG1901 Programmable Gear Ratios Table		Latch
Bit 3	-	FSBG_3	FSB Gear Ratio FS_3	RW			x
Bit 2	-	FSBG_2	FSB Gear Ratio FS_2	RW			0
Bit 1	-	FSBG_1	FSB Gear Ratio FS_1	RW			x
Bit 0	-	FSBG_0	FSB Gear Ratio FS_0	RW			1

SMBusTable: Output Control Register

Byte 1	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7		DIF_7	Output Control	RW	Hi-Z	Enable	1
Bit 6		DIF_6	Output Control	RW	Hi-Z	Enable	1
Bit 5		DIF_5	Output Control	RW	Hi-Z	Enable	1
Bit 4		DIF_4	Output Control	RW	Hi-Z	Enable	1
Bit 3		DIF_3	Output Control	RW	Hi-Z	Enable	1
Bit 2		DIF_2	Output Control	RW	Hi-Z	Enable	1
Bit 1		DIF_1	Output Control	RW	Hi-Z	Enable	1
Bit 0		DIF_0	Output Control	RW	Hi-Z	Enable	1

SMBusTable: Output and PLL BW Control Register

Byte 2	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	see note	PLL_BW# adjust		RW	High BW	Low BW	**1**
Bit 6	see note	BYPASS# test mode / PLL		RW	Bypass	PLL	**1**
Bit 5		DIF_13	Output Control	RW	Hi-Z	Enable	1
Bit 4		DIF_12	Output Control	RW	Hi-Z	Enable	1
Bit 3		DIF_11	Output Control	RW	Hi-Z	Enable	1
Bit 2		DIF_10	Output Control	RW	Hi-Z	Enable	1
Bit 1		DIF_9	Output Control	RW	Hi-Z	Enable	1
Bit 0		DIF_8	Output Control	RW	Hi-Z	Enable	1

Note: Bit 7 is wired OR to the HIGH_BW# input, any 0 selects High BW

Note: Bit 6 is wired OR to the SMB_A2_PLLBYP# input, any 0 selects Fanout Bypass mode

SMBusTable: Output Enable Readback Register

Byte 3	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7		Readback - OE9# Input		R	Readback		X
Bit 6		Readback - OE8# Input		R	Readback		X
Bit 5		Readback - OE7# Input		R	Readback		X
Bit 4		Readback - OE6# Input		R	Readback		X
Bit 3		Readback - OE5# Input		R	Readback		X
Bit 2		Readback - OE_01234# Input		R	Readback		X
Bit 1	8	Readback - HIGH_BW# In		R	Readback		X
Bit 0	72	Readback - SMB_A2_PLLBYP# In		R	Readback		X

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SMBusTable: Output Enable Readback Register

Byte 4	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	69	Readback - OE17_18# Input		R	Readback		X
Bit 6	60	Readback - OE16# Input		R	Readback		X
Bit 5	57	Readback - OE15# Input		R	Readback		X
Bit 4	54	Readback - OE14# Input		R	Readback		X
Bit 3	51	Readback - OE13# Input		R	Readback		X
Bit 2	48	Readback - OE12# Input		R	Readback		X
Bit 1	43	Readback - OE11# Input		R	Readback		X
Bit 0	40	Readback - OE10# Input		R	Readback		X

SMBusTable: Vendor & Revision ID Register

Byte 5	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	-	RID3	REVISION ID	R	-	-	X
Bit 6	-	RID2		R	-	-	X
Bit 5	-	RID1		R	-	-	X
Bit 4	-	RID0		R	-	-	X
Bit 3	-	VID3	VENDOR ID	R	-	-	0
Bit 2	-	VID2		R	-	-	0
Bit 1	-	VID1		R	-	-	0
Bit 0	-	VID0		R	-	-	1

SMBusTable: DEVICE ID

Byte 6	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	-	Device ID 7 (MSB)		RW	Reserved		1
Bit 6	-	Device ID 6		RW	Reserved		0
Bit 5	-	Device ID 5		RW	Reserved		0
Bit 4	-	Device ID 4		RW	Reserved		1
Bit 3	-	Device ID 3		RW	Reserved		0
Bit 2	-	Device ID 2		RW	Reserved		0
Bit 1	-	Device ID 1		RW	Reserved		0
Bit 0	-	Device ID 0		RW	Reserved		1

SMBusTable: Byte Count Register

Byte 7	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	-	BC7	Writing to this register configures how many bytes will be read back.	RW	-	-	0
Bit 6	-	BC6		RW	-	-	0
Bit 5	-	BC5		RW	-	-	0
Bit 4	-	BC4		RW	-	-	0
Bit 3	-	BC3		RW	-	-	0
Bit 2	-	BC2		RW	-	-	1
Bit 1	-	BC1		RW	-	-	1
Bit 0	-	BC0		RW	-	-	1

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SMBusTable: Control Pin Readback Register

Byte 8	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	5	Readback - FS_A_410		R	Readback		X
Bit 6		RESERVED					X
Bit 5		RESERVED					X
Bit 4		DIF_18	Output Control	RW	Hi-Z	Enable	1
Bit 3		DIF_17	Output Control	RW	Hi-Z	Enable	1
Bit 2		DIF_16	Output Control	RW	Hi-Z	Enable	1
Bit 1		DIF_15	Output Control	RW	Hi-Z	Enable	1
Bit 0		DIF_14	Output Control	RW	Hi-Z	Enable	1

SMBusTable: 1:1 PLL Operating Set Point Register

Byte 9	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7		RESERVED					0
Bit 6		RESERVED					0
Bit 5		RESERVED					0
Bit 4		RESERVED					0
Bit 3		RESERVED					0
Bit 2	-	Frequency Select C		RW	See ICS9FG1901H 1:1 PLL Programming Table		x
Bit 1	-	Frequency Select B		RW			1
Bit 0	-	FS_A_410		RW			Latch

9FG1901H 1:1 PLL Programming

Byte 9, bit 2 FSC	Byte 9, bit 1 FSB	Byte 9, bit 0 FS_A_410	CLK_IN (CPU FSB) MHz	1:1 DIF Outputs MHz	Notes
1	0	1	100.00	100.00	3
0	0	1	133.33	133.33	3
0	**1**	**1**	**166.67**	**166.67**	1
0	1	0	200.00	200.00	3
0	0	0	266.67	266.67	3
1	0	0	333.33	333.33	3
1		**0**	**400.00**	**400.00**	2
1	1	1	Reserved		

Notes:FS_A_410 = 1

1. Powerup Default for FS_A_410 = 1
2. Powerup Default for FS_A_410 = 0
3. Setting the exact FSB frequency after Power is required to meet phase jitter specs.

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Absolute Maximum Ratings

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	Notes
3.3V Core Supply Voltage	VDD_A		GND - 0.5		V_{DD} + 0.5V	V	1
3.3V Logic Supply Voltage	VDD_In		GND - 0.5		V_{DD} + 0.5V	V	1
Storage Temperature	Ts		-65		150	°C	1
Ambient Operating Temp	Tambient		0		70	°C	1
Case Temperature	Tcase				115	°C	1
Input ESD protection	ESD prot	Human Body Model	2000			V	1

Electrical Characteristics - Input/Supply/Common Output Parameters

T_A = 0 - 70°C; Supply Voltage V_{DD} = 3.3 V +/-5%

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	Notes
Input High Voltage	V_{IH}	3.3 V +/-5%, Except CLK_IN	2		V_{DD} + 0.3	V	1
Input Low Voltage	V_{IL}	3.3 V +/-5%, Except CLK_IN	V_{SS} - 0.3		0.8	V	1
Input High Current	I_{IH}	V_{IN} = V_{DD}	-5		5	uA	
Input Low Current	I_{IL1}	V_{IN} = 0 V; Inputs with no pull-up resistors	-5			uA	
Low Threshold Input-High Voltage	V_{IH_FS}	3.3 V +/-5%, Applies to FS_A_410 pin	0.7		V_{DD} + 0.3	V	1
Low Threshold Input-Low Voltage	V_{IL_FS}	3.3 V +/-5%, Applies to FS_A_410 pin	V_{SS} - 0.3		0.35	V	1
Operating Current	$I_{DD3.3OP}$	all outputs driven			600	mA	1
Powerdown Current	$I_{DD3.3PD}$	all differential pairs tri-stated			36	mA	1
Input Frequency	F_i	V_{DD} = 3.3 V	100		400	MHz	3
Pin Inductance	L_{pin}				7	nH	1
Input Capacitance	C_{IN}	Logic Inputs			6	pF	1
	C_{OUT}	Output pin capacitance			5	pF	1
Clk Stabilization	T_{STAB}	From V_{DD} Power-Up or de-assertion of PD# to 1st clock			1.8	ms	1
Modulation Frequency		Triangular Modulation	30		33	kHz	1
Tdrive_PD#		DIF output enable after PD# de-assertion			300	us	1
Tfall_Pd#		PD# fall time of			5	ns	1
Trise_Pd#		PD# rise time of			5	ns	2
SMBus Voltage	V_{MAX}	Maximum input voltage			5.5	V	1
Low-level Output Voltage	V_{OL}	@ I_{PULLUP}			0.4	V	1
Current sinking at V_{OL} = 0.4 V	I_{PULLUP}		4			mA	1
SCLK/SDATA Clock/Data Rise Time	T_{RI2C}	(Max VIL - 0.15) to (Min VIH + 0.15)			1000	ns	1
SCLK/SDATA Clock/Data Fall Time	T_{FI2C}	(Min VIH + 0.15) to (Max VIL - 0.15)			300	ns	1

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Electrical Characteristics - DIF 0.7V Current Mode Differential Pair

T_A = 0 - 70°C; V_{DD} = 3.3 V +/-5%; C_L =2pF, R_S=33.2Ω, R_P=49.9Ω, I_{REF} = 475Ω

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	NOTES
Current Source Output Impedance	Zo^1	$V_O = V_x$	3000			Ω	1
Voltage High	VHigh	Statistical measurement on single ended signal using oscilloscope math function.	660		850	mV	1,3
Voltage Low	VLow		-150		150		1,3
Max Voltage	Vovs	Measurement on single ended signal using absolute value.			1150	mV	1
Min Voltage	Vuds		-300				1
Crossing Voltage (abs)	Vcross(abs)		250		550	mV	1
Crossing Voltage (var)	d-Vcross	Variation of crossing over all edges			140	mV	1
Long Accuracy	ppm	see Tperiod min-max values	-300		300	ppm	1,2
Average period	Tperiod	400MHz nominal	2.4993		2.5008	ns	2
		400MHz spread	2.4993		2.5133	ns	2
		333.33MHz nominal	2.9991		3.0009	ns	2
		333.33MHz spread	2.9991		3.016	ns	2
		266.66MHz nominal	3.7489		3.7511	ns	2
		266.66MHz spread	3.7489		3.77	ns	2
		200MHz nominal	4.9985		5.0015	ns	2
		200MHz spread	4.9985		5.0266	ns	2
		166.66MHz nominal	5.9982		6.0018	ns	2
		166.66MHz spread	5.9982		6.0320	ns	2
		133.33MHz nominal	7.4978		7.5023	ns	2
		133.33MHz spread	7.4978		7.5400	ns	2
		100.00MHz nominal	9.9970		10.0030	ns	2
		100.00MHz spread	9.9970		10.0533	ns	2
Absolute min period	T_{absmin}	400MHz nominal/spread	2.4143			ns	1,2
		333.33MHz nominal/spread	2.9141			ns	1,2
		266.66MHz nominal/spread	3.6639			ns	1,2
		200MHz nominal/spread	4.8735			ns	1,2
		166.66MHz nominal/spread	5.8732			ns	1,2
		133.33MHz nominal/spread	7.3728			ns	1,2
		100.00MHz nominal/spread	9.8720			ns	1,2
Rise Time	t_r	V_{OL} = 0.175V, V_{OH} = 0.525V	175		700	ps	1
Fall Time	t_f	V_{OH} = 0.525V V_{OL} = 0.175V	175		700	ps	1
Rise Time Variation	d-t_r				125	ps	1
Fall Time Variation	d-t_f				125	ps	1
Duty Cycle	d_{t3}	Measurement from differential wavefrom	45		55	%	1
Jitter, Cycle to cycle	$t_{JCYC-CYC}$	PLL mode, from differential wavefrom			50	ps	1,4,5
	t_{JBYP}	Bypass mode as additive jitter			50	ps	1,4

Notes:

1.Guaranteed by design and characterization, not 100% tested in production.

2. All Long Term Accuracy and Clock Period specifications are guaranteed assuming that the input frequency meets CK410B accuracy requirements

3.IREF = VDD/(3xRR). For RR = 475Ω (1%), IREF = 2.32mA. IOH = 6 x IREF and VOH = 0.7V @ ZO=50Ω.

4. Measured into fixed 2 pF load cap. Input to output skew is measured at the first output edge following the corresponding input.

5. Measured from differential cross-point to differential cross-point

6. All Bypass Mode Input-to-Output specs refer to the timing between an input edge and the specific output edge created by it.

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Electrical Characteristics - Skew and Differential Jitter Parameters

T_A = 0 - 70°C; Supply Voltage V_{DD} = 3.3 V +/-5%

Group	Parameter	Description	Min	Typ	Max	Units	Notes
CLK_IN, DIF[x:0]	t_{SPO_PLL}	Input-to-Output Skew in PLL mode (1:1 only), nominal value @ 25°C, 3.3V	-500	270	500	ps	1,2,4,5,8, 12
CLK_IN, DIF[x:0]	t_{PD_BYP}	Input-to-Output Skew in Bypass mode (1:1 only), nominal value @ 25°C, 3.3V	2.5	3.8	4.5	ns	1,2,3,5, 12
CLK_IN, DIF [x:0]	Δt_{SPO_PLL}	Input-to-Output Skew Variation in PLL mode (over specified voltage / temperature operating ranges)		270	|500|	ps	1,2,4,5,6, 10,12
CLK_IN, DIF [x:0]	Δt_{PD_BYP}	Input-to-Output Skew Variation in Bypass mode (over specified voltage / temperature operating ranges)		467	|500|	ps	1,2,3,4,5, 6,10,12
DIF[18:17]	t_{SKEW_G2}	Output-to-Output Skew Group of 2 (Common to Bypass and PLL mode)		10	50	ps	1,2,12
DIF[16:0]	t_{SKEW_G17}	Output-to-Output Skew Group of 17 (Common to Bypass and PLL mode)		70	100	ps	1,2,12
DIF[18:0]	t_{SKEW_A19}	Output-to-Output Skew across all 19 outputs (Common to Bypass and PLL mode - all outputs at same gear)		70	150	ps	1,2,3,12
DIF[18:0]	t_{JPH}	Differential Phase Jitter (RMS Value)		5	10	ps	1,4,7,12
DIF[18:0]	$t_{SSTERROR}$	Differential Spread Spectrum Tracking Error (peak to peak)		40	80	ps	1,4,9,12
PLL Jitter Peaking	$j_{peak\text{-}hibw}$	(HIGH_BW# = 0)	0	2.2	2.5	dB	11,12
PLL Jitter Peaking	$j_{peak\text{-}lobw}$	(HIGH_BW# = 1)	0	1.4	2	dB	11,12
PLL Bandwidth	pll_{HIBW}	(HIGH_BW# = 0)	2	3.7	4	MHz	12,13
PLL Bandwidth	pll_{LOBW}	(HIGH_BW# = 1)	0.7	1.2	1.4	MHz	12,13

NOTES on Skew and Differential Jitter Parameters:

1. Measured into fixed 2 pF load cap. Input to output skew is measured at the first output edge following the corresponding input.
2. Measured from differential cross-point to differential cross-point
3. All Bypass Mode Input-to-Output specs refer to the timing between an input edge and the specific output edge created by it.
4. This parameter is deterministic for a given device
5. Measured with scope averaging on to find mean value.
6. Long-term variation from nominal of input-to-output skew over temperature and voltage for a single device.
7. This parameter is measured at the outputs of two separate 9FG1901H devices driven by a single CK410B+. The 9FG1901H must be set to high bandwidth. Differential phase jitter is the accumulation of the phase jitter not shared by the outputs (eg. not including the affects of spread spectrum). Target ranges of consideration are agents with BW of 1-22MHz and 11-33MHz.
8. t is the period of the input clock
9. Differential spread spectrum tracking error is the difference in spread spectrum tracking between two 9FG1901H devices This parameter is measured at the outputs of two separate 9FG1901H devices driven by a single CK410B+ in Spread Spectrum mode. The 9FG1901H must set to high bandwidth. The spread spectrum characterisitics are : maximum of 0.5%, 30 to 33KHz modulation frequency, linear profile.
10. This parameter is an absolute value. It is not a double-sided figure.
11. Measured as maximum pass band gain. At frequencies within the loop BW, highest point of magnification is called PLL jitter peaking.
12. Guaranteed by design and characterization, not 100% tested in production.
13. Measured at 3 db down or half power point.

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Electrical Characteristics - Phase Jitter

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP.	MAX	UNITS	NOTES
Jitter, Phase	$t_{jphPCIe1}$	PCIe Gen 1 REFCLK phase jitter (including PLL BW 8 - 16 MHz, ζ = 0.54, Td=10 ns, Ftrk=1.5 MHz)		42/41	86	ps	1,2,3,5
	$t_{jphFBD1_3.2G}$	FBD REFCLK phase jitter (including PLL BW 11 - 33 MHz, ζ = 0.54, Td=12 ns Ftrl=0.2MHz)		2.8/2.7	3	ps (RMS)	1,2
	$t_{jphFBD1_4.8G}$	FBD REFCLK phase jitter (including PLL BW 11 - 33 MHz, ζ = 0.54, Td=12 ns Ftrl=0.2MHz)		2.4/2.1	2.5	ps (RMS)	1,2

Notes on Phase Jitter:

[1] See http://www.pcisig.com for complete specs. Guaranteed by design and characterization, not tested in production.

[2] Device driven by 932S421BGLF or equivalent

[3] Sample size of at least 100K cycles. This figures extrapolates to 108ps pk-pk @ 1M cycles for a BER of 1^{-12}

[4] Hi-Bandwidth Number/Low Bandwidth Number with Spread On. Spread Off gives lower numbers.

[5] Byte 9 must be properly set to meet these parameters.

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SRC Reference Clock			
Common Recommendations for Differential Routing	Dimension or Value	Unit	Figure
L1 length, route as non-coupled 50ohm trace	0.5 max	inch	1
L2 length, route as non-coupled 50ohm trace	0.2 max	inch	1
L3 length, route as non-coupled 50ohm trace	0.2 max	inch	1
Rs	33	ohm	1
Rt	49.9	ohm	1

Down Device Differential Routing			
L4 length, route as coupled microstrip 100ohm differential trace	2 min to 16 max	inch	1
L4 length, route as coupled stripline 100ohm differential trace	1.8 min to 14.4 max	inch	1

Differential Routing to PCI Express Connector			
L4 length, route as coupled microstrip 100ohm differential trace	0.25 to 14 max	inch	2
L4 length, route as coupled stripline 100ohm differential trace	0.225 min to 12.6 max	inch	2

Figure 1: Down Device Routing

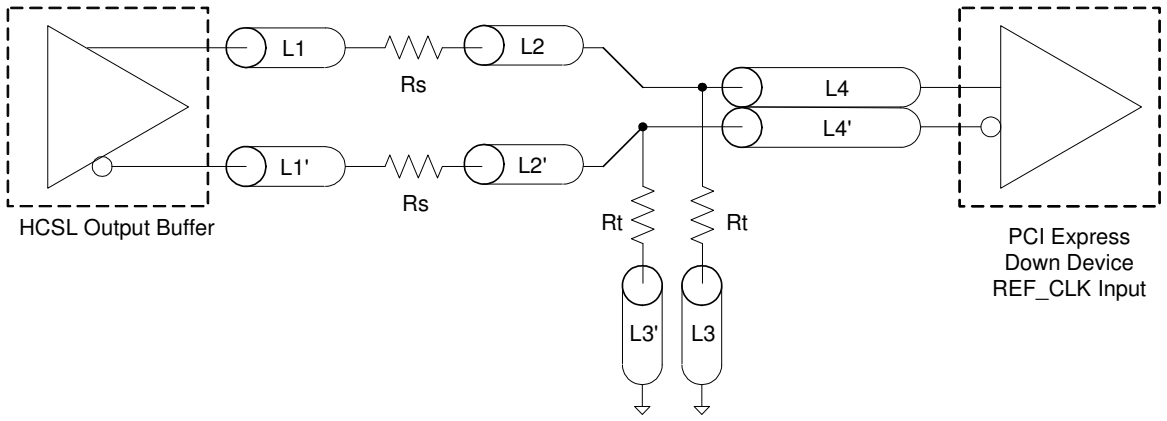
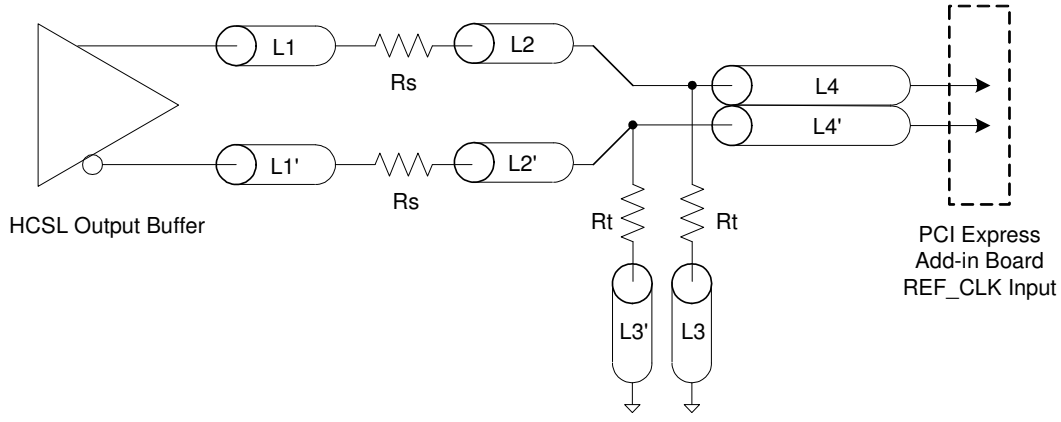


Figure 2: PCI Express Connector Routing

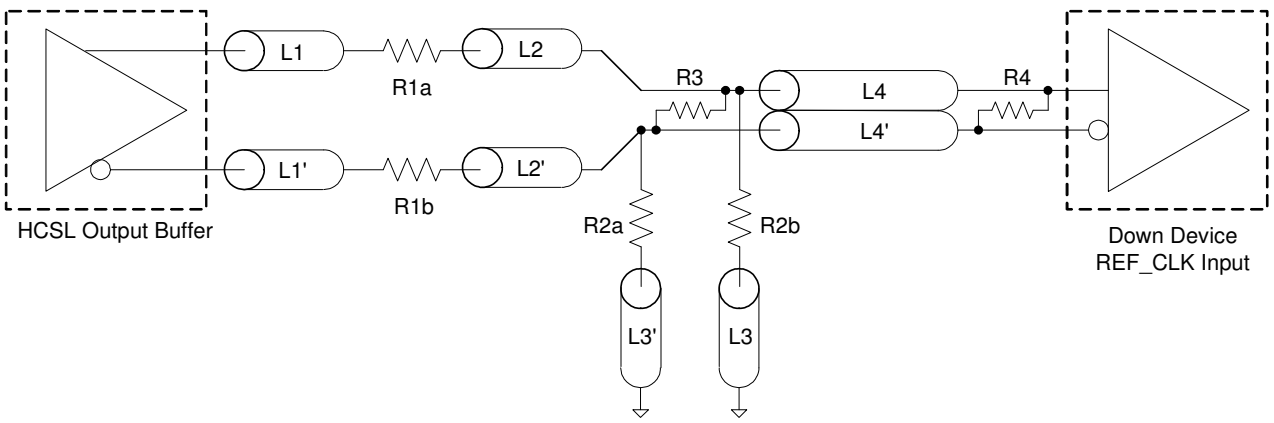


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Alternative Termination for LVDS and other Common Differential Signals (figure 3)							
Vdiff	Vp-p	Vcm	R1	R2	R3	R4	Note
0.45v	0.22v	1.08	33	150	100	100	
0.58	0.28	0.6	33	78.7	137	100	
0.80	0.40	0.6	33	78.7	none	100	ICS874003i-02 input compatible
0.60	0.3	1.2	33	174	140	100	Standard LVDS

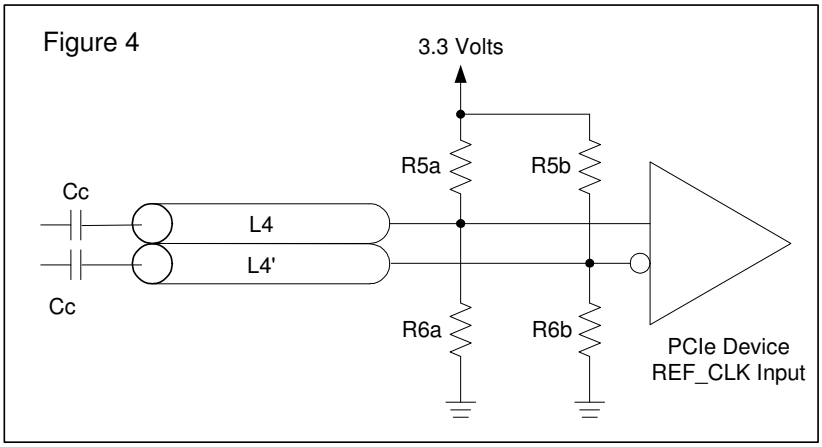
R1a = R1b = R1
R2a = R2b = R2

Figure 3

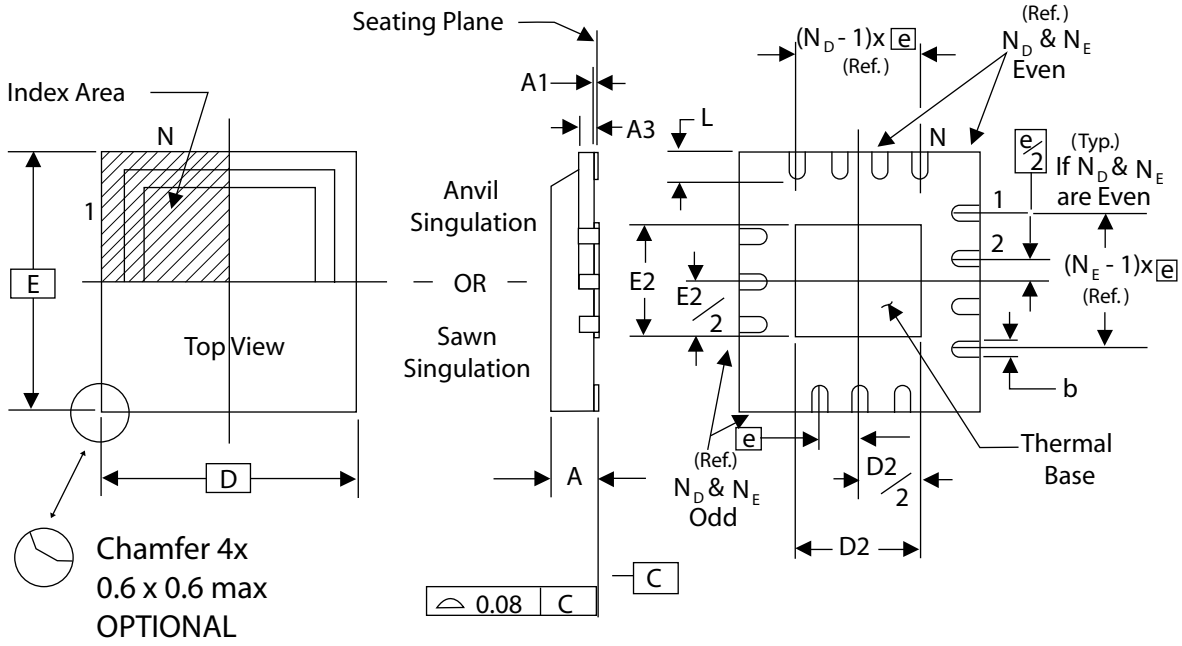


Cable Connected AC Coupled Application (figure 4)		
Component	Value	Note
R5a, R5b	8.2K 5%	
R6a, R6b	1K 5%	
Cc	0.1 µF	
Vcm	0.350 volts	

Figure 4



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THERMALLY ENHANCED, VERY THIN, FINE PITCH
QUAD FLAT / NO LEAD PLASTIC PACKAGE

DIMENSIONS

SYMBOL	72L
N	72
N_D	18
N_E	18

DIMENSIONS (mm)

SYMBOL	MIN.	MAX.
A	0.8	1.0
A1	0	0.05
A3	0.25 Reference	
b	0.18	0.3
e	0.50 BASIC	
D x E BASIC	10.00 x 10.00	
D2 MIN. / MAX.	5.75	6.15
E2 MIN. / MAX.	5.75	6.15
L MIN. / MAX.	0.3	0.5

Ordering Information

Part / Order Number	Shipping Packaging	Package	Temperature
9FG1901HKLF	Tubes	72-pin MLF	0 to +70° C
9FG1901HKLFT	Tape and Reel	72-pin MLF	0 to +70° C

"LF" suffix to the part numbers are the Pb-Free configuration and are RoHS compliant.
"H" is the device revision designator (will not correlate to the datasheet revision).

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Revision History

Rev.	Issue Date	Description	Page #
0.1	9/8/2008	Initial Release	-
0.2	1/22/2009	1. Updated Skews, Phase Jitter, SMBus Address Graphic 2. Removed output divider table. 3. Re-ordered SMBus and electrical tables for consistency.	Various
A	2/2/2010	Released to final.	

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