Eight Output Differential Frequency Generator for PCIe Gen3 and QPI

9FG830

General Description:

The 9FG830 is a Frequency Timing Generator that provides 8 HCSL differential output pairs. These outputs support PCI-Express Gen3, and QPI applications. The part supports Spread Spectrum and synthesizes several additional output frequencies from either a 14.31818 MHz crystal, a 25 MHz crystal or reference input clock. The 9FG830 also outputs a copy of the reference clock. Complete control of the device is available via strapping pins or via the SMBus interface.

Recommended Application:

8 Output Differential Output Frequency Generator for PCIe Gen3 and QPI

Output Features:

- 8 - 0.7V current mode differential HCSL output pairs
- 1 - 3.3V LVTTL REF output

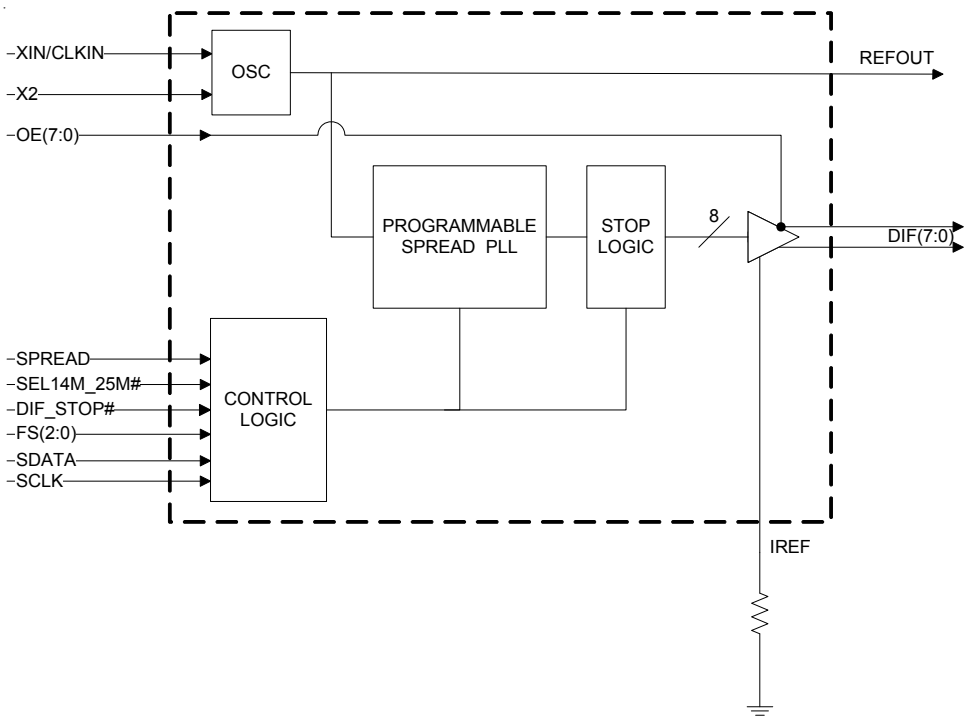
Features/Benefits:

- Pin-to-Pin with 9FG108D; Easy upgrade to PCIe Gen3
- Generates common frequencies from 14.318 MHz or 25 MHz; single part supports mulitple applications
- Provides copy of reference output; eleminates need for additional crystal or oscillator
- Three spread spectrum modes: -0.5%, +/-0.25%, and off; EMI reduction
- Unused outputs may be disabled in Hi-Z; save system power
- Device may be configured by SMBus and/or strap pins; can be used in systems without SMBus

Key Specifications:

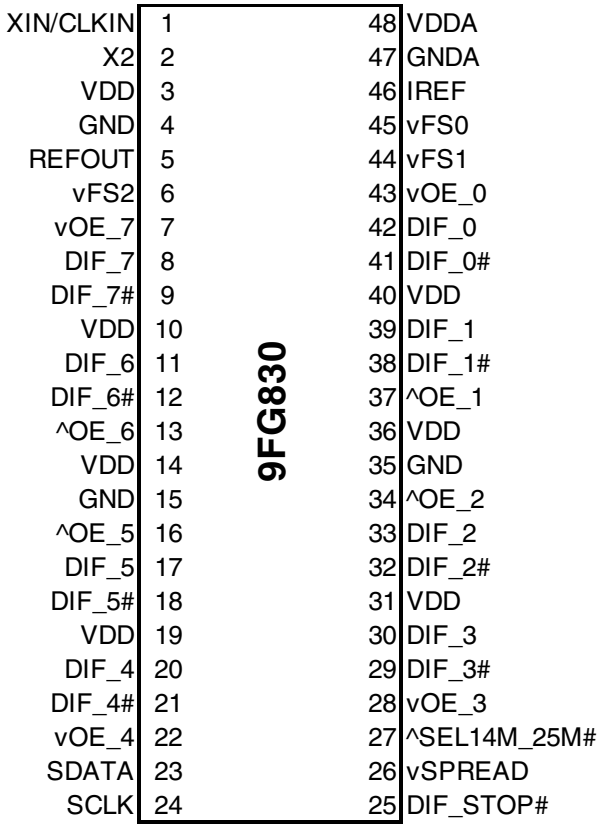
- Cycle-to-cycle jitter: < 50ps with 25MHz input
- Output-to-output skew: <50ps
- Phase jitter: PCIe Gen3 < 1ps rms
- Phase jitter: QPI 9.6GB/s < 0.2ps rms
- 10 ppm synthesis error with 25MHz input and Spread Off

Functional Block Diagram



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Pin Configuration



^ indicates internal 120K pull up
v indicates internal 120K pull down

Power Groups

Pin Number		Description
VDD	GND	
3	4	REFOUT, Digital Inputs, SMBus
10,14,19,31,36,40	15,35	DIF Outputs
N/A	47	IREF
48	47	Analog VDD & GND for PLL Core

Frequency Select Table

SEL14M_25M# (FS3)	FS2	FS1	FS0	OUTPUT(MHz)
0	0	0	0	100.00
0	0	0	1	125.00
0	0	1	0	133.33
0	0	1	1	166.67
0	1	0	0	200.00
0	1	0	1	266.67
0	1	1	0	333.33
0	1	1	1	400.00
1	0	0	0	100.00
1	0	0	1	125.00
1	0	1	0	133.33
1	0	1	1	166.67
1	1	0	0	200.00
1	1	0	1	266.67
1	1	1	0	333.33
1	1	1	1	400.00

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Pin Description

PIN #	PIN NAME	PIN TYPE	DESCRIPTION
1	XIN/CLKIN	IN	Crystal input or Reference Clock input
2	X2	OUT	Crystal output, Nominally 14.318MHz
3	VDD	PWR	Power supply, nominal 3.3V
4	GND	PWR	Ground pin.
5	REFOUT	OUT	Reference Clock output
6	vFS2	IN	Frequency select pin. This pin has an internal 120k pull down resistor
7	vOE_7	IN	Active high input for enabling output 7. This pin has a 120kohm pull down. 0 =disable outputs, 1= enable outputs
8	DIF_7	OUT	0.7V differential true clock output
9	DIF_7#	OUT	0.7V differential Complementary clock output
10	VDD	PWR	Power supply, nominal 3.3V
11	DIF_6	OUT	0.7V differential true clock output
12	DIF_6#	OUT	0.7V differential Complementary clock output
13	^OE_6	IN	Active high input for enabling output 6. This pin has an internal 120kohm pull up. 0 = disable outputs, 1= enable outputs
14	VDD	PWR	Power supply, nominal 3.3V
15	GND	PWR	Ground pin.
16	^OE_5	IN	Active high input for enabling output 5. This pin has an internal 120kohm pull up. 0 = disable outputs, 1= enable outputs
17	DIF_5	OUT	0.7V differential true clock output
18	DIF_5#	OUT	0.7V differential Complementary clock output
19	VDD	PWR	Power supply, nominal 3.3V
20	DIF_4	OUT	0.7V differential true clock output
21	DIF_4#	OUT	0.7V differential Complementary clock output
22	vOE_4	IN	Active high input for enabling output 4. This pin as an internal 120kohm pull down. 0 =disable outputs, 1= enable outputs
23	SDATA	I/O	Data pin for SMBus circuitry, 5V tolerant.
24	SCLK	IN	Clock pin of SMBus circuitry, 5V tolerant.
25	DIF_STOP#	IN	Active low input to stop differential output clocks.
26	vSPREAD	IN	Asynchronous, active high input to enable spread spectrum functionality. This pin has a 120Kohm pull down resistor.
27	^SEL14M_25M#	IN	Select 14.31818 MHz or 25 Mhz input frequency. This pin has an internal 120kohm pull up resistor. 1 = 14.31818 MHz, 0 = 25 MHz
28	vOE_3	IN	Active high input for enabling output 3. This pin has an internal 120kohm pull down resistor. 0 =disable outputs, 1= enable outputs
29	DIF_3#	OUT	0.7V differential Complementary clock output
30	DIF_3	OUT	0.7V differential true clock output

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Pin Description (Continued)

31	VDD	PWR	Power supply, nominal 3.3V
32	DIF_2#	OUT	0.7V differential Complementary clock output
33	DIF_2	OUT	0.7V differential true clock output
34	^OE_2	IN	Active high input for enabling output 2. This pin has in internal 120kohm pull up resistor. 0 = disable outputs, 1= enable outputs
35	GND	PWR	Ground pin.
36	VDD	PWR	Power supply, nominal 3.3V
37	^OE_1	IN	Active high input for enabling output 1. This pin has an internal 120kohm pull up resistor. 0 = disable outputs, 1= enable outputs
38	DIF_1#	OUT	0.7V differential Complementary clock output
39	DIF_1	OUT	0.7V differential true clock output
40	VDD	PWR	Power supply, nominal 3.3V
41	DIF_0#	OUT	0.7V differential Complementary clock output
42	DIF_0	OUT	0.7V differential true clock output
43	vOE_0	IN	Active high input for enabling output 0. This pin has an internal 120kohm pull down resistor. 0 =disable outputs, 1= enable outputs
44	vFS1	IN	3.3V Frequency select latched input pin with internal 120kohm pull down resistor.
45	vFS0	IN	3.3V Frequency select latched input pin with internal 120kohm pull down resistor.
46	IREF	OUT	This pin establishes the reference current for the differential current-mode output pairs. This pin requires a fixed precision resistor tied to ground in order to establish the appropriate current. 475 ohms is the standard value.
47	GNDA	PWR	Ground pin for the PLL core.
48	VDDA	PWR	3.3V power for the PLL core.

Note:

^ indicates internal 120K pull up

v indicates internal 120K pull down

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Electrical Characteristics - Absolute Maximum Ratings

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	NOTES
3.3V Core Supply Voltage	VDDA				4.6	V	1,2
3.3V Logic Supply Voltage	VDD				4.6	V	1,2
Input Low Voltage	V_{IL}		GND-0.5			V	1
Input High Voltage	V_{IH}	Except for SMBus interface			V_{DD}+0.5V	V	1
Input High Voltage	V_{IHSMB}	SMBus clock and data pins			5.5V	V	1
Storage Temperature	Ts		-65		150	°C	1
Junction Temperature	Tj				125	°C	1
Input ESD protection	ESD prot	Human Body Model	2000			V	1

[1]Guaranteed by design and characterization, not 100% tested in production.

[2] Operation under these conditions is neither implied nor guaranteed.

Electrical Characteristics - Input/Supply/Common Parameters

TA = T_{COM} or $T_{IND;}$ Supply Voltage VDD = 3.3 V +/-5%

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	NOTES
Ambient Operating Temperature	T_{COM}	Commmercial range	0		70	°C	1
	T_{IND}	Industrial range	-40		85	°C	1
Input High Voltage	V_{IH}	Single-ended inputs, except SMBus, low threshold and tri-level inputs	2		V_{DD} + 0.3	V	1
Input Low Voltage	V_{IL}	Single-ended inputs, except SMBus, low threshold and tri-level inputs	GND - 0.3		0.8	V	1
Input Current	I_{IN}	Single-ended inputs, V_{IN} = GND, V_{IN} = VDD	-5		5	uA	1
	I_{INP}	Single-ended inputs V_{IN} = 0 V; Inputs with internal pull-up resistors V_{IN} = VDD; Inputs with internal pull-down resistors	-200		200	uA	1
Input Frequency	F_{in}	SEL14M_25M# = 0		25		MHz	1
		SEL14M_25M# = 1		14.31818		MHz	1
Pin Inductance	L_{pin}				7	nH	1
Capacitance	C_{IN}	Logic Inputs	1.5		5	pF	1
	C_{INXTAL}	Crystal inputs			6	pF	1
	C_{OUT}	Output pin capacitance			6	pF	1
Clk Stabilization	T_{STAB}	From V_{DD} Power-Up and after input clock stabilization or de-assertion of PD# to 1st clock			2.5	ms	1,2
SS Modulation Frequency	f_{MODIN}	Allowable Frequency (Triangular Modulation)	30		33	kHz	1
OE# Latency	$t_{LATOE\#}$	DIF start after OE# assertion DIF stop after OE# deassertion	1		3	cycles	1,3
Tdrive_STOP#	t_{DRVDS}	DIF output enable after DIF_STOP# de-assertion			300	us	1,3
Tfall	t_F	Fall time of control inputs			5	ns	1,2
Trise	t_R	Rise time of control inputs			5	ns	1,2
SMBus Input Low Voltage	V_{ILSMB}				0.8	V	1
SMBus Input High Voltage	V_{IHSMB}		2.1		V_{DDSMB}	V	1
SMBus Output Low Voltage	V_{OLSMB}	@ I_{PULLUP}			0.4	V	1
SMBus Sink Current	I_{PULLUP}	@ V_{OL}	4			mA	1
Nominal Bus Voltage	V_{DDSMB}	3V to 5V +/- 10%	2.7		5.5	V	1
SCLK/SDATA Rise Time	t_{RSMB}	(Max VIL - 0.15) to (Min VIH + 0.15)			1000	ns	1
SCLK/SDATA Fall Time	t_{FSMB}	(Min VIH + 0.15) to (Max VIL - 0.15)			300	ns	1
SMBus Operating Frequency	f_{MAXSMB}	Maximum SMBus operating frequency			100	kHz	1

[1]Guaranteed by design and characterization, not 100% tested in production.

[2]Control input must be monotonic from 20% to 80% of input swing.

[3]Time from deassertion until outputs are >200 mV

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Electrical Characteristics - DIF 0.7V Current Mode Differential Outputs

$T_A = T_{COM}$ or $T_{IND;}$ Supply Voltage VDD = 3.3 V +/-5%, See Test Loads for loading conditions

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	NOTES
Slew rate	Trf	Scope averaging on	1		4	V/ns	1, 2, 3
Slew rate matching	ΔTrf	Slew rate matching, Scope averaging on			20	%	1, 2, 4
Voltage High	VHigh	Statistical measurement on single-ended signal using oscilloscope math function. (Scope averaging on)	660		850	mV	1
Voltage Low	VLow		-150		150		1
Max Voltage	Vmax	Measurement on single ended signal using absolute value. (Scope averaging off)			1150	mV	1
Min Voltage	Vmin		-300				1
Vswing	Vswing	Scope averaging off	300			mV	1, 2
Crossing Voltage (abs)	Vcross_abs	Scope averaging off	250		550	mV	1, 5
Crossing Voltage (var)	Δ-Vcross	Scope averaging off			140	mV	1, 6

[1]Guaranteed by design and characterization, not 100% tested in production. IREF = VDD/(3xR_R). For R_R = 475Ω (1%), I_{REF} = 2.32mA. I_{OH} = 6 x I_{REF} and V_{OH} = 0.7V @ Z_O=50Ω (100Ω differential impedance).

[2] Measured from differential waveform

[3] Slew rate is measured through the Vswing voltage range centered around differential 0V. This results in a +/-150mV window around differential 0V.

[4] Matching applies to rising edge rate of Clock / falling edge rate of Clock#. It is measured in a +/-75mV window centered on the average cross point where Clock rising meets Clock# falling. The median cross point is used to calculate the voltage thresholds the oscilloscope uses for the edge rate calculations.

[5] Vcross is defined as voltage where Clock = Clock# measured on a component test board and only applies to the differential rising edge (i.e. Clock rising and Clock# falling).

[6] The total variation of all Vcross measurements in a particular system. This is a subset of V_cross_min/max (V_cross absolute) allowed. The intent is to limit Vcross induced modulation by setting V_cross_delta to be smaller than V_cross absolute.

Electrical Characteristics - Current Consumption

TA = T_{COM} or $T_{IND;}$ Supply Voltage VDD = 3.3 V +/-5%, See Test Loads for loading conditions

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	NOTES
Operating Supply Current	$I_{DD3.3}$	VDD, All outputs active @100MHz			250	mA	1
	$I_{DDA3.3OP}$	VDDA, All outputs active @100MHz			28	mA	1
	$I_{DD3.3}$	VDD, All outputs active @400MHz			200	mA	1
	$I_{DDA3.3OP}$	VDDA, All outputs active @400MHz			28	mA	1
DIF_STOP# Current	$I_{DD3.3DS}$	VDD, All DIF pairs stopped driven			190	mA	1
	$I_{DDA3.3DS}$	VDDA, All DIF pairs stopped driven			28	mA	1
	$I_{DD3.3DZ}$	VDD, All DIF pairs stopped Hi-Z			38	mA	1
	$I_{DDA3.3DZ}$	VDDA, All DIF pairs stopped Hi-Z			28	mA	1

[1]Guaranteed by design and characterization, not 100% tested in production.

[2] I_{REF} = V_{DD}/(3xR_R). For R_R = 475Ω (1%), I_{REF} = 2.32mA. I_{OH} = 6 x I_{REF} and V_{OH} = 0.7V @ Z_O=50Ω.

Electrical Characteristics - Output Duty Cycle, Jitter, and Skew Characterisitics

TA = T_{COM} or $T_{IND;}$ Supply Voltage VDD = 3.3 V +/-5%, See Test Loads for Loading Conditions

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	NOTES
Duty Cycle	t_{DC}	Measured differentially, PLL Mode	45		55	%	1
Skew, Output to Output	t_{sk3}	V_T = 50%			50	ps	1
Jitter, Cycle to cycle	$t_{jcyc-cyc}$	25M input			50	ps	1,3
Jitter, Cycle to cycle	$t_{jcyc-cyc}$	14.318M input			60	ps	1,3

[1]Guaranteed by design and characterization, not 100% tested in production.

[2] I_{REF} = V_{DD}/(3xR_R). For R_R = 475Ω (1%), I_{REF} = 2.32mA. I_{OH} = 6 x I_{REF} and V_{OH} = 0.7V @ Z_O=50Ω.

[3] Measured from differential waveform

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Electrical Characteristics - Phase Jitter Parameters

TA = T_{COM} or $T_{IND;}$ Supply Voltage VDD = 3.3 V +/-5%, See Test Loads for loading conditions

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	Notes
Phase Jitter, PCI Express	$t_{jphPCIeG1}$	PCIe Gen 1			86	ps (p-p)	1,2,3,6
	$t_{jphPCIeG2}$	PCIe Gen 2 Lo Band 10kHz < f < 1.5MHz			3	ps (rms)	1,2,6
		PCIe Gen 2 High Band 1.5MHz < f < Nyquist (50MHz)			3.1	ps (rms)	1,2,6
	$t_{jphPCIeG3}$	PCIe Gen 3 (PLL BW of 2-4MHz, CDR = 10MHz)			1	ps (rms)	1,2,4,5,6
Phase Jitter, QPI/SMI	t_{jphQPI_SMI}	QPI & SMI (100MHz or 133MHz, 4.8Gb/s, 6.4Gb/s 12UI)			0.5	ps (rms)	1,5,6
		QPI & SMI (100MHz, 8.0Gb/s, 12UI)			0.3	ps (rms)	1,5,6
		QPI & SMI (100MHz, 9.6Gb/s, 12UI)			0.2	ps (rms)	1,5,6

[1] Guaranteed by design and characterization, not 100% tested in production.

[2] See http://www.pcisig.com for complete specs

[3] Sample size of at least 100K cycles. This figures extrapolates to 108ps pk-pk @ 1M cycles for a BER of 1-12.

[4] Subject to final radification by PCI SIG.

[5] Calculated from Intel-supplied Clock Jitter Tool v 1.6.3

[6] Applies to all differential outputs

Electrical Characteristics - REF-14.318/25 MHz

TA = T_{COM} or T_{IND}; Supply Voltage VDD = 3.3 V +/-5%; See Test Loads for Loads for loading conditions.

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	Notes
Long Accuracy	ppm	see Tperiod min-max values		0		ppm	1,2
Clock period	T_{period}	14.318MHz output nominal		69.8413		ns	1,2
Clock period	T_{period}	25.000MHz output nominal		40		ns	1,2
Output High Voltage	V_{OH}	I_{OH} = -1 mA	2.4			V	1
Output Low Voltage	V_{OL}	I_{OL} = 1 mA			0.4	V	1
Output High Current	I_{OH}	V_{OH} @MIN = 1.0 V, V_{OH}@MAX = 3.135 V	-29		-23	mA	1
Output Low Current	I_{OL}	V_{OL} @MIN = 1.95 V, V_{OL} @MAX = 0.4 V	29		27	mA	1
Rise/Fall Time	t_{rf1}	V_{OL} = 0.4 V, V_{OH} = 2.4 V	0.5		2	ns	1
Duty Cycle	d_{t1}	V_T = 1.5 V	45		55	%	1
Jitter	$t_{jcyc-cyc}$	VT = 1.5 V		100	250	ps	1

[1]Guaranteed by design and characterization, not 100% tested in production.

[2] All Long Term Accuracy and Clock Period specifications are guaranteed assuming that REF is trimmed to 14.31818 or 25.00 MHz

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SRC Reference Clock			
Common Recommendations for Differential Routing	Dimension or Value	Unit	Notes
L1 length, route as non-coupled 50ohm trace	0.5 max	inch	1
L2 length, route as non-coupled 50ohm trace	0.2 max	inch	1
L3 length, route as non-coupled 50ohm trace	0.2 max	inch	1
Rs	33	ohm	1
Rt	49.9	ohm	1

Down Device Differential Routing			
L4 length, route as coupled microstrip 100ohm differential trace	2 min to 16 max	inch	1
L4 length, route as coupled stripline 100ohm differential trace	1.8 min to 14.4 max	inch	1

Differential Routing to PCI Express Connector			
L4 length, route as coupled microstrip 100ohm differential trace	0.25 to 14 max	inch	2
L4 length, route as coupled stripline 100ohm differential trace	0.225 min to 12.6 max	inch	2

Figure 1: Down Device Routing
(Test Load)

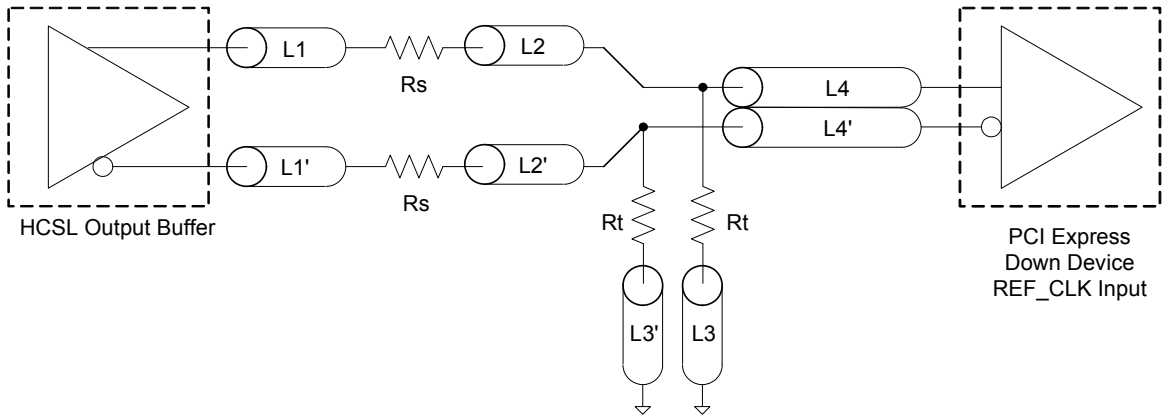
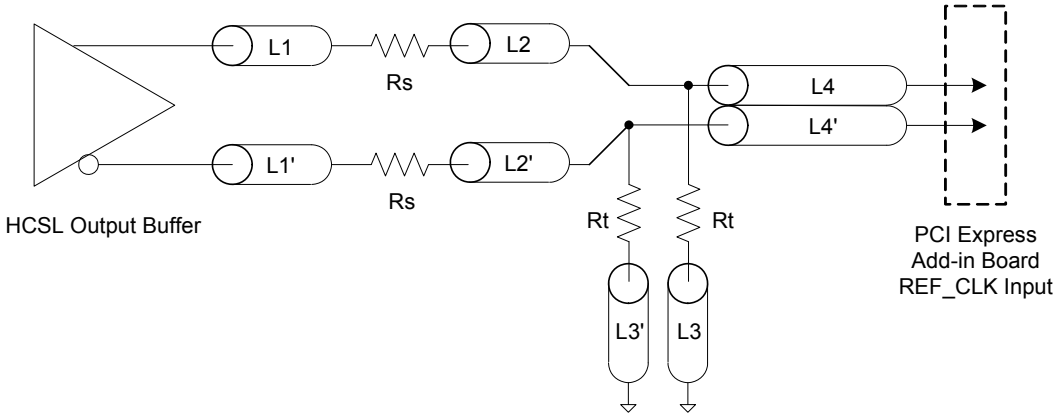


Figure 2: PCI Express Connector Routing



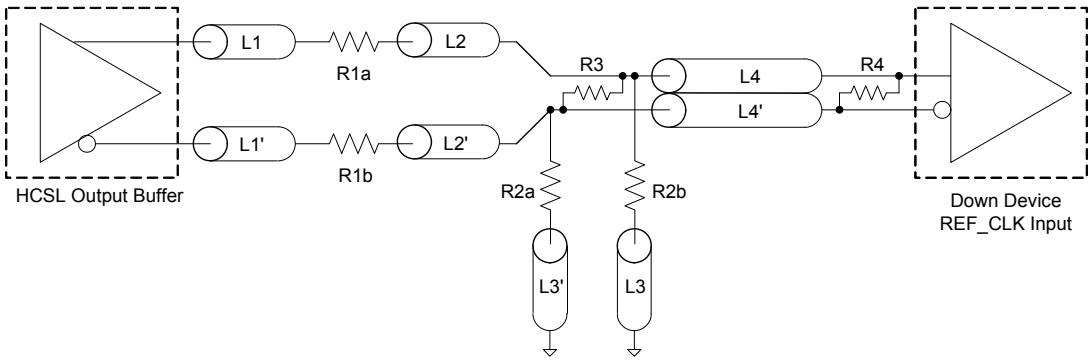
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Alternative Termination for LVDS and other Common Differential Signals (Figure 3)							
Vdiff	Vp-p	Vcm	R1	R2	R3	R4	Note
0.45v	0.22v	1.08	33	150	100	100	
0.58	0.28	0.6	33	78.7	137	100	
0.80	0.40	0.6	33	78.7	none	100	ICS874003i-02 input compatible
0.60	0.3	1.2	33	174	140	100	Standard LVDS

R1a = R1b = R1

R2a = R2b = R2

Figure 3



Cable Connected AC Coupled Application (figure 4)		
Component	Value	Note
R5a, R5b	8.2K 5%	
R6a, R6b	1K 5%	
Cc	0.1 µF	
Vcm	0.350 volts	

Figure 4

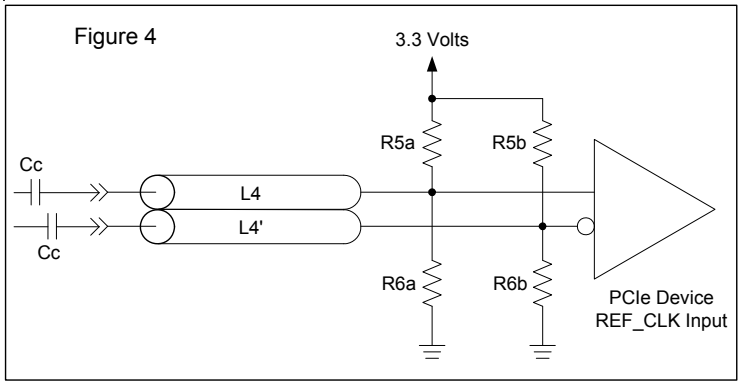
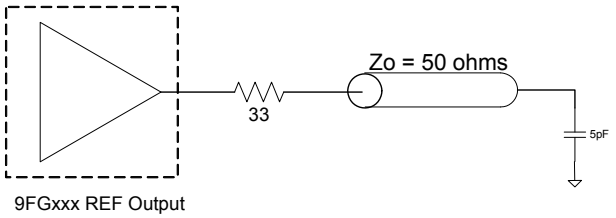


Figure 5. REF Output Test Load



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Differential Clock Tolerances x1 - 25MHz

Clock Periods - Differential Outputs with Spread Spectrum Disabled

SSC OFF or SSC +/- 0.25% Center Spread	Synthesis Error (ppm)	Center Freq. MHz	Measurement Window							Units	Notes
			1 Clock	1us	0.1s	0.1s	0.1s	1us	1 Clock		
			-c2c jitter AbsPer Min	-SSC Short-Term Average Min	- ppm Long-Term Average Min	0 ppm Period Nominal	+ ppm Long-Term Average Max	+SSC Short-Term Average Max	+c2c jitter AbsPer Max		
DIF	0	100.00	9.95000		10.00000	10.00000	10.00000		10.05000	ns	1,2
	0	125.00	7.95000		8.00000	8.00000	8.00000		8.05000	ns	1,2
	0	133.33	7.45000		7.50000	7.50000	7.50000		7.55000	ns	1,2
	10	166.67	5.94994		5.99994	6.00000	6.00006		6.05006	ns	1,2
	0	200.00	4.95000		5.00000	5.00000	5.00000		5.05000	ns	1,2
	6	266.67	3.69998		3.74998	3.75000	3.75002		3.80002	ns	1,2
	10	333.33	2.94997		2.99997	3.00000	3.00003		3.05003	ns	1,2
	0	400.00	2.45000		2.50000	2.50000	2.50000		2.55000	ns	1,2

Clock Periods - Differential Outputs with Spread Spectrum Enabled

SSC ON -0.5% Down Spread	Synthesis Error (ppm)	Center Freq. MHz	Measurement Window							Units	Notes
			1 Clock	1us	0.1s	0.1s	0.1s	1us	1 Clock		
			-c2c jitter AbsPer Min	-SSC Short-Term Average Min	- ppm Long-Term Average Min	0 ppm Period Nominal	+ ppm Long-Term Average Max	+SSC Short-Term Average Max	+c2c jitter AbsPer Max		
DIF	96	99.75	9.94910	9.99910	10.02410	10.02506	10.02603	10.05103	10.10103	ns	1,2
	19	124.69	7.94990	7.99990	8.01990	8.02005	8.02020	8.04020	8.09020	ns	1,2
	96	133.00	7.44933	7.49933	7.51808	7.51880	7.51952	7.53827	7.58827	ns	1,2
	10	166.25	5.94998	5.99998	6.01498	6.01504	6.01510	6.03010	6.08010	ns	1,2
	96	199.50	4.94955	4.99955	5.01205	5.01253	5.01301	5.02551	5.07551	ns	1,2
	-98	266.00	3.70039	3.75039	3.75977	3.75940	3.75903	3.76841	3.81841	ns	1,2
	10	332.50	2.94999	2.99999	3.00749	3.00752	3.00755	3.01505	3.06505	ns	1,2
	96	399.00	2.44978	2.49978	2.50603	2.50627	2.50651	2.51276	2.56276	ns	1,2

[1]Guaranteed by design and characterization, not 100% tested in production.

[2] All Long Term Accuracy specifications are guaranteed with the assumption that the REF output is tuned to the exact target XTAL frequency.

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Differential Clock Tolerances x1 - 14.31818MHz

Clock Periods - Differential Outputs with Spread Spectrum Disabled

SSC OFF or SSC +/- 0.25% Center Spread	Synthesis Error (ppm)	Center Freq. MHz	Measurement Window							Units	Notes
			1 Clock	1us	0.1s	0.1s	0.1s	1us	1 Clock		
			-c2c jitter AbsPer Min	-SSC Short-Term Average Min	- ppm Long-Term Average Min	0 ppm Period Nominal	+ ppm Long-Term Average Max	+SSC Short-Term Average Max	+c2c jitter AbsPer Max		
DIF	35	100.00	9.94965		9.99965	10.00000	10.00035		10.05035	ns	1,2
	-114	125.00	7.95091		8.00091	8.00000	7.99909		8.04909	ns	1,2
	35	133.33	7.44974		7.49974	7.50000	7.50026		7.55026	ns	1,2
	-104	166.67	5.95062		6.00062	6.00000	5.99937		6.04937	ns	1,2
	35	200.00	4.94983		4.99983	5.00000	5.00018		5.05018	ns	1,2
	42	266.67	3.69984		3.74984	3.75000	3.75016		3.80016	ns	1,2
	-104	333.33	2.95031		3.00031	3.00000	2.99969		3.04969	ns	1,2
	35	400.00	2.44991		2.49991	2.50000	2.50009		2.55009	ns	1,2

Clock Periods - Differential Outputs with Spread Spectrum Enabled

SSC ON -0.5% Down Spread	Synthesis Error (ppm)	Center Freq. MHz	Measurement Window							Units	Notes
			1 Clock	1us	0.1s	0.1s	0.1s	1us	1 Clock		
			-c2c jitter AbsPer Min	-SSC Short-Term Average Min	- ppm Long-Term Average Min	0 ppm Period Nominal	+ ppm Long-Term Average Max	+SSC Short-Term Average Max	+c2c jitter AbsPer Max		
DIF	199	99.75	9.94807	9.99807	10.02307	10.02506	10.02706	10.05206	10.10206	ns	1,2
	-100	124.69	7.95085	8.00085	8.02085	8.02005	8.01925	8.03925	8.08925	ns	1,2
	199	133.00	7.44855	7.49855	7.51730	7.51880	7.52029	7.53904	7.58904	ns	1,2
	10	166.25	5.94998	5.99998	6.01498	6.01504	6.01510	6.03010	6.08010	ns	1,2
	199	199.50	4.94903	4.99903	5.01153	5.01253	5.01353	5.02603	5.07603	ns	1,2
	-140	266.00	3.70055	3.75055	3.75992	3.75940	3.75887	3.76825	3.81825	ns	1,2
	10	332.50	2.94999	2.99999	3.00749	3.00752	3.00755	3.01505	3.06505	ns	1,2
	199	399.00	2.44952	2.49952	2.50577	2.50627	2.50676	2.51301	2.56301	ns	1,2

[1]Guaranteed by design and characterization, not 100% tested in production.

[2] All Long Term Accuracy specifications are guaranteed with the assumption that the REF output is tuned to the exact target XTAL frequency.

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General SMBus serial interface information for the 9FG830

How to Write:

- Controller (host) sends a start bit.
- Controller (host) sends the write address $DC_{(H)}$
- IDT clock will ***acknowledge***
- Controller (host) sends the begining byte location = N
- IDT clock will ***acknowledge***
- Controller (host) sends the data byte count = X
- IDT clock will ***acknowledge***
- Controller (host) starts sending ***Byte N through Byte N + X -1***
  (see Note 2)
- IDT clock will ***acknowledge*** each byte ***one at a time***
- Controller (host) sends a Stop bit

How to Read:

- Controller (host) will send start bit.
- Controller (host) sends the write address $DC_{(H)}$
- IDT clock will ***acknowledge***
- Controller (host) sends the begining byte location = N
- IDT clock will ***acknowledge***
- Controller (host) will send a separate start bit.
- Controller (host) sends the read address $DD_{(H)}$
- IDT clock will ***acknowledge***
- IDT clock will send the data byte count = X
- IDT clock sends ***Byte N + X -1***
- IDT clock sends ***Byte 0 through byte X (if $X_{(H)}$ was written to byte 8)***.
- Controller (host) will need to acknowledge each byte
- Controllor (host) will send a not acknowledge bit
- Controller (host) will send a stop bit

Index Block Write Operation

Controller (Host)			IDT (Slave/Receiver)
T	starT bit		
Slave Address $DC_{(H)}$			
WR	WRite		
			ACK
Beginning Byte = N			
			ACK
Data Byte Count = X			
			ACK
Beginning Byte N		X Byte	
			ACK
◇			
◇			◇
◇			◇
			◇
Byte N + X - 1			
			ACK
P	stoP bit		

Index Block Read Operation

Controller (Host)		IDT (Slave/Receiver)	
T	starT bit		
Slave Address $DC_{(H)}$			
WR	WRite		
		ACK	
Beginning Byte = N			
		ACK	
RT	Repeat starT		
Slave Address $DD_{(H)}$			
RD	ReaD		
		ACK	
		Data Byte Count = X	
ACK			
		X Byte	Beginning Byte N
ACK			
			◇
◇			◇
◇			◇
◇			
			Byte N + X - 1
N	Not acknowledge		
P	stoP bit		

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SMBus Table: Device Control Register, READ/WRITE ADDRESS (DC/DD)

Byte 0	Pin #	Name	Control Function	Type	0	1	Default
Bit 7	27		FS3[1]	RW	See Frequency Selection Table.		Pin 27
Bit 6	5		FS2[1]	RW			Pin 5
Bit 5	44		FS1[1]	RW			Pin 44
Bit 4	7		FS0[1]	RW			Pin 7
Bit 3	26		Spread Enable[1]	RW	Off	On	Pin 26
Bit 2	-		Enable Software Control of Frequency, Spread Enable (Spread Type always Software Control)	RW	Hardware Select	Software Select	0
Bit 1	-		DIF_STOP# drive mode	RW	Driven	Hi-Z	0
Bit 0	-		Spread Type	RW	Down	Center	0

Notes:
1. These bits reflect the state of the corresponding pins at power up, but may be written to if Byte 0, bit 2 is set to '1'. FS3 is the SEL14M_25M# pin.

SMBus Table: Output Enable Register

Byte 1	Pin #	Name	Control Function	Type	0	1	Default
Bit 7	-	DIF_7 EN	Output Enable	RW	Disable	Enable	1
Bit 6	-	DIF_6 EN	Output Enable	RW	Disable	Enable	1
Bit 5	-	DIF_5 EN	Output Enable	RW	Disable	Enable	1
Bit 4	-	DIF_4 EN	Output Enable	RW	Disable	Enable	1
Bit 3	-	DIF_3 EN	Output Enable	RW	Disable	Enable	1
Bit 2	-	DIF_2 EN	Output Enable	RW	Disable	Enable	1
Bit 1	-	DIF_1 EN	Output Enable	RW	Disable	Enable	1
Bit 0	-	DIF_0 EN	Output Enable	RW	Disable	Enable	1

Note: Byte 1 sets outputs active or inactive, not the conditons set by the OE inputs.

SMBus Table: Output Stop Mode Register

Byte 2	Pin #	Name	Control Function	Type	0	1	Default
Bit 7	-	DIF_7 STOP EN	Free Run/ Stop Enable	RW	Free-run	Stop-able	0
Bit 6	-	DIF_6 STOP EN	Free Run/ Stop Enable	RW	Free-run	Stop-able	0
Bit 5	-	DIF_5 STOP EN	Free Run/ Stop Enable	RW	Free-run	Stop-able	0
Bit 4	-	DIF_4 STOP EN	Free Run/ Stop Enable	RW	Free-run	Stop-able	0
Bit 3	-	DIF_3 STOP EN	Free Run/ Stop Enable	RW	Free-run	Stop-able	0
Bit 2	-	DIF_2 STOP EN	Free Run/ Stop Enable	RW	Free-run	Stop-able	0
Bit 1	-	DIF_1 STOP EN	Free Run/ Stop Enable	RW	Free-run	Stop-able	0
Bit 0	-	DIF_0 STOP EN	Free Run/ Stop Enable	RW	Free-run	Stop-able	0

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SMBus Table: Frequency Select Readback Register

Byte 3	Pin #	Name	Control Function	Type	0	1	Default
Bit 7	27	SEL14M_25M#[1]	State of pin 27	R	See Frequency Selection Table.		Pin 27
Bit 6	6	FS2[1]	State of pin 6	R			Pin 6
Bit 5	44	FS1[1]	State of pin 44	R			Pin 44
Bit 4	45	FS0[1]	State of pin 45	R			Pin 45
Bit 3	26	SPREAD[1]	State of pin 26	R	Off	On	Pin 26
Bit 2		Reserved		R	Reserved		X
Bit 1		Reserved		R	Reserved		X
Bit 0		Reserved		R	Reserved		X

Notes:
1. These bits reflect the state of the corresponding pins, regardless of whether software programming is enabled or not.

SMBus Table: Vendor & Revision ID Register

Byte 4	Pin #	Name	Control Function	Type	0	1	Default
Bit 7	-	RID3	REVISION ID	R	-	-	X
Bit 6	-	RID2		R	-	-	X
Bit 5	-	RID1		R	-	-	X
Bit 4	-	RID0		R	-	-	X
Bit 3	-	VID3	VENDOR ID	R	-	-	0
Bit 2	-	VID2		R	-	-	0
Bit 1	-	VID1		R	-	-	0
Bit 0	-	VID0		R	-	-	1

SMBus Table: DEVICE ID

Byte 5	Pin #	Name	Control Function	Type	0	1	Default
Bit 7	-	DEVID7	Device ID = 10 hex	R	Reserved		0
Bit 6	-	DEVID6		R	Reserved		0
Bit 5	-	DEVID5		R	Reserved		0
Bit 4	-	DEVID4		R	Reserved		1
Bit 3	-	DEVID3		R	Reserved		0
Bit 2	-	DEVID2		R	Reserved		0
Bit 1	-	DEVID1		R	Reserved		0
Bit 0	-	DEVID0		R	Reserved		0

SMBus Table: Byte Count Register

Byte 6	Pin #	Name	Control Function	Type	0	1	Default
Bit 7	-	BC7	Writing to this register will configure how many bytes will be read back, default is 07 = 7 bytes.	RW	-	-	0
Bit 6	-	BC6		RW	-	-	0
Bit 5	-	BC5		RW	-	-	0
Bit 4	-	BC4		RW	-	-	0
Bit 3	-	BC3		RW	-	-	0
Bit 2	-	BC2		RW	-	-	1
Bit 1	-	BC1		RW	-	-	1
Bit 0	-	BC0		RW	-	-	1

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SMBus Table: Reserved Register

Byte 7	Pin #	Name	Control Function	Type	0	1	Default
Bit 7			Reserved				X
Bit 6			Reserved				X
Bit 5			Reserved				X
Bit 4			Reserved				X
Bit 3			Reserved				X
Bit 2			Reserved				X
Bit 1			Reserved				X
Bit 0			Reserved				X

SMBus Table: Reserved Register

Byte 8	Pin #	Name	Control Function	Type	0	1	Default
Bit 7			Reserved				X
Bit 6			Reserved				X
Bit 5			Reserved				X
Bit 4			Reserved				X
Bit 3			Reserved				X
Bit 2			Reserved				X
Bit 1			Reserved				X
Bit 0			Reserved				X

SMBus Table: M/N Programming Enable

Byte 9	Pin #	Name	Control Function	Type	0	1	Default
Bit 7	-	M/N_EN	PLL M/N Programming Enable	RW	Disable	Enable	0
Bit 6	-	OE_Polarity	Select Polarity of OE inputs	RW	OE#	OE	1
Bit 5	5	REFOUT_En	Enables/Disables REF	RW	Disable	Enable	1
Bit 4			Reserved				0
Bit 3			Reserved				0
Bit 2			Reserved				0
Bit 1			Reserved				0
Bit 0			Reserved				0

SMBus Table: PLL Frequency Control Register

Byte 10	Pin #	Name	Control Function	Type	0	1	Default
Bit 7	-	PLL N Div8	N Divider Prog bit 8	RW	The decimal representation of M and N Divider in Byte 11 and 12 will configure the PLL VCO frequency. Default at power up = latch-in or Byte 0 Rom table. VCO Frequency = fXTAL x [NDiv(9:0)+8] / [MDiv(5:0)+2]		X
Bit 6	-	PLL N Div9	N Divider Prog bit 9	RW			X
Bit 5	-	PLL M Div5	M Divider Programming bit (5:0)	RW			X
Bit 4	-	PLL M Div4		RW			X
Bit 3	-	PLL M Div3		RW			X
Bit 2	-	PLL M Div2		RW			X
Bit 1	-	PLL M Div1		RW			X
Bit 0	-	PLL M Div0		RW			X

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SMBus Table: PLL Frequency Control Register

Byte 11	Pin #	Name	Control Function	Type	0	1	Default
Bit 7	-	PLL N Div7	N Divider Programming Byte11 bit(7:0) and Byte10 bit(7:6)	RW	The decimal representation of M and N Divider in Byte 11 and 12 will configure the PLL VCO frequency. Default at power up = latch-in or Byte 0 Rom table. VCO Frequency = fXTAL x [NDiv(9:0)+8] / [MDiv(5:0)+2]		X
Bit 6	-	PLL N Div6		RW			X
Bit 5	-	PLL N Div5		RW			X
Bit 4	-	PLL N Div4		RW			X
Bit 3	-	PLL N Div3		RW			X
Bit 2	-	PLL N Div2		RW			X
Bit 1	-	PLL N Div1		RW			X
Bit 0	-	PLL N Div0		RW			X

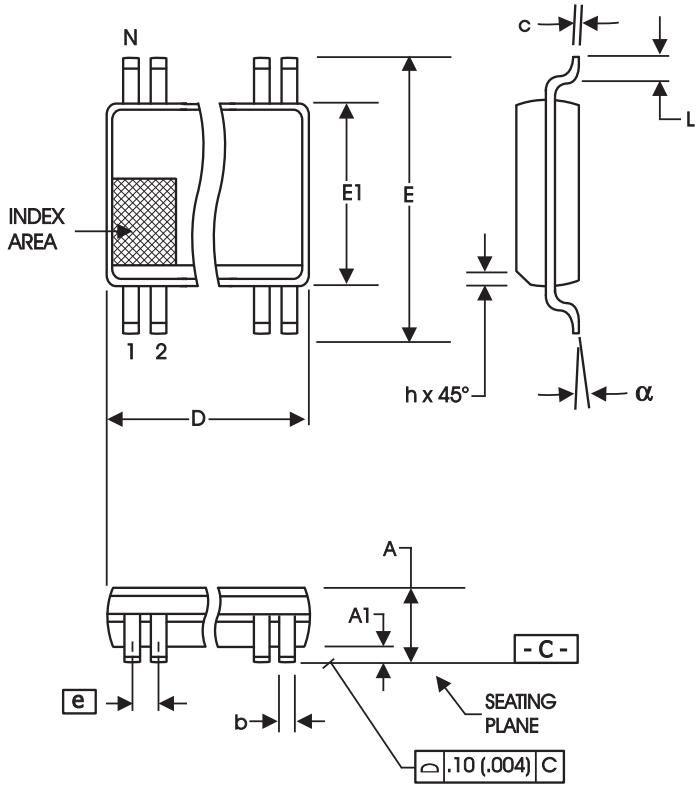
SMBus Table: PLL Spread Spectrum Control Register

Byte 12	Pin #	Name	Control Function	Type	0	1	Default
Bit 7	-	PLL SSP7	Spread Spectrum Programming bit(7:0)	RW	These Spread Spectrum bits in Byte 13 and 14 will program the spread pecentage of PLL		X
Bit 6	-	PLL SSP6		RW			X
Bit 5	-	PLL SSP5		RW			X
Bit 4	-	PLL SSP4		RW			X
Bit 3	-	PLL SSP3		RW			X
Bit 2	-	PLL SSP2		RW			X
Bit 1	-	PLL SSP1		RW			X
Bit 0	-	PLL SSP0		RW			X

SMBus Table: PLL Spread Spectrum Control Register

Byte 13	Pin #	Name	Control Function	Type	0	1	Default
Bit 7	-	Reserved					0
Bit 6	-	PLL SSP14	Spread Spectrum Programming bit(14:8)	RW	These Spread Spectrum bits in Byte 13 and 14 will program the spread pecentage of PLL		X
Bit 5	-	PLL SSP13		RW			X
Bit 4	-	PLL SSP12		RW			X
Bit 3	-	PLL SSP11		RW			X
Bit 2	-	PLL SSP10		RW			X
Bit 1	-	PLL SSP9		RW			X
Bit 0	-	PLL SSP8		RW			X

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300 mil SSOP

SYMBOL	In Millimeters COMMON DIMENSIONS		In Inches COMMON DIMENSIONS	
	MIN	MAX	MIN	MAX
A	2.41	2.80	.095	.110
A1	0.20	0.40	.008	.016
b	0.20	0.34	.008	.0135
c	0.13	0.25	.005	.010
D	SEE VARIATIONS		SEE VARIATIONS	
E	10.03	10.68	.395	.420
E1	7.40	7.60	.291	.299
e	0.635 BASIC		0.025 BASIC	
h	0.38	0.64	.015	.025
L	0.50	1.02	.020	.040
N	SEE VARIATIONS		SEE VARIATIONS	
a	0°	8°	0°	8°

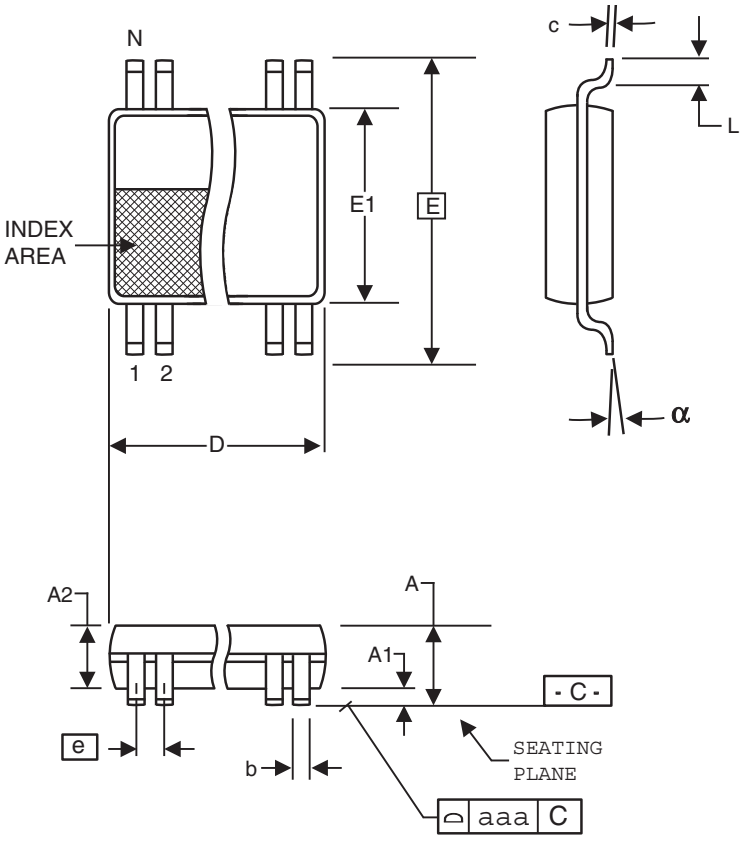
VARIATIONS

N	D mm.		D (inch)	
	MIN	MAX	MIN	MAX
48	15.75	16.00	.620	.630

Reference Doc.: JEDEC Publication 95, MO-118

10-0034

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6.10 mm. Body, 0.50 mm. Pitch TSSOP
(240 mil) (20 mil)

SYMBOL	In Millimeters COMMON DIMENSIONS		In Inches COMMON DIMENSIONS	
	MIN	MAX	MIN	MAX
A	--	1.20	--	.047
A1	0.05	0.15	.002	.006
A2	0.80	1.05	.032	.041
b	0.17	0.27	.007	.011
c	0.09	0.20	.0035	.008
D	SEE VARIATIONS		SEE VARIATIONS	
E	8.10 BASIC		0.319 BASIC	
E1	6.00	6.20	.236	.244
e	0.50 BASIC		0.020 BASIC	
L	0.45	0.75	.018	.030
N	SEE VARIATIONS		SEE VARIATIONS	
α	0°	8°	0°	8°
aaa	--	0.10	--	.004

VARIATIONS

N	D mm.		D (inch)	
	MIN	MAX	MIN	MAX
48	12.40	12.60	.488	.496

Reference Doc.: JEDEC Publication 95, MO-153

10-0039

Ordering Information

Part / Order Number	Shipping Packaging	Package	Temperature
9FG830AFLF	Tubes	48-pin SSOP	0 to +70°C
9FG830AFLFT	Tape and Reel	48-pin SSOP	0 to +70°C
9FG830AFILF	Tubes	48-pin SSOP	-40 to +85°C
9FG830AFILFT	Tape and Reel	48-pin SSOP	-40 to +85°C
9FG830AGLF	Tubes	48-pin TSSOP	0 to +70°C
9FG830AGLFT	Tape and Reel	48-pin TSSOP	0 to +70°C
9FG830AGILF	Tubes	48-pin TSSOP	-40 to +85°C
9FG830AGILFT	Tape and Reel	48-pin TSSOP	-40 to +85°C

"LF" suffix to the part number are the Pb-Free configuration and are RoHS compliant.
"A" is the device revision designator (will not correlate with the datasheet revision).

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Revision History

Rev.	Issue Date	Originator	Description	Page #
A	7/13/2010	RDW	Initial release. Move to final	
B	7/20/2010	RDW	1. Added PPM tables to DS for both 25M and 14.318M inputs 2. Added Test load figures	
C	8/25/2010	RDW	1. Updated/reformatted Electrical Tables 2. Corrected Features/Benefits and General Description 3. Updated termination figures to include Fig 5. for REF output	Various
D	7/3/2013	D. C.	1. Update OE# Latency min/max values from 1 & 3 cycles to 2 & 5 cycles respectively. 2. Update VDDA max current from 28 to 30mA for 100MHz and 400MHz. 3. Added typical values to Phase Jitter Parameters table.	Various
E	4/4/2017	RDW	1. Corrected Byte 5 Device ID from 83hex to 10 hex.	14

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Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,
Koto-ku, Tokyo 135-0061, Japan
www.renesas.com

Contact Information

For further information on a product, technology, the most up-to-date version of a document, or your nearest sales office, please visit:
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