General Description

The 9FGP202A is a peripheral clock for Intel Server. It is driven with a 25MHz crystal and generates CPU outputs up to 400MHz. An SMBus interface allows full control of the device.

Recommended Application

Peripheral Clock for Intel Server

Output Features

- 1 - 0.7V current-mode differential CPU pair
- 8 - 50MHz output
- 1 - DOT 96MHz output
- 1 - 33.33MHz output
- 1 - 32.768KHz output
- 2 - 25MHz REF outputs

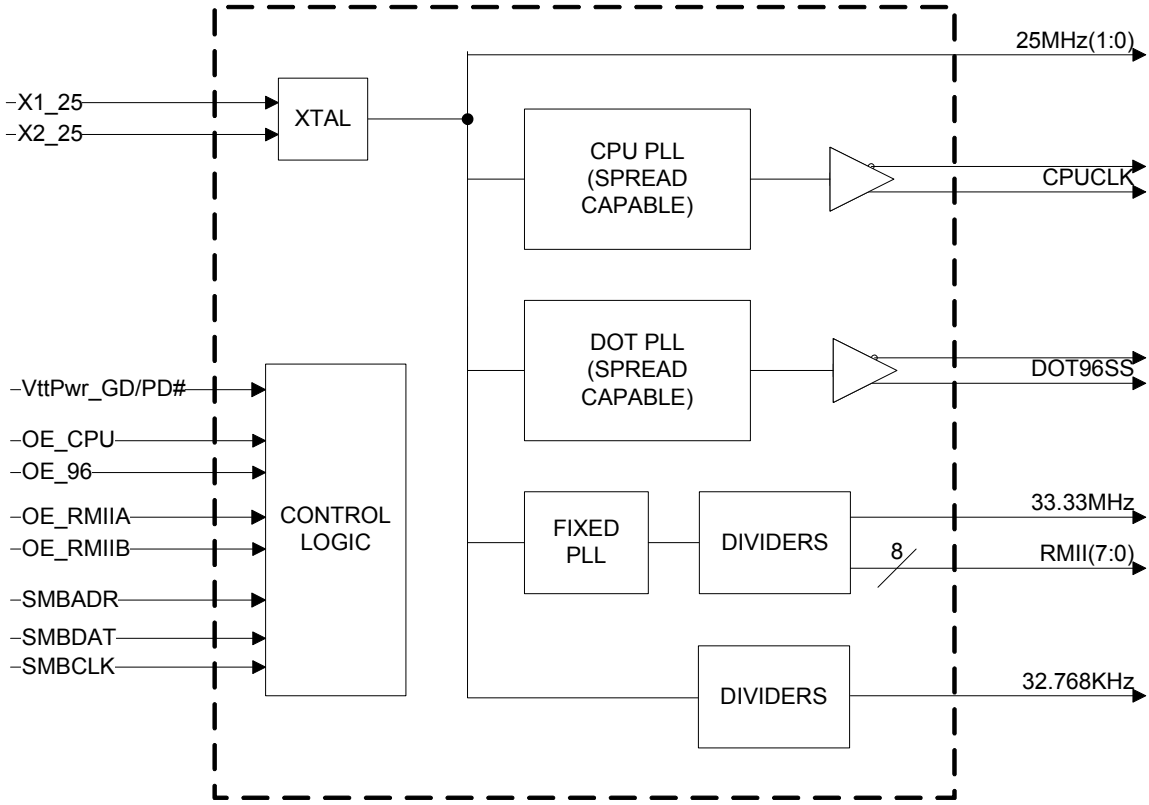
Features/Benefits

- Selectable SMBus Address – D0/D1 or C0/C1
- Spread Spectrum capability on CPU and DOT 96MHz clocks
- SMBus Control:
  - M/N and spread programming on CPU and DOT 96MHz clocks via SMBus
  - Outputs can be disabled via pins or SMBus

Key Specifications

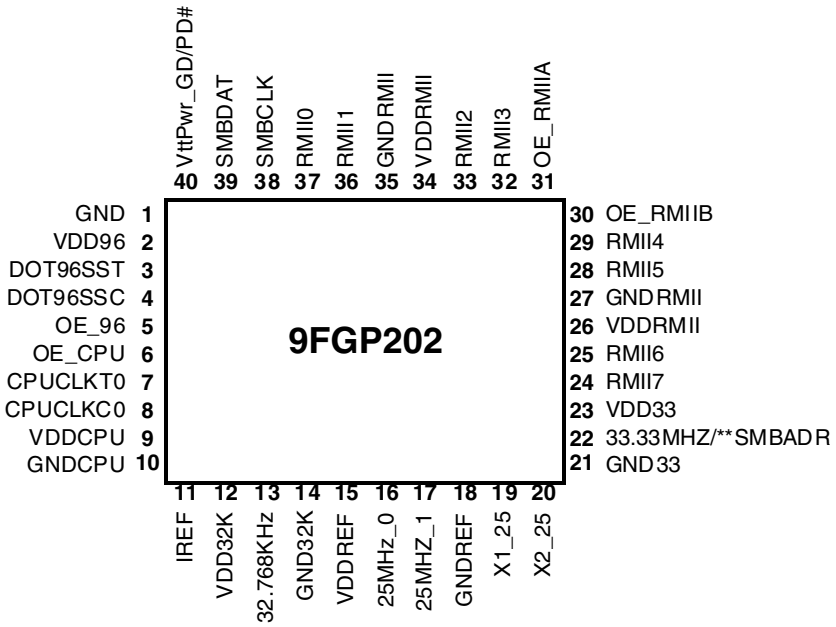
- Exact synthesis on CPU, RMII and 33.33MHz clocks
- +/- 100ppm frequency accuracy on remaining clocks

Block Diagram



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Pin Configuration



40-MLF

* Internal Pull-Up Resistor
** Internal Pull-Down Resistor

SMBus Address Selection

SMBADR	
***SMBADR = 0**	**SMBADR = 1**
D0/D1	C0/C1

* Default value

Power Supply Pins

Pin Number		Description
VDD	**GND**	
9	10	CPUCLK output
2	1	DOT96SS output
26,34	27,35	50 MHz RMII outputs
23	21	33.33MHz output
12	14	32.768KHz output
15	18	XTAL, REF outputs

Note: All VDD should be connected to a common power rail with proper filtering and decoupling.

Functionality

CPU FS2 Byte0 Bit2	CPU FS1 Byte0 Bit1	CPU FS0 Byte0 Bit0	CPUCLK MHz	DOT96SS MHz	33.33 MHz	RMII MHz	25 MHz	32.768 KHz
0	0	0	266.67	96.00	33.33	50.00	25.00	32.768
0	0	1	133.33	96.00	33.33	50.00	25.00	32.768
0	1	0	200.00	96.00	33.33	50.00	25.00	32.768
0	1	1	166.67	96.00	33.33	50.00	25.00	32.768
1	0	0	333.33	96.00	33.33	50.00	25.00	32.768
1	0	1	100.00	96.00	33.33	50.00	25.00	32.768
1	1	0	400.00	96.00	33.33	50.00	25.00	32.768
1	1	1	Reserved	96.00	33.33	50.00	25.00	32.768

Power up default is highlighted.

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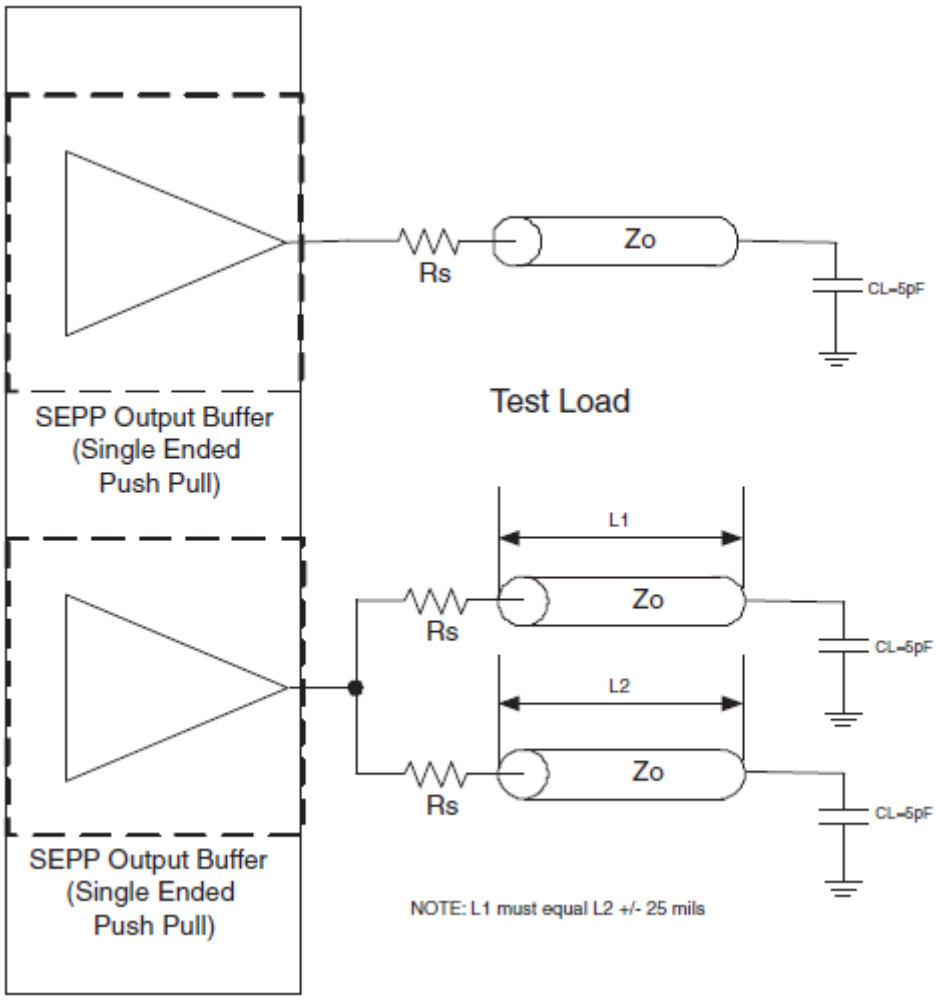
Pin Descriptions

PIN #	PIN NAME	PIN TYPE	DESCRIPTION
1	GND	PWR	Ground pin.
2	VDD96	PWR	Power pin for the DOT96 clocks, nominal 3.3V
3	DOT96SST	OUT	True clock of differential pair for 96.00MHz spread spectrum capable DOT clock.
4	DOT96SSC	OUT	Complement clock of differential pair for 96.00MHz spread spectrum capable DOT clock.
5	OE_96	IN	Active high input for enabling 96Hz outputs. 1 = enable output(s), 0 = tri-state output(s)
6	OE_CPU	IN	Active high input for enabling CPU DIFF pairs. 1 = enable output(s), 0 = tri-state output(s)
7	CPUCLKT0	OUT	True clock of differential pair CPU outputs. These are current mode outputs. External resistors are required for voltage bias.
8	CPUCLKC0	OUT	Complementary clock of differential pair CPU outputs. These are current mode outputs. External resistors are required for voltage bias.
9	VDDCPU	PWR	Supply for CPU clocks, 3.3V nominal
10	GNDCPU	PWR	Ground pin for the CPU outputs
11	IREF	OUT	This pin establishes the reference current for the differential current-mode output pairs. This pin requires a fixed precision resistor tied to ground in order to establish the appropriate current. 475 ohms is the standard value.
12	VDD32K	PWR	Power pin for the 32.768KHz outputs, nominal 3.3V
13	32.768KHz	OUT	32.768KHz clock output
14	GND32K	PWR	Ground pin for the 32.768KHz outputs
15	VDDREF	PWR	Ref, XTAL power supply, nominal 3.3V
16	25MHz_0	OUT	25MHz clock output, 3.3V
17	25MHZ_1	OUT	25MHz clock output, 3.3V
18	GNDREF	PWR	Ground pin for the REF outputs.
19	X1_25	IN	Crystal input, Nominally 25.00MHz.
20	X2_25	OUT	Crystal output, Nominally 25.00MHz.
21	GND33	PWR	Ground pin for the 33.33MHz outputs
22	33.33MHZ/**SMBADR	I/O	33.33MHz clock output / SMBus address select bit.
23	VDD33	PWR	Power pin for the 33.33MHz outputs, nominal 3.3V
24	RMII7	OUT	3.3V RMII clock output
25	RMII6	OUT	3.3V RMII clock output
26	VDDRMII	PWR	3.3V power pin for the RMII clocks.
27	GNDRMII	PWR	Ground pin for the 3V50 outputs
28	RMII5	OUT	3.3V RMII clock output
29	RMII4	OUT	3.3V RMII clock output
30	OE_RMIIB	IN	Active high input for enabling RMII(7:4) outputs. 1 = enable output(s), 0 = low
31	OE_RMIIA	IN	Active high input for enabling RMII(3:0) outputs. 1 = enable output(s), 0 = low
32	RMII3	OUT	3.3V RMII clock output
33	RMII2	OUT	3.3V RMII clock output
34	VDDRMII	PWR	3.3V power pin for the RMII clocks.
35	GNDRMII	PWR	Ground pin for the 3V50 outputs
36	RMII1	OUT	3.3V RMII clock output
37	RMII0	OUT	3.3V RMII clock output
38	SMBCLK	IN	Clock pin of SMBUS circuitry, 5V tolerant
39	SMBDAT	I/O	Data pin of SMBUS circuitry, 5V tolerant
40	VttPwr_GD/PD#	IN	This 3.3V LVTTL input is a level sensitive strobe used to determine when latch inputs are valid and are ready to be sampled. This is an active high input. / Asynchronous active low input pin used to power down the device into a low power state.

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Drive Strengths

9FGP202A



The singled-ended outputs of the 9FGP202A default to either a drive strength of 2 loads or a drive strength of 1 load. Alternate drive strengths can be selected via the SMBus. Using the correct resistor value can properly terminate the output to the transmission line without having to change the default drive strengths via the SMBus. The default drive strengths for the single ended outputs are show below, as are the suggested termination resistors for the above topologies. All values assume Zo = 50 ohms:

Default Drive Strength Table

	Default Drive	Optional Drive
RMII	1 Load	2 Loads
33.33MHz	2 Loads	1 Load
25Mhz	2 Loads	1 Load
32.768KHz	2 Loads	1 Load

Series Termination Resistor Values

Output Drive Strength	Series Resistor (Rs) for driving 1 Load	Series Resistor (Rs) for driving 2 Loads
1 Load	33 ohms	N/A
2 Loads	43 ohms	22 ohms

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Truth Table 1: VttPwr_GD/PD# and OE_96

VttPwr_GD/PD#	OE_96	Clocks
Pin 40	Pin 5	
0	0	All clocks are powered down
0	1	All clocks are powered down
1	0	All clocks are enabled except DOT96SS
1	1	*All clocks are enabled including DOT96SS

*Assuming DOT96 Output Enable from SMBus Byte2 Bit0 sets to enable (default)

Truth Table 2: VttPwr_GD/PD# and OE_CPU

VttPwr_GD/PD#	OE_CPU	Clocks
Pin 40	Pin 6	
0	0	All clocks are powered down
0	1	All clocks are powered down
1	0	All clocks are enabled except CPUCLK
1	1	*All clocks are enabled including CPUCLK

*Assuming CPUCLK Output Enable from SMBus Byte2 Bit1 sets to enable (default)

Table 1: CPU Spread and Frequency Selection

CPU SS_EN	CPU FS2	CPU FS1	CPU FS0	CPU MHz	Down Spread %
Byte 0 Bit 3	Byte 0 Bit 2	Byte 0 Bit 1	Byte 0 Bit 0		
0	0	0	0	266.67	0%
0	0	0	1	133.33	0%
0	0	1	0	200.00	0%
0	0	1	1	166.67	0%
0	1	0	0	333.33	0%
0	1	0	1	100.00	0%
0	1	1	0	400.00	0%
0	1	1	1	200.00	0%
1	0	0	0	266.67	0.5%
1	0	0	1	133.33	0.5%
1	0	1	0	200.00	0.5%
1	0	1	1	166.67	0.5%
1	1	0	0	333.33	0.5%
1	1	0	1	100.00	0.5%
1	1	1	0	400.00	0.5%
1	1	1	1	200.00	0.5%

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Table2: DOT96 Spread and Frequency Selection Table

DOT96 SS_EN	FS3	FS2	FS1	FS0	DOT96SS MHz	Spread %	
Byte 0 bit 4	Byte 3 bit 3	Byte 3 bit 2	Byte 3 bit 1	Byte 3 bit 0			
0	0	0	0	0	96.00	0	
0	0	0	0	1	96.00	0	
0	0	0	1	0	96.00	0	
0	0	0	1	1	96.00	0	
0	0	1	0	0	96.00	0	
0	0	1	0	1	96.00	0	
0	0	1	1	0	96.00	0	
0	0	1	1	1	96.00	0	
0	1	0	0	0	96.00	0	
0	1	0	0	1	96.00	0	
0	1	0	1	0	96.00	0	
0	1	0	1	1	96.00	0	
0	1	1	0	0	96.00	0	
0	1	1	0	1	96.00	0	
0	1	1	1	0	96.00	0	
0	1	1	1	1	96.00	0	
1	0	0	0	0	96.00	+/-0.25	Center
1	0	0	0	1	96.00	+/-0.5	Center
1	0	0	1	0	96.00	+/-0.75	Center
1	0	0	1	1	96.00	+/-1.0	Center
1	0	1	0	0	96.00	-0.25	Down
1	0	1	0	1	96.00	-0.50	Down
1	0	1	1	0	96.00	-0.75	Down
1	0	1	1	1	96.00	-1.0	Down
1	1	0	0	0	96.00	-1.25	Down
1	1	0	0	1	96.00	-1.50	Down
1	1	0	1	0	96.00	-1.75	Down
1	1	0	1	1	96.00	-2.0	Down
1	1	1	0	0	96.00	-2.25	Down
1	1	1	0	1	96.00	-2.5	Down
1	1	1	1	0	96.00	-2.75	Down
1	1	1	1	1	96.00	-3.00	Down

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Absolute Maximum Ratings

Stresses above the ratings listed below can cause permanent damage to the 9FGP202A. These ratings, which are standard values for IDT commercially rated parts, are stress ratings only. Functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods can affect product reliability. Electrical parameters are guaranteed only over the recommended operating temperature range.

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	Notes
3.3V Supply Voltage	VDDxxx	-	GND - 0.5	3.3V	GND + 4.5	V	1
Maximum difference across all VDD pins	VDDdelta	-			0.5	V	1
Storage Temperature	Ts	-	-65		150	˚C	1
Ambient Operating Temp	Tambient	-	0		70	°C	1
Junction Temperature	Tj	-			125	°C	1
Input ESD protection HBM	ESD prot	-	2000			V	1

[1]Guaranteed by design and characterization, not 100% tested in production.

Electrical Characteristics–DOT96SS 0.7V Current Mode Differential Pair

PARAMETER	SYMBOL	CONDITIONS*	MIN	TYP	MAX	UNITS	Notes
Current Source Output Impedance	Zo	$V_O = V_x$	3000			Ω	1
Voltage High	VHigh	Statistical measurement on single ended signal	660		850	mV	1,3
Voltage Low	VLow		-150		150	mV	1,3
Max Voltage	Vovs	Measurement on single ended signal using absolute value.			1150	mV	1
Min Voltage	Vuds		-300			mV	1
Crossing Voltage (abs)	Vx(abs)		250		550	mV	1
Crossing Voltage (var)	d-Vcross	Variation of crossing over all edges			140	mV	1
Long Accuracy	ppm	see Tperiod min-max values	-100		100	ppm	1,2
Average period	Tperiod	96.00MHz nominal	10.4135		10.4198	ns	2
		96.00MHz spread	10.4135		10.4722	ns	2
Absolute min period	Tabsmin	96.00MHz nominal/spread	10.1635		10.7222	ns	1,2
Rise Time	t_r	V_{OL} = 0.175V, V_{OH} = 0.525V	175		700	ps	1
Fall Time	t_f	V_{OH} = 0.525V V_{OL} = 0.175V	175		700	ps	1
Rise Time Variation	d-t_r	V_{OL} = 0.175V, V_{OH} = 0.525V			125	ps	1
Fall Time Variation	d-t_f	V_{OH} = 0.525V V_{OL} = 0.175V			125	ps	1
Duty Cycle	d_{t3}	Measurement from differential wavefrom	45		55	%	1
Jitter, Cycle to cycle	$t_{jcyc-cyc}$	Measurement from differential wavefrom			250	ps	1

*T_A = 0 - 70°C; V_{DD} = 3.3 V +/-5%; C_L =2pF, R_S=33.2ohms, R_P=49.9ohms, I_{REF} = 475ohms

[1]Guaranteed by design and characterization, not 100% tested in production.

[2] All Long Term Accuracy and Clock Period specifications are guaranteed assuming that REFOUT is at 25.00MHz

[3]$I_{REF} = V_{DD}/(3xR_R)$. For R_R = 475ohms (1%), I_{REF} = 2.32mA. I_{OH} = 6 x I_{REF} and V_{OH} = 0.7V @ Z_O=50ohms.

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Electrical Characteristics–Input/Supply/Common Output Parameters

PARAMETER	SYMBOL	CONDITIONS*	MIN	TYP	MAX	UNITS	Notes
Input High Voltage	V_{IH}	3.3 V +/-5%	2		V_{DD} + 0.3	V	1
Input Low Voltage	V_{IL}	3.3 V +/-5%	V_{SS} - 0.3		0.8	V	1
Input High Current	I_{IH}	$V_{IN} = V_{DD}$	-5		5	uA	1
Input Low Current	I_{IL1}	V_{IN} = 0 V; Inputs with no pull-up resistors	-5			uA	1
	I_{IL2}	V_{IN} = 0 V; Inputs with pull-up resistors	-200			uA	1
Low Threshold Input-High Voltage	V_{IH_FS}	3.3 V +/-5%	0.7		V_{DD} + 0.3	V	1
Low Threshold Input-Low Voltage	V_{IL_FS}	3.3 V +/-5%	V_{SS} - 0.3		0.35	V	1
Operating Current	$I_{DD3.3OP}$	all outputs driven			200	mA	1
Powerdown Current	$I_{DD3.3PD}$	all diff pairs driven			30	mA	1
		all differential pairs tri-stated			8	mA	1
Input Frequency	F_i	V_{DD} = 3.3 V		25.00000		MHz	2
Pin Inductance	L_{pin}				7	nH	1
Input Capacitance	C_{IN}	Logic Inputs			4	pF	1
	C_{OUT}	Output pin capacitance			5	pF	1
	C_{INX}	X1 & X2 pins			5	pF	1
Clk Stabilization	T_{STAB}	From VDD Power-Up or de-assertion of PD to 1st clock			2.5	ms	1
Modulation Frequency		Triangular Modulation	30		33	kHz	1
Tdrive_PD		CPU output enable after PD de-assertion			300	us	1
Tfall_PD		PD fall time of			5	ns	1
Trise_PD		PD rise time of			5	ns	1
SMBus Voltage	V_{DD}		2.7		5.5	V	1
Low-level Output Voltage	V_{OL}	@ I_{PULLUP}			0.4	V	1
Current sinking at V_{OL} = 0.4 V	I_{PULLUP}		4			mA	1
SCLK/SDATA Clock/Data Rise Time	T_{RI2C}	(Max VIL - 0.15) to (Min VIH + 0.15)			1000	ns	1
SCLK/SDATA Clock/Data Fall Time	T_{FI2C}	(Min VIH + 0.15) to (Max VIL - 0.15)			300	ns	1

*TA = 0 - 70°C; Supply Voltage VDD = 3.3 V +/-5%

[1]Guaranteed by design and characterization, not 100% tested in production.

[2] Input frequency should be measured at the REF pin and tuned to ideal 25.00MHz to meet ppm frequency accuracy on PLL outputs.

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Electrical Characteristics–CPU 0.7V Current Mode Differential Pair

PARAMETER	SYMBOL	CONDITIONS*	MIN	TYP	MAX	UNITS	NOTES
Current Source Output Impedance	Zo	$V_O = V_x$	3000			Ω	1
Voltage High	VHigh	Statistical measurement on single ended signal	660		850	mV	1,3
Voltage Low	VLow		-150		150	mV	1,3
Max Voltage	Vovs	Measurement on single ended signal using absolute value.			1150	mV	1
Min Voltage	Vuds		-300			mV	1
Crossing Voltage (abs)	Vx(abs)		250		550	mV	1
Crossing Voltage (var)	d-Vx	Variation of crossing over all edges			140	mV	1
Long Accuracy	ppm	see Tperiod min-max values	-100	0	100	ppm	1,2
Average period	Tperiod	400MHz nominal	2.4998	2.5000	2.5003	ns	2
		400MHz spread	2.4998		2.5128	ns	2
		333.33MHz nominal	2.9997	3.0000	3.0003	ns	2
		333.33MHz spread	2.9997		3.0154	ns	2
		266.66MHz nominal	3.7496	3.7500	3.7504	ns	2
		266.66MHz spread	3.7496		3.7692	ns	2
		200MHz nominal	4.9995	5.0000	5.0005	ns	2
		200MHz spread	4.9995		5.0256	ns	2
		166.66MHz nominal	5.9994	6.0000	6.0006	ns	2
		166.66MHz spread	5.9994		6.0307	ns	2
		133.33MHz nominal	7.4993	7.5000	7.5008	ns	2
		133.33MHz spread	7.4993		7.5385	ns	2
		100.00MHz nominal	9.9990	10.0000	10.0010	ns	2
		100.00MHz spread	9.9990		10.0513	ns	2
Absolute min/max period	$T_{absmin/max}$	400MHz nominal/spread	2.4148		2.5978	ns	1,2
		333.33MHz nominal/spread	2.9147		3.1004	ns	1,2
		266.66MHz nominal/spread	3.6646		3.8542	ns	1,2
		200MHz nominal/spread	4.9145		5.1106	ns	1,2
		166.66MHz nominal/spread	5.9144		6.1157	ns	1,2
		133.33MHz nominal/spread	7.4143		7.6235	ns	1,2
		100.00MHz nominal/spread	9.9140		10.1363	ns	1,2
Rise Time	t_r	V_{OL} = 0.175V, V_{OH} = 0.525V	175		700	ps	1
Fall Time	t_f	V_{OH} = 0.525V V_{OL} = 0.175V	175		700	ps	1
Rise Time Variation	d-t_r	V_{OL} = 0.175V, V_{OH} = 0.525V			125	ps	1
Fall Time Variation	d-t_f	V_{OH} = 0.525V V_{OL} = 0.175V			125	ps	1
Duty Cycle	d_{t3}	Measurement from differential wavefrom	45		55	%	1
Jitter, Cycle to cycle	$t_{jcyc-cyc}$	Measurement from differential wavefrom, CPUCLK			85	ps	1

*T_A = 0 - 70°C; V_{DD} = 3.3 V +/-5%; C_L =2pF, R_S=33.2ohms, R_P=49.9ohms, I_{REF} = 475ohms

[1]Guaranteed by design and characterization, not 100% tested in production.

[2] All Long Term Accuracy and Clock Period specifications are guaranteed assuming that REFOUT is at 25.000MHz

[3]$I_{REF} = V_{DD}/(3xR_R)$. For R_R = 475ohms (1%), I_{REF} = 2.32mA. I_{OH} = 6 x I_{REF} and V_{OH} = 0.7V @ Z_O=50ohms.

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Electrical Characteristics–RMII - 50MHz

PARAMETER	SYMBOL	CONDITIONS*	MIN	TYP	MAX	UNITS	NOTES
Long Accuracy	ppm	see Tperiod min-max values	-50	0	50	ppm	1,2
Clock period	Tperiod	50.00MHz output nominal	19.990	20.000	20.010	ns	1
Output High Voltage	V_{OH}	I_{OH} = -1 mA	2.4			V	1
Output Low Voltage	V_{OL}	I_{OL} = 1 mA			0.4	V	1
Output High Current	I_{OH}	V_{OH} @MIN = 1.0 V	-33			mA	1
		V_{OH} @MAX = 3.135 V			-33	mA	1
Output Low Current	I_{OL}	V_{OL} @ MIN = 1.95 V	30			mA	1
		V_{OL} @ MAX = 0.4 V			38	mA	1
Rise Time	t_r	V_{OL} = 0.4 V, V_{OH} = 2.4 V	1		3	ns	1
Fall Time	t_f	V_{OH} = 2.4 V, V_{OL} = 0.4 V	1		3	ns	1
Duty Cycle	d_{t1}	V_T = 1.5 V	35		65	%	1
Group Skew	$t_{skew_3V50(3:0)}$	V_T = 1.5 V, for each group of 4 outputs			200	ps	1
	$t_{skew_3V50(7:4)}$						
Jitter, Long Term	t_{jabs}	V_T = 1.5 V, 10 µsec interval			500	ps	1
Jitter, Peak	t_{jpeak}	V_T = 1.5 V			100	ps	1,3

*TA = 0 - 70°C; Supply Voltage VDD = 3.3 V +/-5%, CL = 5 pF with Rs as shown in the termination table (unless otherwise specified)

[1]Guaranteed by design and characterization, not 100% tested in production.

[2] All Long Term Accuracy and Clock Period specifications are guaranteed assuming that REFOUT is at 25.00MHz

[3]1/2 of the peak-to-peak jitter. (Lg++ lLg-l)/2

Electrical Characteristics–33.33MHz

PARAMETER	SYMBOL	CONDITIONS*	MIN	TYP	MAX	UNITS	NOTES
Long Accuracy	ppm	see Tperiod min-max values	-100	0	100	ppm	1
Clock period	Tperiod	33.33MHz output non-spread	29.970	30.000	30.030	ns	1
Absolute min/max period	Tabs	33.33MHz output non-spread	29.720	30.000	30.280	ns	1
Output High Voltage	V_{OH}	I_{OH} = -1 mA	2.4			V	1
Output Low Voltage	V_{OL}	I_{OL} = 1 mA			0.4	V	1
Output High Current	I_{OH}	V_{OH} @MIN = 1.0 V	-33			mA	1
		V_{OH} @MAX = 3.135 V			-33	mA	1
Output Low Current	I_{OL}	V_{OL} @ MIN = 1.95 V	30			mA	1
		V_{OL} @ MAX = 0.4 V			38	mA	1
Rise Time	t_r	V_{OL} = 0.4 V, V_{OH} = 2.4 V	0.5		2	ns	1
Fall Time	t_f	V_{OH} = 2.4 V, V_{OL} = 0.4 V	0.5		2	ns	1
Duty Cycle	d_{t1}	V_T = 1.5 V	45		55	%	1
Jitter, Cycle to cycle	$t_{jcyc-cyc}$	V_T = 1.5 V			250	ps	1

*TA = 0 - 70°C; Supply Voltage VDD = 3.3 V +/-5%, CL = 5 pF with Rs as shown in the termination table (unless otherwise specified)

[1]Guaranteed by design and characterization, not 100% tested in production.

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Electrical Characteristics–32.768kHz

PARAMETER	SYMBOL	CONDITIONS*	MIN	TYP	MAX	UNITS	NOTES
Long Accuracy	ppm	see Tperiod min-max values	-100		100	ppm	1
Clock period	Tperiod	32.768KHz output nominal		30.518		us	1
Output High Voltage	V_{OH}	I_{OH} = -1 mA	2.4			V	1
Output Low Voltage	V_{OL}	I_{OL} = 1 mA			0.4	V	1
Output High Current	I_{OH}	V_{OH} @MIN = 1.0 V	-33			mA	1
		V_{OH} @MAX = 3.135 V			-33	mA	1
Output Low Current	I_{OL}	V_{OL} @ MIN = 1.95 V	30			mA	1
		V_{OL} @ MAX = 0.4 V			38	mA	1
Rise Time	t_r	V_{OL} = 0.4 V, V_{OH} = 2.4 V	1		4	ns	1
Fall Time	t_f	V_{OH} = 2.4 V, V_{OL} = 0.4 V	1		4	ns	1
Duty Cycle	d_{t1}	V_T = 1.5 V	45		55	%	1
Jitter, Cycle to cycle	$t_{jcyc-cyc}$	V_T = 1.5 V			500	ps	1

*TA = 0 - 70°C; Supply Voltage VDD = 3.3 V +/-5%, CL = 5 pF with Rs as shown in the termination table (unless otherwise specified)

[1]Guaranteed by design and characterization, not 100% tested in production.

Electrical Characteristics–REF - 25MHz

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	Notes
Long Accuracy	ppm	see Tperiod min-max values	-50		50	ppm	1,2
Clock period	T_{period}	25.00MHz output nominal	39.980	40.000	40.020	ns	2
Output High Voltage	V_{OH}	I_{OH} = -1 mA	2.4			V	1
Output Low Voltage	V_{OL}	I_{OL} = 1 mA			0.4	V	1
Output High Current	I_{OH}	V_{OH} @MIN = 1.0 V	-29			mA	1
		V_{OH} @MAX = 3.135 V			-23	mA	1
Output Low Current	I_{OL}	V_{OL} @ MIN = 1.95 V	29			mA	1
		V_{OL} @ MAX = 0.4 V			27	mA	1
Rise Time	t_{r1}	V_{OL} = 0.4 V, V_{OH} = 2.4 V	1		2	ns	1
Fall Time	t_{f1}	V_{OH} = 2.4 V, V_{OL} = 0.4 V	1		2	ns	1
Skew	t_{sk1}	V_T = 1.5 V			500	ps	1
Duty Cycle	d_{t1}	V_T = 1.5 V	45		55	%	1
Jitter	$t_{jcyc-cyc}$	V_T = 1.5 V			500	ps	1

*TA = 0 - 70°C; Supply Voltage VDD = 3.3 V +/-5%, CL = 5 pF with Rs as shown in the termination table (unless otherwise specified)

[1]Guaranteed by design and characterization, not 100% tested in production.

[2] All Long Term Accuracy and Clock Period specifications are guaranteed assuming that REFOUT is at 25.000MHz

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General SMBus Serial Interface Information

How to Write

- Controller (host) sends a start bit
- Controller (host) sends the write address
- IDT clock will **acknowledge**
- Controller (host) sends the beginning byte location = N
- IDT clock will **acknowledge**
- Controller (host) sends the byte count = X
- IDT clock will **acknowledge**
- Controller (host) starts sending Byte **N through Byte N+X-1**
- IDT clock will **acknowledg**e each byte **one at a time**
- Controller (host) sends a Stop bit

Index Block Write Operation			
Controller (Host)			**IDT (Slave/Receiver)**
T	starT bit		
Slave Address			
WR	WRite		
			ACK
Beginning Byte = N			
			ACK
Data Byte Count = X			
			ACK
Beginning Byte N		X Byte	
			ACK
O			
O			O
O			O
			O
Byte N + X - 1			
			ACK
P	stoP bit		

Read Address	Write Address
$*D1_{(H)}$	$*D0_{(H)}$

* By default, SMBADR = 0,
therefore, SMBus WRITE/READ address is D0/D1.
Please see SMBus Address Selection table on page 2.

How to Read

- Controller (host) will send a start bit
- Controller (host) sends the write address
- IDT clock will **acknowledge**
- Controller (host) sends the beginning byte location = N
- IDT clock will **acknowledge**
- Controller (host) will send a separate start bit
- Controller (host) sends the read address
- IDT clock will **acknowledge**
- IDT clock will send the data byte count = X
- IDT clock sends Byte **N+X-1**
- IDT clock sends **Byte 0 through Byte X (if $X_{(H)}$ was written to Byte 8)**
- Controller (host) will need to acknowledge each byte
- Controller (host) will send a not acknowledge bit
- Controller (host) will send a stop bit

Index Block Read Operation			
Controller (Host)			**IDT (Slave/Receiver)**
T	starT bit		
Slave Address			
WR	WRite		
			ACK
Beginning Byte = N			
			ACK
RT	Repeat starT		
Slave Address			
RD	ReaD		
			ACK
			Data Byte Count=X
ACK			
		X Byte	Beginning Byte N
ACK			
			O
O			O
O			O
O			
			Byte N + X - 1
N	Not acknowledge		
P	stoP bit		

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SMBus Table: CPU Frequency Select and Spread Spectrum Control Register

Byte 0	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	-	Reserved	Reserved	RW	Reserved		0
Bit 6	-	Reserved	Reserved	Rev 0.20	Reserved		0
Bit 5	-	Reserved	Reserved	RW	Reserved		0
Bit 4	-	DOT96 SS_EN	DOT96 Spread Spectrum Enable	RW	Disable	Enable	0
Bit 3	-	CPU SS_EN	CPU Spread Spectrum Enable	RW	See Table 1: CPU Frequency Selection Table		0
Bit 2	-	CPU FS2	CPU Freq Select Bit 2	RW			0
Bit 1	-	CPU FS1	CPU Freq Select Bit 1	RW			1
Bit 0	-	CPU FS0	CPU Freq Select Bit 0	RW			0

SMBus Table: RMII Output Control Register

Byte 1	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	24	RMII_7 Enable	RMII_7 Output Control	RW	Disable	Enable	1
Bit 6	25	RMII_6 Enable	RMII_6 Output Control	RW	Disable	Enable	1
Bit 5	28	RMII_5 Enable	RMII_5 Output Control	RW	Disable	Enable	1
Bit 4	29	RMII_4 Enable	RMII_4 Output Control	RW	Disable	Enable	1
Bit 3	32	RMII_3 Enable	RMII_3 Output Control	RW	Disable	Enable	1
Bit 2	33	RMII_2 Enable	RMII_2 Output Control	RW	Disable	Enable	1
Bit 1	36	RMII_1 Enable	RMII_1 Output Control	RW	Disable	Enable	1
Bit 0	37	RMII_0 Enable	RMII_0 Output Control	RW	Disable	Enable	1

SMBus Table: DOT, CPU, 32.768KHz, 25MHz and 33.33MHz Outputs Control Register

Byte 2	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	7,8	CPUCLK PD Drive Mode	Driven in PD	RW	Driven	Hi-Z	0
Bit 6	3,4	DOT96SS PD Drive Mode	Driven in PD	RW	Driven	Hi-Z	0
Bit 5	22	33.33MHz Enable	33.33MHz Output Control	RW	Disable	Enable	1
Bit 4	17	25MHz_1 Enable	25MHz_1 Output Control	RW	Disable	Enable	1
Bit 3	16	25MHz_0 Enable	25MHz_0 Output Control	RW	Disable	Enable	1
Bit 2	13	32.768kHz Enable	32.768KHz Output Control	RW	Disable	Enable	1
Bit 1	6	CPUCLK Enable	CPUCLK Output Control	RW	Disable	Enable	1
Bit 0	5	DOT96SS Enable	DOT96SS Output Control	RW	Disable	Enable	1

SMBus Table: DOT96 Frequency Select and Spread Spectrum Control Register

Byte 3	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	-	Reserved	Reserved	RW	Reserved		0
Bit 6	-	Reserved	Reserved	RW	Reserved		0
Bit 5	-	Reserved	Reserved	RW	Reserved		0
Bit 4	-	Reserved	Reserved	RW	Reserved		0
Bit 3	-	DOT96SS FS3	DOT96 Freq Select Bit 3	RW	See Table 2: DOT Frequency Selection Table		0
Bit 2	-	DOT96SS FS2	DOT96 Freq Select Bit 2	RW			0
Bit 1	-	DOT96SS FS1	DOT96 Freq Select Bit 1	RW			0
Bit 0	-	DOT96SS FS0	DOT96 Freq Select Bit 0	RW			0

SMBus Table: RMII Strength Control Register

Byte 4	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	24	RMII_7 Str	RMII_7 Strength Control	RW	1-Load (1X)	2-Loads (2X)	0
Bit 6	25	RMII_6 Str	RMII_6 Strength Control	RW	1-Load (1X)	2-Loads (2X)	0
Bit 5	28	RMII_5 Str	RMII_5 Strength Control	RW	1-Load (1X)	2-Loads (2X)	0
Bit 4	29	RMII_4 Str	RMII_4 Strength Control	RW	1-Load (1X)	2-Loads (2X)	0
Bit 3	32	RMII_3 Str	RMII_3 Strength Control	RW	1-Load (1X)	2-Loads (2X)	0
Bit 2	33	RMII_2 Str	RMII_2 Strength Control	RW	1-Load (1X)	2-Loads (2X)	0
Bit 1	36	RMII_1 Str	RMII_1 Strength Control	RW	1-Load (1X)	2-Loads (2X)	0
Bit 0	37	RMII_0 Str	RMII_0 Strength Control	RW	1-Load (1X)	2-Loads (2X)	0

SMBus Table: 32.768KHz, 25Mhz and 33.33MHz Strength Control Register

Byte 5	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	-	Reserved	Reserved	RW	Reserved		0
Bit 6	-	Reserved	Reserved	RW	Reserved		0
Bit 5	22	33.33MHz Str	33.33MHz Strength Control	RW	1-Load (1X)	2-Loads (2X)	1
Bit 4	17	25MHz_1 Str	25MHz_1 Strength Control	RW	1-Load (1X)	2-Loads (2X)	1
Bit 3	16	25MHz_0 Str	25MHz_1 Strength Control	RW	1-Load (1X)	2-Loads (2X)	1
Bit 2	13	32.768kHz Str	32.768kHz Strength Control	RW	1-Load (1X)	2-Loads (2X)	1
Bit 1	-	Reserved	Reserved	RW	Reserved		0
Bit 0	-	Reserved	Reserved	RW	Reserved		0

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SMBus Table: Vendor & Revision ID Register

Byte 6	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	-	RID3	REVISION ID	R	-	-	X
Bit 6	-	RID2		R	-	-	X
Bit 5	-	RID1		R	-	-	X
Bit 4	-	RID0		R	-	-	X
Bit 3	-	VID3	VENDOR ID	R	-	-	0
Bit 2	-	VID2		R	-	-	0
Bit 1	-	VID1		R	-	-	0
Bit 0	-	VID0		R	-	-	1

SMBus Table: Device ID

Byte 7	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	-	Device ID 7 (MSB)	Device ID	RW	Reserved		0
Bit 6	-	Device ID 6		RW	Reserved		0
Bit 5	-	Device ID 5		RW	Reserved		1
Bit 4	-	Device ID 4		RW	Reserved		0
Bit 3	-	Device ID 3		RW	Reserved		0
Bit 2	-	Device ID 2		RW	Reserved		0
Bit 1	-	Device ID 1		RW	Reserved		1
Bit 0	-	Device ID 0 (LSB)		RW	Reserved		0

SMBus Table: Byte Count Register

Byte 8	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	-	BC7	Writing to this register configures how many bytes will be read back.	RW	-	-	0
Bit 6	-	BC6		RW	-	-	0
Bit 5	-	BC5		RW	-	-	0
Bit 4	-	BC4		RW	-	-	0
Bit 3	-	BC3		RW	-	-	1
Bit 2	-	BC2		RW	-	-	0
Bit 1	-	BC1		RW	-	-	0
Bit 0	-	BC0		RW	-	-	1

SMBus Table: Reserved

Byte 9	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	Reserved						0
Bit 6	Reserved						0
Bit 5	Reserved						0
Bit 4	Reserved						0
Bit 3	Reserved						0
Bit 2	Reserved						0
Bit 1	Reserved						0
Bit 0	Reserved						0

SMBus Table: PLLs M/N Programming Enable Register

Byte 10	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	-	M/N_EN	PLLs M/N Programming Enable	RW	Disable	Enable	0
Bit 6	Reserved						0
Bit 5	Reserved						0
Bit 4	Reserved						0
Bit 3	Reserved						0
Bit 2	Reserved						0
Bit 1	Reserved						0
Bit 0	Reserved						0

SMBus Table: CPU PLL VCO Frequency Control Register

Byte 11	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	-	N Div8	N Divider Prog bit 8	RW	The decimal representation of M and N Divier in Byte 11 and 12 will configure the VCO frequency. Default at power up = latch-in or Byte 0 Rom table. VCO Frequency = 14.318 x [NDiv(9:0)+8] / [MDiv(5:0)+2]		X
Bit 6	-	N Div 9	N Divider Prog bit 9	RW			X
Bit 5	-	M Div5	M Divider Programming bits	RW			X
Bit 4	-	M Div4		RW			X
Bit 3	-	M Div3		RW			X
Bit 2	-	M Div2		RW			X
Bit 1	-	M Div1		RW			X
Bit 0	-	M Div0		RW			X

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SMBus Table: CPU PLL VCO Frequency Control Register

Byte 12	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	-	N Div7	N Divider Programming b(7:0)	RW	The decimal representation of M and N Divier in Byte 11 and 12 will configure the VCO frequency. Default at power up = latch-in or Byte 0 Rom table. VCO Frequency = 14.318 x [NDiv(9:0)+8] / [MDiv(5:0)+2]		X
Bit 6	-	N Div6		RW			X
Bit 5	-	N Div5		RW			X
Bit 4	-	N Div4		RW			X
Bit 3	-	N Div3		RW			X
Bit 2	-	N Div2		RW			X
Bit 1	-	N Div1		RW			X
Bit 0	-	N Div0		RW			X

SMBus Table: CPU PLL Spread Spectrum Control Register

Byte 13	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	-	SSP7	Spread Spectrum Programming b(7:0)	RW	These Spread Spectrum bits in Byte 13 and 14 will program the spread pecentage. It is recommended to use ICS Spread % table for spread programming.		X
Bit 6	-	SSP6		RW			X
Bit 5	-	SSP5		RW			X
Bit 4	-	SSP4		RW			X
Bit 3	-	SSP3		RW			X
Bit 2	-	SSP2		RW			X
Bit 1	-	SSP1		RW			X
Bit 0	-	SSP0		RW			X

SMBus Table: CPU PLL Spread Spectrum Control Register

Byte 14	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	Reserved						0
Bit 6	-	SSP14	Spread Spectrum Programming b(14:8)	RW	These Spread Spectrum bits in Byte 13 and 14 will program the spread pecentage. It is recommended to use ICS Spread % table for spread programming.		X
Bit 5	-	SSP13		RW			X
Bit 4	-	SSP12		RW			X
Bit 3	-	SSP11		RW			X
Bit 2	-	SSP10		RW			X
Bit 1	-	SSP9		RW			X
Bit 0	-	SSP8		RW			X

SMBus Table: DOT PLL VCO Frequency Control Register

Byte 15	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	-	N Div8	N Divider Prog bit 8	RW	The decimal representation of M and N Divier in Byte 17 and 18 will configure the VCO frequency. Default at power up = Byte 0 Rom table. VCO Frequency = 14.318 x [NDiv(9:0)+8] / [MDiv(5:0)+2]		X
Bit 6	-	N Div9	N Divider Prog bit 9	RW			X
Bit 5	-	M Div5	M Divider Programming bits	RW			X
Bit 4	-	M Div4		RW			X
Bit 3	-	M Div3		RW			X
Bit 2	-	M Div2		RW			X
Bit 1	-	M Div1		RW			X
Bit 0	-	M Div0		RW			X

SMBus Table: DOT PLL VCO Frequency Control Register

Byte 16	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	-	N Div7	N Divider Programming b(7:0)	RW	The decimal representation of M and N Divier in Byte 17 and 18 will configure the VCO frequency. Default at power up = Byte 0 Rom table. VCO Frequency = 14.318 x [NDiv(9:0)+8] / [MDiv(5:0)+2]		X
Bit 6	-	N Div6		RW			X
Bit 5	-	N Div5		RW			X
Bit 4	-	N Div4		RW			X
Bit 3	-	N Div3		RW			X
Bit 2	-	N Div2		RW			X
Bit 1	-	N Div1		RW			X
Bit 0	-	N Div0		RW			X

SMBus Table: DOT PLL Spread Spectrum Control Register

Byte 17	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	-	SSP7	Spread Spectrum Programming b(7:0)	RW	These Spread Spectrum bits in Byte 19 and 20 will program the spread pecentage. It is recommended to use ICS Spread % table for spread programming.		X
Bit 6	-	SSP6		RW			X
Bit 5	-	SSP5		RW			X
Bit 4	-	SSP4		RW			X
Bit 3	-	SSP3		RW			X
Bit 2	-	SSP2		RW			X
Bit 1	-	SSP1		RW			X
Bit 0	-	SSP0		RW			X

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SMBus Table: DOT PLL Spread Spectrum Control Register

Byte 18	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7			Reserved				0
Bit 6	-	SSP14	Spread Spectrum Programming b(14:8)	RW	These Spread Spectrum bits in Byte 19 and 20 will program the spread pecentage. It is recommended to use ICS Spread % table for spread programming.		X
Bit 5	-	SSP13		RW			X
Bit 4	-	SSP12		RW			X
Bit 3	-	SSP11		RW			X
Bit 2	-	SSP10		RW			X
Bit 1	-	SSP9		RW			X
Bit 0	-	SSP8		RW			X

SMBus Table: Reserved

Byte 19	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7			Reserved				0
Bit 6			Reserved				0
Bit 5			Reserved				0
Bit 4			Reserved				0
Bit 3			Reserved				0
Bit 2			Reserved				0
Bit 1			Reserved				0
Bit 0			Reserved				0

SMBus Table: Reserved

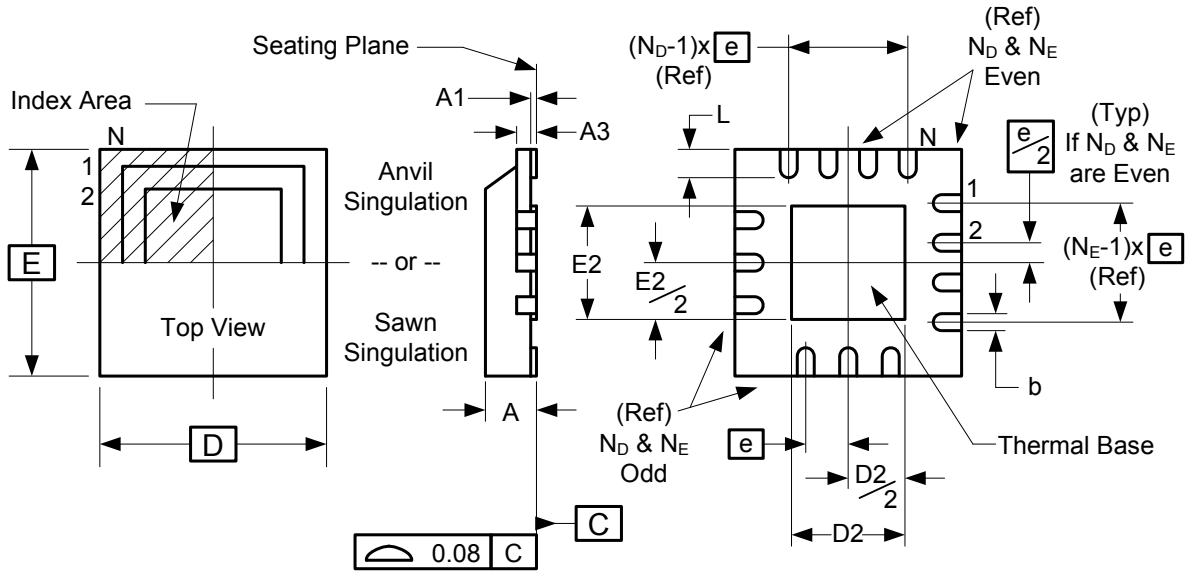
Byte 20	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7			Reserved				0
Bit 6			Reserved				0
Bit 5			Reserved				0
Bit 4			Reserved				0
Bit 3			Reserved				0
Bit 2			Reserved				0
Bit 1			Reserved				0
Bit 0			Reserved				0

SMBus Table: Reserved

Byte 21	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7			Reserved				0
Bit 6			Reserved				0
Bit 5			Reserved				0
Bit 4			Reserved				0
Bit 3			Reserved				0
Bit 2			Reserved				0
Bit 1			Reserved				0
Bit 0			Reserved				0

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Package Outline and Package Dimensions (40-pin MLF)



	Millimeters	
Symbol	**Min**	**Max**
A	0.8	1.0
A1	0	0.05
A3	0.25 Reference	
b	0.18	0.3
e	0.50 BASIC	
D x E BASIC	6.00 x 6.00	
D2 MIN./MAX.	2.75	3.00
E2 MIN./MAX.	2.75	3.00
L MIN./MAX.	0.3	0.5
N_D	10	
N_E	10	

Ordering Information

Part / Order Number	Shipping Packaging	Package	Temperature
9FGP202AKLF	Trays	40-pin MLF	0 to +70°C
9FGP202AKLFT	Tape and Reel	40-pin MLF	0 to +70°C

"LF" suffix to the part number are the Pb-Free configuration and are RoHS compliant.

"A" is the device revision designator (will not correlate with the datasheet revision).

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Revision History

Rev.	Issue Date	Who	Description	Page #
D	7/5/2011	D. Chan	Updated datasheet template	

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