64-PIN CK505 W/FULLY INTEGRATED VOLTAGE REGULATOR

ICS9LPR501

Recommended Application:

CK505 compliant clock with fully integrated voltage regulator, PCIe Gen 1 compliant

Output Features:

- 2 - CPU differential low power push-pull pairs
- 10 - SRC differential low power push-pull pairs
- 1 - CPU/SRC selectable differential low power push-pull pair
- 1 - SRC/DOT selectable differential low power push-pull pair
- 5 - PCI, 33MHz
- 1 - PCI_F, 33MHz free running
- 1 - USB, 48MHz
- 1 - REF, 14.318MHz

Key Specifications:

- CPU outputs cycle-cycle jitter < 85ps
- SRC output cycle-cycle jitter < 125ps
- PCI outputs cycle-cycle jitter < 250ps
- +/- 100ppm frequency accuracy on CPU & SRC clocks

Features/Benefits:

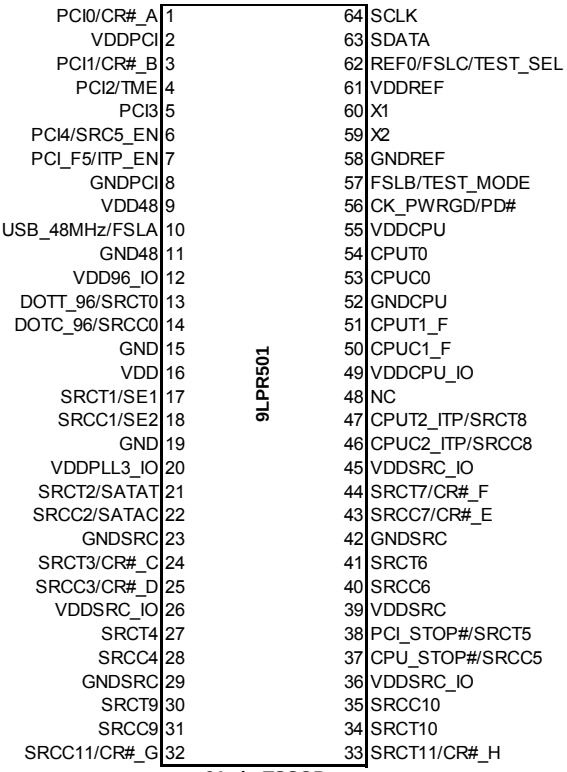
- Does not require external pass transistor for voltage regulator
- Supports spread spectrum modulation, default is 0.5% down spread
- Uses external 14.318MHz crystal, external crystal load caps are required for frequency tuning
- One differential push-pull pair selectable between SRC and two single-ended outputs

Table 1: CPU Frequency Select Table

FS_LC[2] B0b7	FS_LB[1] B0b6	FS_LA[1] B0b5	CPU MHz	SRC MHz	PCI MHz	REF MHz	USB MHz	DOT MHz
0	0	0	266.66	100.00	33.33	14.318	48.00	96.00
0	0	1	133.33					
0	1	0	200.00					
0	1	1	166.66					
1	0	0	333.33					
1	0	1	100.00					
1	1	0	400.00					
1	1	1	Reserved					

1. FS_LA and FS_LB are low-threshold inputs.Please see V_{IL_FS} and V_{IH_FS} specifications in the Input/Supply/Common Output Parameters Table for correct values. Also refer to the Test Clarification Table.
2. FS_LC is a three-level input. Please see the V_{IL_FS} and V_{IH_FS} specifications in the Input/Supply/Common Output Parameters Table for correct values.

Pin Configuration



64-pin TSSOP

* Internal Pull-Up Resistor

** Internal Pull-Down Resistor

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Pin Description

PIN #	PIN NAME	TYPE	DESCRIPTION
1	PCI0/CR#_A	I/O	3.3V PCI clock output or Clock Request control A for either SRC0 or SRC2 pair The power-up default is PCI0 output, but this pin may also be used as a Clock Request control of SRC pair 0 or SRC pair 2 via SMBus. Before configuring this pin as a Clock Request Pin, the PCI output must first be disabled in byte 2, bit 0 of SMBus address space . After the PCI output is disabled (high-Z), the pin can then be set to serve as a Clock Request pin for either SRC pair 2 or pair 0 using the CR#_A_EN bit located in byte 5 of SMBUs address space. Byte 5, bit 7 0 = PCI0 enabled (default) 1= CR#_A enabled. Byte 5, bit 6 controls whether CR#_A controls SRC0 or SRC2 pair Byte 5, bit 6 0 = CR#_A controls SRC0 pair (default), 1= CR#_A controls SRC2 pair
2	VDDPCI	PWR	Power supply pin for the PCI outputs, 3.3V nominal
3	PCI1/CR#_B	I/O	3.3V PCI clock output/Clock Request control B for either SRC1 or SRC4 pair The power-up default is PCI1 output, but this pin may also be used as a Clock Request control of SRC pair 1 or SRC pair 4 via SMBus. Before configuring this pin as a Clock Request Pin, the PCI output must first be disabled in byte 2, bit 1 of SMBus address space . After the PCI output is disabled (high-Z), the pin can then be set to serve as a Clock Request pin for either SRC pair 1 or pair 4 using the CR#_B_EN bit located in byte 5 of SMBUs address space. Byte 5, bit 5 0 = PCI1 enabled (default) 1= CR#_B enabled. Byte 5, bit 6 controls whether CR#_B controls SRC1 or SRC4 pair Byte 5, bit 4 0 = CR#_B controls SRC1 pair (default) 1= CR#_B controls SRC4 pair
4	PCI2/TME	I/O	3.3V PCI clock output / Trusted Mode Enable (TME) Latched Input. This pin is sampled on power-up as follows 0 = Overclocking of CPU and SRC Allowed 1 = Overclocking of CPU and SRC NOT allowed After being sampled on power-up, this pin becomes a 3.3V PCI Output
5	PCI3	OUT	3.3V PCI clock output.
6	PCI4/SRC5_EN	I/O	3.3V PCI clock output / SRC5 pair or PCI_STOP#/CPU_STOP# enable strap. On powerup, the logic value on this pin determines if the SRC5 pair is enabled or if CPU_STOP#/PCI_STOP# is enabled (pins 37 and 38). The latched value controls the pin function on pins 37 and 38 as follows 0 = PCI_STOP#/CPU_STOP# 1 = SRC5/SRC5#
7	PCI_F5/ITP_EN	I/O	Free running PCI clock output and ITP/SRC8 enable strap. This output is not affected by the state of the PCI_STOP# pin. On powerup, the state of this pin determines whether pins 38 and 39 are an ITP or SRC pair. 0 =SRC8/SRC8# 1 = ITP/ITP#
8	GNDPCI	PWR	Ground for PCI clocks.
9	VDD48	PWR	Power supply for USB clock, nominal 3.3V.
10	USB_48MHz/FSLA	I/O	Fixed 48MHz USB clock output. 3.3V./ 3.3V tolerant input for CPU frequency selection. Refer to input electrical characteristics for Vil_FS and Vih_FS values.
11	GND48	PWR	Ground pin for the 48MHz outputs.
12	VDD96_IO	PWR	Power supply for DOT96 outputs, VDD96_IO is 1.05 to 3.3V with +/-5% tolerance
13	DOTT_96/SRCT0	OUT	True clock of SRC or DOT96. The power-up default function is SRC0. After powerup, this pin function may be changed to DOT96 via SMBus Byte 1, bit 7 as follows: 0= SRC0 1=DOT96
14	DOTC_96/SRCC0	OUT	Complement clock of SRC or DOT96. The power-up default function is SRC0#. After powerup, this pin function may be changed to DOT96# via SMBus Byte 1, bit 7 as follows 0= SRC0# 1=DOT96#
15	GND	PWR	Ground pin for the DOT96 clocks.
16	VDD	PWR	Power supply for SRC / SE1 and SE2 clocks, 3.3V nominal.

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Pin Description (continued)

PIN #	PIN NAME	TYPE	DESCRIPTION
17	SRCT1/SE1	OUT	True clock of differential SRC1 clock pair / 3.3V single-ended output. The powerup default is 100 MHz SRC, -0.5% downspread. The pin function may be changed via SMBus B1b[4:1]
18	SRCC1/SE2	OUT	Complement clock of differential SRC1 clock pair / 3.3V single-ended output. The powerup default is 100 MHz SRC, -0.5% downspread. The pin function may be changed via SMBus B1b[4:1]
19	GND	PWR	Ground pin for SRC / SE1 and SE2 clocks, PLL3.
20	VDDPLL3_IO	PWR	Power supply for PLL3 output. VDDPLL3_IO is 1.05 to 3.3V with +/-5% tolerance
21	SRCT2/SATAT	OUT	True clock of differential SRC/SATA clock pair.
22	SRCC2/SATAC	OUT	Complement clock of differential SRC/SATA clock pair.
23	GNDSRC	PWR	Ground pin for SRC clocks.
24	SRCT3/CR#_C	I/O	True clock of differential SRC clock pair/ Clock Request control C for either SRC0 or SRC2 pair The power-up default is SRCCLK3 output, but this pin may also be used as a Clock Request control of SRC pair 0 or SRC pair 2 via SMBus. Before configuring this pin as a Clock Request Pin, the SRC3 output must first be disabled in byte 4, bit 7 of SMBus address space . After the SRC3 output is disabled, the pin can then be set to serve as a Clock Request pin for either SRC pair 2 or pair 0 using the CR#_C_EN bit located in byte 5 of SMBUs address space. Byte 5, bit 3 0 = SRC3 enabled (default) 1= CR#_C enabled. Byte 5, bit 2 controls whether CR#_C controls SRC0 or SRC2 pair Byte 5, bit 2 0 = CR#_C controls SRC0 pair (default), 1= CR#_C controls SRC2 pair
25	SRCC3/CR#_D	I/O	Complementary clock of differential SRC clock pair/ Clock Request control D for either SRC1 or SRC4 pair The power-up default is SRCCLK3 output, but this pin may also be used as a Clock Request control of SRC pair 1 or SRC pair 4 via SMBus. Before configuring this pin as a Clock Request Pin, the SRC3 output must first be disabled in byte 4, bit 7 of SMBus address space . After the SRC3 output is disabled, the pin can then be set to serve as a Clock Request pin for either SRC pair 1 or pair 4 using the CR#_D_EN bit located in byte 5 of SMBUs address space. Byte 5, bit 1 0 = SRC3 enabled (default) 1= CR#_D enabled. Byte 5, bit 0 controls whether CR#_D controls SRC1 or SRC4 pair Byte 5, bit 0 0 = CR#_D controls SRC1 pair (default), 1= CR#_D controls SRC4 pair
26	VDDSRC_IO	PWR	Power supply for SRC clocks. VDDSRC_IO is 1.05 to 3.3V with +/-5% tolerance
27	SRCT4	I/O	True clock of differential SRC clock pair 4
28	SRCC4	I/O	Complement clock of differential SRC clock pair 4
29	GNDSRC	PWR	Ground pin for SRC clocks.
30	SRCT9	OUT	True clock of differential SRC clock pair.
31	SRCC9	OUT	Complement clock of differential SRC clock pair.
32	SRCC11/CR#_G	I/O	SRC11 complement /Clock Request control for SRC9 pair The power-up default is SRC11#, but this pin may also be used as a Clock Request control of SRC9 via SMBus. Before configuring this pin as a Clock Request Pin, the SRC11 output pair must first be disabled in byte 3, bit 7 of SMBus configuration space After the SRC11 output is disabled (high-Z), the pin can then be set to serve as a Clock Request for SRC9 pair using byte 6, bit 5 of SMBus configuration space **Byte 6, bit 5** 0 = SRC11# enabled (default) 1= CR#_G controls SRC9

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Pin Description (Continued)

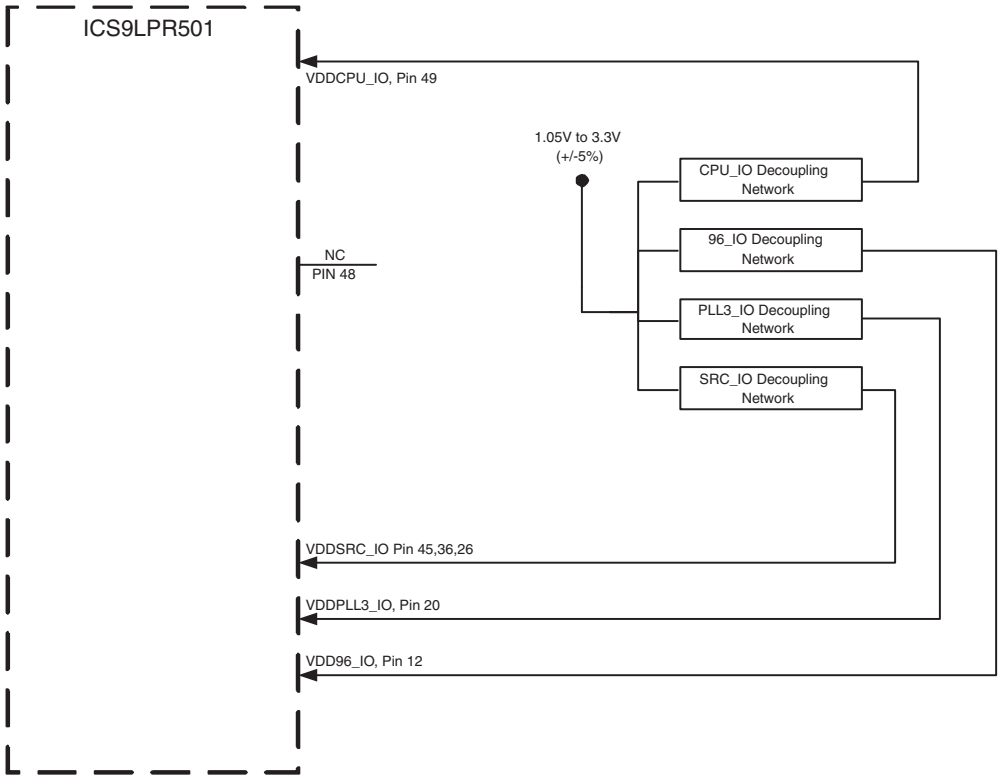
PIN #	PIN NAME	TYPE	DESCRIPTION
33	SRCT11/CR#_H	I/O	SRC11 true or Clock Request control H for SRC10 pair The power-up default is SRC11, but this pin may also be used as a Clock Request control of SRC10 via SMBus. Before configuring this pin as a Clock Request Pin, the SRC11 output pair must first be disabled in byte 3 bit 7 of SMBus configuration space After the SRC11 output is disabled (high-Z), the pin can then be set to serve as a Clock Request for SRC10 pair using byte 6, bit 4 of SMBus configuration space Byte 6, bit 4 0 = SRC11 enabled (default) 1= CR#_H controls SRC10.
34	SRCT10	OUT	True clock of differential SRC clock pair.
35	SRCC10	OUT	Cpmplement clock of differential SRC clock pair.
36	VDDSRC_IO	PWR	Power supply for SRC outputs. VDDSRC_IO is 1.05 to 3.3V with +/-5% tolerance
37	CPU_STOP#/SRCC5	I/O	Stops all CPU Clocks, except those set to be free running clocks / Complement clock of differential SRC pair. The function of this pin is set up by the power-up strap on pin 6, PCI4/SRC5_EN. The logic value sampled on pin 6 at power-up sets the function as follows: 0= CPU_STOP# 1 = SRC5 In AMT mode 3 bits are shifted in from the ICH to set the FSC, FSB, FSA values
38	PCI_STOP#/SRCT5	I/O	Stops all PCI Clocks, except those set to be free running clocks / Complement clock of differential SRC pair. The function of this pin is set up by the power-up strap on pin 6, PCI4/SRC5_EN. The logic value sampled on pin 6 at power-up sets the function as follows: 0= PCI_STOP# 1 = SRC5# In AMT mode, this pin is a clock input which times the FSC, FSB, FSA bits shifted in on pin 37.
39	VDDSRC	PWR	VDD pin for SRC internal circuits, 3.3V nominal
40	SRCC6	OUT	Complement clock of low power differential SRC clock pair.
41	SRCT6	OUT	True clock of low power differential SRC clock pair.
42	GNDSRC	PWR	Ground for SRC clocks
43	SRCC7/CR#_E	I/O	SRC7 complement or Clock Request control E for SRC6 pair The power-up default is SRC7#, but this pin may also be used as a Clock Request control of SRC6 via SMBus. Before configuring this pin as a Clock Request Pin, the SRC7 output pair must first be disabled in byte 3, bit 3 of SMBus configuration space . After the SRC output is disabled (high-Z), the pin can then be set to serve as a Clock Request for SRC6 pair using byte 6, bit 7 of SMBus configuration space **Byte 6, bit 7** 0 = SRC7# enabled (default) 1= CR#_E controls SRC6.
44	SRCT7/CR#_F	I/O	SRC7 true or Clock Request control 8 for SRC8 pair The power-up default is SRC7, but this pin may also be used as a Clock Request control of SRC8 via SMBus. Before configuring this pin as a Clock Request Pin, the SRC7 output pair must first be disabled in byte 3, bit 3 of SMBus configuration space After the SRC output is disabled (high-Z), the pin can then be set to serve as a Clock Request for SRC8 pair using byte 6, bit 6 of SMBus configuration space **Byte 6, bit 6** 0 = SRC7# enabled (default) 1 = CR#_F controls SRC8.
45	VDDSRC_IO	PWR	Power supply for SRC outputs. VDDSRC_IO is 1.05 to 3.3V with +/-5% tolerance
46	CPUC2_ITP/SRCC8	OUT	Complement clock of low power differential CPU2/Complement clock of differential SRC pair. The function of this pin is determined by the latched input value on pin 7, PCIF5/ITP_EN on powerup. The function is as follows: Pin 7 latched input Value 0 = SRC8# 1 = ITP#
47	CPUT2_ITP/SRCT8	OUT	True clock of low power differential CPU2/True clock of differential SRC pair. The function of this pin is determined by the latched input value on pin 7, PCIF5/ITP_EN on powerup. The function is as follows: Pin 7 latched input Value 0 = SRC8 1 = ITP
48	NC	N/A	No Connect

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Pin Description (Continued)

PIN #	PIN NAME	TYPE	DESCRIPTION
49	VDDCPU_IO	PWR	Supply for CPU outputs. VDDCPU_IO is 1.05 to 3.3V with +/-5% tolerance
50	CPUC1_F	OUT	Complement clock of low power differenatial CPU clock pair. This clock will be free-running during iAMT.
51	CPUT1_F	OUT	True clock of low power differential CPU clock pair. This clock will be free-running during iAMT.
52	GNDCPU	PWR	Ground Pin for CPU Outputs
53	CPUC0	OUT	Complement clock of low power differential CPU clock pair.
54	CPUT0	OUT	True clock of low power differential CPU clock pair.
55	VDDCPU	PWR	Power Supply 3.3V nominal.
56	CK_PWRGD/PD#	IN	Notifies CK505 to sample latched inputs, or iAMT entry/exit, or PWRDWN# mode
57	FSLB/TEST_MODE	IN	3.3V tolerant input for CPU frequency selection. Refer to input electrical characteristics for Vil_FS and Vih_FS values. TEST_MODE is a real time input to select between Hi-Z and REF/N divider mode while in test mode. Refer to Test Clarification Table.
58	GNDREF	PWR	Ground pin for crystal oscillator circuit
59	X2	OUT	Crystal output, nominally 14.318MHz.
60	X1	IN	Crystal input, Nominally 14.318MHz.
61	VDDREF	PWR	Power pin for the REF outputs, 3.3V nominal.
62	REF0/FSLC/TEST_SEL	I/O	3.3V 14.318MHz reference clock/3.3V tolerant low threshold input for CPU frequency selection. Refer to input electrical characteristics for Vil_FS and Vih_FS values/ TEST_SEL: 3-level latched input to enable test mode. Refer to Test Clarification Table.
63	SDATA	I/O	Data pin for SMBus circuitry, 5V tolerant.
64	SCLK	IN	Clock pin of SMBus circuitry, 5V tolerant.

Fully Integrated Regulator Connection for Desktop/Mobile Applications

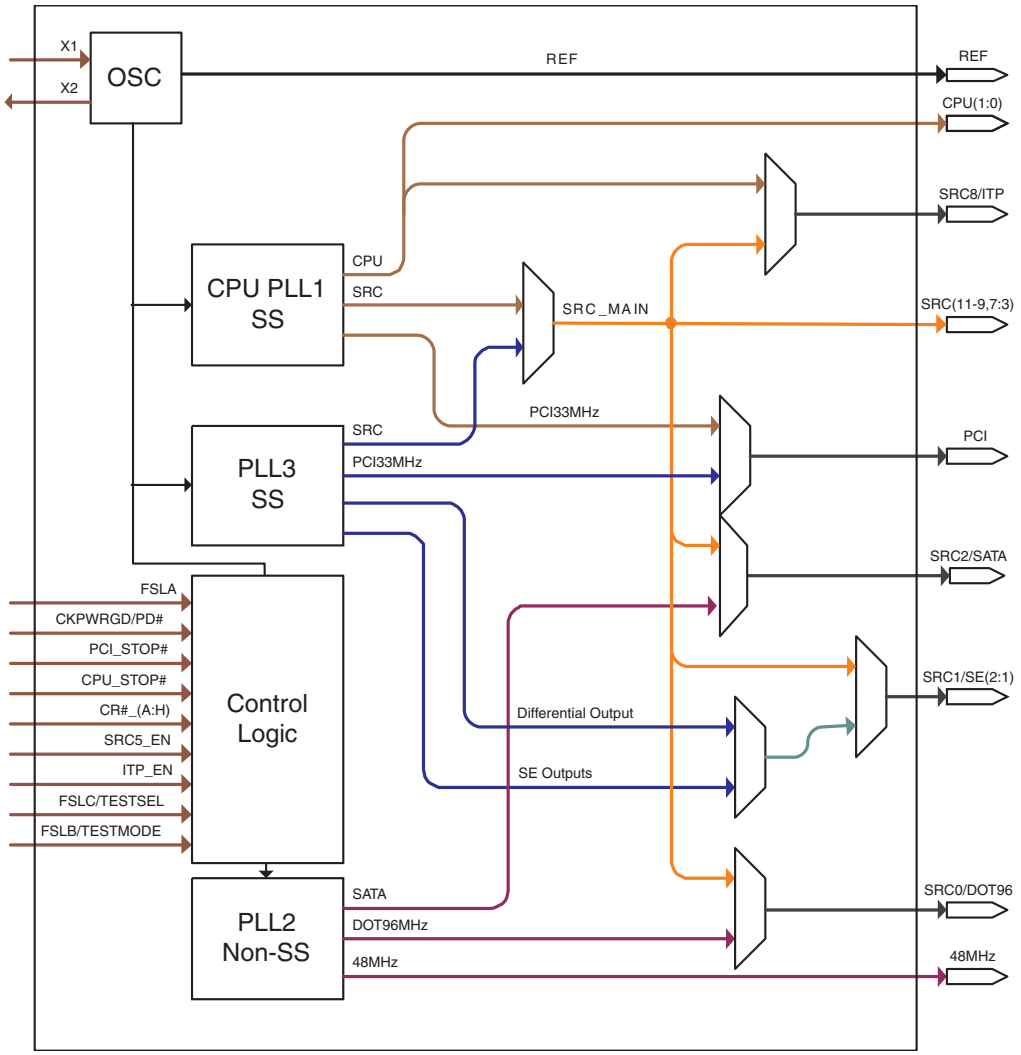


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General Description

ICS9LPR501 follows Intel CK505 Yellow Cover specification. This clock synthesizer provides a single chip solution for next generation Intel processors and Intel chipsets. **ICS9LPR501** is driven with a 14.318MHz crystal. It also provides a tight ppm accuracy output for Serial ATA and PCI-Express support.

Functional Block Diagram



Power Groups

Pin Number		Description	
VDD	GND		
49	52	CPUCLK	Low power outputs
55	52	Master Clock, Analog	
26, 36, 45	23, 29, 42	SRCCLK	Low power outputs
39	23, 29, 42		PLL 1
20	19	PLL3/SE	Low power outputs
16	19		PLL 3
12	11	DOT 96Mhz	Low power outputs
9	11	USB 48	
61	58	Xtal, REF	
2	8	PCICLK	

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Absolute Maximum Ratings - DC Parameters

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	Notes
Maximum Supply Voltage	VDDxxx	Supply Voltage			4.6	V	7
Maximum Supply Voltage	VDDxxx_IO	Low-Voltage Differential I/O Supply			3.8	V	7
Maximum Input Voltage	V_{IH}	3.3V Inputs			4.6	V	4,5,7
Minimum Input Voltage	V_{IL}	Any Input	GND - 0.5			V	4,7
Case Temperature	Tcase				115	°C	
Thermal Resistance from Die to Ambient Air	JA				32.5	°C/W	
Thermal Resistance from Die to Package Case	JC				68.2	°C/W	
Storage Temperature	Ts	-	-65		150	°C	4,7
Input ESD protection	ESD prot	Human Body Model	2000			V	6,7

[1]Guaranteed by design and characterization, not 100% tested in production.

[2] Operation under these conditions is neither implied, nor guaranteed.

[3] Maximum input voltage is not to exceed VDD

AC Electrical Characteristics - Low Power Differential Outputs

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	NOTES
Rising Edge Slew Rate	tSLR	Averaging on	2.5	3.35	4	V/ns	2, 3
Falling Edge Slew Rate	tFLR	Averaging on	2.5	3.30	4	V/ns	2, 3
Slew Rate Variation	tSLVAR	Averaging on			20	%	1, 10
Differential Voltage Swing	VSWING	Averaging off	300			mV	2
Crossing Point Voltage	VXABS	Averaging off	300	405.5	550	mV	1,4,5
Crossing Point Variation	VXABSVAR	Averaging off		60	140	mV	1,4,9
Maximum Output Voltage	VHIGH	Averaging off		894	1150	mV	1,7
Minimum Output Voltage	VLOW	Averaging off	-300	59.5		mV	1,8
Duty Cycle	DCYC	Averaging on	45	51.0	55	%	2
CPU[1:0] Skew	CPUSKEW10	Differential Measurement		47	100	ps	1
CPU[2_ITP:0] Skew	CPUSKEW20	Differential Measurement		125	150	ps	1
SRC[10:0] Skew	SRCSKEW	Differential Measurement		704	3000	ps	1,6

NOTES on DIF Output AC Specs: (unless otherwise noted, guaranteed by design and characterization, not 100% tested in production).

[1]Measurement taken for single ended waveform on a component test board (not in system)

[2] Measurement taken from differential waveform on a component test board. (not in system)

[3] Slew rate emastured through V_swing voltage range centered about differential zero

[4] Vcross is defined at the voltage where Clock = Clock#, measured on a component test board (not in system)

[5] Only applies to the differential rising edge (Clock rising, Clock# falling)

[6] Total distributed intentional SRC to SRC skew.

[7] The max voltage including overshoot.

[8] The min voltage including undershoot.

[9] The total variation of all Vcross measurements in any particular system. Note this is a subset of V_cross min/mas (V_Cross absolute) allowed. The intent is to limit Vcross induced modulation by setting C_cross_delta to be smaller than V_Cross absolute.

[10] Matching applies to rising edge rate for Clock and falling edge rate for Clock#. It is measured using a +/-75mV window centered on the average cross point where Clock rising meets Clock# falling. The median cross point is used to calculate the voltage thresholds the oscilloscope is to use for the edge rate calculations.

Clock Jitter Specs - Low Power Differential Outputs

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	NOTES
CPU Jitter - Cycle to Cycle	CPUJC2C	Differential Measurement		58.1	85	ps	1
SRC Jitter - Cycle to Cycle	SRCJC2C	Differential Measurement		36.2	125	ps	1,2
SATA Jitter - Cycle to Cycle	SATAJC2C	Differential Measurement		46.8	125	ps	1
DOT Jitter - Cycle to Cycle	DOTJC2C	Differential Measurement		73.0	250	ps	1

NOTES on DIF Output Jitter: (unless otherwise noted, guaranteed by design and characterization, not 100% tested in production).

[1]JItter specs are specified as measured on a clock characterization board. System designers need to take special care not to use these numbers, as the in-system performance will be somewhat degraded. The receiver EMTS (chispet or CPU) will have the receiver jitter specs as measured in a real system.

[2] Phase jitter requirement: The SRC outputs will meet the reference clock jitter requiremernts from the PCI Express Gen1 Base Spec. The test is performed on a component test board under quiet conditions with all outputs on. Jitter analysis is performed using the standardized tool provided by the PCI SIG.

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Electrical Characteristics - Input/Supply/Common Output DC Parameters

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	Notes
Ambient Operating Temp	Tambient	-	0	25	70	°C	
Supply Voltage	VDDxxx	Supply Voltage	3.135	3.3	3.465	V	
Supply Voltage	VDDxxx_IO	Low-Voltage Differential I/O Supply	0.9975	1.05	3.465	V	10
Input High Voltage	V_{IHSE}	Single-ended 3.3V inputs	2.2		V_{DD} + 0.3	V	3
Input Low Voltage	V_{ILSE}	Single-ended 3.3V inputs	V_{SS} - 0.3		0.8	V	3
Low Threshold Input- High Voltage FSC = Test Mode	$V_{IH_FSC_TEST}$	3.3 V +/-5%	2			V	8
Low Threshold Input- FSC = '1' Voltage	$V_{IH_FSC_1}$	3.3 V +/-5%	0.7		1.5	V	8
Low Threshold Input- FSA,FSB = '1' Voltage	$V_{IH_FSAB_1}$	3.3 V +/-5%	0.7			V	
Low Threshold Input- Low Voltage	V_{IL_FS}	3.3 V +/-5%	V_{SS} - 0.3		0.35	V	
Input Leakage Current	I_{IN}	$V_{IN} = V_{DD}$, V_{IN} = GND	-5		5	uA	2
Input Leakage Current	I_{INRES}	Inputs with pull up or pull down resistors $V_{IN} = V_{DD}$, V_{IN} = GND	-200		200	uA	
Output High Voltage	V_{OHSE}	Single-ended outputs, I_{OH} = -1mA	2.4			V	
Output Low Voltage	V_{OLSE}	Single-ended outputs, I_{OL} = 1 mA			0.4	V	
Operating Supply Current	$I_{DDOP3.3}$	Full Active, C_L = Full load; IDD 3.3V		135	200	mA	
	I_{DDOPIO}	Full Active, C_L = Full load; IDD IO		72	80	mA	
iAMT Mode Current	$I_{DDiAMT3.3}$	M1 mode, 3.3V Rail		53	65	mA	
	$I_{DDiAMTIO}$	M1 Mode, IO Rail		7	10	mA	
Powerdown Current	$I_{DDPD3.3}$	Power down mode, 3.3V Rail, B63b0 = '1'		22	25	mA	
	I_{DDPDIO}	Power down mode, IO Rail		0.01	0.1	mA	
Input Frequency	F_i	V_{DD} = 3.3 V		14.31818	15	MHz	
Pin Inductance	L_{pin}				7	nH	
Input Capacitance	C_{IN}	Logic Inputs	1.5		5	pF	
	C_{OUT}	Output pin capacitance			6	pF	
	C_{INX}	X1 & X2 pins			6	pF	
Clk Stabilization	T_{STAB}	From VDD Power-Up or de-assertion of PD to 1st clock		1.2	1.8	ms	
Tdrive_CR_off	$T_{DRCROFF}$	Output stop after CR deasserted			400	ns	
Tdrive_CR_on	T_{DRCRON}	Output run after CR asserted			0	us	
Tdrive_CPU	T_{DRSRC}	CPU output enable after PCI_STOP# de-assertion			10	ns	
Tfall_SE	T_{FALL}	Fall/rise time of all 3.3V control inputs from 20-80%. Inputs must be monotonic			10	ns	1
Trise_SE	T_{RISE}				10	ns	1
SMBus Voltage	V_{DD}		2.7		5.5	V	
Low-level Output Voltage	V_{OLSMB}	@ I_{PULLUP}			0.4	V	
Current sinking at V_{OLSMB} = 0.4 V	I_{PULLUP}	SMB Data Pin	4			mA	
SCLK/SDATA Clock/Data Rise Time	T_{RI2C}	(Max VIL - 0.15) to (Min VIH + 0.15)			1000	ns	
SCLK/SDATA Clock/Data Fall Time	T_{FI2C}	(Min VIH + 0.15) to (Max VIL - 0.15)			300	ns	
Maximum SMBus Operating Frequency	F_{SMBUS}				100	kHz	
Spread Spectrum Modulation Frequency	f_{SSMOD}	Triangular Modulation	30	32.54	33	kHz	

NOTES on DC Parameters: (unless otherwise noted, guaranteed by design and characterization, not 100% tested in production).

[1] Signal is required to be monotonic in this region.

[2] input leakage current does not include inputs with pull-up or pull-down resistors

[3] 3.3V referenced inputs are: PCI_STOP#, CPU_STOP#, TME, SRC5_EN, ITP_EN, SCLKL, SDATA, TESTMODE, TESTSEL, CKPWRGD and CR# inputs if selected.

[4] Intentionally blank

[5] Maximum VIH is not to exceed VDD

[6] Human Body Model

[7] Operation under these conditions is neither implied, nor guaranteed.

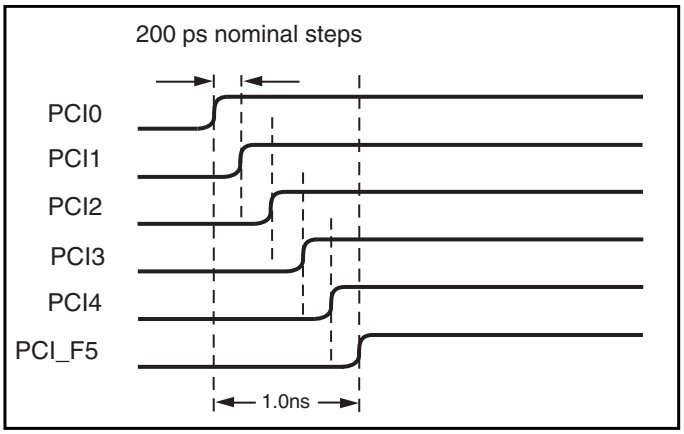
[8] Frequency Select pins which have tri-level input

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Electrical Characteristics - PCICLK/PCICLK_F

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	NOTES
Long Accuracy	ppm	see Tperiod min-max values	-100	0	100	ppm	1,2
Clock period	T_{period}	33.33MHz output no spread	29.99700		30.00300	ns	2
		33.33MHz output spread	30.08421		30.23459	ns	2
Absolute min/max period	T_{abs}	33.33MHz output no spread	29.49700		30.50300	ns	2
		33.33MHz output nominal/spread	29.56617		30.58421	ns	2
Rising Edge Slew Rate	t_{SLR}	Measured from 0.8 to 2.0 V	1	1.71	4	V/ns	1
Falling Edge Slew Rate	t_{FLR}	Measured from 2.0 to 0.8 V	1	1.78	4	V/ns	1
Pin to Pin Skew	t_{skew}	V_T = 1.5 V			250	ps	2
Intential PCI to PCI delay	t_{skew}	V_T = 1.5 V	100	187	300	ps	2
Duty Cycle	d_{t1}	V_T = 1.5 V	45	51	55	%	2
Jitter, Cycle to cycle	$t_{jcyc-cyc}$	V_T = 1.5 V		103	500	ps	2

Intentional PCI Clock to Clock Delay



Electrical Characteristics - USB48MHz

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	NOTES
Long Accuracy	ppm	see Tperiod min-max values	-100	0	100	ppm	2,4
Clock period	T_{period}	48.00MHz output nominal	20.83125		20.83542	ns	2,3
Absolute min/max period	T_{abs}	48.00MHz output nominal	20.48125		21.18542	ns	2
CLK High Time	T_{HIGH}		8.216563		11.15198	V	
CLK Low time	T_{LOW}		7.816563		10.95198	V	
Rising Edge Slew Rate	t_{SLR}	Measured from 0.8 to 2.0 V	1	1.2	2	V/ns	1
Falling Edge Slew Rate	t_{FLR}	Measured from 2.0 to 0.8 V	1	1.3	2	V/ns	1
Duty Cycle	d_{t1}	V_T = 1.5 V	45	50.8%	55	%	2
Jitter, Cycle to cycle	$t_{jcyc-cyc}$	V_T = 1.5 V		132.2	350	ps	2

Electrical Characteristics - REF-14.318MHz

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	Notes
Long Accuracy	ppm	see Tperiod min-max values	-100	0	100	ppm	2, 4
Clock period	Tperiod	14.318MHz output nominal	69.82033		69.86224	ns	2, 3
Absolute min/max period	Tabs	14.318MHz output nominal	69.83400		70.84800	ns	2
CLK High Time	THIGH		29.97543		38.46654	V	
CLK Low time	TLOW		29.57543		38.26654	V	
Rising Edge Slew Rate	tSLR	Measured from 0.8 to 2.0 V	1	1.4	4	V/ns	1
Falling Edge Slew Rate	tFLR	Measured from 2.0 to 0.8 V	1	1.7	4	V/ns	1
Duty Cycle	dt1	VT = 1.5 V	45	53.1	55	%	2
Jitter, Cycle to cycle	tjcyc-cyc	VT = 1.5 V		138	1000	ps	2

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Electrical Characteristics - SE1/2=25MHz

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	NOTES
Long Accuracy	ppm	see Tperiod min-max values	-100	0	100	ppm	1,2
Clock period	T_{period}	25.00MHz output nominal	39.99600		40.00400	ns	1
Absolute min/max period	T_{abs}	25.00MHz output nominal	39.32360		40.67640	ns	1
Rising Edge Slew Rate	t_{SLR}	Measured from 0.8 to 2.0 V	1	1.2	2	V/ns	1
Falling Edge Slew Rate	t_{FLR}	Measured from 2.0 to 0.8 V	1	1.3	2	V/ns	1
Duty Cycle	d_{t1}	V_T = 1.5 V	45	50.8	55	%	1
Jitter, Cycle to cycle	$t_{jcyc-cyc}$	V_T = 1.5 V		60	500	ps	1
Jitter, Long Term	t_{LTJ}	V_T = 1.5 V @ 10us delay		780	1000	ps	1

NOTES on SE outputs: (unless otherwise noted, guaranteed by design and characterization, not 100% tested in production).

[1] Edge rate in system is measured from 0.8V to 2.0V.

[2] Duty cycle, Peroid and Jitter are measured with respect to 1.5V

[3] The average period over any 1us period of time

[4] Using frequency counter with the measurment interval equal or greater that 0.15s, target frequencies are 14.318180 MHz, 33.333333MHz and 48.000000MHz

Table 1: CPU Frequency Select Table

FS_LC[2] B0b7	FS_LB[1] B0b6	FS_LA[1] B0b5	CPU MHz	SRC MHz	PCI MHz	REF MHz	USB MHz	DOT MHz
0	0	0	266.66	100.00	33.33	14.318	48.00	96.00
0	0	1	133.33					
0	1	0	200.00					
0	1	1	166.66					
1	0	0	333.33					
1	0	1	100.00					
1	1	0	400.00					
1	1	1	Reserved					

1. FS_LA and FS_LB are low-threshold inputs.Please see V_{IL_FS} and V_{IH_FS} specifications in the Input/Supply/Common Output Parameters Table for correct values. Also refer to the Test Clarification Table.
2. FS_LC is a three-level input. Please see the V_{IL_FS} and V_{IH_FS} specifications in the Input/Supply/Common Output Parameters Table for correct values.

Table 2: PLL3 Quick Configuration

B1b4	B1b3	B1b2	B1b1	Pin 17 MHz	Pin 18 MHz	Spread %	Comment
0	0	0	0	PLL 3 disabled			
0	0	0	1	100.00	100.00	0.5% Down Spread	SRCCLK1 from SRC_MAIN
0	0	1	0	100.00	100.00	0.5% Down Spread	Only SRCCLK1 from PLL3
0	0	1	1	100.00	100.00	1% Down Spread	Only SRCCLK1 from PLL3
0	1	0	0	100.00	100.00	1.5% Down Spread	Only SRCCLK1 from PLL3
0	1	0	1	100.00	100.00	2% Down Spread	Only SRCCLK1 from PLL3
0	1	1	0	100.00	100.00	2.5% Down Spread	Only SRCCLK1 from PLL3
0	1	1	1	**N/A**	**N/A**	**N/A**	**N/A**
1	0	0	0	24.576	24.576	None	24.576Mhz on SE1 and SE2
1	0	0	1	24.576	98.304	None	24.576Mhz on SE1, 98.304Mhz on SE2
1	0	1	0	98.304	98.304	None	98.304Mhz on SE1 and SE2
1	0	1	1	27.000	27.000	None	27Mhz on SE1 and SE2
1	1	0	0	25.000	25.000	None	25Mhz on SE1 and SE2
1	1	0	1	**N/A**	**N/A**	**N/A**	**N/A**
1	1	1	0	**N/A**	**N/A**	**N/A**	**N/A**
1	1	1	1	**N/A**	**N/A**	**N/A**	**N/A**

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Table 3: IO_Vout select table

B9b2	B9b1	B9b0	IO_Vout
0	0	0	0.3V
0	0	1	0.4V
0	1	0	0.5V
0	1	1	0.6V
1	0	0	0.7V
1	0	1	0.8V
1	1	0	0.9V
1	1	1	1.0V

Table 4: Device ID table

B8b7	B8b6	B8b5	B8b4	Comment
0	0	0	0	56 pin TSSOP/QFN
0	0	0	1	64 pin TSSOP/QFN
0	0	1	0	Reserved
0	0	1	1	Reserved
0	1	0	0	Reserved
0	1	0	1	Reserved
0	1	1	0	Reserved
0	1	1	1	Reserved
1	0	0	0	Reserved
1	0	0	1	Reserved
1	0	1	0	Reserved
1	0	1	1	Reserved
1	1	0	0	Reserved
1	1	0	1	Reserved
1	1	1	0	Reserved
1	1	1	1	Reserved

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PCI_STOP# Power Management

			Single-ended Clocks		Differential Clocks (Except CPU)	
SMBus OE Bit	**PCI_STOP#**	**Stop Drive Mode**	**Stoppable**	**Free running**	**Stoppable**	**Free running**
Enable	**1**	**X**	Running	Running	Running	Running
	0	**0**	Low	Low	CK= High CK# = Low	Running
		1			CK= Pull down CK# = Low	Running
Disable	**X**	**X**	Low		CK= Pull down, CK# = Low	

CPU_STOP# Power Management

			Differential Clocks	
SMBus OE Bit	**PCI_STOP#**	**Stop Drive Mode**	**Stoppable**	**Free running**
Enable	**1**	**X**	Running	Running
	0	**0**	CK= High CK# = Low	Running
		1	CK= Pull down CK# = Low	Running
Disable	**X**	**X**	Low	

CR# Power Management

			Differential Clocks	
SMBus OE Bit	**CR#**	**Stop Drive Mode**	**Stoppable**	**Free running**
Enable	**1**	**X**	Running	Running
	0		CK= Pull down, CK# = Low	
Disable	**X**		CK = Pull down, CK# = Low	

PD# Power Management

	Single-ended Clocks		Differential Clocks (Except CPU1)	CPU1
Device State	**w/o Latched input**	**w/Latched input**		
Latches Open	Low	Hi-Z	CK= Pull down, CK# = Low	CK= Pull down, CK# = Low
Power Down			CK= Pull down CK# = Low	CK= Pull down CK# = Low
M1			CK= Pull down CK# = Low	Running
Virtual Power Cycle to Latches Open			CK= Pull down, CK# = Low	CK= Pull down, CK# = Low

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General SMBus serial interface information for the ICS9LPR501

How to Write:

- Controller (host) sends a start bit.
- Controller (host) sends the write address D2 (H)
- ICS clock will ***acknowledge***
- Controller (host) sends the begining byte location = N
- ICS clock will ***acknowledge***
- Controller (host) sends the data byte count = X
- ICS clock will ***acknowledge***
- Controller (host) starts sending ***Byte N through Byte N + X -1***
- ICS clock will ***acknowledge*** each byte ***one at a time***
- Controller (host) sends a Stop bit

How to Read:

- Controller (host) will send start bit.
- Controller (host) sends the write address D2 (H)
- ICS clock will ***acknowledge***
- Controller (host) sends the begining byte location = N
- ICS clock will ***acknowledge***
- Controller (host) will send a separate start bit.
- Controller (host) sends the read address D3 (H)
- ICS clock will ***acknowledge***
- ICS clock will send the data byte count = X
- ICS clock sends ***Byte N + X -1***
- ICS clock sends ***Byte 0 through byte X (if $X_{(H)}$ was written to byte 8)***.
- Controller (host) will need to acknowledge each byte
- Controllor (host) will send a not acknowledge bit
- Controller (host) will send a stop bit

Index Block Write Operation

Controller (Host)		ICS (Slave/Receiver)
T	starT bit	
Slave Address $D2_{(H)}$		
WR	WRite	
		ACK
Beginning Byte = N		
		ACK
Data Byte Count = X		
		ACK
Beginning Byte N	X Byte	
		ACK
O		
O		O
O		O
		O
Byte N + X - 1		
		ACK
P	stoP bit	

Index Block Read Operation

Controller (Host)		ICS (Slave/Receiver)	
T	starT bit		
Slave Address $D2_{(H)}$			
WR	WRite		
		ACK	
Beginning Byte = N			
		ACK	
RT	Repeat starT		
Slave Address $D3_{(H)}$			
RD	ReaD		
		ACK	
		Data Byte Count = X	
ACK			
	X Byte		Beginning Byte N
ACK			
			O
O			O
O			O
O			
			Byte N + X - 1
N	Not acknowledge		
P	stoP bit		

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Byte 0 FS Readback and PLL Selection Register

Bit	Pin	Name	Description	Type	0	1	Default
7	-	FSLC	CPU Freq. Sel. Bit (Most Significant)	R	See Table 1 : CPU Frequency Select Table		Latch
6	-	FSLB	CPU Freq. Sel. Bit	R			Latch
5	-	FSLA	CPU Freq. Sel. Bit (Least Significant)	R			Latch
4	-	iAMT_EN	Set via SMBus or dynamically by CK505 if detects dynamic M1	RW	Legacy Mode	iAMT Enabled	0
3		Reserved	Reserved	RW			0
2	-	SRC_Main_SEL	Select source for SRC Main	RW	SRC Main = PLL1	SRC Main = PLL3	0
1	-	SATA_SEL	Select source for SATA clock	RW	SATA = SRC_Main	SATA = PLL2 See Note	0
0	-	PD_Restore	1 = on Power Down de-assert return to last known state 0 = clear all SMBus configurations as if cold power-on and go to latches open state This bit is ignored and treated at '1' if device is in iAMT mode.	RW	Configuration Not Saved	Configuration Saved	1

Note: If setting Byte 0, bit 1 to 1 to make SATA non-spreading, Byte63, bit 1 must be set to '1' first to turn on the SATA PLL.

Byte 1 DOT96 Select and PLL3 Quick Config Register

Bit	Pin	Name	Description	Type	0	1	Default
7	13/14	SRC0_SEL	Select SRC0 or DOT96	RW	SRC0	DOT96	0
6	-	PLL1_SSC_SEL	Select 0.5% down or center SSC	RW	Down spread	Center spread	0
5		PLL3_SSC_SEL	Select 0.5% down or center SSC	RW	Down spread	Center spread	0
4		PLL3_CF3	PLL3 Quick Config Bit 3	RW	See Table 2: PLL3 Quick Configuration **Only applies if Byte 0, bit 2 = 0.**		0
3		PLL3_CF2	PLL3 Quick Config Bit 2	RW			0
2		PLL3_CF1	PLL3 Quick Config Bit 1	RW			0
1		PLL3_CF0	PLL3 Quick Config Bit 0	RW			1
0		PCI_SEL	PCI_SEL	RW	PCI from PLL1	PCI from SRC_MAIN	1

Byte 2 Output Enable Register

Bit	Pin	Name	Description	Type	0	1	Default
7		REF_OE	Output enable for REF, if disabled output is Hi-Z	RW	Output Disabled	Output Enabled	1
6		USB_OE	Output enable for USB	RW	Output Disabled	Output Enabled	1
5		PCIF5_OE	Output enable for PCI5	RW	Output Disabled	Output Enabled	1
4		PCI4_OE	Output enable for PCI4	RW	Output Disabled	Output Enabled	1
3		PCI3_OE	Output enable for PCI3	RW	Output Disabled	Output Enabled	1
2		PCI2_OE	Output enable for PCI2	RW	Output Disabled	Output Enabled	1
1		PCI1_OE	Output enable for PCI1	RW	Output Disabled	Output Enabled	1
0		PCI0_OE	Output enable for PCI0	RW	Output Disabled	Output Enabled	1

Byte 3 Output Enable Register

Bit	Pin	Name	Description	Type	0	1	Default
7		SRC11_OE	Output enable for SRC11	RW	Output Disabled	Output Enabled	1
6		SRC10_OE	Output enable for SRC10	RW	Output Disabled	Output Enabled	1
5		SRC9_OE	Output enable for SRC9	RW	Output Disabled	Output Enabled	1
4		SRC8/ITP_OE	Output enable for SRC8 or ITP	RW	Output Disabled	Output Enabled	1
3		SRC7_OE	Output enable for SRC7	RW	Output Disabled	Output Enabled	1
2		SRC6_OE	Output enable for SRC6	RW	Output Disabled	Output Enabled	1
1		SRC5_OE	Output enable for SRC5	RW	Output Disabled	Output Enabled	1
0		SRC4_OE	Output enable for SRC4	RW	Output Disabled	Output Enabled	1

Byte 4 Output Enable and Spread Spectrum Disable Register

Bit	Pin	Name	Description	Type	0	1	Default
7		SRC3_OE	Output enable for SRC3	RW	Output Disabled	Output Enabled	1
6		SATA/SRC2_OE	Output enable for SATA/SRC2	RW	Output Disabled	Output Enabled	1
5		SRC1_OE	Output enable for SRC1	RW	Output Disabled	Output Enabled	1
4		SRC0/DOT96_OE	Output enable for SRC0/DOT96	RW	Output Disabled	Output Enabled	1
3		CPU1_OE	Output enable for CPU1	RW	Output Disabled	Output Enabled	1
2		CPU0_OE	Output enable for CPU0	RW	Output Disabled	Output Enabled	1
1		PLL1_SSC_ON	Enable PLL1's spread modulation	RW	Spread Disabled	Spread Enabled	1
0		PLL3_SSC_ON	Enable PLL3's spread modulation	RW	Spread Disabled	Spread Enabled	1

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Byte 5 Clock Request Enable/Configuration Register

Bit	Pin	Name	Description	Type	0	1	Default
7		CR#_A_EN	Enable CR#_A (clk req), PCI0_OE must be = 1 for this bit to take effect	RW	Disable CR#_A	Enable CR#_A	0
6		CR#_A_SEL	Sets CR#_A to control either SRC0 or SRC2	RW	CR#_A -> SRC0	CR#_A -> SRC2	0
5		CR#_B_EN	Enable CR#_B (clk req)	RW	Disable CR#_B	Enable CR#_B	0
4		CR#_B_SEL	Sets CR#_B -> SRC1 or SRC4	RW	CR#_B -> SRC1	CR#_B -> SRC4	0
3		CR#_C_EN	Enable CR#_C (clk req)	RW	Disable CR#_C	Enable CR#_C	0
2		CR#_C_SEL	Sets CR#_C -> SRC0 or SRC2	RW	CR#_C -> SRC0	CR#_C -> SRC2	0
1		CR#_D_EN	Enable CR#_D (clk req)	RW	Disable CR#_D	Enable CR#_D	0
0		CR#_D_SEL	Sets CR#_D -> SRC1 or SRC4	RW	CR#_D -> SRC1	CR#_D -> SRC4	0

Byte 6 Clock Request Enable/Configuration and Stop Control Register

Bit	Pin	Name	Description	Type	0	1	Default
7		CR#_E_EN	Enable CR#_E (clk req) -> SRC6	RW	Disable CR#_E	Enable CR#_E	0
6		CR#_F_EN	Enable CR#_F (clk req) -> SRC8	RW	Disable CR#_F	Enable CR#_F	0
5		CR#_G_EN	Enable CR#_G (clk req) -> SRC9	RW	Disable CR#_G	Enable CR#_G	0
4		CR#_H_EN	Enable CR#_H (clk req) -> SRC10	RW	Disable CR#_H	Enable CR#_H	0
3		Reserved	Reserved	RW			0
2		Reserved	Reserved	RW			0
1		SSCD_STP_CRTL (SRC1)	If set, SSCD (SRC1) stops with PCI_STOP#	RW	Free Running	Stops with PCI_STOP# assertion	0
0		SRC_STP_CRTL	If set, SRCs (except SRC1) stop with PCI_STOP#	RW	Free Running	Stops with PCI_STOP# assertion	0

Byte 7 Vendor ID/ Revision ID

Bit	Pin	Name	Description	Type	0	1	Default
7		Rev Code Bit 3	Revision ID	R	Vendor specific		X
6		Rev Code Bit 2		R			X
5		Rev Code Bit 1		R			X
4		Rev Code Bit 0		R			X
3		Vendor ID bit 3	Vendor ID ICS is 0001, binary	R			0
2		Vendor ID bit 2		R			0
1		Vendor ID bit 1		R			0
0		Vendor ID bit 0		R			1

Byte 8 Device ID and Output Enable Register

Bit	Pin	Name	Description	Type	0	1	Default
7		**Device_ID3**	**Table of Device identifier codes, used for differentiating between CK505 package options, etc.**	**R**	**See Device ID Table**		**0**
6		**Device_ID2**		**R**			**0**
5		**Device_ID1**		**R**			**0**
4		**Device_ID0**		**R**			**1**
3		Reserved	Reserved	RW	-	-	0
2		Reserved	Reserved	RW	-	-	0
1		SE1_OE	Output enable for SE1	RW	Disabled	Enabled	0
0		SE2_OE	Output enable for SE2	RW	Disabled	Enabled	0

Byte 9 Output Control Register

Bit	Pin	Name	Description	Type	0	1	Default
7		PCIF5 STOP EN	Allows control of PCIF5 with assertion of PCI_STOP#	RW	Free running	Stops with PCI_STOP# assertion	0
6		TME_Readback	Truested Mode Enable (TME) strap status	**R**	normal operation	no overclocking	0
5		REF Strength	Sets the REF output drive strength	RW	1X (2Loads)	2X (3 Loads)	1
4		Test Mode Select	Allows test select, ignores REF/FSC/TestSel	RW	Outputs HI-Z	Outputs = REF/N	0
3		Test Mode Entry	Allows entry into test mode, ignores FSB/TestMode	RW	Normal operation	Test mode	0
2		IO_VOUT2	IO Output Voltage Select (Most Significant Bit)	RW	See Table 3: V_IO Selection (Default is 0.8V)		1
1		IO_VOUT1	IO Output Voltage Select	RW			0
0		IO_VOUT0	IO Output Voltage Select (Least Significant Bit)	RW			1

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Byte 10 CK505 Rev 0.85 Functions (ICS Rev H Silicon and Higher)

Bit	Pin	Name	Description	Type	0	1	Default
7		SRC5_EN Readback	Readback of SRC5 enable latch	R	CPU/PCI Stop Enabled	SRC5 Enabled	Latch
6		Reserved	Reserved	RW	TBD	TBD	0
5		Reserved		RW	TBD	TBD	0
4		Reserved		RW	TBD	TBD	0
3		Reserved		RW	TBD	TBD	0
2		Reserved		RW	TBD	TBD	0
1		CPU 1 Stop Enable	Enables control of CPU1 with CPU_STOP#	RW	Free Running	Stoppable	1
0		CPU 0 Stop Enable	Enables control of CPU 0 with CPU_STOP#	RW	Free Running	Stoppable	1

Byte 11 CK505 Rev 1.0 functions (ICS Rev P silicon and higher)

Bit	Pin	Name	Description	Type	0	1	Default
7		Reserved	Reserved	RW	TBD	TBD	0
6		Reserved		RW	TBD	TBD	0
5		Reserved		RW	TBD	TBD	0
4		Reserved		RW	TBD	TBD	0
3		CPU2_iAMT_EN	Enables CPU2(ITP) output in iAMT state (M1)	RW	Off in iAMT	Free running in iAMT	0
2		CPU1_iAMT_EN	Enables CPU1 output in iAMT state (M1)	RW	Off in iAMT	Free running in iAMT	1
1		PCIe-Gen2	PCIe-Gen2 status	R	PCIe Gen1 compliant	PCIe Gen2 compliant	0
0		CPU2 Stop Enable	Enables control of CPU2(ITP) with CPU_STOP#	RW	Free Running	Stoppable	1

Byte 12 Byte Count Register

Bit	Pin	Name	Description	Type	0	1	Default
7		Reserved		RW			0
6		Reserved		RW			0
5		BC5	Read Back byte count register	RW			0
4		BC4		RW			0
3		BC3		RW			1
2		BC2		RW			1
1		BC1		RW			0
0		BC0		RW			1

Byte 13 CK505 PLL1 M/N Programming Register

Bit	Pin	Name	Description	Type	0	1	Default
7		N Div8	N Divider 8	RW	-	-	X
6		N Div9	N Divider 9	RW	-	-	X
5		M Div5	The decimal representation of M Div (5:0) is equal to reference divider value. Default at power up = latch-in or Byte 0 Rom table.	RW	-	-	X
4		M Div4		RW	-	-	X
3		M Div3		RW	-	-	X
2		M Div2		RW	-	-	X
1		M Div1		RW	-	-	X
0		M Div0		RW	-	-	X

Byte 14 CK505 PLL1 M/N Programming Register

Bit	Pin	Name	Description	Type	0	1	Default
7		N Div7	The decimal representation of N Div (9:0) is equal to VCO divider value. Default at power up = latch-in or Byte 0 Rom table.	RW	-	-	X
6		N Div6		RW	-	-	X
5		N Div5		RW	-	-	X
4		N Div4		RW	-	-	X
3		N Div3		RW	-	-	X
2		N Div2		RW	-	-	X
1		N Div1		RW	-	-	X
0		N Div0		RW	-	-	X

Byte 15 CK505 PLL1 Spread Spectrum Control Register

Bit	Pin	Name	Description	Type	0	1	Default
7		SSP7	These Spread Spectrum bits will program the spread pecentage. Contact ICS for the correct values.	RW	-	-	X
6		SSP6		RW	-	-	X
5		SSP5		RW	-	-	X
4		SSP4		RW	-	-	X
3		SSP3		RW	-	-	X
2		SSP2		RW	-	-	X
1		SSP1		RW	-	-	X
0		SSP0		RW	-	-	X

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Byte 16 CK505 PLL1 Spread Spectrum Control Register

Bit	Pin	Name	Description	Type	0	1	Default
7		Reserved	Reserved	RW	-	-	0
6		SSP14	These Spread Spectrum bits will program the spread pecentage. Contact ICS for the correct values.	RW	-	-	x
5		SSP13		RW	-	-	X
4		SSP12		RW	-	-	X
3		SSP11		RW	-	-	X
2		SSP10		RW	-	-	X
1		SSP9		RW	-	-	X
0		SSP8		RW	-	-	X

Byte 17 CK505 PLL3 M/N Programming Register

Bit	Pin	Name	Description	Type	0	1	Default
7		N Div8	N Divider 8	RW	-	-	X
6		N Div9	N Divider 9	RW	-	-	X
5		M Div5	The decimal representation of M Div (5:0) is equal to reference divider value. Default at power up = latch-in or Byte 0 Rom table.	RW	-	-	X
4		M Div4		RW	-	-	X
3		M Div3		RW	-	-	X
2		M Div2		RW	-	-	X
1		M Div1		RW	-	-	X
0		M Div0		RW	-	-	X

Byte 18 CK505 PLL3 M/N Programming Register

Bit	Pin	Name	Description	Type	0	1	Default
7		N Div7	The decimal representation of N Div (9:0) is equal to VCO divider value. Default at power up = latch-in or Byte 0 Rom table.	RW	-	-	X
6		N Div6		RW	-	-	X
5		N Div5		RW	-	-	X
4		N Div4		RW	-	-	X
3		N Div3		RW	-	-	X
2		N Div2		RW	-	-	X
1		N Div1		RW	-	-	X
0		N Div0		RW	-	-	X

Byte 19 CK505 PLL3 Spread Spectrum Control Register

Bit	Pin	Name	Description	Type	0	1	Default
7		SSP7	These Spread Spectrum bits will program the spread pecentage. Contact ICS for the correct values.	RW	-	-	X
6		SSP6		RW	-	-	X
5		SSP5		RW	-	-	X
4		SSP4		RW	-	-	X
3		SSP3		RW	-	-	X
2		SSP2		RW	-	-	X
1		SSP1		RW	-	-	X
0		SSP0		RW	-	-	X

Byte 20 CK505 PLL3 Spread Spectrum Control Register

Bit	Pin	Name	Description	Type	0	1	Default
7		Reserved	Reserved	RW	-	-	0
6		SSP14	These Spread Spectrum bits will program the spread pecentage. Contact ICS for the correct values.	RW	-	-	X
5		SSP13		RW	-	-	X
4		SSP12		RW	-	-	X
3		SSP11		RW	-	-	X
2		SSP10		RW	-	-	X
1		SSP9		RW	-	-	X
0		SSP8		RW	-	-	X

Byte 21 M/N Enables

Bit	Pin	Name	Description	Type	0	1	Default
7		Reserved		RW			0
6		Reserved		RW			0
5		Reserved		RW			0
4		Reserved		RW			0
3		Reserved		RW			0
2		Reserved		RW			0
1		M/N Enable CPU		RW	Disable	Enable	0
0		M/N Enable SRC/PCI		RW	Disable	Enable	0

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Byte 22 CPU M/N Programming

Bit	Pin	Name	Description	Type	0	1	Default
7		N Div bit 8	PLL 1 M/N Programming	RW	-	-	X
6		N Div bit 9	(Intel PLL1 CPU)	RW	-	-	X
5		M Div Bit 5		RW	-	-	X
4		M Div Bit 4		RW	-	-	X
3		M Div Bit 3		RW	-	-	X
2		M Div Bit 2		RW	-	-	X
1		M Div Bit 1		RW	-	-	X
0		M Div Bit 0		RW	-	-	X

Byte 23 CPU M/N Programming

Bit	Pin	Name	Description	Type	0	1	Default
7		N Div bit 7	PLL 1 M/N Programming	RW	-	-	X
6		N Div bit 6	(Intel PLL1 CPU)	RW	-	-	X
5		N Div bit 5		RW	-	-	X
4		N Div bit 4		RW	-	-	X
3		N Div bit 3		RW	-	-	X
2		N Div bit 2		RW	-	-	X
1		N Div bit 1		RW	-	-	X
0		N Div Bit 0		RW	-	-	X

Bytes 24-62 Reserved

Byte 63 Special Power Management Features (Rev P Silicon and Higher)

Bit	Pin	Name	Description	RW	0	1	Default
7		Reserved		RW			0
6		Reserved		RW			0
5		Reserved		RW			0
4		Reserved		RW			0
3		Reserved		RW			0
2		Reserved		RW			0
1		SATA PLL	Power Management Feature	RW	off	on	Note
0		XTAL PD Control	Controls XTAL on/off in legacy PD	RW	off	on	1

Note: Default is "off" for Rev P Silicon and higher.

***Accessing any SMBus bytes not shown in the datasheet could result in incorrect clock functions.**

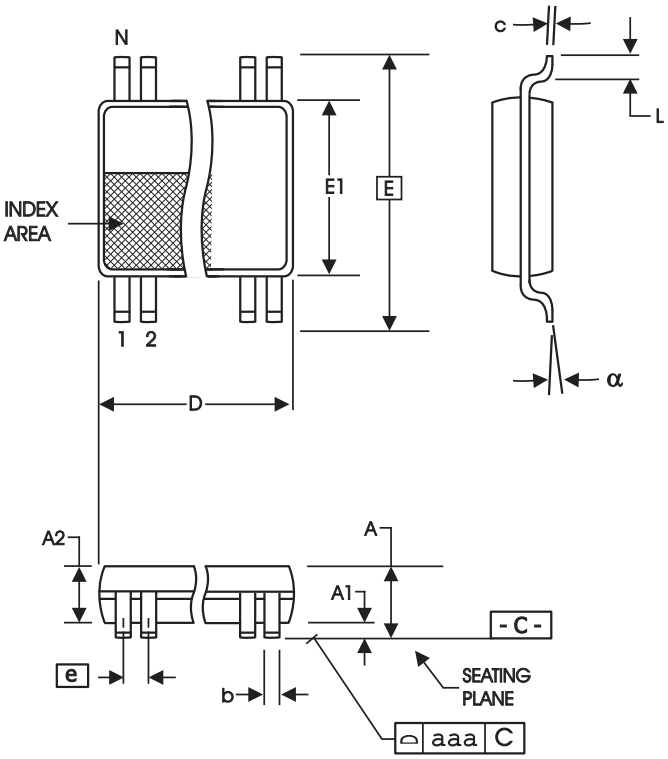
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Test Clarification Table

Comments	HW		SW		
	FSLC/ TEST_SEL HW PIN	FSLB/ TEST_MODE HW PIN	TEST ENTRY BIT B9b3	REF/N or HI-Z B9b4	OUTPUT
	<2.0V	X	0	0	NORMAL
Power-up w/ TEST_SEL = 1 to enter test mode Cycle power to disable test mode FSLC./TEST_SEL -->3-level latched input If power-up w/ V>2.0V then use TEST_SEL If power-up w/ V<2.0V then use FSLC FSLB/TEST_MODE -->low Vth input TEST_MODE is a real time input	>2.0V	0	X	0	HI-Z
	>2.0V	0	X	1	REF/N
	>2.0V	1	X	0	REF/N
	>2.0V	1	X	1	REF/N
If TEST_SEL HW pin is 0 during power-up, test mode can be invoked through B9b3. If test mode is invoked by B9b3, only B9b4 is used to select HI-Z or REF/N FSLB/TEST_Mode pin is not used. Cycle power to disable test mode, one shot control	<2.0V	X	1	0	HI-Z
	<2.0V	X	1	1	REF/N

B9b3: 1= ENTER TEST MODE, Default = 0 (NORMAL OPERATION)
B9b4: 1= REF/N, Default = 0 (HI-Z)

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6.10 mm. Body, 0.50 mm. Pitch TSSOP
(240 mil) (20 mil)

SYMBOL	In Millimeters COMMON DIMENSIONS		In Inches COMMON DIMENSIONS	
	MIN	MAX	MIN	MAX
A	--	1.20	--	.047
A1	0.05	0.15	.002	.006
A2	0.80	1.05	.032	.041
b	0.17	0.27	.007	.011
c	0.09	0.20	.0035	.008
D	SEE VARIATIONS		SEE VARIATIONS	
E	8.10 BASIC		0.319 BASIC	
E1	6.00	6.20	.236	.244
e	0.50 BASIC		0.020 BASIC	
L	0.45	0.75	.018	.030
N	SEE VARIATIONS		SEE VARIATIONS	
α	0°	8°	0°	8°
aaa	--	0.10	--	.004

VARIATIONS

N	D mm.		D (inch)	
	MIN	MAX	MIN	MAX
64	16.90	17.10	.665	.673

Reference Doc.: JEDEC Publication 95, MO-153

10-0039

Ordering Information

Part / Order Number	Shipping Packaging	Package	Temperature
9LPR501SGLF	Tubes	64-pin TSSOP	0 to +70° C
9LPR501SGLFT	Tape and Reel	64-pin TSSOP	0 to +70° C

“LF” suffix to the part number are the Pb-Free configuration, RoHS compliant.

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Revision History

Rev.	Issue Date	Description	Page #
A	10/27/2006	1. Updated Byte 11 2. Updated IDD to CK505 Rev 1.0 spec	Various
B	2/9/2007	1. Updated M/N programming bytes, removed the +2 and +8 2. Added Byte 63 bit 1 for SATA PLL on/off	Various
C	4/3/2007	Added Bytes 24-25.	20
D	4/17/2007	Removed SSOP Ordering Information.	22
E	8/8/2007	Release to Final.	-
F	11/6/2007	Added Foot Note on SMBus.	19
G	2/19/2008	1. Updated PLL3 Configuration Table. 2. Updated Power Management Table to Show Hi-z on latched inputs during PD.	11
H	3/7/2008	Updated Electrical Characteristics	7-9
J	12/5/2008	Added Electrical table for SE1/2-25MHz.	10
K	2/9/2009	Updated Electrical Characteristics	Various
L	2/23/2009	Updated note under Byte 63 table.	18
M	11/24/2009	Removed references to PCIe Gen2 performance.	Various
N	5/19/2011	1. Updated Electrical Tables to latest CK505 format 2. Added note to SMBus byte 0 clarifying interaction with Byte 63 3. Updated ordering information to latest format	7-10, 14, 20

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