Description

The 9SBV0802 provides two banks of four 1.05V LVCMOS outputs. Each bank has its own input. There are three OE pins. Two OE pins control two outputs each and one OE pin controls four outputs. One 9SBV0802 allows one PCH to easily support four CPUs with point to point routing of the PM signals. Two 9SBV0802 devices allow one PCH to easily support up to eight CPUs with point-to-point routing of the PM signals.

Features

- 1.8V power supply, 15mW typical power consumption; eliminate thermal concerns
- OE pins; support 1, 2, 3 or 4 socket systems
- 1.05V LVCMOS inputs with VREF pin; input thresholds matched to chipset power supply
- Space saving 4 × 4 mm 20-VFQFPN; minimal board space

Typical Application

Fanout buffer for PM-SYNC and PM_SYNC CLK in Intel Servers

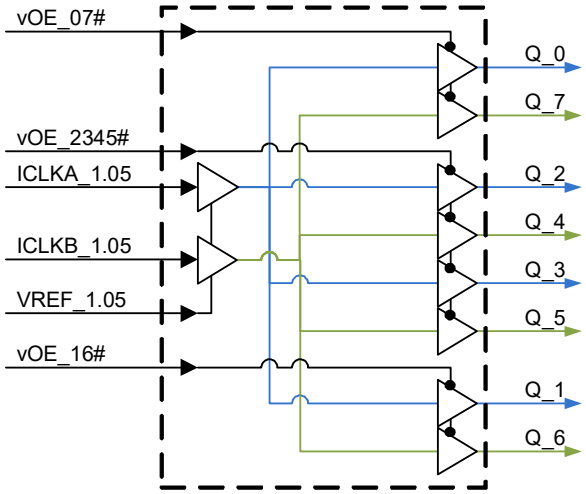
Output Features

- Eight 1–48MHz 1.05V LVCMOS outputs

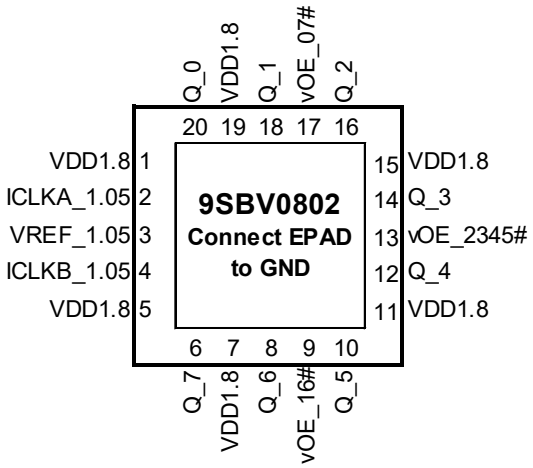
Key Specifications

- *Additive* cycle-to-cycle jitter < 8ps
- Output-to-output skew within a bank < 50ps
- Output-to-output skew between banks < 100ps

Block Diagram



Pin Configuration



4 × 4 mm 20-VFQFPN, 0.5mm pitch

^ prefix indicates internal 120kOhm pull-up resistor

v prefix indicates internal 120kOhm pull-down resistor

Output Control Table

ICLKA_1.05 ICLKB_1.05	OE_07	OE_16	OE_2345	Q_7	Q_6	Q_5	Q_4	Q_3	Q_2	Q_1	Q_0
X	X	X	X	X	X	X	X	X	X	X	X
Running	1	1	1	0	0	0	0	0	0	0	0
Running	1	1	0	0	0	Run	Run	Run	Run	0	0
Running	1	0	1	0	Run	0	0	0	0	Run	0
Running	1	0	0	0	Run	Run	Run	Run	Run	Run	0
Running	0	1	1	Run	0	0	0	0	0	0	Run
Running	0	1	0	Run	0	Run	Run	Run	Run	0	Run
Running	0	0	1	Run	Run	0	0	0	0	Run	Run
Running	0	0	0	Run	Run	Run	Run	Run	Run	Run	Run

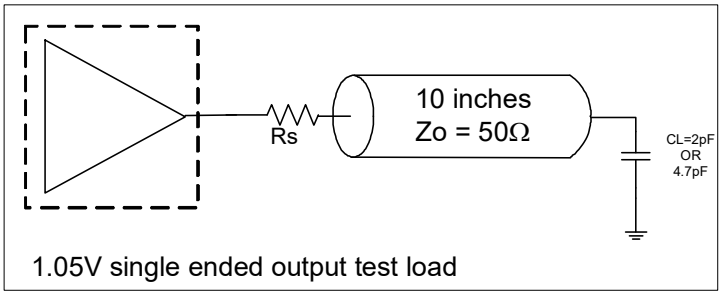
Power Connections

Description	Pin Number	
	VDD	GND
Input Circuits	1,5	21
1.05V reference	3	21
Outputs	7,11, 15,19	21

Pin Descriptions

Pin#	Pin Name	Type	Pin Description
1	VDD1.8	PWR	Power supply, nominally 1.8V.
2	ICLKA_1.05	IN	1.05V LVCMOS single-ended input clock. Voltage reference is set by the VREF_1.05 pin.
3	VREF_1.05	IN	Voltage reference for 1.05V single-ended inputs. Connect the VDDIO 1.05V power rail from chipset to this pin.
4	ICLKB_1.05	IN	1.05V LVCMOS single-ended input clock. Voltage reference is set by the VREF_1.05 pin.
5	VDD1.8	PWR	Power supply, nominally 1.8V.
6	Q_7	OUT	LVCMOS single-ended output
7	VDD1.8	PWR	Power supply, nominally 1.8V.
8	Q_6	OUT	LVCMOS single-ended output
9	vOE_16#	IN	Active low input for enabling outputs 1 and 6. This pin has an internal pull down. 0 = enable outputs, 1 = disable outputs
10	Q_5	OUT	LVCMOS single-ended output
11	VDD1.8	PWR	Power supply, nominally 1.8V.
12	Q_4	OUT	LVCMOS single-ended output
13	vOE_2345#	IN	Active low input for enabling outputs 2 through 5. This pin has an internal pull down. 0 = enable outputs, 1 = disable outputs
14	Q_3	OUT	LVCMOS single-ended output
15	VDD1.8	PWR	Power supply, nominally 1.8V.
16	Q_2	OUT	LVCMOS single-ended output
17	vOE_07#	IN	Active low input for enabling outputs 0 and 7. This pin has an internal pull down. 0 = enable outputs, 1 = disable outputs
18	Q_1	OUT	LVCMOS single-ended output
19	VDD1.8	PWR	Power supply, nominally 1.8V.
20	Q_0	OUT	LVCMOS single-ended output
21	EPAD	GND	Connect to Ground.

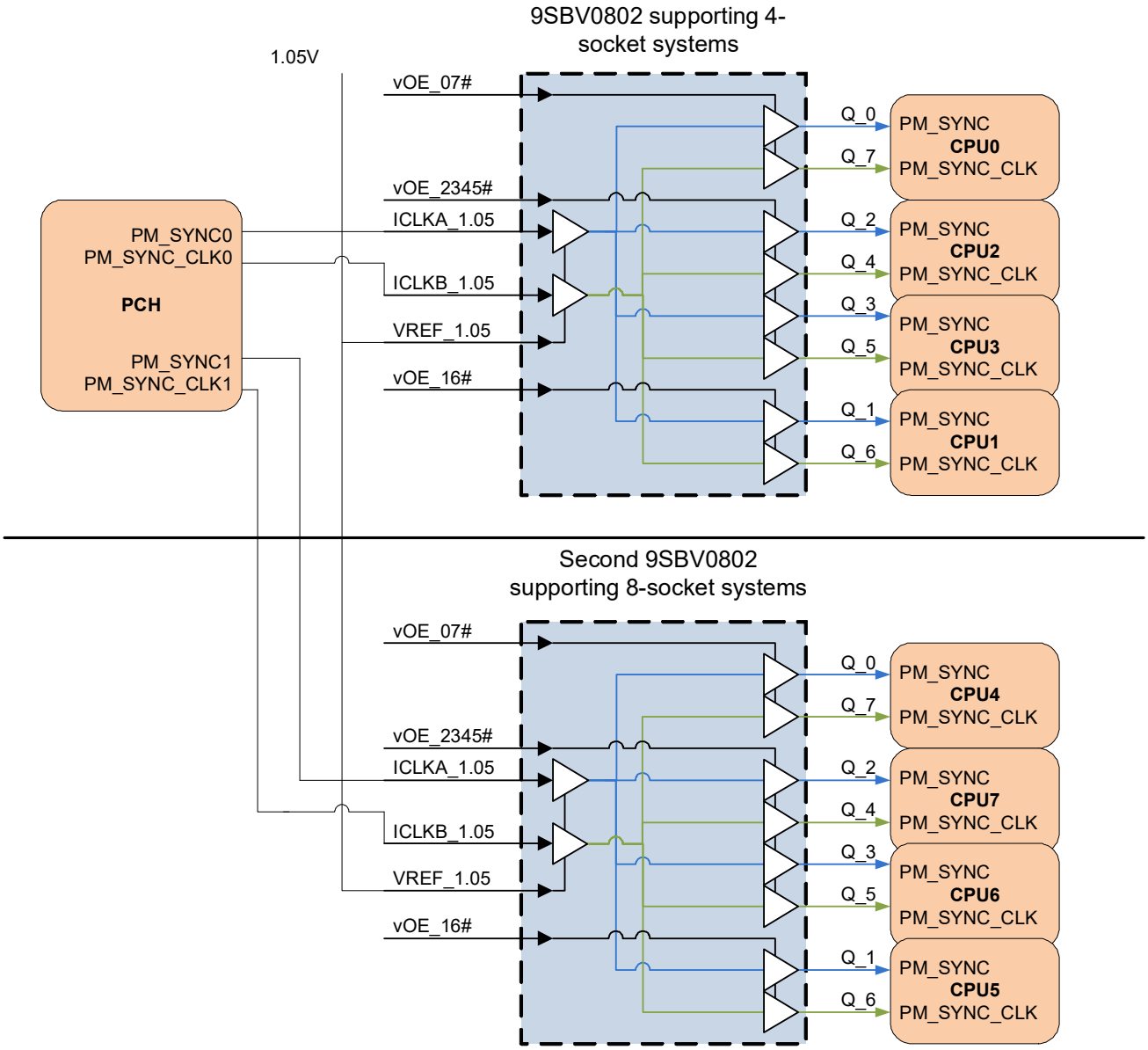
Test Loads



1.05V single ended output test load

Rs = 33Ω for Zo=50Ω

Applications Diagram



Electrical Characteristics–Absolute Maximum Ratings

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	NOTES
Supply Voltage	VDDx		-0.5		2.5	V	1,2
Input Voltage	V_{IN}		-0.5		V_{DD}+0.5	V	1,3
Input High Voltage, SMBus	V_{IHSMB}	SMBus clock and data pins			3.6	V	1
Storage Temperature	Ts		-65		150	°C	1
Junction Temperature	Tj				125	°C	1
Input ESD protection	ESD prot	Human Body Model	2000			V	1

[1]Guaranteed by design and characterization, not 100% tested in production.

[2] Operation under these conditions is neither implied nor guaranteed.

[3] Not to exceed 2.5V.

Electrical Characteristics–Input/Supply/Common Parameters–Normal Operating Conditions

TA = T_{AMB}, Supply Voltages per normal operation conditions, See Test Loads for Loading Conditions

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	NOTES
Supply Voltage	VDD1.8	Supply voltage for core and analog	1.7	1.8	1.9	V	
Reference Supply Voltage	VDDREF_1.05	Reference for 1.05V inputs	0.8	1.05	1.1	V	
Ambient Operating Temperature	T_{AMB}	Industrial range	-40	25	85	°C	
Input High Voltage	V_{IH}	Control Inputs	0.75 V_{DD}	1.6	V_{DD} + 0.3	V	
Input Low Voltage	V_{IL}	Control Inputs	-0.3	0.2	0.25 V_{DD}	V	
Input Current	I_{IN}	Single-ended inputs, V_{IN} = GND, V_{IN} = VDD	-5	0.0	5	uA	
	I_{INP}	Single-ended inputs V_{IN} = 0 V; Inputs with internal pull-up resistors V_{IN} = VDD; Inputs with internal pull-down resistors	-200	0.0	200	uA	
Input Frequency	F_{in}		1	24	48	MHz	
Pin Inductance	L_{pin}				7	nH	1
Capacitance	C_{IN}	Logic Inputs, except DIF_IN	1.5		5	pF	1
	C_{INDIF_IN}	DIF_IN differential clock inputs	1.5		2.7	pF	1
	C_{OUT}	Output pin capacitance			6	pF	1
Clk Stabilization	T_{STAB}	From V_{DD} Power-Up and after input clock stabilization or de-assertion of PD# to 1st clock			1	ms	1,2
Input SS Modulation Frequency non-PCIe	f_{MODIN}	Allowable Frequency for non-PCIe Applications (Triangular Modulation)	0		66	kHz	1
OE Latency	$t_{LATOE\#}$	Output start after OE assertion Output stop after OE deassertion	1		3	clocks	1
Tfall	t_F	Fall time of single-ended control inputs			5	ns	2
Trise	t_R	Rise time of single-ended control inputs			5	ns	2

[1]Guaranteed by design and characterization, not 100% tested in production.

[2]Control input must be monotonic from 20% to 80% of input swing.

Electrical Characteristics–Clock Input Parameters

TA = T_{AMB}, Supply Voltages per normal operation conditions, See Test Loads for Loading Conditions

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	NOTES
Input High Voltage	V_{IH}	ICLKx_1.05	800	1.0	VREF_1.05 + 200mV	mV	1
Input Low Voltage	V_{IL}	ICLKx_1.05	-200	0	200	mV	1
Input Slew Rate	dv/dt	Single-ended measurement, between 40% and 60% of VREF	0.5	-	5	V/ns	1
Input Leakage Current	I_{IN}	V_{IN} = V_{DD} , V_{IN} = GND	-5	0	5	uA	

[1] Guaranteed by design and characterization, not 100% tested in production.

Electrical Characteristics–Q_x 1.05V Single-ended Outputs

TA = T_{AMB}, Supply Voltages per normal operation conditions, See Test Loads for Loading Conditions

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	NOTES
Slew Rate	dV/dt	Scope averaging on, CL = 2pF	0.8	1.5	2.5	V/ns	1, 2
		Scope averaging on, CL = 4.7pF	0.5	1	1.5	V/ns	1, 2
Voltage High	V_{HIGH}	Statistical measurement on single-ended signal using oscilloscope math function. (Scope averaging on)	875	1000	1100	mV	
Voltage Low	V_{LOW}		-150	0	150		

[1]Guaranteed by design and characterization, not 100% tested in production.

[2] Measured from 20% to 80% of swing.

Electrical Characteristics–Current Consumption

TA = T_{AMB}, Supply Voltages per normal operation conditions, See Test Loads for Loading Conditions

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	NOTES
Operating Supply Current	$I_{DDVref1.05}$	VREF_1.05V pin		0.07	0.5	mA	
	$I_{DD1.8}$	VDD, All outputs active at 24MHz, CL = 2pF		8.2	12	mA	
Powerdown Current	I_{DDAPD}	VREF_1.05V pin		0.07	0.5	mA	1
	I_{DDPD}	VDD, All outputs disabled.		3.3	5	mA	1

[1] Input clock stopped.

Electrical Characteristics–Output Duty Cycle, Jitter, and Skew Characteristics

TA = T_{AMB}, Supply Voltages per normal operation conditions, See Test Loads for Loading Conditions

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	NOTES
Duty Cycle Distortion	t_{DCD}	At 24MHz	-2	-0.8%	0	%	1, 2
Skew, Input to Output	t_{I2O}	V_T = 50%	2000	2474	3000	ps	1
Skew, Output to Output	t_{o2oA}	Within banks Q[3:0] or Q[7:4], V_T = 50%		10	50	ps	1
Skew, Matching	t_{o2oB}	Between banks Q[3:0] and Q[7:4], V_T = 50%		47	100	ps	1
Jitter, Cycle to cycle	$t_{jcyc-cyc}$	*Additive* Jitter, V_T = 50%		3.5	8	ps	1

[1] Guaranteed by design and characterization, not 100% tested in production.

[2] Duty cycle distortion is the difference in duty cycle between the output and the input clock.

Marking Diagram



- Line 1: “LOT” denotes the lot number.
- Line 2: truncated part number.
- Line 3: “YYWW” is the last two digits of the year and week that the part was assembled.

Thermal Characteristics

PARAMETER	SYMBOL	CONDITIONS	PKG	TYP VALUE	UNITS	NOTES
Thermal Resistance	θ_{JC}	Junction to Case	NLG20	42	°C/W	1
	θ_{Jb}	Junction to Base		2.4	°C/W	1
	θ_{JA0}	Junction to Air, still air		39	°C/W	1
	θ_{JA1}	Junction to Air, 1 m/s air flow		33	°C/W	1
	θ_{JA3}	Junction to Air, 3 m/s air flow		28	°C/W	1
	θ_{JA5}	Junction to Air, 5 m/s air flow		27	°C/W	1

[1]ePad soldered to board

Package Outline Drawings

The package outline drawings are appended at the end of this document and are accessible from the link below. The package information is the most current data available.

www.idt.com/document/psc/20-vfqfpn-package-outline-drawing-40-x-40-x-090-mm-body-05mm-pitch-epad-21-x-21-mm-nlg20p1

Ordering Information

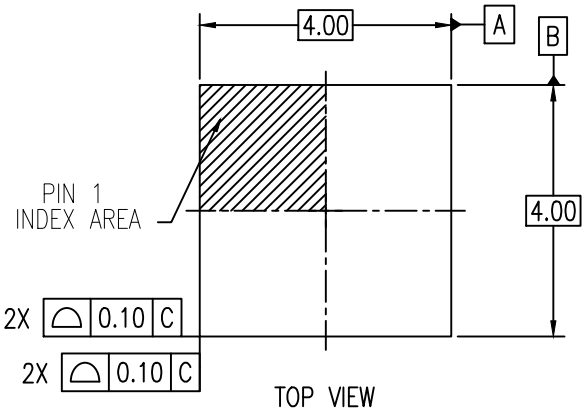
Part / Order Number	Shipping Packaging	Package	Temperature
9SBV0802AKILF	Tubes	20-pin VFQFPN	-40° to +85°C
9SBV0802AKILFT	Tape and Reel	20-pin VFQFPN	-40° to +85°C

“LF” to the suffix denotes Pb-Free configuration, RoHS compliant.

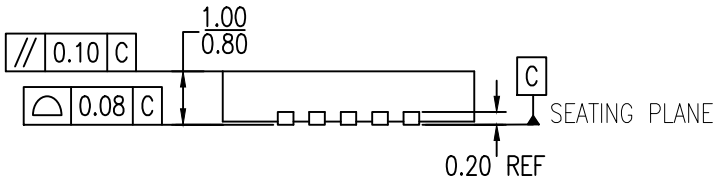
“A” is the device revision designator (will not correlate with the datasheet revision).

Revision History

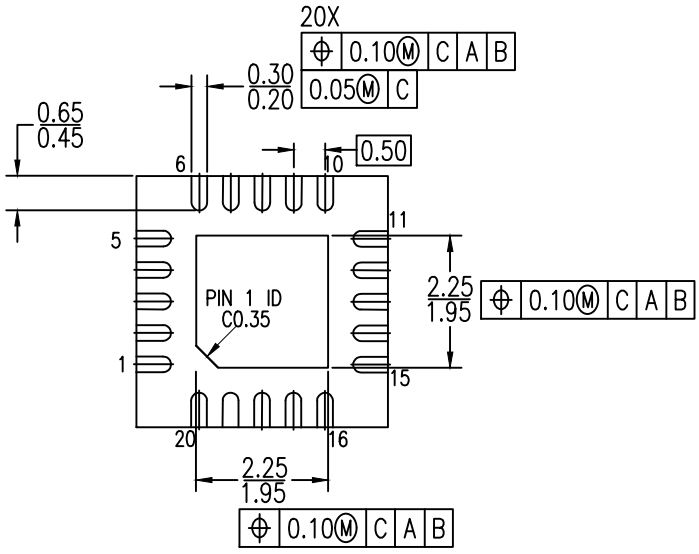
Revision Date	Description
April 21, 2020	1. Removed input duty cycle specification, it is not needed. 2. Removed mention of bypass mode from footnote 2 of Output Duty Cycle, Jitter and Skew Characteristics table.
October 3, 2019	1. Updated measurement conditions of input clock slew rate to specify 40% to 60% of VREF. 2. Removed erroneous references to footnote 2 and duplicate footnote 1.
December 15, 2016	Updated POD drawings with latest showing 2.1 mm SQ. EPAD (PSC-4170-01).
December 15, 2015	1. Update front page text. 2. Add Applications Diagram. 3. Update Electrical tables with characterization data. 4. Added "Output Duty Cycle, Jitter, and Skew Characteristics" Table 5. Correct pin description for pin 9. 6. Move to final.
September 22, 2015	1. Corrected polarity of OE inputs to be active low instead of active high. 2. Added 2pF test loads in addition to 4.7pF. 3. Updated electrical tables with preliminary data. 4. Updated block diagram with proper OE polarity. 5. Moved from Advance to Preliminary.



TOP VIEW



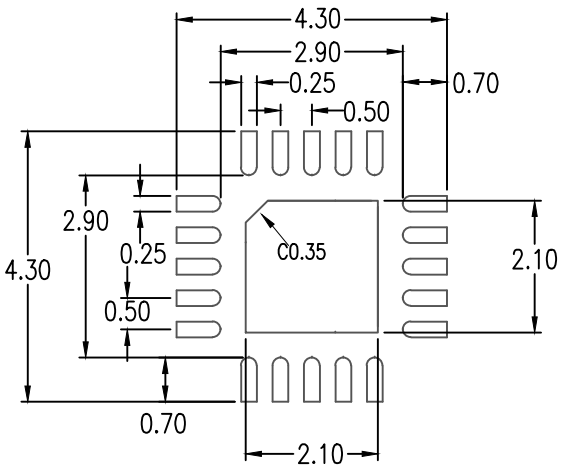
SIDE VIEW



BOTTOM VIEW

NOTES:
1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. ALL DIMENSIONING AND TOLERANCING CONFROM TO ANSI Y14.5M–1982.

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RECOMMENDED LAND PATTERN DIMENSION

NOTES:
1. ALL DIMENSIONING AND TOLERANCING CONFORM TO ANSI Y14.5M–1994
2. ALL DIMENSONS ARE IN MILLIMETERS
3. LAND PATTERN RECOMMENDATION PER IPC–7351B GENERIC REQUIREMENT FOR SURFACE MOUNT DESIGN AND LAND PATTERN

Package Revision History		
Date Created	Rev No.	Description
March 1, 2018	Rev 01	New Format, Add P1, Re-calculate Land Pattern
May 19, 2016	Rev 00	Initial Release

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