General Description

The 9VRS4818B is a 1.5V Core main clock synthesizer chip for AMD Fusion platform. An SMBus interface allows full control of the device.

Recommended Application

Very Low Power Clock Generator for AMD Fusion II Platforms

Input/Output Features

- Low power differential outputs with integrated series resistors for Zo=50ohm systems
- 12 - Differential PCIe Gen2 SRC pairs w/dedicated CLKREQ# pins
- 3 - Differential PCIe Gen2 SATA_DISPLAY pairs w/microspread capability
- 2 - 48MHz USB clocks (180 degrees out of phase for EMI reduction)
- 2 - 14.318MHz REF clock outputs
- 1 - 25MHz LAN clock output that can run from VDD suspend rail
- 1 - CkPwrGd/WOL_STOP#
- 1 - VDD_SUSPEND pin
- 1- RESET_IN# pin

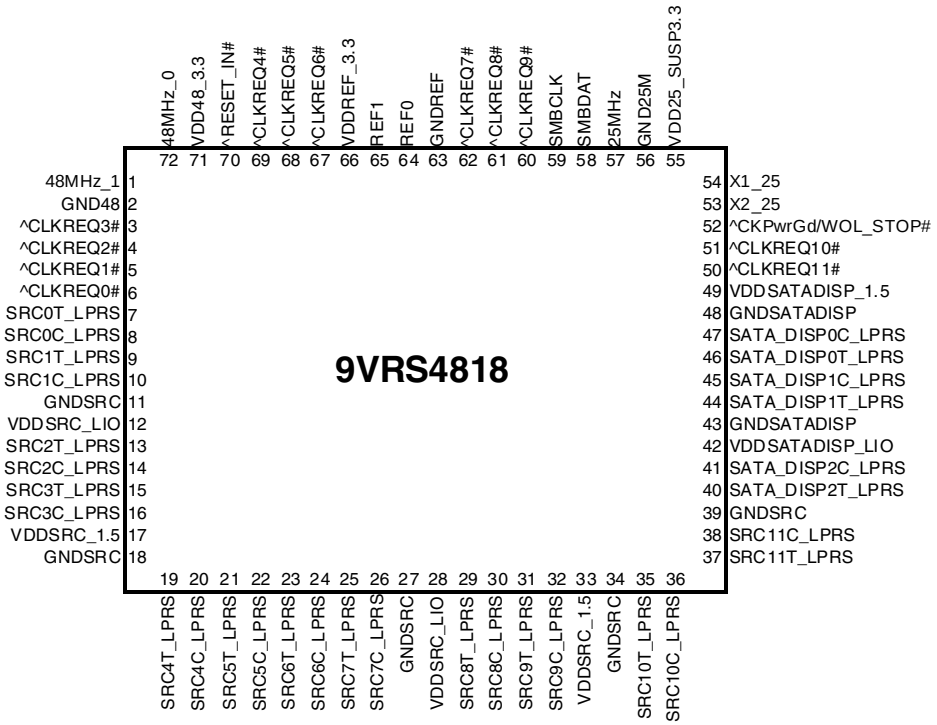
Features/Benefits

- 1.5V Core for minimal Power consumption
- Spread Spectrum for EMI reduction
- Outputs may be disabled via SMBus
- External crystal load capacitors for maximum frequency accuracy

Key Specifications

- SRC/SATA_DISP output cycle-to-cycle jitter < 125ps
- 14.318MHz output cycle-to-cycle jitter < 200ps
- 48MHz output cycle-to-cycle jitter < 130ps
- SRC/SATA_DISP output phase jitter < 3.1ps rms (PCIe Gen2)
- +/- 100ppm frequency accuracy on all clocks, (assuming REF is trimmed to 0 ppm)
- 31.5KHz spread modulation frequency; passes USB3.0 compliance test

Pin Configuration



^ Indicates that pin has 100Kohm internal pullup resistor.

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Pin Descriptions

PIN #	PIN NAME	PIN TYPE	DESCRIPTION
1	48MHz_1	OUT	48MHz clock output. (180 degrees out of phase with 48MHz_0)
2	GND48	GND	Ground pin for the 48MHz outputs
3	^CLKREQ3#	IN	Output enable for SRC/PCI Express output pair '3' 0 = enabled, 1 = Low/Low. This pin has a 120K internal pull up resistor.
4	^CLKREQ2#	IN	Output enable for SRC/PCI Express output pair '2' 0 = enabled, 1 = Low/Low. This pin has a 120K internal pull up resistor.
5	^CLKREQ1#	IN	Output enable for SRC/PCI Express output pair '1' 0 = enabled, 1 = Low/Low. This pin has a 120K internal pull up resistor.
6	^CLKREQ0#	IN	Output enable for SRC/PCI Express output pair '0' 0 = enabled, 1 = Low/Low. This pin has a 120K internal pull up resistor.
7	SRC0T_LPRS	OUT	True clock of low power differential SRC clock pair. (no 50 ohm shunt resistor to GND and no 33 ohm series resistor needed)
8	SRC0C_LPRS	OUT	Complement clock of low power differential SRC clock pair. (no 50 ohm shunt resistor to GND and no 33 ohm series resistor needed)
9	SRC1T_LPRS	OUT	True clock of low power differential SRC clock pair. (no 50 ohm shunt resistor to GND and no 33 ohm series resistor needed)
10	SRC1C_LPRS	OUT	Complement clock of low power differential SRC clock pair. (no 50 ohm shunt resistor to GND and no 33 ohm series resistor needed)
11	GNDSRC	GND	Ground pin for the SRC outputs
12	VDDSRC_LIO	PWR	Supply for SRC outputs, 1.05V to 1.5V nominal
13	SRC2T_LPRS	OUT	True clock of low power differential SRC clock pair. (no 50 ohm shunt resistor to GND and no 33 ohm series resistor needed)
14	SRC2C_LPRS	OUT	Complement clock of low power differential SRC clock pair. (no 50 ohm shunt resistor to GND and no 33 ohm series resistor needed)
15	SRC3T_LPRS	OUT	True clock of low power differential SRC clock pair. (no 50 ohm shunt resistor to GND and no 33 ohm series resistor needed)
16	SRC3C_LPRS	OUT	Complement clock of low power differential SRC clock pair. (no 50 ohm shunt resistor to GND and no 33 ohm series resistor needed)
17	VDDSRC_1.5	PWR	Supply for SRC core and outputs, 1.5V nominal
18	GNDSRC	GND	Ground pin for the SRC outputs
19	SRC4T_LPRS	OUT	True clock of low power differential SRC clock pair. (no 50 ohm shunt resistor to GND and no 33 ohm series resistor needed)
20	SRC4C_LPRS	OUT	Complement clock of low power differential SRC clock pair. (no 50 ohm shunt resistor to GND and no 33 ohm series resistor needed)
21	SRC5T_LPRS	OUT	True clock of low power differential SRC clock pair. (no 50 ohm shunt resistor to GND and no 33 ohm series resistor needed)
22	SRC5C_LPRS	OUT	Complement clock of low power differential SRC clock pair. (no 50 ohm shunt resistor to GND and no 33 ohm series resistor needed)
23	SRC6T_LPRS	OUT	True clock of low power differential SRC clock pair. (no 50 ohm shunt resistor to GND and no 33 ohm series resistor needed)
24	SRC6C_LPRS	OUT	Complement clock of low power differential SRC clock pair. (no 50 ohm shunt resistor to GND and no 33 ohm series resistor needed)
25	SRC7T_LPRS	OUT	True clock of low power differential SRC clock pair. (no 50 ohm shunt resistor to GND and no 33 ohm series resistor needed)
26	SRC7C_LPRS	OUT	Complement clock of low power differential SRC clock pair. (no 50 ohm shunt resistor to GND and no 33 ohm series resistor needed)
27	GNDSRC	GND	Ground pin for the SRC outputs
28	VDDSRC_LIO	PWR	Supply for SRC outputs, 1.05V to 1.5V nominal
29	SRC8T_LPRS	OUT	True clock of low power differential SRC clock pair. (no 50 ohm shunt resistor to GND and no 33 ohm series resistor needed)
30	SRC8C_LPRS	OUT	Complement clock of low power differential SRC clock pair. (no 50 ohm shunt resistor to GND and no 33 ohm series resistor needed)
31	SRC9T_LPRS	OUT	True clock of low power differential SRC clock pair. (no 50 ohm shunt resistor to GND and no 33 ohm series resistor needed)
32	SRC9C_LPRS	OUT	Complement clock of low power differential SRC clock pair. (no 50 ohm shunt resistor to GND and no 33 ohm series resistor needed)
33	VDDSRC_1.5	PWR	Supply for SRC core and outputs, 1.5V nominal
34	GNDSRC	GND	Ground pin for the SRC outputs
35	SRC10T_LPRS	OUT	True clock of low power differential SRC clock pair. (no 50 ohm shunt resistor to GND and no 33 ohm series resistor needed)
36	SRC10C_LPRS	OUT	Complement clock of low power differential SRC clock pair. (no 50 ohm shunt resistor to GND and no 33 ohm series resistor needed)

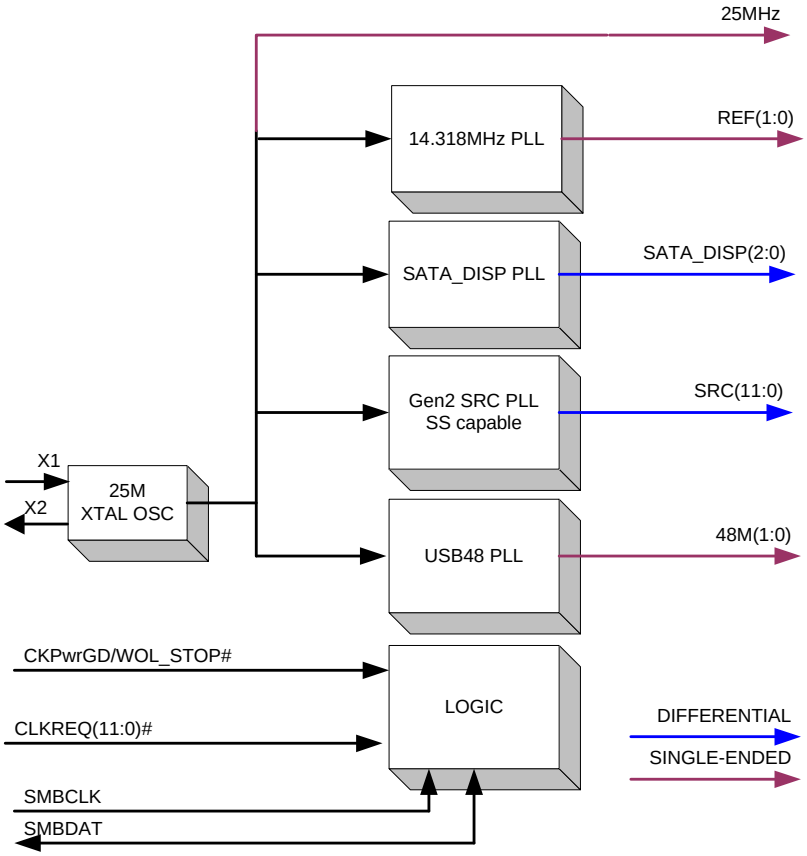
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Pin Descriptions (cont.)

PIN #		PIN TYPE	DESCRIPTION
37	SRC11T_LPRS	OUT	True clock of low power differential SRC clock pair. (no 50 ohm shunt resistor to GND and no 33 ohm series resistor needed)
38	SRC11C_LPRS	OUT	Complement clock of low power differential SRC clock pair. (no 50 ohm shunt resistor to GND and no 33 ohm series resistor needed)
39	GNDSRC	GND	Ground pin for the SRC outputs
40	SATA_DISP2T_LPRS	OUT	True clock of low power differential SATA_DISPlay clock pair. (no 50 ohm shunt resistor to GND and no 33 ohm series resistor needed)
41	SATA_DISP2C_LPRS	OUT	Complement clock of low power differential SATA_DISPlay clock pair. (no 50 ohm shunt resistor to GND and no 33 ohm series resistor needed)
42	VDDSATADISP_LIO	PWR	Supply for SATA_DISPlay outputs, 1.05V to 1.5V nominal
43	GNDSATADISP	GND	Ground pin for the SATA_DISPlay outputs
44	SATA_DISP1T_LPRS	OUT	True clock of low power differential SATA_DISPlay clock pair. (no 50 ohm shunt resistor to GND and no 33 ohm series resistor needed)
45	SATA_DISP1C_LPRS	OUT	Complement clock of low power differential SATA_DISPlay clock pair. (no 50 ohm shunt resistor to GND and no 33 ohm series resistor needed)
46	SATA_DISP0T_LPRS	OUT	True clock of low power differential SATA_DISPlay clock pair. (no 50 ohm shunt resistor to GND and no 33 ohm series resistor needed)
47	SATA_DISP0C_LPRS	OUT	Complement clock of low power differential SATA_DISPlay clock pair. (no 50 ohm shunt resistor to GND and no 33 ohm series resistor needed)
48	GNDSATADISP	GND	Ground pin for the SATA_DISPlay outputs
49	VDDSATADISP_1.5	PWR	Supply for SATA_DISPlay core and outputs, 1.5V nominal
50	^CLKREQ11#	IN	Output enable for SRC/PCI Express output pair '11' 0 = enabled, 1 = Low/Low. This pin has a 120K internal pull up resistor.
51	^CLKREQ10#	IN	Output enable for SRC/PCI Express output pair '10' 0 = enabled, 1 = Low/Low. This pin has a 120K internal pull up resistor.
52	^CKPwrGd/WOL_STOP#	IN	This devices powers up the clock chip and latched strap pins when asserted high. When asserted low, the clock is powered down except for the 25M output, if VDD25_SUSP3.3 is maintained. 0 = Power Down, 1 = normal operation.
53	X2_25	OUT	Crystal output, nominally 25MHz
54	X1_25	IN	Crystal input, nominally 25MHz
55	VDD25_SUSP3.3	PWR	Power pin for the 25M output and XTAL oscillator. This pin allows the 25MHz output when the rest of the power is collapsed and VttPwrGd/WOL_ STOP# is low.
56	GND25M	GND	Ground pin for the 25MHz output and XTAL oscillator circuit
57	25MHz	OUT	25MHz clock output.
58	SMBDAT	I/O	Data pin for SMBus circuitry, 5V tolerant.
59	SMBCLK	IN	Clock pin of SMBus circuitry, 5V tolerant.
60	^CLKREQ9#	IN	Output enable for SRC/PCI Express output pair '9' 0 = enabled, 1 = Low/Low. This pin has a 120K internal pull up resistor.
61	^CLKREQ8#	IN	Output enable for SRC/PCI Express output pair '8' 0 = enabled, 1 = Low/Low. This pin has a 120K internal pull up resistor.
62	^CLKREQ7#	IN	Output enable for SRC/PCI Express output pair '7' 0 = enabled, 1 = Low/Low. This pin has a 120K internal pull up resistor.
63	GNDREF	GND	Ground pin for the REF outputs.
64	REF0	OUT	14.318 MHz reference clock, 3.3V
65	REF1	OUT	14.318 MHz reference clock, 3.3V
66	VDDREF_3.3	PWR	Ref, XTAL power supply, nominal 3.3V
67	^CLKREQ6#	IN	Output enable for SRC/PCI Express output pair '6' 0 = enabled, 1 = Low/Low. This pin has a 120K internal pull up resistor.
68	^CLKREQ5#	IN	Output enable for SRC/PCI Express output pair '5' 0 = enabled, 1 = Low/Low. This pin has a 120K internal pull up resistor.
69	^CLKREQ4#	IN	Output enable for SRC/PCI Express output pair '4' 0 = enabled, 1 = Low/Low. This pin has a 120K internal pull up resistor.
70	^RESET_IN#	OD I/O	As an input it resets the device to the power up default state. As an output, it is driven low when the internal watchdog hardware timer expires. It is cleared when the internal watchdog hardware timer is reset or disabled. The input is falling edge triggered. 0 = Restore Settings, 1 = normal operation.
71	VDD48_3.3	PWR	Power pin for the 48MHz and SIO outputs and core. 3.3V
72	48MHz_0	OUT	48MHz clock output.

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Block Diagram



Power Groups

Pin Number				Description
VDD3.3	VDD1.5	VDD_LIO	GND	
	17, 33	12, 28,	11, 18, 27, 34, 39	Power for SRC PLL and Outputs
	49	42	43, 48	Power for SATA_DISP PLL and Outputs
	47		50	Power for HTT output
66			63	Power for REF PLL and Outputs
55			56	Power for XTAL osc.and 25M outputs
71			2	Power for 48MHz PLL and outputs.

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SATA_DISP Frequency Selection Table

Line	SATA_DISP FS4 Byte 3, Bit 4	SATA_DISP FS3 Byte 3, Bit 3	SATA_DISP FS2 Byte 3, Bit2	SATA_DISP FS1 Byte 3, Bit1	SATA_DISP FS0 Byte 3, Bit0	SATA_DISP Speed (MHz)	Spread %
0	0	0	0	0	0	91.25	
1	0	0	0	0	1	91.25	
2	0	0	0	1	0	92.50	
3	0	0	0	1	1	92.50	
4	**0**	**0**	**1**	**0**	**0**	93.75	
5	0	0	1	0	1	93.75	
6	0	0	1	1	0	95.00	
7	0	0	1	1	1	95.00	
8	0	1	0	0	0	96.25	
9	0	1	0	0	1	96.25	
10	0	1	0	1	0	97.50	
11	0	1	0	1	1	97.50	
12	0	1	1	0	0	98.75	
13	0	1	1	0	1	98.75	
14	0	1	1	1	0	100.00	
15	**0**	**1**	**1**	**1**	**1**	100.00	N/A
16	1	0	0	0	0	100.00	
17	1	0	0	0	1	100.00	
18	1	0	0	1	0	101.25	
19	1	0	0	1	1	101.25	
20	1	0	1	0	0	102.50	
21	1	0	1	0	1	102.50	
22	1	0	1	1	0	103.75	
23	1	0	1	1	1	103.75	
24	1	1	0	0	0	105.00	
25	1	1	0	0	1	105.00	
26	1	1	0	1	0	106.25	
27	1	1	0	1	1	106.25	
28	1	1	1	0	0	107.50	
29	1	1	1	0	1	107.50	
30	1	1	1	1	0	108.75	
31	1	1	1	1	1	108.75	

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SRC Spread Selection Table

Line	SS Type Byte 4, Bit 4	SS Range Byte 4, Bit 3	SRC SS_EN Byte 4, Bit2	SRC FS1 Byte 4, Bit1	SRC FS0 Byte 4, Bit0	SRC Speed (MHz)	Spread %
0	0	0	0	0	0	100.00	
1	0	0	0	0	1	100.00	SS OFF
2	0	0	0	1	0	100.00	0%
3	0	0	0	1	1	100.00	
4	0	0	1	0	0	100.00	-0.49
5	0	0	1	0	1	100.00	-0.45
6	0	0	1	1	0	100.00	-0.40
7	0	0	1	1	1	100.00	-0.35
8	0	1	0	0	0	100.00	
9	0	1	0	0	1	100.00	SS OFF
10	0	1	0	1	0	100.00	0%
11	0	1	0	1	1	100.00	
12	0	1	1	0	0	100.00	-0.3
13	0	1	1	0	1	100.00	-0.25
14	0	1	1	1	0	100.00	-0.25
15	0	1	1	1	1	100.00	-0.25
16	1	0	0	0	0	100.00	
17	1	0	0	0	1	100.00	SS OFF
18	1	0	0	1	0	100.00	0%
19	1	0	0	1	1	100.00	
20	1	0	1	0	0	100.00	+/-0.25
21	1	0	1	0	1	100.00	+/-0.225
22	1	0	1	1	0	100.00	+/-0.20
23	1	0	1	1	1	100.00	+/-0.175
24	1	1	0	0	0	100.00	
25	1	1	0	0	1	100.00	SS OFF
26	1	1	0	1	0	100.00	0%
27	1	1	0	1	1	100.00	
28	1	1	1	0	0	100.00	+/-0.15
29	1	1	1	0	1	100.00	+/-0.125
30	1	1	1	1	0	100.00	+/-0.125
31	1	1	1	1	1	100.00	+/-0.125

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Absolute Maximum Ratings

Stresses above the ratings listed below can cause permanent damage to the 9VRS4818B. These ratings, which are standard values for IDT commercially rated parts, are stress ratings only. Functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods can affect product reliability. Electrical parameters are guaranteed only over the recommended operating temperature range.

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	Notes
I/O Supply Voltage	VDDxxx_LIO	-		1.05	GND+1.9V	V	1
1.5V Core Supply Voltage	VDDxxx_1.5	-		1.5	GND+1.9V	V	1
3.3V Core Supply Voltage	VDDxxx_3.3	-		3.3	GND+3.8V	V	1
Storage Temperature	Ts	-	-65		150	°C	1
Ambient Operating Temp	Tambient	-	0		70	°C	1
Case Temperature	Tcase	-			115	°C	1
Input ESD protection	ESD prot	Human Body Model	2000			V	1

[1]Guaranteed by design and characterization, not 100% tested in production.

Electrical Characteristics–USB - 48MHz

PARAMETER	SYMBOL	CONDITIONS*	MIN	TYP	MAX	UNITS	NOTES
Long Accuracy	ppm	see Tperiod min-max values	-100	0	100	ppm	1
Clock period	T_{PERIOD}	USB output nominal	20.831	20.833	20.836	ns	1,3
Clock Low Time	T_{LOW}	Measure from < 0.6V	9.375	10.400	11.458	ns	1
Clock High Time	T_{HIGH}	Measure from > 2.0V	9.375	10.750	11.458	ns	1
Output High Voltage	V_{OH}	I_{OH} = -1 mA	2.4	2.8	3.3	V	1
Output Low Voltage	V_{OL}	I_{OL} = 1 mA	0		0.4	V	1
Rise Time	t_{r_USB}	V_{OL} = 20% of Voh, V_{OH} = 80%of Voh	0.5	1.9	3	ns	1
Fall Time	t_{f_USB}	V_{OL} = 20% of Voh, V_{OH} = 80%of Voh	0.5	2	3	ns	1
Output High Voltage	V_{OHUSB1}	I_{OH} = -1 mA	2.4			V	1
Output Low Voltage	V_{OLUSB1}	I_{OL} = 1 mA			0.4	V	1
Output High Voltage	V_{OHUSB2}	I_{OH} = -0.2 mA	1.8	2	2.2	V	1
Output Low Voltage	V_{OLUSB2}	I_{OL} = 0.2 mA			0.4	V	1
Skew(out of phase)	t_{SKEW}	V_T = 1.5 V		240	250	ps	1,4
Jitter, Cycle to cycle	$t_{jCYC-CYC}$	V_T = 1.5 V		115	130	ps	1,2
Jitter, Short Term	$t_{jSHORT-TERM}$	V_T = 1.5 V, integrated from 10MHz to 250Mhz	-100		100	ps	1,2
Jitter, Long Term	$t_{jLONG-TERM}$	V_T = 1.5 V, integrated from 0.1MHz to 10Mhz	-30		30	ps	1,2,3
Duty Cycle	d_{CYCUSB}	V_T = 1.5 V	45	50	55	%	1

*TA = 0 - 70°C; Supply Voltage VDD = 3.3 V +/-5%

[1]Guaranteed by design and characterization, not 100% tested in production.

[2]IDT recommended and/or chipset vendor layout guidelines must be followed to meet this specification

[3] All Long Term Accuracy and Clock Period specifications are guaranteed assuming that 25MHz output is at 25MHz

[4]USB outputs are 180 degrees out of phase.

[5]The Ncycle jitter (N periods after trigger) must not exceed +/- 130 ps for any N-cuycle inside a winder starting at trigger and finsihing 100ns after trigger. (N=1..4)

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Electrical Characteristics–Input/Supply/Common Output Parameters

PARAMETER	SYMBOL	CONDITIONS*	MIN	TYP	MAX	UNITS	Notes
I/O Supply Voltage	VDDxxx_LIO	-	0.9975	1.05	1.1025	V	1
1.5V Core Supply Voltage	VDDxxx_1.5	-	1.425	1.5	1.575	V	1
3.3V Core Supply Voltage	VDDxxx_3.3	-	3.135	3.3	3.465	V	1
Input High Voltage	V_{IH}	3.3V Inputs	2		V_{DD} + 0.3	V	1, 3
Input Low Voltage	V_{IL}	3.3V inputs	V_{SS} - 0.3		0.8	V	1, 3
Input High Current	I_{IH}	V_{IN} = V_{DD}	-5		5	uA	1
Input Low Current	I_{IL1}	V_{IN} = 0 V; Inputs with no pull-up resistors	-5			uA	1
	I_{IL2}	V_{IN} = 0 V; Inputs with pull-up resistors	-200			uA	1
Suspend Current	$I_{DD_3.3SUSP}$	WOL_STOP (25M) Enabled in Power Down			10	mA	1
	$I_{DD_1.5SUSP}$				1	mA	1
	$I_{DD_I/OSUSP}$				1	mA	1
Power Down Current	$I_{DD_3.3PD}$	WOL_STOP (25M) Disabled in Power down			2	mA	1
	$I_{DD_1.5PD}$				1	mA	1
	$I_{DD_I/OPD}$				0.1	mA	1
Operating Current	$I_{DD_3.3}$	all outputs driven			30	mA	1
	$I_{DD_1.5}$				30	mA	1
	$I_{DD_I/O}$				70	mA	1
Input Frequency	F_i	VDD = 3.3 V +/-5%		25.00		MHz	2
Pin Inductance	L_{pin}				7	nH	1
Input Capacitance	C_{IN}	Logic Inputs			5	pF	1
	C_{OUT}	Output pin capacitance			6	pF	1
	C_{INX}	X1 & X2 pins			5	pF	1
Clk Stabilization	T_{STAB}	From VDD Power-Up to 1st clock			1.8	ms	1
Modulation Frequency		Triangular Modulation	31	31.500	32	kHz	1
Tdrive_PD		SATA_DISP output enable after PD de-assertion			300	us	1
Tfall_PD		PD fall time of			5	ns	1
Trise_PD		PD rise time of			5	ns	1
SMBus Voltage	V_{DDSMB}		2.7		5.5	V	1
Low-level Output Voltage	V_{OLSMB}	@ I_{PULLUP}			0.4	V	1
Current sinking at V_{OL} = 0.4 V	$I_{PULLUPSMB}$		4	6		mA	1
SMBCLK/SMBDAT Clock/Data Rise Time	T_{RSMB}	(Max VIL - 0.15) to (Min VIH + 0.15)			1000	ns	1
SMBCLK/SMBDAT Clock/Data Fall Time	T_{FSMB}	(Min VIH + 0.15) to (Max VIL - 0.15)			300	ns	1

*TA = 0 - 70°C; All Supply Voltages at nominal+/-5%

[1]Guaranteed by design and characterization, not 100% tested in production.

[2] Input frequency should be measured at the 25M output pin and tuned to ideal 25MHz to meet ppm frequency accuracy on PLL outputs.

[3] CLKREQ# Inputs are 3.3V tolerant

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AC Electrical Characteristics–Low-Power DIF Outputs: SATA_DISP and SRC

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	NOTES
SRC/SATA Frequency	f_{SRC_SATA}	Spread Specturm Off		100		MHz	1,6
Long Term Accuracy	ppm	Spread Specturm Off	-100	0	+100	ppm	1,6
Rising Edge Slew Rate	t_{SLR}	Differential Measurement	0.6	3.5	4	V/ns	1,2
Falling Edge Slew Rate	t_{FLR}	Differential Measurement	0.6	3.5	4	V/ns	1,2
Slew Rate Variation	t_{SLVAR}	Single-ended Measurement		10	20	%	1
Maximum Output Voltage	V_{HIGH}	Includes overshoot		925	1150	mV	1
Minimum Output Voltage	V_{LOW}	Includes undershoot	-300	-50		mV	1
Differential Voltage Swing	V_{SWING}	Differential Measurement	300	1950		mV	1
Crossing Point Voltage	V_{XABS}	Single-ended Measurement	300	445	550	mV	1,3,4
Crossing Point Variation	$V_{XABSVAR}$	Single-ended Measurement		28	140	mV	1,3,5
Duty Cycle	t_{dCYC}	Differential Measurement	47	50	53	%	1
Jitter - Cycle to Cycle	$t_{jCYC-CYC}$	Differential Measurement		55	125	ps	1
SRC[11:0] Skew Even Outputs	$t_{SRCSKEW_E}$	Differential Measurement		46	200	ps	1,8
SRC[11:0] Skew Odd Outputs	$t_{SRCSKEW_O}$	Differential Measurement		60	200	ps	1,8
SRC[11:0] Even to Odd Skew	$t_{SRCSKEW}$	Differential Measurement		1.925		ns	1,8
Jitter - SSC Residual	t_{SSC_RES}	Differential Measurement		10	75	ps	1
Jitter, Phase	t_{jphase}	PCIe Gen 1 specs (1.5 - 22 MHz)		38	86	ps	1, 7
		PCIe Gen 2 (8-16 MHz, 5-16 MHz) Lo-band content (10kHz to 1.5MHz)		1.5	3	ps rms	1, 7
		PCIe Gen 2 (8-16 MHz, 5-16 MHz) Hi-band content (1.5MHz to Nyquist)		2.4	3.1	ps rms	1, 7
SSC	$t_{jphaseSRC}$	Default Spread when enabled			-0.49	%	1, 9
		Spread Option 1			-0.48	%	1, 9
		Spread Option 2			-0.47	%	1, 9
		Spread Option 3			-0.46	%	1, 9

*TA = 0 - 70°C; All Supply Voltages at nominal+/-5%

[1]Guaranteed by design and characterization, not 100% tested in production.

[2] Slew rate measured through Vswing centered around differential zero

[3] Vxabs is defined as the voltage where CLK = CLK#

[4] Only applies to the differential rising edge (CLK rising and CLK# falling)

[5] Defined as the total variation of all crossing voltages of CLK rising and CLK# falling. Matching applies to rising edge rate of CLK and falling edge of CLK#. It is measured using a +/-75mV window centered on the average cross point where CLK meets CLK#.

[6] All Long Term Accuracy and Clock Period specifications are guaranteed assuming that 25MHz output is at 25MHz

[7] Applicable to all SRC outputs. See http://www.pcisig.com for complete specs. Guaranteed by design/characterization, not tested in production.

[8] SRC outputs are divided into two banks, odd and even. The odd bank skew window is 200 ps. The even bank skew window is 200ps. The skew between the even and odd banks is intentionally set at 1.925 ns.

[9] Only applies to SRC outputs. SATA_DISP outputs do not spread.

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Electrical Characteristics–REF-14.318MHz

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	Notes
Long Accuracy	ppm	see Tperiod min-max values	-50	0	50	ppm	1,2
Long Term Jitter	t_{jLT}	@ 10us		200	500	ps	1,2,3
Clock period	T_{PERIOD}	14.318MHz output nominal		69.8413		ns	2
Clock Low Time	T_{LOW}	Measure from V_T = 50%	2	33		ns	2
Clock High Time	T_{HIGH}	Measure from V_T = 50%	2	34		ns	2
Output High Voltage	V_{OH}	I_{OH} = -1 mA	2.4	2.8	3.3	V	1
Output Low Voltage	V_{OL}	I_{OL} = 1 mA	0		0.4	V	1
Rise Time	t_R	V_{OL} = 20% of V_{OH}, V_{OH} = 80%of V_{OH}		1.2	1.5	ns	1
Fall Time	t_F	V_{OL} = 20% of V_{OH}, V_{OH} = 80%of V_{OH}		1.2	1.5	ns	1
Skew	t_{SKEW}	Measure from V_T = 50%		71	250	ps	1
Duty Cycle	d_{t1}	$V_T = V_{OH}/2$	45	50	55	%	1
Jitter, Cycle to Cycle	$t_{jCYC-CYC}$	Measure from V_T = 50%		125	200	ps	1,3
Jitter, Peak to Peak	t_{jPK-PK}	Measure from V_T = 50% (0.9V) $t_{jpk-pk} = [\|t_{jcyc-cyc}max\| + \|t_{jcyc-cyc}min\|]/2$		100	200	ps	1,3

*TA = 0 - 70°C; Supply Voltage VDD = 3.3 V +/-5%

[1]Guaranteed by design and characterization, not 100% tested in production.

[2] All Long Term Accuracy and Clock Period specifications are guaranteed assuming that 25MHz output is at 25MHz

[3]IDT recommended and/or chipset vendor layout guidelines must be followed to meet this specification

Electrical Characteristics–25MHz

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	Notes
Long Accuracy	ppm	see Tperiod min-max values	-50	0	50	ppm	1,2
Long Term Jitter	t_{jLT}	@ 10us		200	250	ps	1,2,3
Clock period	T_{PERIOD}	25MHz XTAL output nominal		40.0000		ns	2
Clock Low Time	T_{LOW}	Measure from V_T = 50%	2	16.6		ns	2
Clock High Time	T_{HIGH}	Measure from V_T = 50%	2	17.2		ns	2
Output High Voltage	V_{OH}	I_{OH} = -1 mA	2.4	2.8	3.3	V	1
Output Low Voltage	V_{OL}	I_{OL} = 1 mA	0		0.4	V	1
Rise Time	t_R	V_{OL} = 10% of V_{OH}, V_{OH} = 90%of V_{OH}		2.4	3	ns	1
Fall Time	t_F	V_{OL} = 10% of V_{OH}, V_{OH} = 90%of V_{OH}		2.4	3	ns	1
Duty Cycle	d_{t1}	V_T = 50%	45	48	55	%	1
Jitter, Cycle to Cycle	$t_{jCYC-CYC}$	Measure from V_T = 50%		180	200	ps	1,3
Jitter, Peak to Peak	t_{jPK-PK}	Measure from V_T = 50% $t_{jpk-pk} = [\|t_{jcyc-cyc}max\| + \|t_{jcyc-cyc}min\|]/2$		160	200	ps	1,3

*TA = 0 - 70°C; Supply Voltage VDD = 3.3 V +/-5%

[1]Guaranteed by design and characterization, not 100% tested in production.

[2] All Long Term Accuracy and Clock Period specifications are guaranteed assuming that 25MHz output is at 25MHz

[3]IDT recommended and/or chipset vendor layout guidelines must be followed to meet this specification

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General SMBus Serial Interface Information for 9VRS4818B

How to Write

- Controller (host) sends a start bit
- Controller (host) sends the write address
- IDT clock will **acknowledge**
- Controller (host) sends the beginning byte location = N
- IDT clock will **acknowledge**
- Controller (host) sends the byte count = X
- IDT clock will **acknowledge**
- Controller (host) starts sending Byte **N through Byte N+X-1**
- IDT clock will **acknowledg**e each byte **one at a time**
- Controller (host) sends a Stop bit

Index Block Write Operation			
Controller (Host)			**IDT (Slave/Receiver)**
T	starT bit		
Slave Address			
WR	WRite		
			ACK
Beginning Byte = N			
			ACK
Data Byte Count = X			
			ACK
Beginning Byte N		X Byte	
			ACK
O			
O			O
O			O
			O
Byte N + X - 1			
			ACK
P	stoP bit		

Read Address	Write Address
$D3_{(H)}$	$D2_{(H)}$

How to Read

- Controller (host) will send a start bit
- Controller (host) sends the write address
- IDT clock will **acknowledge**
- Controller (host) sends the beginning byte location = N
- IDT clock will **acknowledge**
- Controller (host) will send a separate start bit
- Controller (host) sends the read address
- IDT clock will **acknowledge**
- IDT clock will send the data byte count = X
- IDT clock sends Byte **N+X-1**
- IDT clock sends **Byte 0 through Byte X (if $X_{(H)}$ was written to Byte 8)**
- Controller (host) will need to acknowledge each byte
- Controller (host) will send a not acknowledge bit
- Controller (host) will send a stop bit

Index Block Read Operation			
Controller (Host)			**IDT (Slave/Receiver)**
T	starT bit		
Slave Address			
WR	WRite		
			ACK
Beginning Byte = N			
			ACK
RT	Repeat starT		
Slave Address			
RD	ReaD		
			ACK
			Data Byte Count=X
ACK			
		X Byte	Beginning Byte N
ACK			
			O
O			O
O			O
O			
			Byte N + X - 1
N	Not acknowledge		
P	stoP bit		

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Byte SMBus Table: Output Enable Control Register

0	Name	Description	Type	0	1	Default
Bit 7	25M_OE	Output Enable	RW	Low	Enabled	1
Bit 6	REF1_OE	Output Enable	RW	Low	Enabled	1
Bit 5	REF0_OE	Output Enable	RW	Low	Enabled	1
Bit 4	SATA_DISP2_OE	Output Enable	RW	Low/Low	Enabled	1
Bit 3	SATA_DISP1_OE	Output Enable	RW	Low/Low	Enabled	1
Bit 2	SATA_DISP0_OE	Output Enable	RW	Low/Low	Enabled	1
Bit 1	48MHz_1_OE	Output Enable	RW	Low	Enabled	1
Bit 0	48MHz_0_OE	Output Enable	RW	Low	Enabled	1

Byte SMBus Table:CKLREQ and Output Control Register

1	Name	Control Function	Type	0	1	Default
Bit 7	CLKREQ7	CLKREQ 7controls SRC7	RW	Does not control	Controls	0
Bit 6	CLKREQ6	CLKREQ6 controls SRC6	RW	Does not control	Controls	0
Bit 5	CLKREQ5	CLKREQ5 controls SRC5	RW	Does not control	Controls	0
Bit 4	CLKREQ4	CLKREQ4 controls SRC4	RW	Does not control	Controls	0
Bit 3	SRC11_OE	Output Enable	RW	Low/Low	Enabled	1
Bit 2	SRC10_OE	Output Enable	RW	Low/Low	Enabled	1
Bit 1	SRC9_OE	Output Enable	RW	Low/Low	Enabled	1
Bit 0	SRC8_OE	Output Enable	RW	Low/Low	Enabled	1

Byte SMBus Table: Output Enable Control Register

2	Name	Control Function	Type	0	1	Default
Bit 7	SRC7_OE	Output Enable	RW	Low/Low	Enabled	1
Bit 6	SRC6_OE	Output Enable	RW	Low/Low	Enabled	1
Bit 5	SRC5_OE	Output Enable	RW	Low/Low	Enabled	1
Bit 4	SRC4_OE	Output Enable	RW	Low/Low	Enabled	1
Bit 3	SRC3_OE	Output Enable	RW	Low/Low	Enabled	1
Bit 2	SRC2_OE	Output Enable	RW	Low/Low	Enabled	1
Bit 1	SRC1_OE	Output Enable	RW	Low/Low	Enabled	1
Bit 0	SRC0_OE	Output Enable	RW	Low/Low	Enabled	1

Byte SMBus Table: SATA_DISP/HTT Frequency and Output Enable Control Register

3	Name	Control Function	Type	0	1	Default
Bit 7	CLKREQ3	CLKREQ3 controls SRC3	RW	Does not control	Controls	0
Bit 6	CLKREQ2	CLKREQ2 controls SRC2	RW	Does not control	Controls	0
Bit 5	WOL_EN	Enables 25M output in Suspend State	RW	25M does not run when VDD_SUSP is present and WOL_STOP# = 0	25M does RUNS when VDD_SUSP is present and WOL_STOP# = 0	1
Bit 4	SATA_DISP_FS4	SATA_DISP Freq. Select MSB	RW	See SATA_DISP Frequency Select Table		0
Bit 3	SATA_DISP_FS3	SATA_DISP Freq. Select	RW			1
Bit 2	SATA_DISP_FS2	SATA_DISP Freq. Select	RW			1
Bit 1	SATA_DISP_FS1	SATA_DISP Freq. Select	RW			1
Bit 0	SATA_DISP_FS0	SATA_DISP Freq. Select LSB	RW			1

Byte SMBus Table: SRC Frequency Control Register

4	Name	Control Function	Type	0	1	Default
Bit 7	CLKREQ1	CLKREQ1 controls SRC1	RW	Does not control	Controls	0
Bit 6	CLKREQ0	CLKREQ0 controls SRC0	RW	Does not control	Controls	0
Bit 5	Reserved					0
Bit 4	SRC SS TYPE	Down or Center Spread	RW	Down	Center	0
Bit 3	SRC_SS_RNG	Normal or Low Range	RW	Normal	Low Range (<0.25%)	0
Bit 2	SRC_SS_EN	SRC Spread Enable	RW	Off	On	0
Bit 1	SRC_SS_SEL1	SRC Spread Amount	RW	See SRC Spread Select Table		0
Bit 0	SRC_SS_SEL0	SRC Spread Amount	RW	Default Corresponds to 100MHz.		0

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Byte **SMBus Table: I/O Vout and M/N Enable Register**

5	Name	Control Function	Type	0	1	Default
Bit 7	Reserved					0
Bit 6	SATA_DISP M/N En	SATA_DISP PLL M/N Prog. Enable	RW	M/N Prog. Disabled	M/N Prog. Enabled	0
Bit 5	SRC M/N En	SRC M/N Prog.Enable	RW	M/N Prog. Disabled	M/N Prog. Enabled	0
Bit 4	Test_Sel	Selects Test Type	RW	Outputs are Tri-state	Outputs are REF/4	0
Bit 3	Test_Mode	Enable Test Mode	RW	Normal mode	Enable Test Mode	0
Bit 2	IO_VOUT2	IO Output Voltage Select (Most Significant Bit)	RW	100 = 0.7V 110 = 0.9V	101 = 0.8V 111 = 1.0V	1
Bit 1	IO_VOUT1	IO Output Voltage Select	RW			0
Bit 0	IO_VOUT0	IO Output Voltage Select (Least Significant Bit)	RW			1

Byte **SMBus Table: Byte Count Register**

6	Name	Control Function	Type	0	1	Default
Bit 7	Reserved					0
Bit 6	Reserved					0
Bit 5	Reserved					0
Bit 4	BC4	Byte Count bit 4	RW	Determines the number of bytes that are read back from the device. Default is 08 hex.		0
Bit 3	BC3	Byte Count bit 3	RW			1
Bit 2	BC2	Byte Count bit 2	RW			0
Bit 1	BC1	Byte Count bit 1	RW			0
Bit 0	BC0	Byte Count bit 0 (LSB)	RW			0

Byte **SMBus Table: Device ID register**

7	Name	Control Function	Type	0	1	Default
Bit 7	Device ID7	Device ID	**R**	18 hex for 9VRS4818		0
Bit 6	Device ID6		**R**			0
Bit 5	Device ID5		**R**			0
Bit 4	Device ID4		**R**			1
Bit 3	Device ID3		**R**			1
Bit 2	Device ID2		**R**			0
Bit 1	Device ID1		**R**			0
Bit 0	Device ID0		**R**			0

Byte **SMBus Table: Vendor & Revision ID Register**

8	Name	Control Function	Type	0	1	Default
Bit 7	RID3	REVISION ID	**R**	Rev B = 0001		x
Bit 6	RID2		**R**			x
Bit 5	RID1		**R**			x
Bit 4	RID0		**R**			x
Bit 3	VID3	VENDOR ID	**R**	IDT/ICS = 0001		0
Bit 2	VID2		**R**			0
Bit 1	VID1		**R**			0
Bit 0	VID0		**R**			1

Byte **SMBus Table: WatchDog Timer Control Register**

9	Name	Control Function	Type	0	1	Default
Bit 7	HWD_EN	Watchdog Hard Alarm Enable	RW	Disable and Reload Hartd Alarm Timer, Clear WD Hard status bit.	Enable Timer	0
Bit 6	SWD_EN	Watchdog Soft Alarm Enable	RW	Disable	Enable	0
Bit 5	WD Hard Status	WD Hard Alarm Status	**R**	Normal	Alarm	X
Bit 4	WD Soft Status	WD Soft Alarm Status	**R**	Normal	Alarm	X
Bit 3	WDTCtrl	Watch Dog Alarm Time base Control	RW	290ms Base	1160ms Base	0
Bit 2	HWD2	WD Hard Alarm Timer Bit 2	RW	These bits represent the number of Watch Dog Time Base Units that pass before the Watch Alarm expires. Default is 7 X 290ms = 2s.		1
Bit 1	HWD1	WD Hard Alarm Timer Bit 1	RW			1
Bit 0	HWD0	WD Hard Alarm Timer Bit 0	RW			1

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Byte SMBus Table: WD Timer Safe Frequency Control Register

10	Name	Control Function	Type	0	1	Default
Bit 7	SWD2	WD Soft Alarm Timer Bit 2	RW	These bits represent the number of Watch Dog Time Base Units that pass before the Watch Alarm expires. Default is 7 X 290ms = 2s.		1
Bit 6	SWD1	WD Soft Alarm Timer Bit 1	RW			1
Bit 5	SWD0	WD Soft Alarm Timer Bit 0	RW			1
Bit 4	Reserved					0
Bit 3	Reserved					0
Bit 2	Reserved					1
Bit 1	Reserved					0
Bit 0	Reserved					0

Byte SMBus Table: CLKREQ8 and 9 Control Register

11	Name	Control Function	Type	0	1	Default
Bit 7	Reserved					0
Bit 6	Reserved					0
Bit 5	Reserved					0
Bit 4	Reserved					0
Bit 3	CLKREQ11	CLKREQ11 controls SRC11	RW	Does not control	Controls	0
Bit 2	CLKREQ10	CLKREQ10 controls SRC10	RW	Does not control	Controls	0
Bit 1	CLKREQ9	CLKREQ9 controls SRC09	RW	Does not control	Controls	0
Bit 0	CLKREQ8	CLKREQ8 controls SRC8	RW	Does not control	Controls	0

Byte SMBus Table: SATA_DISP PLL Frequency Control Register

12	Name	Control Function	Type	0	1	Default
Bit 7	N Div2	N Divider Prog bit 2	RW	The decimal representation of M and N Divider in Byte 12 and 13 will configure the VCO frequency. Contact IDT for the M/N Calculation Tables for VCO frequency formulas.		X
Bit 6	N Div1	N Divider Prog bit 1	RW			X
Bit 5	M Div5	M Divider Programming bits	RW			X
Bit 4	M Div4		RW			X
Bit 3	M Div3		RW			X
Bit 2	M Div2		RW			X
Bit 1	M Div1		RW			X
Bit 0	M Div0		RW			X

Byte SMBus Table: SATA_DISP PLL Frequency Control Register

13	Name	Control Function	Type	0	1	Default
Bit 7	N Div10	N Divider Programming b(10:3)	RW	The decimal representation of M and N Divider in Byte 12 and 13 will configure the VCO frequency. Contact IDT for the M/N Calculation Tables for VCO frequency formulas.		X
Bit 6	N Div9		RW			X
Bit 5	N Div8		RW			X
Bit 4	N Div7		RW			X
Bit 3	N Div6		RW			X
Bit 2	N Div5		RW			X
Bit 1	N Div4		RW			X
Bit 0	N Div3		RW			X

Byte SMBus Table: Slew Rate Control Register

14	Name	Control Function	Type	0	1	Default
Bit 7	Reserved					0
Bit 6	Reserved					0
Bit 5	Reserved					0
Bit 4	Reserved					0
Bit 3	Reserved					0
Bit 2	Reserved					0
Bit 1	25M SLEW1	25M Slew Rate Control MSB	RW	00 = 1.3V/ns, 01 = 1.9V/ns		0
Bit 0	25M SLEW0	25M Slew Rate Control LSB	RW	10 = 2.5V/ns, 11 = 2.9V/ns		0

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Byte SMBus Table:Slew Rate Control Register

15	Name	Control Function	Type	0	1	Default
Bit 7	48M_1 SLEW1	48M_1 Slew Rate Control	RW	00 = 1.3V/ns, 01 = 1.9V/ns		0
Bit 6	48M_1 SLEW0	48M_1 Slew Rate Control	RW	10 = 2.5V/ns, 11 = 2.9V/ns		0
Bit 5	48M_0 SLEW1	48M_0 Slew Rate Control	RW	00 = 1.3V/ns, 01 = 1.9V/ns		0
Bit 4	48M_0 SLEW0	48M_0 Slew Rate Control	RW	10 = 2.5V/ns, 11 = 2.9V/ns		0
Bit 3	REF1 SLEW1	REF1 Slew Rate Control MSB	RW	00 = 1.3V/ns, 01 = 1.9V/ns		0
Bit 2	REF1 SLEW0	REF1 Slew Rate Control LSB	RW	10 = 2.5V/ns, 11 = 2.9V/ns		1
Bit 1	REF0 SLEW1	REF0 Slew Rate Control MSB	RW	00 = 1.3V/ns, 01 = 1.9V/ns		0
Bit 0	REF0 SLEW0	REF0 Slew Rate Control LSB	RW	10 = 2.5V/ns, 11 = 2.9V/ns		1

Byte SMBUS Table: SRC Frequency Control Register

16	Name	Control Function	Type	0	1	Default
Bit 7	N Div2	N Divider Prog bit 2	RW	The decimal representation of M and N Divider in Byte 16 and 17 configure the SRC VCO frequency. Contact IDT for M/N Calculation Tables for VCO frequency formulas.		X
Bit 6	N Div1	N Divider Prog bit 1	RW			X
Bit 5	M Div5	M Divider Programming bit (5:0)	RW			X
Bit 4	M Div4		RW			X
Bit 3	M Div3		RW			X
Bit 2	M Div2		RW			X
Bit 1	M Div1		RW			X
Bit 0	M Div0		RW			X

Byte SMBUS Table: SRC Frequency Control Register

17	Name	Control Function	Type	0	1	Default
Bit 7	N Div10	N Divider Programming Byte16 bit(7:0) and Byte15 bit(7:6)	RW	The decimal representation of M and N Divider in Byte 16 and 17 configure the SRC VCO frequency. Contact IDT for M/N Calculation Tables for VCO frequency formulas.		X
Bit 6	N Div9		RW			X
Bit 5	N Div8		RW			X
Bit 4	N Div7		RW			X
Bit 3	N Div6		RW			X
Bit 2	N Div5		RW			X
Bit 1	N Div4		RW			X
Bit 0	N Div3		RW			X

Byte SMBUS Table: SRC Spread Spectrum Control Register

18	Name	Control Function	Type	0	1	Default
Bit 7	SSP7	Spread Spectrum Programming bit(7:0)	RW	These bits set the SRC spread pecentages.Please contact IDT for the appropriate values.		X
Bit 6	SSP6		RW			X
Bit 5	SSP5		RW			X
Bit 4	SSP4		RW			X
Bit 3	SSP3		RW			X
Bit 2	SSP2		RW			X
Bit 1	SSP1		RW			X
Bit 0	SSP0		RW			X

Byte SMBUS Table: SRC Spread Spectrum Control Register

19	Name	Control Function	Type	0	1	Default
Bit 7	SSP15	Spread Spectrum Programming bit(15:8)	RW	These bits set the SRC spread pecentages.Please contact IDT for the appropriate values.		X
Bit 6	SSP14		RW			X
Bit 5	SSP13		RW			X
Bit 4	SSP12		RW			X
Bit 3	SSP11		RW			X
Bit 2	SSP10		RW			X
Bit 1	SSP9		RW			X
Bit 0	SSP8		RW			X

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Byte SMBUS Table: SRC PLL NDiv0 Output Divider and Single Ended Output Slew Rate Control Register

20	Name	Control Function	Type	0	1	Default
Bit 7	SRC NDiv0	LSB N Divider Programming	RW	N Divider LSB (bit 0) for SRC M/N programming.		X
Bit 6	Reserved					0
Bit 5	Reserved					0
Bit 4	Reserved					1
Bit 3	Reserved					1
Bit 2	Reserved					0
Bit 1	Reserved					1
Bit 0	Reserved					1

Byte SMBUS Table: SATA_DISP PLL NDiv0 and SATA_DISP Output Divider Register

21	Name	Control Function	Type	0	1	Default
Bit 7	SATA_DISP NDiv0	LSB N Divider Programming	RW	N Divider LSB (bit 0) for SATA_DISP M/N programming.		X
Bit 6	Reserved					0
Bit 5	Reserved					0
Bit 4	Reserved					1
Bit 3	Reserved					1
Bit 2	SATA_DISPDiv2	SATA_DISP Divider Ratio Programming Bits	RW	000 = /2	001 = /3	0
Bit 1	SATA_DISPDiv1		RW	010= /4	011 = /5	1
Bit 0	SATA_DISPDiv0		RW	100 = /7	101 - 111 = /1	1

Bytes 22 to 63 Are Reserved

Clock Periods Differential Outputs with Spread Spectrum Enabled

Measurement Window		1 Clock	1us	0.1s	0.1s	0.1s	1us	1 Clock		
Symbol		Lg-	-SSC	-ppm error	0ppm	+ ppm error	+SSC	Lg+		
Definition		Absolute Period	Short-term Average	Long-Term Average	Period	Long-Term Average	Short-term Average	Period		
		Minimum Absolute Period	Minimum Absolute Period	Minimum Absolute Period	Nominal	Maximum	Maximum	Maximum	Units	Notes
Signal Name	SRC	9.87400	9.99900	9.99900	10.00000	10.00100	10.05130	10.17630	ns	1,2

Clock Periods Differential Outputs with Spread Spectrum Disabled

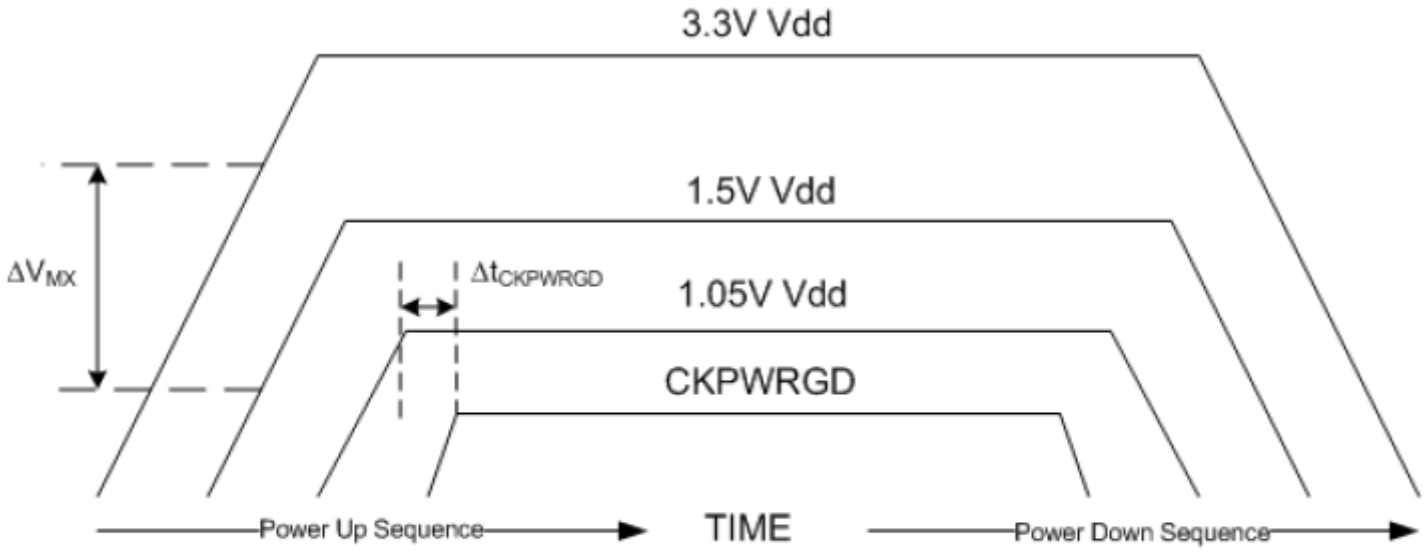
Measurement Window		1 Clock	1us	0.1s	0.1s	0.1s	1us	1 Clock		
Symbol		Lg-	-SSC	-ppm error	0ppm	+ ppm error	+SSC	Lg+		
Definition		Absolute Period	Short-term Average	Long-Term Average	Period	Long-Term Average	Short-term Average	Period		
		Minimum Absolute Period	Minimum Absolute Period	Minimum Absolute Period	Nominal	Maximum	Maximum	Maximum	Units	Notes
Signal Name	SRC/SATA_DISP	9.87400		9.99900	10.00000	10.00100		10.17630	ns	1,2

[1]Guaranteed by design and characterization, not 100% tested in production.

[2] All Long Term Accuracy and Clock Period specifications are guaranteed assuming that 25MHz output is at 25MHz

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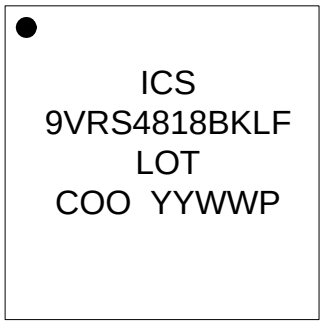
Power-up Sequence Requirement



Notes:

1. The maximum difference (ΔV_{MX}) between any two voltages is 0.7V if the lower power supply is powered up first.
2. There are no timing requirements between the higher and lower voltages if the higher voltages power up first.
3. The minimum time before CKPWRGD can be set ($\Delta t_{CKPWRGD} = 0$) is 0 sec from the last power supply that is powered up.

Marking Diagram

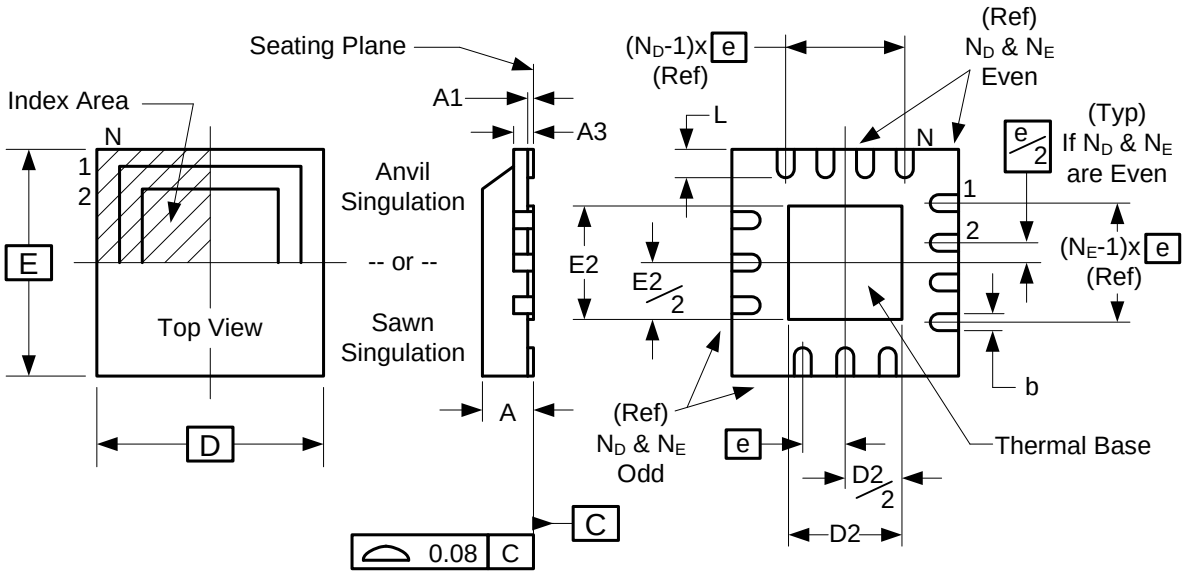


Notes:

1. “LOT” is the lot code.
2. “COO” denotes country of origin.
3. YYWW is the last two digits of the year and week that the part was assembled.
4. “LF” designates RoHS compliant package.

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Package Outline and Package Dimensions (72-pin MLF)



	Millimeters	
Symbol	**Min**	**Max**
A	0.8	1.0
A1	0	0.05
A3	0.25 Reference	
b	0.18	0.3
e	0.50 BASIC	
D x E BASIC	10.00 x 10.00	
D2 MIN./MAX.	5.75	6.15
E2 MIN./MAX.	5.75	6.15
L MIN./MAX.	0.3	0.5
N_D	18	
N_E	18	

Ordering Information

Part / Order Number	Shipping Packaging	Package	Temperature
9VRS4818BKLF	Trays	72-pin MLF	0 to +70° C
9VRS4818BKLF8	Tape and Reel	72-pin MLF	0 to +70° C

"LF" suffix to the part number are the Pb-Free configuration and are RoHS compliant.

“B” is the device revision designator (will not correlate with the datasheet revision).

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Revision History

Rev.	Issue Date	Who	Description	Page #
A	6/25/2012	RDW	1. Corrected Differential Vswing value. 2. Updates to all electrical tables. 3. Move to final	

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