Description

The 9Z61195D is a second-generation, enhanced-performance DB1900Z derivative differential buffer. The part is a pin-compatible upgrade to the 9Z61195A, offering much improved phase jitter performance. A fixed external feedback maintains low drift for critical QPI/UPI applications. In fanout mode, the 9Z61195D meets the DB2000Q additive phase jitter specification.

PCIe Clocking Architectures

- Common Clocked (CC)
- Independent Reference (IR) with and without spread spectrum

Typical Applications

- Servers
- Storage
- Networking
- SSDs

Output Features

- 19 Low-Power (LP) HCSL output pairs with 85Ω Zout

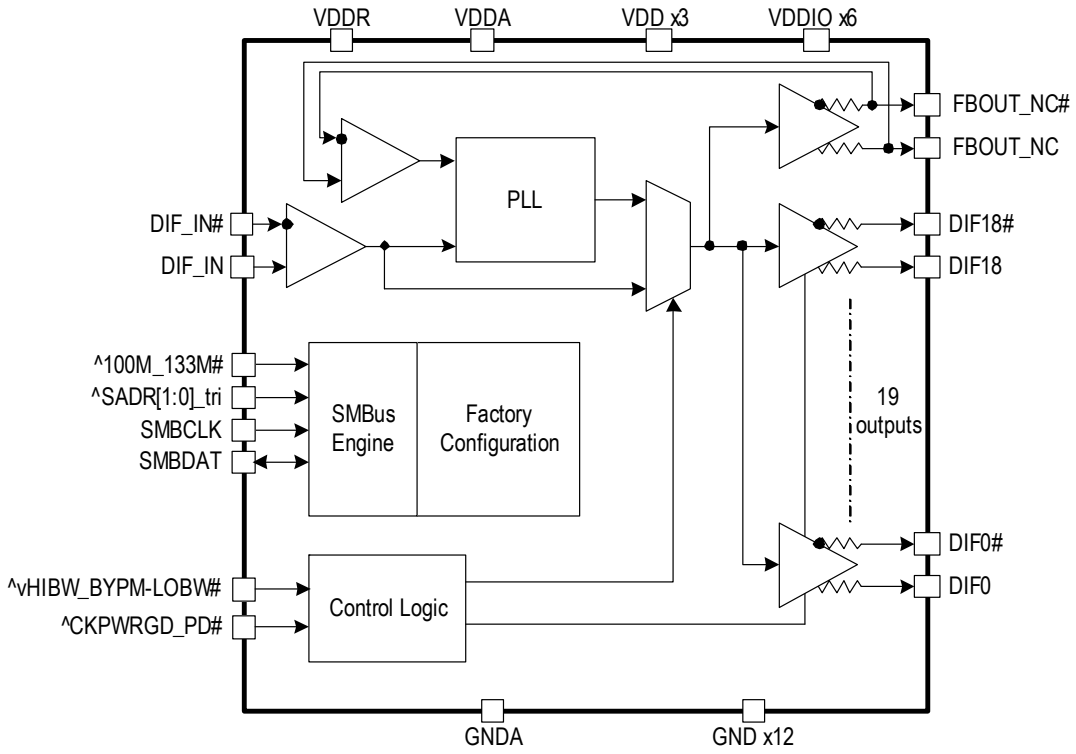
Features

- LP-HCSL outputs with 85Ω Zout; eliminate 76 resistors, save 130mm^2 of area
- SMBus OE bits; software control of each output
- 9 selectable SMBus addresses; multiple devices can share same SMBus segment
- Selectable PLL bandwidths; minimizes jitter peaking in cascaded PLL topologies
- Hardware/SMBus control of PLL bandwidth and bypass; change mode without power cycle
- Spread spectrum compatible; tracks spreading input clock for EMI reduction
- 10 × 10 mm 72-VFQFPN package; small board footprint

Key Specifications

- Cycle-to-cycle jitter: < 50ps
- Output-to-output skew: < 50ps
- Input-to-output delay: Fixed at 0ps
- Input-to-output delay variation: < 50ps
- Additive Phase jitter: PCIe Gen4 < 53fs rms
- Additive Phase jitter: IF-UPI < 70fs rms
- Additive Phase jitter: DB2000Q filter < 30fs rms

Block Diagram

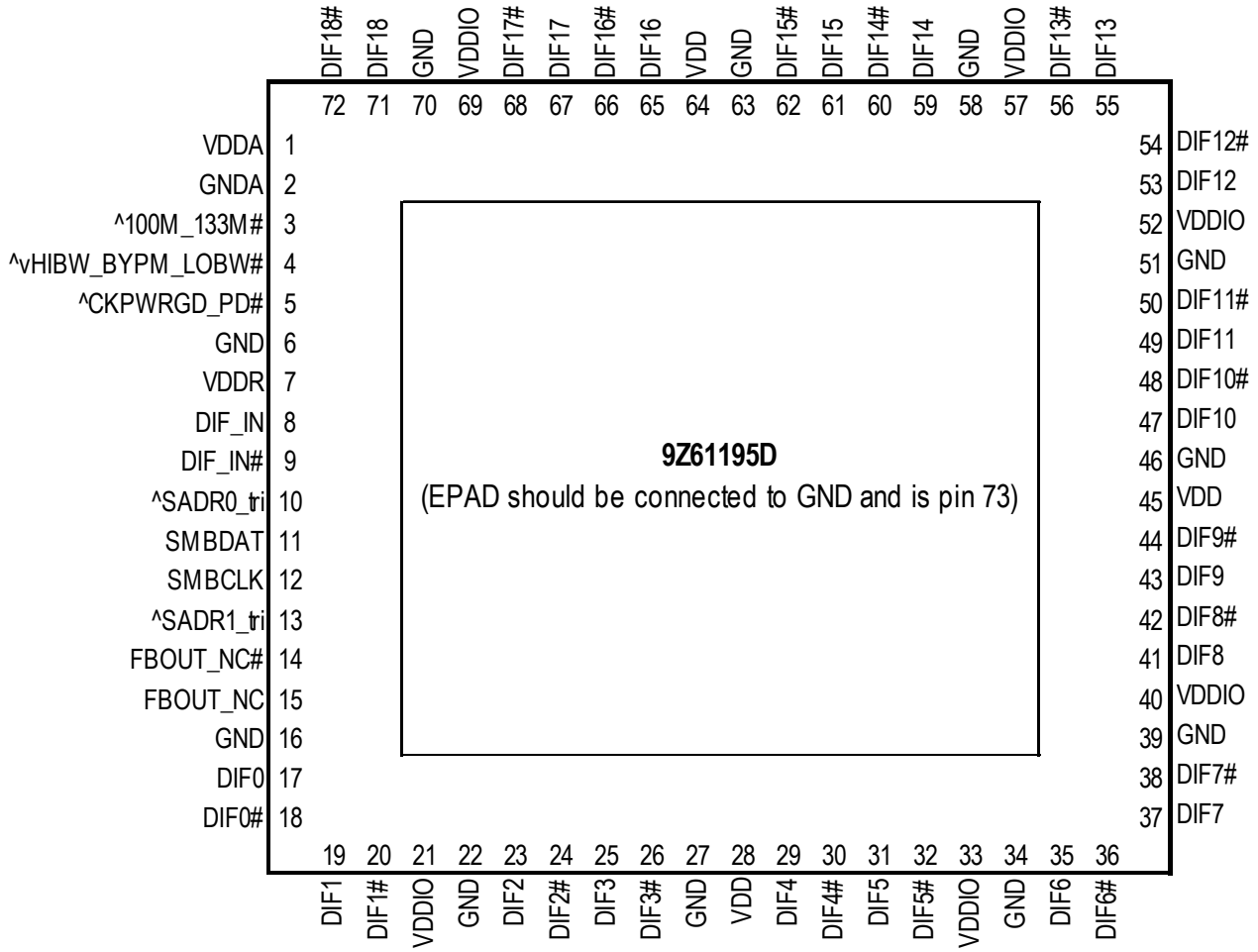


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Pin Assignments

Figure 1. Pin Assignments for 10 × 10 mm 72-VFQFPN Package – Top View



10 x 10 mm 72-VFQFPN

Notes: Pins with ^ prefix have internal 120kohm pull-up
Pins with v prefix have internal 120kohm pull-down
Pins with ^v prefix have internal 120kohm pull-up/pull-down (biased to VDD/2)

Pin Descriptions

Table 1. Pin Descriptions

Number	Name	Type	Description
1	V_{DDA}	Power	Power supply for PLL core.
2	GNDA	GND	Ground pin for the PLL core.
3	^100M_133M#	Latched In	3.3V input to select operating frequency. This pin has an internal 120kΩ pull-up resistor. See *Functionality* table for definition.
4	^vHIBW_BYPM_LOBW#	Latched In	Tri-level input to select High BW, Bypass or Low BW mode. This pin is biased to $V_{DD}/2$ (Bypass Mode) with internal pull up/pull down resistors. See *PLL Operating Mode* table for details.
5	^CKPWRGD_PD#	Input	Input notifies device to sample latched inputs and start up on first high assertion. Low enters Power Down Mode, subsequent high assertions exit Power Down Mode. This pin has internal 120kΩ pull-up resistor.
6	GND	GND	Ground pin.
7	V_{DDR}	Power	Power supply for differential input clock (receiver). This V_{DD} should be treated as an analog power rail and filtered appropriately. Nominally 3.3V.
8	DIF_IN	Input	HCSL true input.
9	DIF_IN#	Input	HCSL complementary input.
10	^SADR0_tri	Input	SMBus address bit. This is a tri-level input that works in conjunction with other SADR pins, if present, to decode SMBus addresses. It has an internal 120kΩ pull-up resistor. See the *SMBus Address Selection* table.
11	SMBDAT	I/O	Data pin of SMBUS circuitry.
12	SMBCLK	Input	Clock pin of SMBUS circuitry.
13	^SADR1_tri	Input	SMBus address bit. This is a tri-level input that works in conjunction with other SADR pins, if present, to decode SMBus addresses. It has an internal 120kΩ pull-up resistor. See the *SMBus Address Selection* table.
14	FBOUT_NC#	Output	Complementary half of differential feedback output. This pin should NOT be connected to anything outside the chip. It exists to provide delay path matching to get 0 propagation delay.
15	FBOUT_NC	Output	True half of differential feedback output. This pin should NOT be connected to anything outside the chip. It exists to provide delay path matching to get 0 propagation delay.
16	GND	GND	Ground pin.
17	DIF0	Output	Differential true clock output.
18	DIF0#	Output	Differential complementary clock output.
19	DIF1	Output	Differential true clock output.
20	DIF1#	Output	Differential complementary clock output.
21	V_{DDIO}	Power	Power supply for differential outputs.
22	GND	GND	Ground pin.
23	DIF2	Output	Differential true clock output.
24	DIF2#	Output	Differential complementary clock output.
25	DIF3	Output	Differential true clock output.

Table 1. Pin Descriptions (Cont.)

Number	Name	Type	Description
26	DIF3#	Output	Differential complementary clock output.
27	GND	GND	Ground pin.
28	V_{DD}	Power	Power supply, nominally 3.3V.
29	DIF4	Output	Differential true clock output.
30	DIF4#	Output	Differential complementary clock output.
31	DIF5	Output	Differential true clock output.
32	DIF5#	Output	Differential complementary clock output.
33	V_{DDIO}	Power	Power supply for differential outputs.
34	GND	GND	Ground pin.
35	DIF6	Output	Differential true clock output.
36	DIF6#	Output	Differential complementary clock output.
37	DIF7	Output	Differential true clock output.
38	DIF7#	Output	Differential complementary clock output.
39	GND	GND	Ground pin.
40	V_{DDIO}	Power	Power supply for differential outputs.
41	DIF8	Output	Differential true clock output.
42	DIF8#	Output	Differential complementary clock output.
43	DIF9	Output	Differential true clock output.
44	DIF9#	Output	Differential complementary clock output.
45	V_{DD}	Power	Power supply, nominally 3.3V.
46	GND	GND	Ground pin.
47	DIF10	Output	Differential true clock output.
48	DIF10#	Output	Differential complementary clock output.
49	DIF11	Output	Differential true clock output.
50	DIF11#	Output	Differential complementary clock output.
51	GND	GND	Ground pin.
52	V_{DDIO}	Power	Power supply for differential outputs.
53	DIF12	Output	Differential true clock output.
54	DIF12#	Output	Differential complementary clock output.
55	DIF13	Output	Differential true clock output.
56	DIF13#	Output	Differential complementary clock output.
57	V_{DDIO}	Power	Power supply for differential outputs.
58	GND	GND	Ground pin.
59	DIF14	Output	Differential true clock output.
60	DIF14#	Output	Differential complementary clock output.
61	DIF15	Output	Differential true clock output.

Table 1. Pin Descriptions (Cont.)

Number	Name	Type	Description
62	DIF15#	Output	Differential complementary clock output.
63	GND	GND	Ground pin.
64	V_{DD}	Power	Power supply, nominally 3.3V.
65	DIF16	Output	Differential true clock output.
66	DIF16#	Output	Differential complementary clock output.
67	DIF17	Output	Differential true clock output.
68	DIF17#	Output	Differential complementary clock output.
69	V_{DDIO}	Power	Power supply for differential outputs.
70	GND	GND	Ground pin.
71	DIF18	Output	Differential true clock output.
72	DIF18#	Output	Differential complementary clock output.
73	EPAD	GND	Connect EPAD to ground.

Absolute Maximum Ratings

The absolute maximum ratings are stress ratings only. Stresses greater than those listed below can cause permanent damage to the device. Functional operation of the 9Z61195D at absolute maximum ratings is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

Table 2. Absolute Maximum Ratings

Parameter	Symbol	Conditions	Minimum	Typical	Maximum	Units	Notes
Supply Voltage	V_{DDx}				3.9	V	1,2
Input Low Voltage	V_{IL}		GND - 0.5			V	1
Input High Voltage	V_{IH}	Except for SMBus interface.			V_{DD} + 0.5	V	1,3
Input High Voltage	V_{IHSMB}	SMBus clock and data pins.			3.9	V	1
Storage Temperature	Ts		-65		150	°C	1
Junction Temperature	Tj				125	°C	1
Input ESD Protection	ESD prot	Human Body Model.	2000			V	1

[1] Guaranteed by design and characterization, not 100% tested in production.

[2] Operation under these conditions is neither implied nor guaranteed.

[3] Not to exceed 3.9V.

Electrical Characteristics

T_{AMB} = over the specified operating range. Supply voltages per normal operation conditions; see Test Loads for loading conditions.

Table 3. SMBus Parameters

Parameter	Symbol	Conditions	Minimum	Typical	Maximum	Units	Notes
SMBus Input Low Voltage	V_{ILSMB}				0.8	V	
SMBus Input High Voltage	V_{IHSMB}		2.1		V_{DDSMB}	V	
SMBus Output Low Voltage	V_{OLSMB}	At $I_{PULLUP.}$			0.4	V	
SMBus Sink Current	I_{PULLUP}	At $V_{OL.}$	4			mA	
Nominal Bus Voltage	V_{DDSMB}		2.7		3.6	V	1
SCLK/SDATA Rise Time	t_{RSMB}	(Max V_{IL} - 0.15V) to (Min V_{IH} + 0.15V).			1000	ns	1
SCLK/SDATA Fall Time	t_{FSMB}	(Min V_{IH} + 0.15V) to (Max V_{IL} - 0.15V).			300	ns	1
SMBus Operating Frequency	f_{MAXMB}	Maximum SMBus operating frequency.			400	kHz	5

[1] Guaranteed by design and characterization, not 100% tested in production.

[2] Control input must be monotonic from 20% to 80% of input swing.

[3] Time from deassertion until outputs are > 200 mV.

[4] DIF_IN input.

[5] The differential input clock must be running for the SMBus to be active.

Table 4. DIF_IN Clock Input Parameters

Parameter	Symbol	Conditions	Minimum	Typical	Maximum	Units	Notes
Input Crossover Voltage – DIF_IN	V_{CROSS}	Cross over voltage.	150		900	mV	1
Input Swing – DIF_IN	V_{SWING}	Differential value.	300			mV	1
Input Slew Rate – DIF_IN	dv/dt	Measured differentially.	0.35		8	V/ns	1,2
Input Leakage Current	I_{IN}	$V_{IN} = V_{DD}$, V_{IN} = GND.	-5		5	µA	
Input Duty Cycle	d_{tin}	Measurement from differential waveform.	45		55	%	1
Input Jitter –Cycle to Cycle	J_{DIFIn}	Differential measurement.	0		125	ps	1

[1] Guaranteed by design and characterization, not 100% tested in production.

[2] Slew rate measured through ±75mV window centered around differential zero.

Table 5. Input/Supply/Common Parameters

Parameter	Symbol	Conditions	Minimum	Typical	Maximum	Units	Notes
Supply Voltage	$V_{DD}x$	Supply voltage for core and analog.	3.135	3.3	3.465	V	
Output Supply Voltage	V_{DDIO}	Supply voltage for DIF outputs, if present.	0.9975	1.05	3.465	V	
Ambient Operating Temperature	T_{AMB}	Industrial range.	-40	25	85	°C	
Input High Voltage	V_{IH}	Single-ended inputs, except SMBus, tri-level inputs.	2		V_{DD} + 0.3	V	
Input Low Voltage	V_{IL}	Single-ended inputs, except SMBus, tri-level inputs.	GND - 0.3		0.8	V	
Input High Voltage	V_{IH}	Tri-level inputs ("_tri" suffix).	2.2		V_{DD} + 0.3	V	
Input Mid Voltage	V_{IM}	Tri-level inputs ("_tri" suffix).	1.2	$V_{DD}/2$	1.8	V	
Input Low Voltage	V_{IL}	Tri-level inputs ("_tri" suffix).	GND - 0.3		0.8	V	
Input Current	I_{IN}	Single-ended inputs, V_{IN} = GND, V_{IN} = V_{DDx}.	-5		5	µA	
	I_{INP}	Single-ended inputs V_{IN} = 0 V; Inputs with internal pull-up resistors. V_{IN} = $V_{DD;}$ Inputs with internal pull-down resistors.	-50		50	µA	
Input Frequency	F_{IBYP}	Bypass Mode.	1		400	MHz	
	F_{IPLL}	100MHz PLL Mode.	98	100.00	102	MHz	
	F_{IPLL}	133.33MHz PLL Mode.	130	133.33	136	MHz	
Pin Inductance	L_{pin}				7	nH	1
Capacitance	C_{IN}	Logic Inputs, except DIF_IN.	1.5		5	pF	1
	C_{INDIF_IN}	DIF_IN differential clock inputs.	1.5		2.7	pF	1,4
	C_{OUT}	Output pin capacitance.			6	pF	1
Clk Stabilization	t_{STAB}	From V_{DD} power-up and after input clock stabilization or deassertion of PD# to 1st clock.			1.8	ms	1,2
Input SS Modulation Frequency PCIe	$f_{MODINPCIe}$	Allowable frequency for PCIe applications (triangular modulation).	30		33	kHz	
Tdrive_PD#	t_{DRVPD}	DIF output enable after PD# deassertion.			300	µs	1,3
Tfall	t_F	Fall time of control inputs.			5	ns	2
Trise	t_R	Rise time of control inputs.			5	ns	2

[1] Guaranteed by design and characterization, not 100% tested in production.

[2] Control input must be monotonic from 20% to 80% of input swing.

[3] Time from deassertion until outputs are > 200mV, PLL Mode.

[4] DIF_IN input.

Table 6. Current Consumption

Parameter	Symbol	Conditions	Minimum	Typical	Maximum	Units	Notes
Operating Supply Current	I_{DDA+R}	V_{DDA} + V_{DDR} pins, all outputs at 100MHz, C_L = 2pF; Zo = 85Ω.		54	65	mA	
	I_{DDIO}	V_{DDIO} pins, all outputs at 100MHz, C_L = 2pF; Zo = 85Ω.		136	169	mA	
	I_{DDx}	All other V_{DD} pins, all outputs at 100MHz, C_L = 2pF; Zo = 85Ω.		28	38	mA	
Power Down Current	I_{DDA+R}	V_{DDA} + V_{DDR} pins, all outputs Low/Low.		4	5	mA	
	I_{DDIO}	V_{DDIO} pins, all outputs Low/Low.		0.04	0.1	mA	
	I_{DDx}	All other V_{DD} pins, all outputs Low/Low.		0.4	1	mA	

Table 7. Skew and Differential Jitter Parameters

Parameter	Symbol	Conditions	Minimum	Typical	Maximum	Units	Notes
CLK_IN, DIF[x:0]	t_{SPO_PLL}	Input-to-output skew in PLL Mode at 100MHz, nominal temperature and voltage.	-100	22	100	ps	1,2,4, 5,8
CLK_IN, DIF[x:0]	t_{PD_BYP}	Input-to-output skew in Bypass Mode at 100MHz, nominal temperature and voltage.	2.2	2.9	3.5	ns	1,2,3, 5,8
CLK_IN, DIF[x:0]	t_{DSPO_PLL}	Input-to-output skew variation in PLL Mode at 100MHz, across voltage and temperature.	-50	0	50	ps	1,2,3, 5,8
CLK_IN, DIF[x:0]	t_{DSPO_BYP}	Input-to-output skew variation in Bypass Mode at 100MHz, across voltage and temperature, T_{AMB} = -40 to 85°C.	-250		250	ps	1,2,3, 5,8
		Input-to-output skew variation in Bypass Mode at 100MHz, across voltage and temperature, T_{AMB} = -40 to 85°C.	-350		350	ps	1,2,3, 5,8
	t_{DTE}	Random differential tracking error between two 9ZX devices in Hi BW Mode.			5	ps (rms)	1,2,3, 5,8
	t_{DSSTE}	Random differential spread spectrum tracking error between two 9ZX devices in Hi BW Mode.			75	ps	1,2,3, 5,8
DIF[x:0]	t_{SKEW_ALL}	Output-to-output skew across all outputs, common to PLL and Bypass Mode, at 100MHz.		36	50	ps	1,2,3, 8
PLL Jitter Peaking	$j_{peak\text{-}hibw}$	LOBW#_BYPASS_HIBW = 1.	0	1	2.5	dB	7,8
PLL Jitter Peaking	$j_{peak\text{-}lobw}$	LOBW#_BYPASS_HIBW = 0.	0	1	2	dB	7,8
PLL Bandwidth	pll_{HIBW}	LOBW#_BYPASS_HIBW = 1.	2	3	4	MHz	8,9
PLL Bandwidth	pll_{LOBW}	LOBW#_BYPASS_HIBW = 0.	0.7	1	1.4	MHz	8,9
Duty Cycle	t_{DC}	Measured differentially, PLL Mode.	45	50	55	%	1

Table 7. Skew and Differential Jitter Parameters (Cont.)

Parameter	Symbol	Conditions	Minimum	Typical	Maximum	Units	Notes
Duty Cycle Distortion	t_{DCD}	Measured differentially, Bypass Mode at 100MHz.	-1	0	1	%	1,10
Jitter, Cycle to Cycle	$t_{jcyc-cyc}$	PLL Mode.		20	50	ps	1,11
		Additive jitter in Bypass Mode.		3	10	ps	1,11

[1] Measured into fixed 2pF load cap. Input to output skew is measured at the first output edge following the corresponding input.

[2] Measured from differential cross-point to differential cross-point. This parameter can be tuned with external feedback path, if present.

[3] All Bypass Mode input-to-output specs refer to the timing between an input edge and the specific output edge created by it.

[4] This parameter is deterministic for a given device.

[5] Measured with scope averaging on to find mean value.

[6] "t" is the period of the input clock.

[7] Measured as maximum pass band gain. At frequencies within the loop BW, highest point of magnification is called PLL jitter peaking.

[8] Guaranteed by design and characterization, not 100% tested in production.

[9] Measured at 3db down or half power point.

[10] Duty cycle distortion is the difference in duty cycle between the output and the input clock when the device is operated in Bypass Mode.

[11] Measured from differential waveform.

Table 8. DIF HCSL/LP-HCSL Outputs

Parameter	Symbol	Conditions	Minimum	Typical	Maximum	Industry Limits	Units	Notes
Slew Rate	dV/dt	Scope averaging on.	2	2.6	3.5	1 – 4	V/ns	1,2,3
Slew Rate Matching	ΔdV/dt	Slew rate matching, scope averaging on.		10	19	20	%	1,4,7
Maximum Voltage	V_{MAX}	Measurement on single-ended signal using absolute value (scope averaging off).	660	815	876	1150	mV	7
Minimum Voltage	V_{MIN}		-123	-40		-300	mV	7
Crossing Voltage (abs)	V_{CROSS_ABS}	Scope averaging off.	325	397	475	250 – 550	mV	1,5,7
Crossing Voltage (var)	$\Delta\text{-}V_{CROSS}$	Scope averaging off.		27	69	140	mV	1,6,7

[1] Guaranteed by design and characterization, not 100% tested in production.

[2] Measured from differential waveform.

[3] Slew rate is measured through the V_{SWING} voltage range centered around differential 0 V. This results in a ±150mV window around differential 0V.

[4] Matching applies to rising edge rate for Clock and falling edge rate for Clock#. It is measured using a ±75mV window centered on the average cross point where Clock rising meets Clock# falling. The median cross point is used to calculate the voltage thresholds the oscilloscope is to use for the edge rate calculations.

[5] V_{CROSS} is defined as voltage where Clock = Clock# measured on a component test board and only applies to the differential rising edge (i.e. Clock rising and Clock# falling).

[6] The total variation of all V_{CROSS} measurements in any particular system. Note that this is a subset of $V_{CROSS_MIN/MAX}$ (V_{CROSS} absolute) allowed. The intent is to limit V_{CROSS} induced modulation by setting $\Delta\text{-}V_{CROSS}$ to be smaller than V_{CROSS} absolute.

[7] At default SMBus settings.

Table 9. Filtered Phase Jitter Parameters - PCIe Common Clocked (CC) Architectures

Parameter	Symbol	Conditions	Minimum	Typical	Maximum	Industry Limits	Units	Notes
Phase Jitter, PLL Mode	$t_{jphPCIeG1-CC}$	PCIe Gen1		13	34	86	ps (p-p)	1,2,3
	$t_{jphPCIeG2-CC}$	PCIe Gen2 Low Band 10kHz < f < 1.5MHz (PLL BW of 5–16MHz or 8–16MHz, CDR = 5MHz).		0.2	0.63	3	ps (rms)	1,2
		PCIe Gen2 High Band 1.5MHz < f < Nyquist (50MHz) (PLL BW of 5–16MHz or 8–16MHz, CDR = 5MHz).		1.0	1.47	3.1	ps (rms)	1,2
	$t_{jphPCIeG3-CC}$	PCIe Gen3 (PLL BW of 2–4MHz or 2–5MHz, CDR = 10MHz).		0.2	0.34	1	ps (rms)	1,2
	$t_{jphPCIeG4-CC}$	PCIe Gen4 (PLL BW of 2–4MHz or 2–5MHz, CDR = 10MHz).		0.2	0.34	0.5	ps (rms)	1,2
Additive Phase Jitter, Bypass Mode	$t_{jphPCIeG1-CC}$	PCIe Gen1		0.01	0.052	Not Applicable	ps (p-p)	1,2,3,4
	$t_{jphPCIeG2-CC}$	PCIe Gen2 Low Band 10kHz < f < 1.5MHz (PLL BW of 5–16MHz or 8–16MHz, CDR = 5MHz).		0.01	0.052		ps (rms)	1,2,3,4
		PCIe Gen2 High Band 1.5MHz < f < Nyquist (50MHz) (PLL BW of 5–16MHz or 8–16MHz, CDR = 5MHz).		0.0	0.052		ps (rms)	1,2,3,4
	$t_{jphPCIeG3-CC}$	PCIe Gen3 (PLL BW of 2–4MHz or 2–5MHz, CDR = 10MHz).		0.01	0.052		ps (rms)	1,2,3,4
	$t_{jphPCIeG4-CC}$	PCIe Gen4 (PLL BW of 2–4MHz or 2–5MHz, CDR = 10MHz).		0.01	0.052		ps (rms)	1,2,3,4

Table 10. Filtered Phase Jitter Parameters - PCIe Independent Reference (IR) Architectures

Parameter	Symbol	Conditions	Minimum	Typical	Maximum	Industry Limits	Units	Notes
Phase Jitter, PLL Mode	$t_{jphPCIeG2-SRIS}$	PCIe Gen2 (PLL BW of 16MHz, CDR = 5MHz).		0.9	1.05	2	ps (rms)	1,2,5
	$t_{jphPCIeG3-SRIS}$	PCIe Gen3 (PLL BW of 2–4MHz, CDR = 10MHz).		0.6	0.68	0.7	ps (rms)	1,2,5
Additive Phase Jitter, Bypass Mode	$t_{jphPCIeG2-SRIS}$	PCIe Gen2 (PLL BW of 16MHz, CDR = 5MHz).		0.01	0.042	Not Applicable	ps (rms)	1,2,4,5
	$t_{jphPCIeG3-SRIS}$	PCIe Gen3 (PLL BW of 2–4MHz, CDR = 10MHz).		0.01	0.042		ps (rms)	1,2,4,5

Notes for PCIe Filtered Phase Jitter tables (CC) and (IR).

[1] Applies to all differential outputs when driven by 9SQL495x or equivalent, guaranteed by design and characterization.

[2] Calculated from Intel-supplied clock jitter tool when driven by 9SQL495x or equivalent with spread on and off.

[3] Sample size of at least 100K cycles. This figure extrapolates to 108ps pk-pk at 1M cycles for a BER of 1^{-12}.

[4] For RMS values, additive jitter is calculated by solving the following equation for b [$b = sqrt(c^2 - a^2)$] where "a" is rms input jitter and "c" is rms total jitter.

[5] IR is the new name for Separate Reference Independent Spread (SRIS) and Separate Reference no Spread (SRNS) PCIe clock architectures. According to the PCIe Base Specification Rev4.0 version 0.7 draft, the jitter transfer functions and corresponding jitter limits are not defined for the IR clock architecture. Widely accepted industry limits using widely accepted industry filters are used to populate this table. There are no accepted filters or limits for IR clock architectures at PCIe Gen1 or Gen4 data rates.

Table 11. Filtered Phase Jitter Parameters – QPI/UPI

Parameter	Symbol	Conditions	Minimum	Typical	Maximum	Industry Limits	Units	Notes
Phase Jitter, PLL Mode	t_{jphQPI_UPI}	QPI and UPI (100MHz or 133MHz, 4.8Gb/s, 6.4Gb/s 12UI).		0.14	0.25	0.5	ps (rms)	1,2
		QPI and UPI (100MHz, 8.0Gb/s, 12UI).		0.07	0.09	0.3	ps (rms)	1,2
		QPI & UPI (100MHz, ≥ 9.6Gb/s, 12UI).		0.06	0.074	0.2	ps (rms)	1,2
	$t_{jphIF-UPI}$	IF-UPI		0.1 0.17	0.14 0.2	1	ps (rms)	1,4,5

Table 11. Filtered Phase Jitter Parameters – QPI/UPI (Cont.)

Parameter	Symbol	Conditions	Minimum	Typical	Maximum	Industry Limits	Units	Notes
Additive Phase Jitter, Bypass Mode	t_{jphQPI_UPI}	QPI and UPI (100MHz or 133MHz, 4.8Gb/s, 6.4Gb/s 12UI).		0.00	0.01	Not Applicable	ps (rms)	1,2,3
		QPI and UPI (100MHz, 8.0Gb/s, 12UI).		0.00	0.01		ps (rms)	1,2,3
		QPI and UPI (100MHz, ≥ 9.6Gb/s, 12UI).		0.00	0.01		ps (rms)	1,2,3
	$t_{jphIF-UPI}$	IF-UPI		0.06	0.07		ps (rms)	1,4

[1] Applies to all differential outputs, guaranteed by design and characterization.

[2] Calculated from Intel-supplied clock jitter tool when driven by 9SQL495x or equivalent with spread on and off.

[3] Additive jitter for RMS values is calculated by solving for b [$b = sqrt(c^2 - a^2)$] where "a" is rms input jitter and "c" is rms total jitter.

[4] Calculated from phase noise analyzer when driven by Wenzel Associates source with Intel-specified brick-wall filter applied.

[5] Top number is when the buffer is in Low BW mode; bottom number is when the buffer is in High BW mode.

Table 12. Filtered Phase Jitter Parameters – DB2000Q Filter

Parameter	Symbol	Conditions	Minimum	Typical	Maximum	Industry Limits	Units	Notes
Additive Phase Jitter	$t_{jph12k-20Madd}$	100MHz		20	30	80	fs (rms)	1,2

[1] Applies to all outputs when driven by Wenzel Associates source.

[2] For RMS values, additive jitter is calculated by solving for b [$b = sqrt(c^2 - a^2)$] where "a" is rms input jitter and "c" is rms total jitter.

Table 13. Unfiltered Phase Jitter Parameters – 12kHz to 20MHz

Parameter	Symbol	Conditions	Minimum	Typical	Maximum	Industry Limits	Units	Notes
Phase Jitter, PLL Mode	$t_{jph12k-20MHi}$	PLL High BW, SSC Off, 100MHz.		194	233	Not applicable	fs (rms)	1,2
Phase Jitter, PLL Mode	$t_{jph12k-20MLo}$	PLL Low BW, SSC Off, 100MHz.		212	248		fs (rms)	1,2
Additive Phase Jitter, Bypass Mode	$t_{jph12k-20MByp}$	Bypass Mode, SSC Off, 100MHz.		105	124		fs (rms)	1,2,3

[1] Applies to all outputs when driven by Wenzel Associates source.

[2] 12kHz to 20MHz brick wall filter.

[3] For RMS values, additive jitter is calculated by solving for b [$b = sqrt(c^2 - a^2)$] where "a" is rms input jitter and "c" is rms total jitter.

Power Management

Inputs		Control Bits	Outputs		
CKPWRGD_PD#	DIF_IN/DIF_IN#	SMBus EN bit	DIFx/DIFx#	FBOUT_NC/ FBOUT_NC#	PLL State
0	X	X	Low/Low	Low/Low	Off
1	Running	0	Low/Low	Running	On
		1	Running	Running	On

Power Connections

Pin Number			
V_{DD}	V_{DDIO}	GND	Description
1		2	Analog PLL
7		6	Analog input
28, 45, 64	21, 33, 40, 52, 57, 69	16, 22, 27, 34, 39, 46, 51, 58, 63, 70, 73	DIF clocks

Functionality at Power-Up

100M_133M#	Input (MHz)	Output (MHz)
1	100.00	100.00
0	133.33	133.33

PLL Operating Mode

HIBW_BYPM_LOBW#	Byte0[7:6]
Low (PLL Low BW)	00
Mid (Bypass)	01
High (PLL High BW)	11

Note: PLL is off in Bypass Mode.

SMBus Addressing

SADR(1:0)_tri	SMBus Address (Read/Write bit = 0)
00	D8
0M	DA
01	DE
M0	C2
MM	C4
M1	C6
10	CA
1M	CC
11	CE

Test Loads

Low-Power HCSL Output Test Load
(standard PCIe source-terminated test load)

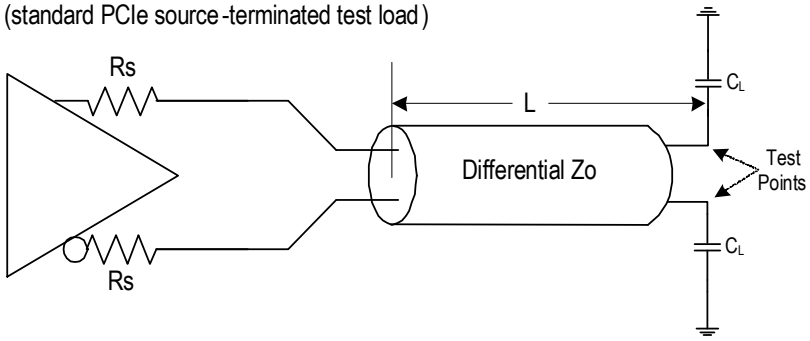


Table 14. Parameters for Low-Power HCSL Output Test Load

Device	Rs (Ω)	Zo (Ω)	L (inches)	C_L (pF)
9Z61195*	Internal	85	10	2
9Z61195*	7.5	100	10	2

*Contact factory for versions of this device with Zo=100Ω.

Alternate Terminations

The LP-HCSL can easily drive other logic families. See "AN-891 Driving LVPECL, LVDS, and CML Logic with IDT's "Universal" Low-Power HCSL Outputs" for termination schemes for LVPECL, LVDS, CML and SSTL.

Clock Periods

Table 15. Clock Periods – Differential Outputs with Spread Spectrum Disabled

SSC On	Center Frequency MHz	Measurement Window							Units	Notes
		1 Clock	1µs	0.1s	0.1s	0.1s	1µs	1 Clock		
		-c2cjitter AbsPer Minimum	-SSC Short-Term Average Minimum	-ppm Long-Term Average Minimum	0 ppm Period Nominal	+ppm Long-Term Average Maximum	+SSC Short-Term Average Maximum	+c2cjitter AbsPer Maximum		
DIF	100.00	9.94900	—	9.99900	10.00000	10.00100	—	10.05100	ns	1,2,3
	133.33	7.44925		7.49925	7.50000	7.50075		7.55075	ns	1,2,4

Table 16. Clock Periods – Differential Outputs with Spread Spectrum Enabled

SSC On	Center Frequency MHz	Measurement Window							Units	Notes
		1 Clock	1µs	0.1s	0.1s	0.1s	1µs	1 Clock		
		-c2cjitter AbsPer Minimum	-SSC Short-Term Average Minimum	-ppm Long-Term Average Minimum	0 ppm Period Nominal	+ppm Long-Term Average Maximum	+SSC Short-Term Average Maximum	+c2cjitter AbsPer Maximum		
DIF	99.75	9.94906	9.99906	10.02406	10.02506	10.02607	10.05107	10.10107	ns	1,2,3
	133.00	7.44930	7.49930	7.51805	7.51880	7.51955	7.53830	7.58830	ns	1,2,4

[1] Guaranteed by design and characterization, not 100% tested in production.

[2] All Long Term Accuracy specifications are guaranteed with the assumption that the input clock complies with CK420BQ accuracy requirements (+/-100ppm). The buffer itself does not contribute to ppm error.

[3] Driven by SRC output of main clock, 100MHz PLL Mode or Bypass Mode.

[4] Driven by CPU output of main clock, 133 MHz PLL Mode or Bypass Mode.

General SMBus Serial Interface Information

How to Write

- Controller (host) sends a start bit
- Controller (host) sends the write address
- Renesas clock will **acknowledge**
- Controller (host) sends the beginning byte location = N
- Renesas clock will **acknowledge**
- Controller (host) sends the byte count = X
- Renesas clock will **acknowledge**
- Controller (host) starts sending **Byte N–Byte N+X-1**
- Renesas clock will **acknowledg**e each byte **one at a time**
- Controller (host) sends a stop bit

Index Block Write Operation			
Controller (Host)			**Renesas (Slave/Receiver)**
T	starT bit		
Slave Address			
WR	WRite		
			ACK
Beginning Byte = N			
			ACK
Data Byte Count = X			
			ACK
Beginning Byte N		X Byte	
			ACK
O			
O			O
O			O
			O
Byte N + X - 1			
			ACK
P	stoP bit		

How to Read

- Controller (host) will send a start bit
- Controller (host) sends the write address
- Renesas clock will **acknowledge**
- Controller (host) sends the beginning byte location = N
- Renesas clock will **acknowledge**
- Controller (host) will send a separate start bit
- Controller (host) sends the read address
- Renesas clock will **acknowledge**
- Renesas clock will send the data byte count = X
- Renesas clock sends Byte **N+X-1**
- Renesas clock sends **Byte 0–Byte X (if $X_{(H)}$ was written to Byte 8)**
- Controller (host) will need to acknowledge each byte
- Controller (host) will send a not acknowledge bit
- Controller (host) will send a stop bit

Index Block Read Operation			
Controller (Host)			**Renesas (Slave/Receiver)**
T	starT bit		
Slave Address			
WR	WRite		
			ACK
Beginning Byte = N			
			ACK
RT	Repeat starT		
Slave Address			
RD	ReaD		
			ACK
			Data Byte Count=X
ACK			
		X Byte	Beginning Byte N
ACK			
			O
O			O
O			O
O			
			Byte N + X - 1
N	Not acknowledge		
P	stoP bit		

SMBus Table: PLL Mode and Frequency Select Register

Byte 0	Name	Control Function	Type	0	1	Default
Bit 7	PLL Mode 1	PLL Operating Mode Rd back 1	R	See PLL Operating Mode Readback Table		Latch
Bit 6	PLL Mode 0	PLL Operating Mode Rd back 0	R			Latch
Bit 5	DIF_18_En	Output Control	RW	Disable (Low/Low)	Enable	1
Bit 4	DIF_17_En	Output Control	RW			1
Bit 3	DIF_16_En	Output Control	RW			1
Bit 2	Reserved					0
Bit 1	Reserved					0
Bit 0	100M_133M#	Frequency Select Readback	R	133MHz	100MHz	Latch

SMBus Table: Output Control Register

Byte 1	Name	Control Function	Type	0	1	Default
Bit 7	DIF_7_En	Output Enable	RW	Disable (Low/Low)	Enable	1
Bit 6	DIF_6_En	Output Enable	RW			1
Bit 5	DIF_5_En	Output Enable	RW			1
Bit 4	DIF_4_En	Output Enable	RW			1
Bit 3	DIF_3_En	Output Enable	RW			1
Bit 2	DIF_2_En	Output Enable	RW			1
Bit 1	DIF_1_En	Output Enable	RW			1
Bit 0	DIF_0_En	Output Enable	RW			1

SMBus Table: Output Control Register

Byte 2	Name	Control Function	Type	0	1	Default
Bit 7	DIF_15_En	Output Control	RW	Disable (Low/Low)	Enable	1
Bit 6	DIF_14_En	Output Control	RW			1
Bit 5	DIF_13_En	Output Control	RW			1
Bit 4	DIF_12_En	Output Control	RW			1
Bit 3	DIF_11_En	Output Enable	RW			1
Bit 2	DIF_10_En	Output Enable	RW			1
Bit 1	DIF_9_En	Output Enable	RW			1
Bit 0	DIF_8_En	Output Enable	RW			1

SMBus Table: Reserved Register

Byte 3	Name	Control Function	Type	0	1	Default
Bit 7	amp[2]	Global Differential output Control (LP-HCSL Outputs Only)	RW	0.3V–1V 100mV/step Default=0.8V		1
Bit 6	amp[1]		RW			0
Bit 5	amp[0]		RW			1
Bit 4	Reserved					0
Bit 3	PLL_SW_EN	Enable S/W control of PLL BW	RW	Hardware Latch	SMBus Control	0
Bit 2	PLL Mode 1	PLL Operating Mode 1	RW	See PLL Operating Mode Readback Table		Latch
Bit 1	PLL Mode 0	PLL Operating Mode 1	RW			Latch
Bit 0	Reserved					0

SMBus Table: Reserved Register

Byte 4	Name	Control Function	Type	0	1	Default
Bit 7	Reserved					0
Bit 6	Reserved					0
Bit 5	Reserved					0
Bit 4	Reserved					0
Bit 3	Reserved					0
Bit 2	Reserved					0
Bit 1	Reserved					0
Bit 0	Reserved					0

SMBus Table: Vendor & Revision ID Register

Byte 5	Name	Control Function	Type	0	1	Default
Bit 7	RID3	REVISION ID	R	D = 0011		0
Bit 6	RID2		R			0
Bit 5	RID1		R			1
Bit 4	RID0		R			1
Bit 3	VID3	VENDOR ID	R	ICS/Renesas = 0001		0
Bit 2	VID2		R			0
Bit 1	VID1		R			0
Bit 0	VID0		R			1

SMBus Table: Device ID

Byte 6	Name	Control Function	Type	0	1	Default
Bit 7	Device ID 7 (MSB)		R	9Z61195D = 195 Decimal or C3 Hex		1
Bit 6	Device ID 6		R			X
Bit 5	Device ID 5		R			0
Bit 4	Device ID 4		R			X
Bit 3	Device ID 3		R			X
Bit 2	Device ID 2		R			0
Bit 1	Device ID 1		R			1
Bit 0	Device ID 0		R			1

SMBus Table: Byte Count

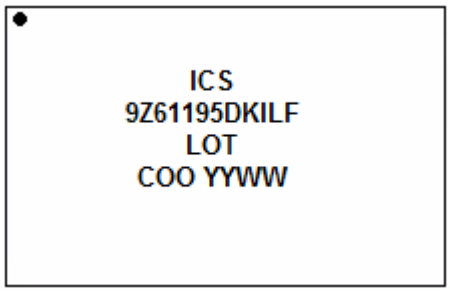
Byte 7	Name	Control Function	Type	0	1	Default
Bit 7	Reserved					0
Bit 6	Reserved					0
Bit 5	Reserved					0
Bit 4	BC4	Writing to this register configures how many bytes will be read back.	RW	Default value is 8 hex, so 9 bytes (0 to 8) will be read back by default.		0
Bit 3	BC3		RW			1
Bit 2	BC2		RW			0
Bit 1	BC1		RW			0
Bit 0	BC0		RW			0

Package Outline Drawings

The package outline drawings are appended at the end of this document and are accessible from the link below. The package information is the most current data available.

www.idt.com/us/en/document/psc/72-vfqfpn-package-outline-drawing-100-x-100-x-090-mm-body-epad-595-x-595-mm-050mm-pitch-nlg72p1

Marking Diagram



- Line 2: part number.
- Line 3: “LOT” denotes the sequential lot number.
- Line 4:
  - “COO” denotes the country of origin.
  - “YYWW” is the last digits of the year and week that the part was assembled.

Ordering Information

Orderable Part Number	Differential Output Impedance (Ω)	Package	Carrier Type	Temperature
9Z61195DKILF	85	10 x 10 mm, 0.5mm pitch 72-VFQFPN	Tray	-40° to +85°C
9Z61195DKILFT	85	10 x 10 mm, 0.5mm pitch 72-VFQFPN	Tape and Reel	-40° to +85°C

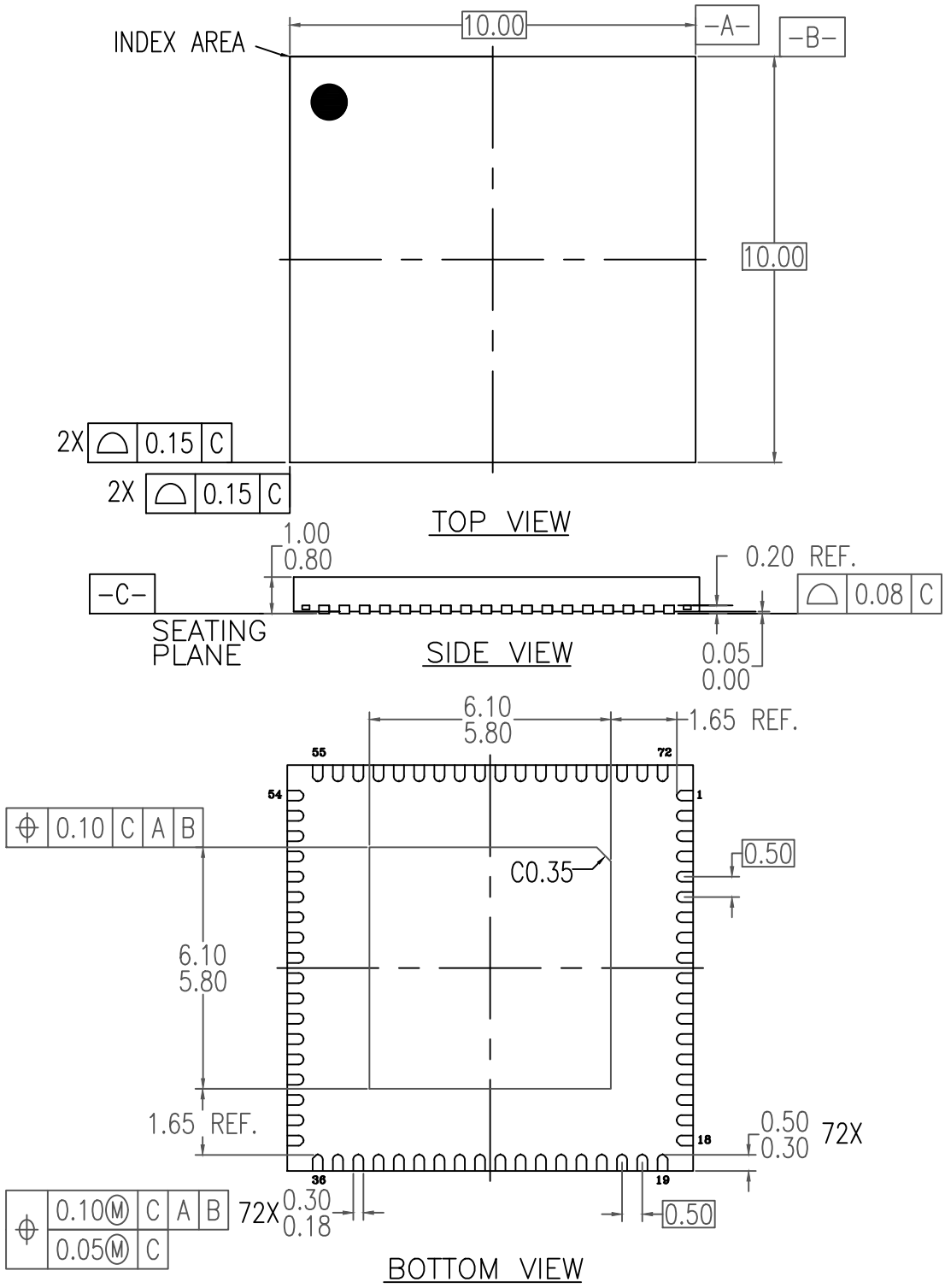
Revision History

Revision Date	Description of Change
September 14, 2020	▪ Reformatted datasheet to Renesas template. ▪ Updated Package Outline Drawings and Marking Diagrams sections.
May 17, 2018	Updated values in the “DIF HCSL/LP-HCSL” and “Filtered Phase Jitter Parameters - DB2000Q” tables.
April 13, 2018	Updated absolute maximum supply voltage rating and VIHSMB to 3.9V.
February 13, 2018	▪ Updated front page text to indicate DB2000Q compatibility. ▪ Removed reference to 5V tolerance in description of SMBDAT and SMBCLK pins. ▪ Added DB2000Q Additive phase jitter table.
November 2, 2017	Initial release.

72-VFQFPN, Package Outline Drawing

10.0 x 10.0 x 0.90 mm Body, Epad 5.95 x 5.95 mm 0.50mm Pitch

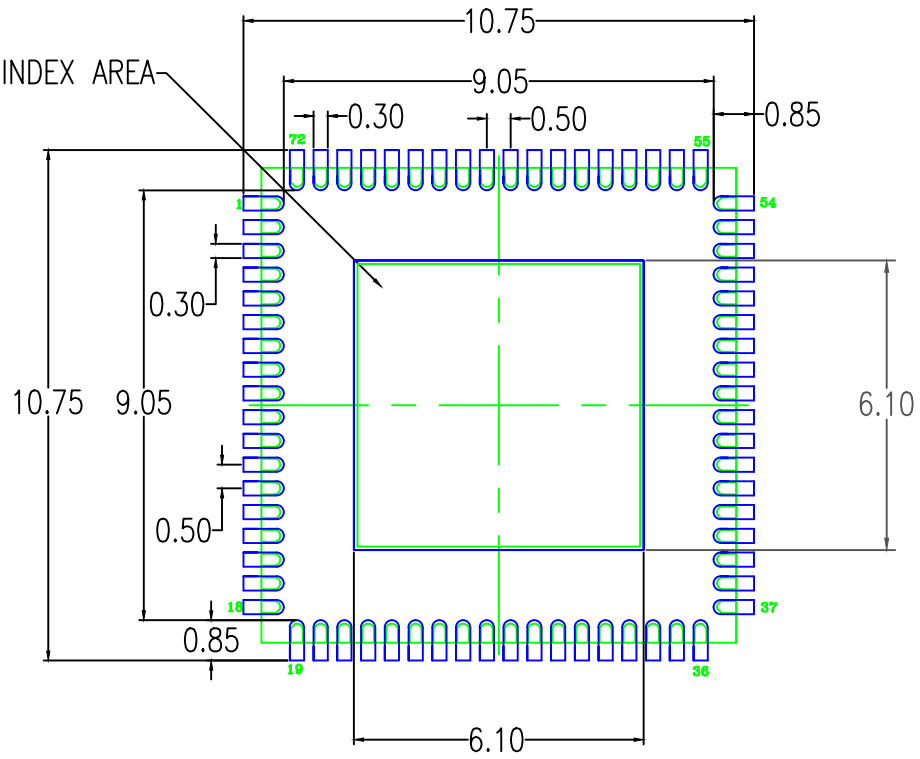
NLG72P1, PSC-4208-01, Rev 03, Page 1



NOTES:

1. ALL DIMENSIONING AND TOLERANCING CONFORM TO ANSI Y14.5M–1994
2. ALL DIMENSIONS ARE IN MILLIMETERS.
3. INDEX AREA (PIN1 IDENTIFIER)

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RECOMMENDED LAND PATTERN DIMENSION

NOTES:
1. ALL DIMENSIONS ARE IN MM. ANGLES IN DEGREES.
2. TOP DOWN VIEW. AS VIEWED ON PCB.
3. COMPONENT OUTLINE SHOWS FOR REFERENCE IN GREEN.
4. LAND PATTERN IN BLUE. NSMD PATTERN ASSUMED.
5. LAND PATTERN RECOMMENDATION PER IPC-7351B GENERIC REQUIREMENT FOR SURFACE MOUNT DESIGN AND LAND PATTERN.

Package Revision History		
Date Created	Rev No.	Description
Sept 3, 2019	Rev 03	Update P1 Dimension from 5. 8 to 5.95 mm SQ
May 8, 2017	Rev 02	Change Package Code QFN to VFQFPN

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