AT25QL128A

1.7 V Minimum, 128-Mbit SPI Serial Flash Memory with Dual I/O, Quad I/O, and QPI Support

Features

- Single 1.7 V - 2.0 V Supply
- 128 Mbit (16 x 8 Mbit physical block) Flash Memory
- Serial Peripheral Interface (SPI) and Quad Peripheral Interface (QPI) Compatible
  - Supports SPI Modes 0 and 3
  - Supports Dual Output Read and Quad I/O Program and Read
  - Supports QPI Program and Read
  - 133 MHz Maximum Operating Frequency
  - Clock-to-Output (t_{V1}) of 6 ns
  - Up to 65 Mbytes/s continuous data transfer rate
- Quad enabled (factory default settings; see Section 7.7).
- Full Chip Erase
- Flexible, Optimized Erase Architecture for Code and Data Storage Applications
  - 0.6 ms Typical Page Program (256 bytes) Time
  - 60 ms Typical 4 kB Block Erase Time
  - 200 ms Typical 32 kB Block Erase Time
  - 350 ms Typical 64 kB Block Erase Time
- Hardware Controlled Locking of Status Registers via $\overline{WP}$ Pin
- 4 kbit secured One-Time Programmable Security Register
- Hardware Write Protection
- Serial Flash Discoverable Parameters (SFDP) Register
- Flexible Programming
  - Byte/Page Program (1 to 256 bytes)
  - Dual or Quad Input Byte/Page Program (1 to 256 bytes)
- Erase/Program Suspend and Resume
- JEDEC Standard Manufacturer and Device ID Read Methodology
- Low Power Dissipation
  - 2 µA Deep Power-Down Current (Typical)
  - 10 µA Standby current (Typical)
  - 5 mA Active Read Current (Typical)
- Endurance: 100,000 program/erase cycles (4 kbytes, 32 kbytes or 64 kbytes blocks)
- Data Retention: 20 Years
- Industrial Temperature Range: -40 °C to +85 °C
- Industry Standard Green (Pb/Halide-free/RoHS Compliant) Package Options
  - 8-pad DFN (6 x 5 x 0.6 mm)
  - 21-ball die Ball Grid Array (dBGA - WLCSP)
  - 21-ball low-profile die Ball Grid Array (dBGA - WLCSP)

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1. Introduction

The AT25QL128A is a serial interface Flash memory device designed for use in a wide variety of high-volume consumer based applications in which program code is shadowed from Flash memory into embedded or external RAM for execution. The flexible erase architecture of the AT25QL128A is ideal for data storage as well, eliminating the need for additional data storage devices.

The erase block sizes of the AT25QL128A have been optimized to meet the needs of today's code and data storage applications. By optimizing the size of the erase blocks, the memory space can be used much more efficiently. Because certain code modules and data storage segments must reside by themselves in their own erase regions, the wasted and unused memory space that occurs with large block erase Flash memory devices can be greatly reduced. This increased memory space efficiency allows additional code routines and data storage segments to be added while still maintaining the same overall device density.

SPI clock frequencies of up to 133 MHz are supported, allowing equivalent clock rates of 266 MHz for Dual Output, and 532 MHz for Quad Output when using the QPI and Fast Read Dual/Quad I/O commands.The AT25QL128A array is organized into 65,536 programmable pages of 256-bytes each. Up to 256 bytes can be programmed at a time using the Page Program commands. Pages can be erased in block increments of 4 kbytes, 32 kbytes, or 64 kbytes, or the entire chip.

The devices operate on a single 1.7 V to 2.0 V power supply with current consumption as low as 5 mA active and 2 µA for Deep Power-Down. All devices offered in space-saving packages. The device supports JEDEC standard manufacturer and device identification with a 4-kbit secured OTP.

The physical block size of this device is 8 Mbit.

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2. Pinouts and Pin Descriptions

The following figures show the available package types.

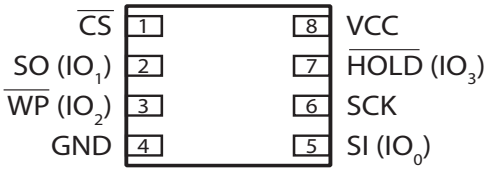

Figure 1. 8-UDFN (Top View)

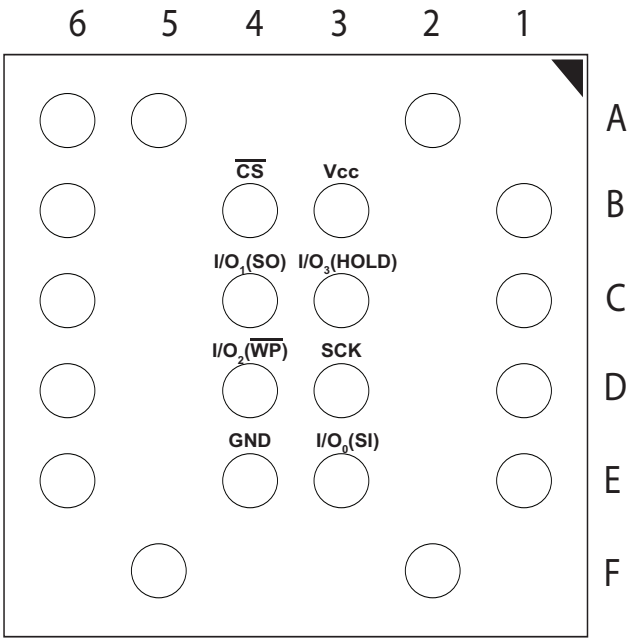

Figure 2. 21-WLCSP (Bottom View)

During all operations, V_{CC} must be held stable and within the specified valid range, V_{CC} (min) to V_{CC} (max).

All of the input and output signals must be held high or low (according to voltages of V_{IH}, V_{OH}, V_{IL}, or V_{OL}.

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Table 1. Pin Descriptions

Symbol	Name and Function	Asserted State	Type
$\overline{CS}$	**CHIP SELECT** When this input signal is high, the device is deselected and serial data output pins are at high impedance. Unless an internal program, erase, or write status register cycle is in progress, the device is in the Standby Power Mode (this is not the Deep Power-Down mode). Driving Chip Select ($\overline{CS}$) low enables the device, placing it in the active power mode. After power-up, a falling edge on Chip Select ($\overline{CS}$) is required before issuing any command.	Low	Input
SCK	**SERIAL CLOCK** This input signal provides the timing for the serial interface. Commands, addresses, or data present at serial data input are latched on the rising edge of Serial Clock (SCK). Data are shifted out on the falling edge of the Serial Clock (SCK).	–	Input
SI (I/O_0)	**SERIAL INPUT** The SI pin is used to shift data into the device. The SI pin is used for all data input including command and address sequences. Data on the SI pin is always latched in on the rising edge of SCK. With the Dual-Output and Quad-Output Read commands, the SI Pin becomes an output pin (I/O_0) in conjunction with other pins to allow two or four bits of data on (I/O_{3-0}) to be clocked in on every falling edge of SCK To maintain consistency with the SPI nomenclature, the SI (I/O_0) pin is referenced as the SI pin unless specifically addressing the Dual-I/O and Quad-I/O modes, in which case it is referenced as I/O_0. Data present on the SI pin is ignored whenever the device is deselected ($\overline{CS}$ is deasserted).	–	Input/Output
SO (I/O_1)	**SERIAL OUTPUT** The SO pin is used to shift data out from the device. Data on the SO pin is always clocked out on the falling edge of SCK. With the Dual-Output Read commands, the SO Pin remains an output pin (I/O0) in conjunction with other pins to allow two bits of data on (I/O_{1-0}) to be clocked in on every falling edge of SCK To maintain consistency with the SPI nomenclature, the SO (I/O_1) pin is referenced as the SO pin unless specifically addressing the Dual-I/O modes, in which case it is referenced as I/O_1. The SO pin is in a high-impedance state whenever the device is deselected ($\overline{CS}$ is deasserted).	–	Input/Output
$\overline{WP}$ (I/O_2)	**WRITE PROTECT** The Write Protect ($\overline{WP}$) pin can be used to protect the Status Register against data modification. Used with the Status Register's Block Protect (SEC, TB, BP2, BP1 and BP0) bits and Status Register Protect ($\overline{SRP}$) bits, a portion or the entire memory array can be hardware protected. The $\overline{WP}$ pin is active low. When the QE bit of Status Register-2 is set for Quad I/O, the $\overline{WP}$ pin (Hardware Write Protect) function is not available because this pin is used for IO_2. The $\overline{WP}$ pin does not have an internal pull-up; thus, it must be either driven or, if not used, pulled up with an external resistor to V_{CC}. See Figure 1 and Figure 2 for the pin configuration of Quad I/O and QPI operation.	–	Input/Output

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Table 1. Pin Descriptions (Continued)

Symbol	Name and Function	Asserted State	Type
$\overline{HOLD}$ (I/O_3)	**HOLD** The $\overline{HOLD}$ pin is used to temporarily pause serial communication without deselecting or resetting the device. While the $\overline{HOLD}$ pin is asserted, transitions on the SCK pin and data on the SI pin are ignored, and the SO pin is placed in a high-impedance state. The $\overline{CS}$ pin must be asserted, and the SCK pin must be in the low state in order for a Hold condition to start. A Hold condition pauses serial communication only and does not have an effect on internally self-timed operations such as a program or erase cycle. With the Quad-Input Byte/Page Program command, the $\overline{HOLD}$ pin becomes an input pin (I/O_3) and with other pins, allows four bits (on I/O_{3-0}) of data to be clocked in on every rising edge of SCK. With the Quad-Output Read commands, the $\overline{HOLD}$ Pin becomes an output pin (I/O_3) in conjunction with other pins to allow four bits of data on ($I/O3_{3-0}$) to be clocked in on every falling edge of SCK. To maintain consistency with SPI nomenclature, the $\overline{HOLD}$ (I/O_3) pin is referenced as the $\overline{HOLD}$ pin unless specifically addressing the Quad-I/O modes, in which case it is referenced as I/O_3. The $\overline{HOLD}$ pin does not have an internal pull-up; thus, it must be either driven or, if not used, pulled up with an external resistor to V_{CC}. See Figure 1 and Figure 2 for the pin configuration of Quad I/O and QPI operation.	–	Input/Output
V_{CC}	**DEVICE POWER SUPPLY:** V_{CC} is the supply voltage. It is the single voltage used for all device functions, including read, program, and erase. The V_{CC} pin is used to supply the source voltage to the device. Operations at invalid V_{CC} voltages can produce spurious results; do not attempt this.	–	Power
GND	**GROUND:** V_{SS} is the reference for the V_{CC} supply voltage. The ground reference for the power supply. Connect GND to the system ground.	–	Power

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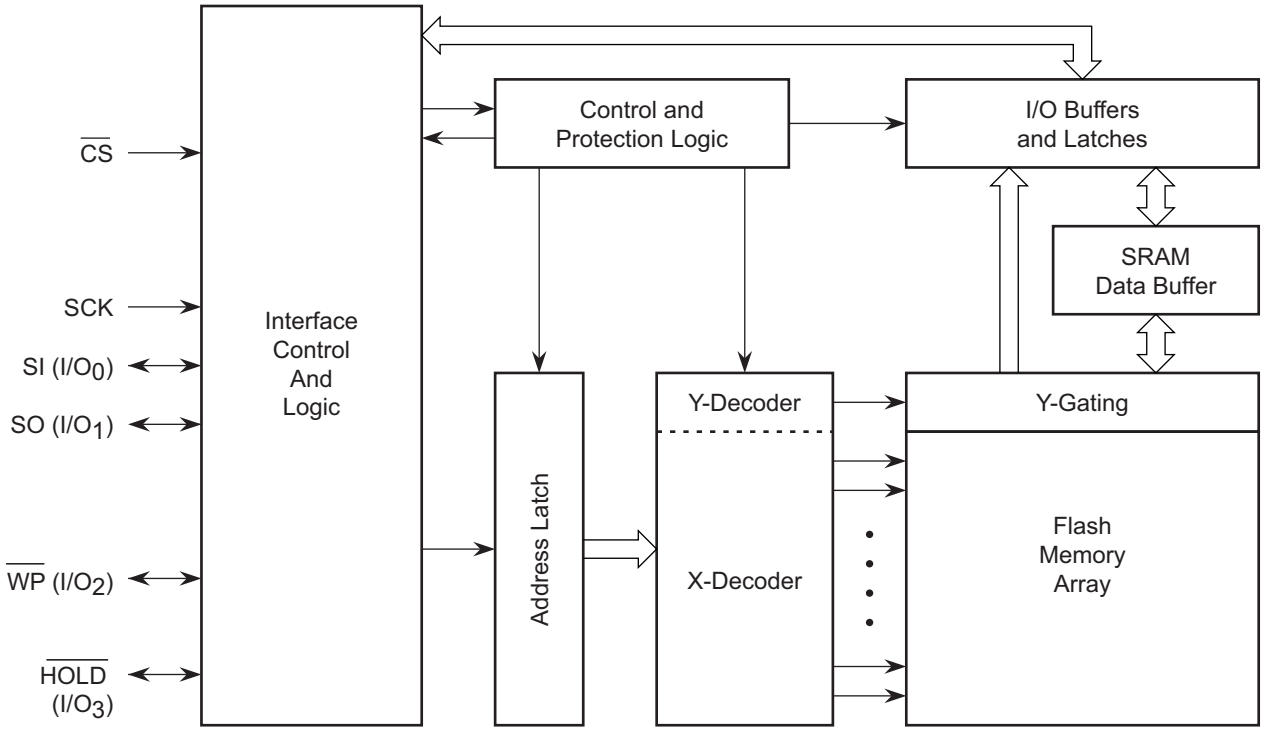
3. Block Diagram

Figure 3 shows a block diagram of the AT25QL128A serial Flash.



Note: I/O_{3-0} pin naming convention is used for Dual-I/O and Quad-I/O commands.

Figure 3. AT25QL128A Block Diagram

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4. Memory Array

To provide the greatest flexibility, the memory array of the AT25QL128A can be erased in four levels of granularity, including a full chip erase. The size of the erase blocks is optimized for both code and data storage applications, allowing both code and data segments to reside in their own erase regions. The Memory Architecture Diagram shows the components of each erase level.

Block Erase Detail				Page Program Detail	
64KB	32KB	4KB	Block Address Range	1-256 Byte	Page Address Range
Block 255	Block 511	4KB	FFFFFFh – FFF000h	256 Bytes	FFFFFFh – FFFF00h
		4KB	FFEFFFh – FFE000h	256 Bytes	FFFEFFh – FFFE00h
		4KB	FFDFFFh – FFD000h	256 Bytes	FFFDFFh - FFFD00h
		4KB	FFCFFFh – FFC000h	256 Bytes	FFFCFFh – FFFC00h
		4KB	FFBFFFh – FFB000h	256 Bytes	FFFBFFh – FFFB00h
		4KB	FFAFFFh – FFA000h	256 Bytes	FFFAFFh – FFFA00h
		4KB	FF9FFFh – FF9000h	256 Bytes	FFF9FFh – FFF900h
		4KB	FF8FFFh – FF8000h	256 Bytes	FFF8FFh – FFF800h
	Block 510	4KB	FF7FFFh – FF7000h	256 Bytes	FFF7FFh – FFF700h
		4KB	FF6FFFh – FF6000h	256 Bytes	FFF6FFh – FFF600h
		4KB	FF5FFFh – FF5000h	256 Bytes	FFF5FFh – FFF500h
		4KB	FF4FFFh – FF4000h	256 Bytes	FFF4FFh – FFF400h
		4KB	FF3FFFh – FF3000h	256 Bytes	FFF3FFh – FFF300h
		4KB	FF2FFFh – FF2000h	256 Bytes	FFF2FFh – FFF200h
		4KB	FF1FFFh – FF1000h	256 Bytes	FFF1FFh – FFF100h
		4KB	FF0FFFh – FF0000h	256 Bytes	FFF0FFh – FFF000h
Block 254	Block 509	4KB	FEFFFFh – FEF000h	256 Bytes	FFEFFFh – FFEF00h
		4KB	FEEFFFh – FEE000h	256 Bytes	FFEEFFh – FFEE00h
		4KB	FEDFFFh – FED000h	256 Bytes	FFEDFFh – FFED00h
		4KB	FECFFFh – FEC000h	256 Bytes	FFECFFh – FFEC00h
		4KB	FEBFFFh – FEB000h	256 Bytes	FFEBFFh – FFEB00h
		4KB	FEAFFFh – FEA000h	256 Bytes	FFEAFFh – FFEA00h
		4KB	FE9FFFh – FE9000h	256 Bytes	FFE9FFh – FFE900h
		4KB	FE8FFFh – FE8000h	256 Bytes	FFE8FFh – FFE800h
	Block 508	4KB	FE7FFFh – FE7000h	⋮	
		4KB	FE6FFFh – FE6000h		
		4KB	FE5FFFh – FE5000h		
		4KB	FE4FFFh – FE4000h	256 Bytes	0017FFh – 001700h
		4KB	FE3FFFh – FE3000h	256 Bytes	0016FFh – 001600h
		4KB	FE2FFFh – FE2000h	256 Bytes	0015FFh – 001500h
		4KB	FE1FFFh – FE1000h	256 Bytes	0014FFh – 001400h
		4KB	FE0FFFh – FE0000h	256 Bytes	0013FFh – 001300h
⋮	⋮	⋮		256 Bytes	0012FFh – 001200h
				256 Bytes	0011FFh – 001100h
				256 Bytes	0010FFh – 001000h
Block 0	Block 1	4KB	00FFFFh – 00F000h	256 Bytes	000FFFh – 000F00h
		4KB	00EFFFh – 00E000h	256 Bytes	000EFFh – 000E00h
		4KB	00DFFFh – 00D000h	256 Bytes	000DFFh – 000D00h
		4KB	00CFFFh – 00C000h	256 Bytes	000CFFh – 000C00h
		4KB	00BFFFh – 00B000h	256 Bytes	000BFFh – 000B00h
		4KB	00AFFFh – 00A000h	256 Bytes	000AFFh – 000A00h
		4KB	009FFFh – 009000h	256 Bytes	0009FFh – 000900h
		4KB	008FFFh – 008000h	256 Bytes	0008FFh – 000800h
	Block 0	4KB	007FFFh – 007000h	256 Bytes	0007FFh – 000700h
		4KB	006FFFh – 006000h	256 Bytes	0006FFh – 000600h
		4KB	005FFFh – 005000h	256 Bytes	0005FFh – 000500h
		4KB	004FFFh – 004000h	256 Bytes	0004FFh – 000400h
		4KB	003FFFh – 003000h	256 Bytes	0003FFh – 000300h
		4KB	002FFFh – 002000h	256 Bytes	0002FFh – 000200h
		4KB	001FFFh – 001000h	256 Bytes	0001FFh – 000100h
		4KB	000FFFh – 000000h	256 Bytes	0000FFh – 000000h

Figure 4. Memory Architecture Diagram

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5. Device Operation

5.1 Standard SPI Operation

The AT25QL128A features a serial peripheral interface on four signals: Serial Clock (SCK). Chip Select ($\overline{CS}$), Serial Data Input (SI) and Serial Data Output (SO). Standard SPI commands use the SI input pin to serially write commands, addresses or data to the device on the rising edge of SCK. The SO output pin is used to read data or status from the device on the falling edge of SCK.

SPI bus operation Modes 0 (0, 0) and 3 (1, 1) are supported. The primary difference between Mode 0 and Mode 3 is the normal state of the SCK signal when the SPI bus master is in standby and data is not being transferred to the Serial Flash. For Mode 0 the SCK signal is normally low on the falling and rising edges of $\overline{CS}$. For Mode 3 the SCK signal is normally high on the falling and rising edges of $\overline{CS}$.

5.2 Dual SPI Operation

The AT25QL128A supports Dual SPI operation. This command allows data to be transferred to, or from, the device at two times the rate of the standard SPI. The Dual Read command is ideal for quickly downloading code to RAM upon power-up (code-shadowing) or for executing non-speed-critical code directly from the SPI bus (XIP). When using Dual SPI commands the SI and SO pins become bidirectional I/0 pins; IO_0 and IO_1.

5.3 Quad SPI Operation

The AT25QL128A supports Quad SPI operation. This command allows data to be transferred to, or from, the device at four times the rate of the standard SPI. The Quad Read command offers a significant improvement in continuous and random access transfer rates allowing fast code-shadowing to RAM or execution directly from the SPI bus (XIP). When using Quad SPI command the SI and SO pins become bidirectional IO_0 and IO_1, and the $\overline{WP}$ and $\overline{HOLD}$ pins become IO_2 and IO_3 respectively. Quad SPI commands require the non-volatile Quad Enable bit (QE) in Status Register-2 to be set.

5.4 QPI Operation

The AT25QL128A supports Quad Peripheral Interface (QPI) operation when the device is switched from Standard/ Dual/ Quad SPI mode to QPI mode using the Enable QPI (38h) command. To enable QPI mode, the non-volatile Quad Enable bit (QE) in Status Register-2 is required to be set. When using QPI commands, the SI and SO pins become bidirectional IO_0 and IO_1, and the $\overline{WP}$ and $\overline{HOLD}$ pins become IO_2 and IO_3, respectively.

The typical SPI protocol requires that the byte-long command code is shifted into the device only through the SI pin in eight serial clocks. The QPI mode uses all four IO pins to input the command code; thus, only two serial clocks are required. This can significantly reduce the SPI command overhead and improve system performance in an XIP environment. Standard / Dual / Quad SPI mode and QPI mode are exclusive. Only one mode can be active at any given time, the Enable QPI and Disable QPI/ Disable QPI 2 commands are used to switch between these two modes. Upon power-up, or after software reset using Reset (99h) command, the default state of the device is Standard / Dual / Quad SPI mode.

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6. Write Protection

To protect inadvertent writes by noise, several means of protection are applied to the Flash memory.

6.1 Write Protect Features

- During power-on reset, all operations are disabled, and no command is recognized.
- An internal time delay of t_{PUW} can protect the data against inadvertent changes while the power supply is outside the operating specification. This includes the Write Enable, Page program, Block Erase, Chip Erase, Write Security Register, and Write Status Register commands.
- For data changes, the Write Enable command must be issued to set the Write Enable Latch (WEL) bit to 0. Power-up, completion of the Write Disable, Write Status Register, Page Program, Block Erase, and Chip Erase commands are must meet this condition.
- Setting the Status Register protect (SRP) and Block protect (SEC, TB, BP2, BP1, and BP0) bits, a portion of memory can be configured as read only; this is called software protection.
- The Write Protect ($\overline{WP}$) pin can change the Status Register under hardware control.
- The Deep Power-Down mode provides extra protection from unexpected data changes because all commands are ignored in this mode except for the Release Deep Power-Down command.

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7. Status Register

The Read Status Register command can be used to provide status on the availability of the Flash memory array, if the device is write enabled or disabled the state of write protection and the Quad SPI setting. The Write Status Register command can be used to configure the device's write protection features and the Quad SPI setting. Write access to the Status Register is controlled in some cases by the $\overline{WP}$ pin.

Table 2. Status Register Upper Bits Definitions

S7	S6	S5	S4	S3	S2	S1	S0
SRP	**SEC**	**TB**	**BP2**	**BP1**	**BP0**	**WEL**	**BUSY**
Status Register Protect 0 (Non-Volatile)	Sector Protect (Non- Volatile)	Top/Bottom Write Protect (Non- Volatile)	Block Protect (Non- Volatile)	Block Protect (Non- Volatile)	Block Protect (Non- Volatile)	Write Enable Latch	Erase or Write in Progress

Table 3. Status Register Lower Bits Definition

S15	S14	S13	S12	S11	S10	S9	S8
SUS	**CMP**	**(R)**	**(R)**	**(R)**	**(R)**	**QE**	**SRP1**
Suspend Status	Complement Protect (Non-Volatile)	Reserved	Reserved	Reserved	Reserved	Quad Enable (Non- Volatile)	Register Protect 1 (Non- Volatile)

7.1 Busy

BUSY is a read-only bit in the status register (S0) that is set to 1 when the device is executing a Page Program, Erase, Write Status Register, or Write Security Register command. During this time, the device ignores further commands, except for the Read Status Register and Erase / Program Suspend command (see t_W, t_{PP}, t_{SE}, t_{BE1}, t_{BE2}, and t_{CE} in Section 9.6, AC Electrical Characteristics). When the Program, Erase, Write Status Register, or Write Security Register command has completed, the BUSY bit is cleared to a 0 state, indicating the device is ready for further commands.

Other exceptions are the Enable Reset (66h) and Reset (99h) commands. Even if the BUSY bit is active (1), the device accepts and executes a RESET command from the host system. The host system must wait for the BUSY bit to become inactive (0) before sending the RESET command. If the device receives a RESET command during an ERASE or in Program mode, memory corruption can occur. See Section 8.35, Enable Reset (66h) and Reset (99h) for more information.

7.2 Write Enable Latch (WEL)

Write Enable Latch (WEL) is a read-only bit in the status register (S1) that is set to a 1 after executing a Write Enable command. It is cleared to 0 when device is write-disabled. A write disable state occurs upon power-up or after any of the following commands: Write Disable, Page Program, Erase and Write Status Register.

7.3 Block Protect Bits (BP2, BP1, BP0)

The Block Protect Bits (BP2, BP1, BP0) are non-volatile read/write bits in the status register (S4, S3, and S2) that provide write protection control and status. Block protect bits can be set using the Write Status Register Command (see t_W in Section 9.6, AC Electrical Characteristics). All, none, or a portion of the memory array can be protected from Program and Erase commands (see Table 5, and Table 6). The factory default setting for the block protection bits is 0, none of the array protected.

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7.4 Top/Bottom Block Protect (TB)

The Top/Bottom bit (TB) is a non-volatile bit in the status register (S5) that specifies if the Block Protect Bits (BP2, BP1, BP0) protect from the top (TB = 0) or the bottom (TB = 1) of the array, as shown in Table 5 and Table 6. The factory default setting is TB = 0. The TB bit can be set with the Write Status Register command, depending on the state of the SRP0, SRP1 and WEL bits.

7.5 Sector/Block Protect (SEC)

The Sector protect bit (SEC) is a non-volatile bit in the status register (S6) that specifies if the Block Protect Bits (BP2, BP1, BP0) protect a 4-kbyte sector (SEC = 1) or 64-kbyte blocks (SEC = 0) in the top (TB = 0) or the bottom (TB = 1) of the array, as shown in Table 5 and Table 6. The default setting is SEC = 0.

7.6 Status Register Protect (SRP1, SRP0)

The Status Register Protect bits (SRP1 and SRP0) are non-volatile read/write bits in the status register (S8 and S7). The SRP bits control the method of write protection: software protection, hardware protection, power supply lock-down, or one-time programmable (OTP) protection.

Table 4. Encoding of SRP[1:0] Bits and Write Protection

SRP1	SRP0	WP	Status Register	Description
0	0	X	Software Protection	$\overline{WP}$ pin no control. The register can be written to after a Write Enable command, WEL = 1. [Factory Default]
0	1	0	Hardware Protected	When the $\overline{WP}$ pin is low, the Status Register is locked and can not be written to.
0	1	1	Hardware Unprotected	When the $\overline{WP}$ pin is high, the Status register is unlocked and can be written to after a Write Enable command, WEL = 1.
1	0	X	Power Supply Lock-Down	Status Register is protected and cannot be written to again until the next power-down, power-up cycle.(1)
1	1	X	One Time Program	Status Register is permanently protected and cannot be written to.

Note: 1. When SRP1, SRP0 = (1,0), a power-down, power-up cycle changes SRP1, SRP0 to (0,0).

7.7 Quad Enable (QE)

The Quad Enable (QE) bit is a non-volatile read/write bit in the Status Register (S9) that allows Quad operation. When the QE bit is set to 1 (factory default), the Quad IO_2 and IO_3 pins are enabled.

7.8 Complement Protect (CMP)

The Complement Protect bit (CMP) is a non-volatile read/write bit in the status register (S14). It is used in conjunction with SEC, TB, BP2, BP1, and BP0 bits to provide more flexibility for the array protection. Once CMP is set to 1, previous array protection set by SEC, TB, BP2, BP1, and BP0 is reversed. For instance, when CMP = 0, a top 4-kbyte sector can be protected while the rest of the array is not; when CMP = 1, the top 4-kbyte sector becomes unprotected while the rest of the array becomes read-only. See Table 5 and Table 6 for details. The default setting is CMP = 0.

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7.9 Erase/Program Suspend Status (SUS)

The Suspend Status bit (SUS) is a read-only bit in the status register (S15) that is set to 1 after executing an Erase/Program Suspend (75h) command. The SUS status bit is cleared to 0 by the Erase/Program Resume (7Ah) command, as well as a power-down/power-up cycle.

Table 5. Status Register Memory Protection (CMP = 0)

Status Register					Memory Protection			
SEC	TB	BP2	BP1	BP0	Sector(s)	Addresses	Density	Portion
X	X	0	0	0	NONE	NONE	NONE	NONE
0	0	0	0	1	252 – 255	FC0000h - FFFFFFh	256 kbytes	Upper 1/64
0	0	0	1	0	248 – 255	F80000h - FFFFFFh	512 kbytes	Upper 1/32
0	0	0	1	1	240 – 255	F00000h - FFFFFFh	1 Mbytes	Upper 1/16
0	0	1	0	0	224 – 255	E00000h - FFFFFFh	2 Mbytes	Upper 1/8
0	0	1	0	1	192 – 255	C00000h - FFFFFFh	4 Mbytes	Upper 1/4
0	0	1	1	0	128 – 255	800000h - FFFFFFh	8 Mbytes	Upper 1/2
0	1	0	0	1	0 – 3	000000h - 03FFFFh	256 kbytes	Lower 1/64
0	1	0	1	0	0 – 7	000000h - 07FFFFh	512 kbytes	Lower 1/32
0	1	0	1	1	0 – 15	000000h - 0FFFFFh	1 Mbytes	Lower 1/16
0	1	1	0	0	0 – 31	000000h - 1FFFFFh	2 Mbytes	Lower 1/8
0	1	1	0	1	0 – 63	000000h - 3FFFFFh	4 Mbytes	Lower 1/4
0	1	1	1	0	0 – 127	000000h - 7FFFFFh	8 Mbytes	Lower 1/2
X	X	1	1	1	0 – 255	000000h - FFFFFFh	16 Mbytes	ALL
1	0	0	0	1	255	FFF000h - FFFFFFh	4 kbytes	U – 1/4096 (4)
1	0	0	1	0	255	FFE000h - FFFFFFh	8 kbytes	U – 1/2048
1	0	0	1	1	255	FFC000h - FFFFFFh	16 kbytes	U – 1/1024
1	0	1	0	X	255	FF8000h - FFFFFFh	32 kbytes	U – 1/512
1	1	0	0	1	0	000000h - 000FFFh	4 kbytes	L – 1/4096
1	1	0	1	0	0	000000h - 001FFFh	8 kbytes	L – 1/2048
1	1	0	1	1	0	000000h - 003FFFh	16 kbytes	L – 1/1024
1	1	1	0	X	0	000000h - 007FFFh	32 kbytes	L – 1/512

Note:

1. X = Don’t care
2. L = Lower; U = Upper
3. If any Erase or Program command specifies a memory region that contains protected data portion, this command is ignored.
4. Note 3 does not apply to this Status Register Bit setting. See Errata 1 in Appendix A for details.

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Table 6. Status Register Memory Protection (CMP = 1)

Status Register					Memory Protection			
SEC	TB	BP2	BP1	BP0	Sector(s)	Addresses	Density	Portion
X	X	0	0	0	0 – 255	000000h – FFFFFFh	16 Mbytes	ALL
0	0	0	0	1	0 – 251	000000h – FBFFFFh	16,128 kbytes	Lower 63/64
0	0	0	1	0	0 and 247	000000h – F7FFFFh	15,872 kbytes	Lower 31/32
0	0	0	1	1	0 – 239	000000h – EFFFFFh	15 Mbytes	Lower 15/16
0	0	1	0	0	0 – 223	000000h – DFFFFFh	14 Mbytes	Lower 7/8
0	0	1	0	1	0 – 191	000000h – BFFFFFh	12 Mbytes	Lower 3/4
0	0	1	1	0	0 – 127	000000h – 7FFFFFh	8 Mbytes	Lower 1/2
0	1	0	0	1	4 – 255	040000h - FFFFFFh	16,128 kbytes	Upper 63/64
0	1	0	1	0	8 and 255	080000h - FFFFFFh	15,872 kbytes	Upper 31/32
0	1	0	1	1	16 – 255	100000h - FFFFFFh	15 Mbytes	Upper 15/16
0	1	1	0	0	32 – 255	200000h - FFFFFFh	14 Mbytes	Upper 7/8
0	1	1	0	1	64 – 255	400000h - FFFFFFh	12 Mbytes	Upper 3/4
0	1	1	1	0	128 – 255	800000h - FFFFFFh	8 Mbytes	Upper 1/2
X	X	1	1	1	NONE	NONE	NONE	NONE
1	0	0	0	1	0 – 255	000000h - FFEFFFh	16,380 kbytes	L – 4095/4096
1	0	0	1	0	0 – 255	000000h - FFDFFFh	16,376 kbytes	L – 2047/2048
1	0	0	1	1	0 – 255	000000h - FFBFFFh	16,368 kbytes	L – 1023/1024
1	0	1	0	X	0 – 255	000000h - FF7FFFh	16,352 kbytes	L – 511/512
1	1	0	0	1	0 – 255	001000h - FFFFFFh	16,380 kbytes	U – 4095/4096 (4)
1	1	0	1	0	0 – 255	002000h - FFFFFFh	16,376 kbytes	U – 2047/2048
1	1	0	1	1	0 – 255	004000h - FFFFFFh	16,368 kbytes	U – 1023/1024
1	1	1	0	X	0 – 255	008000h - FFFFFFh	16,352 kbytes	U – 511/512

Note:

1. X = don't care
2. L = Lower; U = Upper
3. If any Erase or Program command specifies a memory region that contains protected data portion, this command is ignored.
4. Note 3 does not apply to this Status Register Bit setting. See Errata 2 in Appendix A for details.

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8. Commands

Commands are initiated with the falling edge of Chip Select ($\overline{CS}$). The first byte of data clocked into the input pins (SI or IO [3:0]) provides the command code. Data on the SI input is sampled on the rising edge of clock, with most significant bit (MSB) first.

Commands are completed with the rising edge of edge $\overline{CS}$. Clock relative timing diagrams are included with the description of each command. All read commands can be completed after any clocked bit; however, all commands that Write, Program, or Erase must complete on a byte ($\overline{CS}$ driven high after a full eight bits have been clocked); otherwise, the command is terminated. This feature further protects the device from inadvertent writes. Also, while the memory is being programmed or erased, or when the Status Register is being written, all commands except for Read Register are ignored until the program or erase cycle has completed.

Table 7. Manufacturer and Device Identification

		ID code	Command
Manufacturer ID	Renesas Electronics	1Fh	90h, 92h, 94h, 9Fh
Device ID	AT25QL128A	17h	90h, 92h, 94h, ABh
Memory Type ID	SPI / QPI	42h	9Fh
Capacity Type ID	128M	18h	9Fh

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8.1 Command Set Tables

Table 8. Command Set Table 1 (SPI Commands)

Command Byte	0	1	2	3	4	5
Clock Number	**0 - 7**	**8 - 15**	**16 - 23**	**24 - 31**	**32 - 39**	**40 - 47**
Write Enable	06h					
Write Enable (for volatile Status registers)	50h					
Write Disable	04h					
Read Status Register 1	05h	SR7:SR0 [1]				
Read Status Register 2	35h	SR15:SR8(2)				
Write Status Register 1	01h	SR7:SR0	SR15:SR8			
Write Status Register 2	31h	SR15:SR8				
Read Data	03h	A23:A16	A15:A8	A7:A0	D7:D0	
Fast Read Data	0Bh	A23:A16	A15:A8	A7:A0	Dummy	D7:D0
Page Program	02h	A23:A16	A15:A8	A7:A0	D7:D0 [2]	
Enable QPI	38h					
Block Erase (4 kbytes)	20h	A23:A16	A15:A8	A7:A0		
Block Erase (32 kbytes)	52h	A23:A16	A15:A8	A7:A0		
Block Erase (64 kbytes)	D8h	A23:A16	A15:A8	A7:A0		
Chip Erase	60h/C7h					
Erase/Program Suspend	75h					
Erase/Program Resume	7Ah					
Deep Power-Down	B9h					
Release from Deep Power-Down/Device ID	ABh	Dummy	Dummy	Dummy	D7:D0(2)	
Read Manufacturer ID [3]	90h	00h	00h	00h or 01h	MID7:MID0	DID7:DID0
Read JEDEC ID	9Fh	MID7:MID0	D7:D0	D7:D0		
Reset Enable	66h					
Reset	99h					
Enter Secured OTP	B1h					
Exit Secured OTP	C1h					
Read Security Register	2Bh	SC7:SC0 [4]				
Write Security Register	2Fh					
Read Serial Flash Discovery Parameters	5Ah	A23:A16	A15:A8	A7:A0	Dummy	D7:D0

1. SR = status register, The Status Register contents and Device ID repeat continuously until CS terminates the command.
2. At least one byte of data input is required for Page Program, Quad Page Program and Program Security Register, up to 256 bytes of data input. If more than 256 bytes of data are sent to the device, the addressing wraps to the beginning of the page and overwrites previously sent data.
3. See Manufacturer and Device Identification table for Device ID information.
4. SC = security register.

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Table 9. Command Set Table 2 (Dual SPI Commands)

Command Byte	0	1	2	3	4	5
Clock Number	**0 - 7**	**8 - 15**	**16 - 23**	**24 - 31**	**32 - 39**	**40 - 47**
Fast Read Dual Output	3Bh	A23:A16	A15:A8	A7:A0	Dummy	D7:D0 [1]
Fast Read Dual I/O	BBh	A23:A8 [1]	A7:A0	D7:D0.... [1]		
Read Manufacturer ID [2]	92h	0000h	(00h, xxxx) or 01h, xxxx)	MID7:MID0 DID7:DID0 [1]		

1. Dual Output data: IO_0 = (D6, D4, D2, D0), IO_1 = (D7, D5, D3, D1)
2. Dual input address:
   IO_0 = A22, A20, A18, A16, A14, A12, A10, A8, A6, A4, A2, A0, M6, M4, M2, M0
   IO_1 = A23, A21, A19, A17, A15, A13, A11, A9, A7, A5, A3, A1, M7, M5, M3, M1
3. See Manufacturer and Device Identification table for Device ID information.

Table 10. Command Set Table 3 (Quad SPI Commands)

Command Byte	0	1	2	3	4	5
Clock Number	**0 - 7**	**8 - 15**	**16 - 23**	**24 - 31**	**32 - 39**	**40 - 47**
Fast Read Quad Output	6Bh	A23:A16	A15:A8	A7:A0	Dummy	D7:D0 [1]
Fast Read Quad I/O	EBh	A23:A0, M7:M0 [2]	(xxxx, D7:D0...) [3]	D7:D0.... [1]		
Quad Page Program	33h	A23:A0 (D7:D0, ...) [1]				
Read Quad Manufacturer ID [4]	94h	00_0000h, xx or 00_00001h, xx	(xxxx, MID7:MID0) (xxxx, DID7:DID0)(3)			
Fast Read Quad I/O	EBh	A23:A0 M7:M0 [2]	(xx, D7:D0)	D7:D0 [1]		
Set Burst with Wrap	77h	xxxxxx, W6:W4 [5]	(xx, D7:D0)	D7:D0		

1. Quad Input/ Output Data
   IO_0 = (D4, D0...)
   IO_1 = (D5, D1...)
   IO_2 = (D6, D2...)
   IO_3 = (D7, D3...)
2. Quad Input Address
   IO_0 = A20, A16, A12, A8, A0, M4, M0
   IO_1 = A21, A17, A13, A9, A1, M5, M1
   IO_2 = A22, A18, A14, A10, A2, M6, M2
   IO_3 = A23, A19, A15, A11, A3, M7, M3
3. Fast Read Quad I/O Data Output
   IO_0 = (x, x, x, x, D4, D0...)
   IO_1 = (x, x, x, x, D5, D1...)
   IO_2 = (x, x, x, x, D6, D2...)
   IO_3 = (x, x, x, x, D7, D3...)
4. See Table 7 for Device ID information.
5. Set Burst With Wrap
   IO_0 = x, x, x, x, x, x, W4, x
   IO_1 = x, x, x, x, x, x, W5, x
   IO_2 = x, x, x, x, x, x, W6, x
   IO_3 = x, x, x, x, x, x, W7, x

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Table 11. Command Set Table 4 (QPI Commands)

Command Byte [1]		0	1	2	3	4	5	6	7	8
Clock Number		**0, 1**	**2, 3**	**4, 5**	**6, 7**	**8, 9**	**10, 11**	**12, 13**	**14, 15**	**16, 17**
Write Enable		06h								
Write Enable (for volatile Status registers)		50h								
Write Disable		04h								
Read Status Register 1		05h	(SR7:SR0) [2]							
Read Status Register 2		35h	(SR15:SR8)(2)							
Write Status Register 1 [2]		01h	(SR7:SR0)	(SR15:SR8)						
Write Status Register 2		31h	(SR15:SR8)							
Fast Read Data	up to 80 MHz	0Bh	A23:A16	A15:A8	A7:A0	Dummy	Dummy	(D7:D0)		
	up to 104 MHz		A23:A16	A15:A8	A7:A0	Dummy	Dummy	Dummy	(D7:D0)	
Page Program		02h	A23:A16	A15:A8	A7:A0	(D7:D0) [3]				
Block Erase (4 kbytes)		20h	A23:A16	A15:A8	A7:A0					
Block Erase (32 kbytes)		52h	A23:A16	A15:A8	A7:A0					
Block Erase (64 kbytes)		D8h	A23:A16	A15:A8	A7:A0					
Chip Erase		60h/C7h								
Erase/Program Suspend		75h								
Erase/Program Resume		7Ah								
Deep Power-Down		B9h								
Release from Deep Power-Down		ABh								
Read Manufacturer/ Device ID [4]		90h	00h	00h	00h or 01h	(MID7: MID0)	(DID7: DID0)			
Read JEDEC ID		9Fh	(MID7:MID0) (Mfg ID)	(D7:D0) (Mem Typ)	(D7:D0) (Cap)					
Enter Secured OTP		B1h								
Exit Secured OTP		C1h								
Read Security Register		2Bh	(SC7:SC0) [5]							
Write Security Register		2Fh								
Fast Read Quad I/O	up to 80 MHz	EBh	A23:A16	A15:A8	A7:A0	(M7:M0)	Dummy	(D7:D0)		
	up to 104 MHz		A23:A16	A15:A8	A7:A0	(M7:M0)	Dummy	Dummy	(D7:D0)	
	up to 133 MHz		A23:A16	A15:A8	A7:A0	(M7:M0)	Dummy	Dummy	Dummy	(D7:D0)
Reset Enable		66h								
Reset		99h								
Disable QPI		FFh								

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Table 11. Command Set Table 4 (QPI Commands) (Continued)

Command Byte [1]		0	1	2	3	4	5	6	7	8
Clock Number		**0, 1**	**2, 3**	**4, 5**	**6, 7**	**8, 9**	**10, 11**	**12, 13**	**14, 15**	**16, 17**
Burst Read with Wrap	up to 80 MHz	0Ch	A23:A16	A15:A8	A7:A0	Dummy	Dummy	(D7:D0)		
	up to 104 MHz		A23:A16	A15:A8	A7:A0	Dummy	Dummy	Dummy	(D7:D0)	
	up to 133 MHz		A23:A16	A15:A8	A7:A0	Dummy	Dummy	Dummy	Dummy	(D7:D0)
Set Read Parameter		C0h	P7:P0							
Quad Page Program		33h	A23:A16	A15:A8	A7:A0	(D7:D0)				

1. Data bytes are shifted with Most Significant Bit first. Byte fields with data in parenthesis () indicate data being read from the device on the IO pin.
2. SR = Status Register. The Status Register contents and Device ID repeat continuously until CS terminates the command.
3. At least one byte of data input is required for Page Program, Quad Page Program and Program Security Register, up to 256 bytes of data input. If more than 256 bytes of data are sent to the device, the addressing wraps to the beginning of the page and overwrites previously sent data.
4. See Table 7 for Device ID information.
5. SC = Security Register.

8.2 Write Enable (06h)

The Write Enable command is for setting the Write Enable Latch (WEL) bit in the Status Register. The WEL bit must be set before every Program, Erase, and Write Status Register command. To enter the Write Enable command, $\overline{CS}$ goes low before the command 06h into Data Input (SI) pin on the rising edge of SCK; then $\overline{CS}$ goes high.

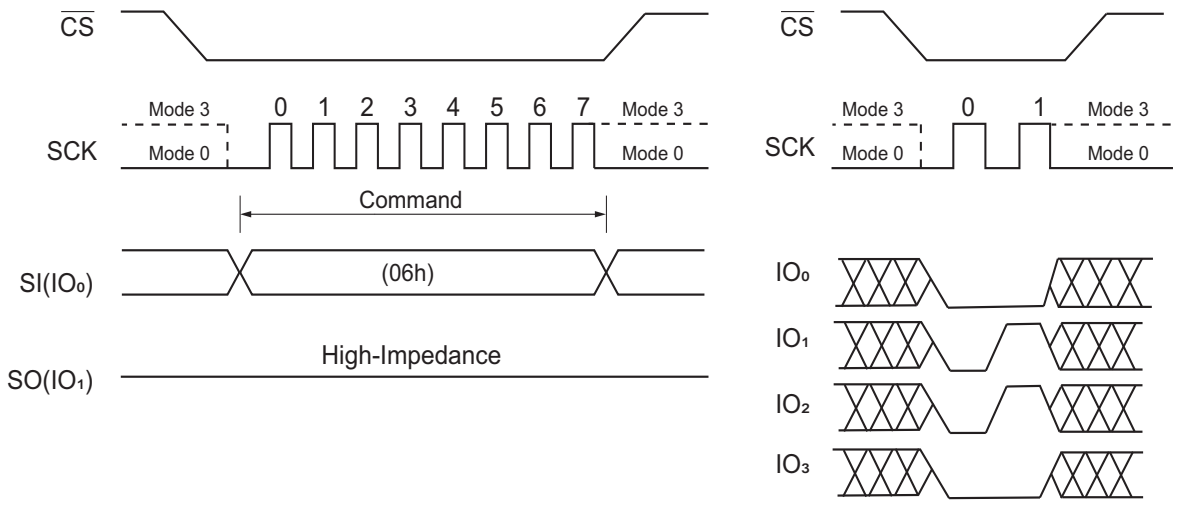

Figure 5. Write Enable Command for SPI Mode (left) and QPI Mode (right)

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8.3 Write Enable for Volatile Status Register (50h)

This gives more flexibility to change the system configuration and memory protection schemes quickly, without waiting for the typical non-volatile bit write cycles or affecting the endurance of the Status Register non-volatile bits. To write the volatile values into the Status Register bits, the Write Enable for Volatile Status Register (50h) command must be issued before a Write Status Register (01h) command. The Write Enable for Volatile Status Register command (Figure 6) does not set the Write Enable Latch (WEL) bit. Once Write Enable for Volatile Status Register is set, a Write Enable command must not have been issued before issuing the Write Status Register command (01h or 31h). When Write Enable for Volatile Status Register (50h) is set in QPI Mode, the SUS bit (S15) and Reserved bits (S13, S12, S11 and S10) of the Status Register-2 must be driven to high after Write Status Register command (01h).Once Read Status Register (05h or 31h) is issued the read values of SUS bit (S15) and Reserved bits (S13, S12, S11 and S10) of the Status Register-2 are ignored.

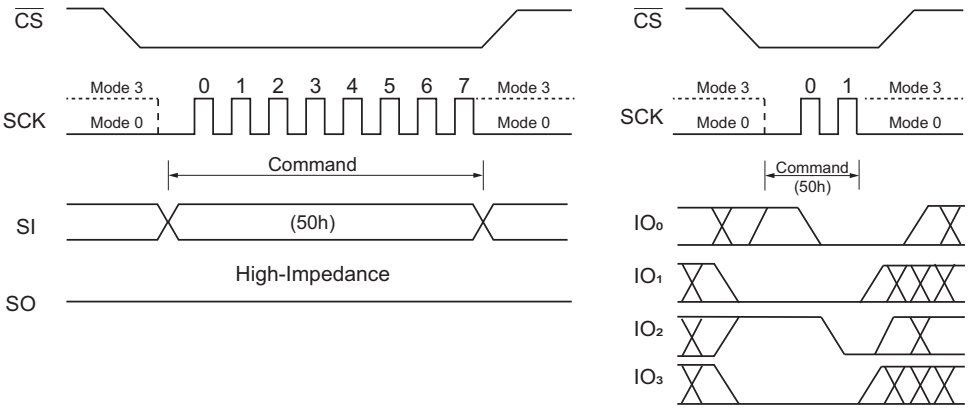

Figure 6. Write Enable for Volatile Status Register Command for SPI Mode (left) and QPI Mode (right)

8.4 Write Disable (04h)

The Write Disable command is to reset the Write Enable Latch (WEL) bit in the Status Register. To enter the Write Disable command, $\overline{CS}$ goes low before the command 04h goes into the Data Input (SI) pin on the rising edge of SCK,; then $\overline{CS}$ goes high. WEL bit is automatically reset write- disable status of 0 after Power-up and upon completion of the every Program, Erase and Write Status Register commands.

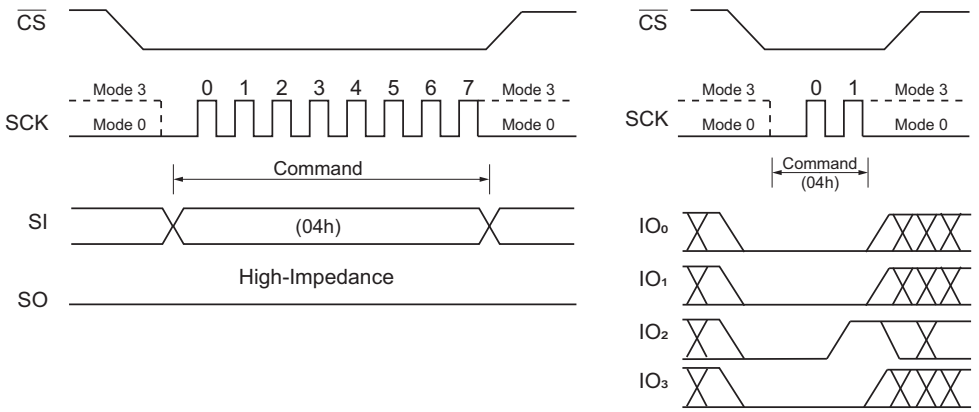

Figure 7. Write Disable Command for SPI Mode (left) and QPI Mode (right)

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8.5 Read Status Register-1 (05h) and Read Status Register-2 (35h)

The Read Status Register commands are to read the Status Register. The Read Status Register can be read at any time (even in program/erase/write Status Register and Write Security Register condition). It is recommended to check the BUSY bit before sending a new command when a Program, Erase, Write Status Register or Write Status Register operation is in progress.

The command is entered by driving $\overline{CS}$ low and sending the command code 05h for Status Register-1 or 35h for Status Register-2 into the SI pin on the rising edge of SCK. The status register bits are then shifted out on the SO pin at the falling edge of SCK with most significant bit (MSB) first, as shown in (Figure 8 and Figure 9). The Status Register can be read continuously. The command is completed by driving $\overline{CS}$ high.

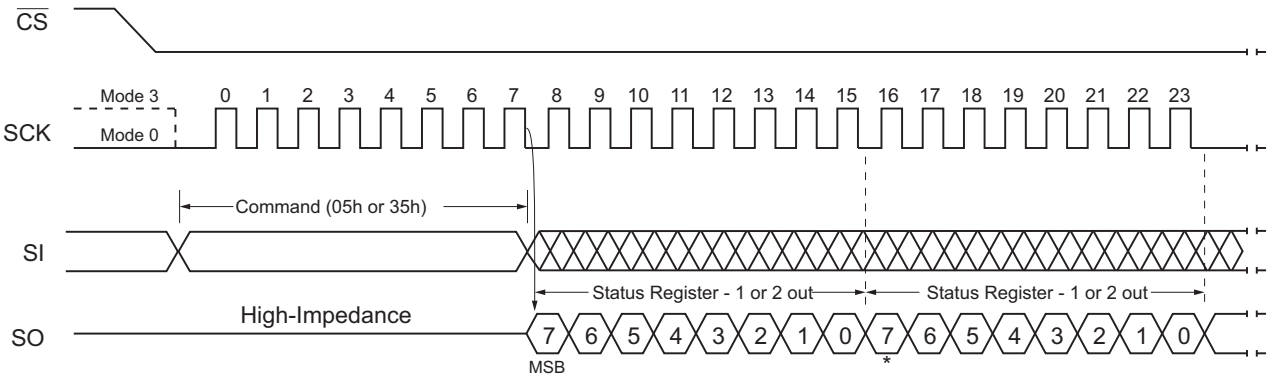

Figure 8. Read Status Register Command (SPI Mode)

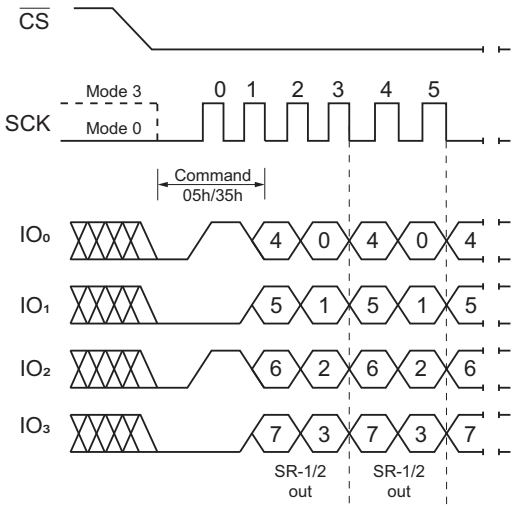

Figure 9. Read Status Register Command (QPI Mode)

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8.6 Write Status Register (01h)

The Write Status Register command is to write only non-volatile Status Register-1 bits (SRP0) and Status Register-2 bits (QE and SRP1). All other Status Register bit locations are read-only and are not affected by the Write Status Register command.

A Write Enable command must previously have been issued before setting Write Status Register Command (Status Register bit WEL must equal 1). Once write is enabled, the command is entered by driving $\overline{CS}$ low, sending the command code, and then writing the status register data byte, as shown in Figure 10 and Figure 11.

The $\overline{CS}$ pin must be driven high after the eighth or sixteenth bit of data that is clocked in. If this is not done, the Write Status Register command is not executed. If $\overline{CS}$ is driven high after the eighth clock, the QE and SRP1 bits are cleared to 0. After $\overline{CS}$ is driven high, the self- timed Write Status Register cycle commences for a time duration of t_W (see Section 9.6, AC Electrical Characteristics).

While the Write Status Register cycle is in progress, the Read Status Register command can still be accessed to check the status of the BUSY bit. The BUSY bit is a 1 during the Write Status Register cycle and a 0 when the cycle is finished and ready to accept other commands again. When the BUSY bit is asserted, the Write Enable Latch (WEL) bit in Status Register is cleared to 0.

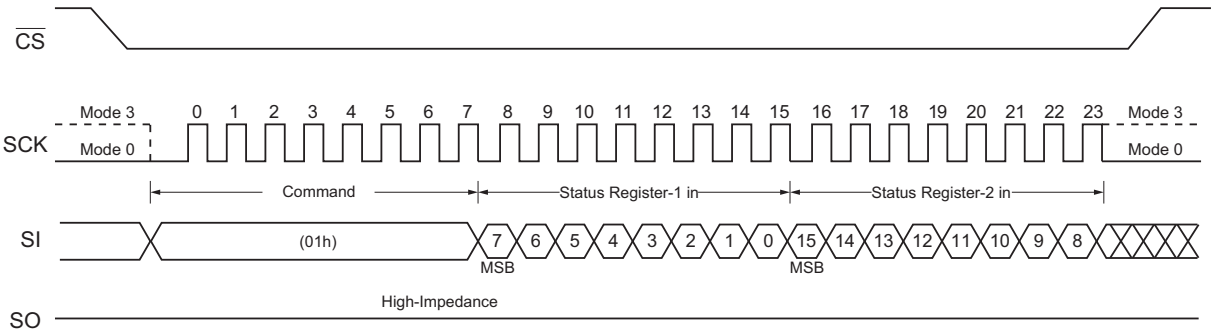

Figure 10. Write Status Register Command (SPI Mode)

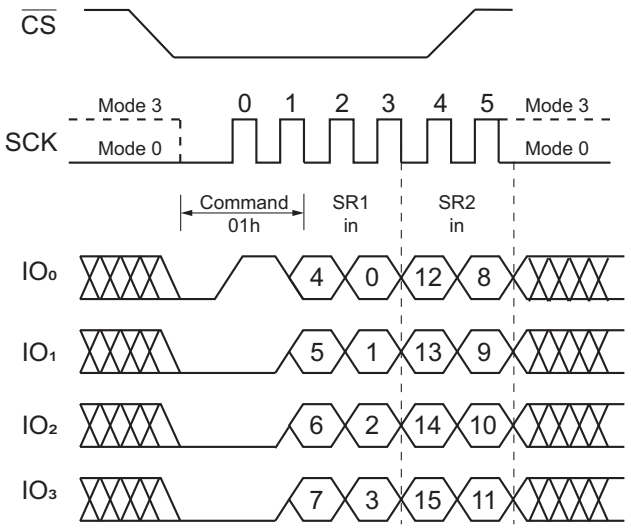

Figure 11. Write Status Register Command (QPI Mode)

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8.7 Write Status Register-2 (31h)

The Write Status Register-2 command is to write only non-volatile Status Register-2 bits (QE and SRP1).

A Write Enable command must previously have been issued before setting Write Status Register Command (Status Register bit WEL must equal 1). Once write is enabled, the command is entered by driving $\overline{CS}$ low, sending the command code, and then writing the status register data byte, as shown in Figure 11 and Figure 12.

Using Write Status Register-2 (31h) command, software can individually access each one-byte status registers via different commands.

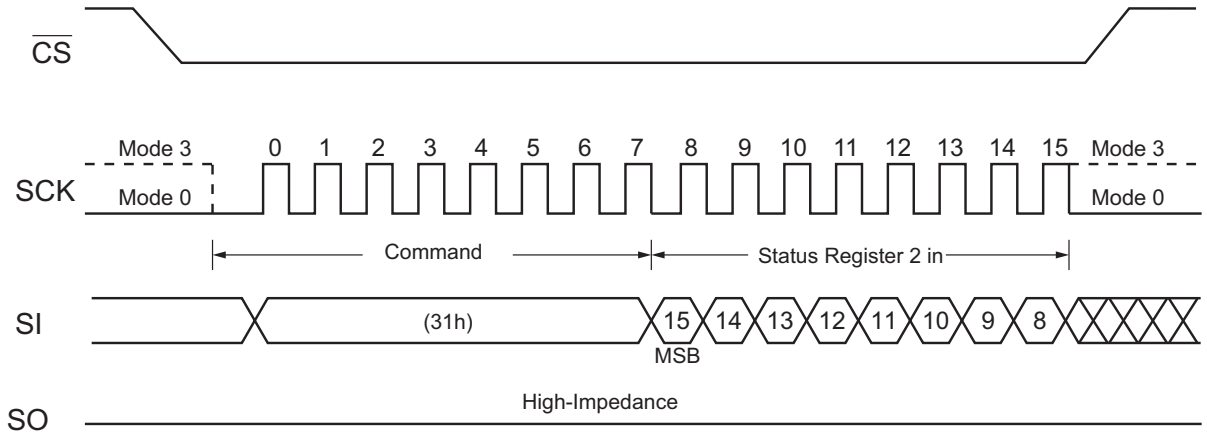

Figure 12. Write Status Register-2 Command (SPI Mode)

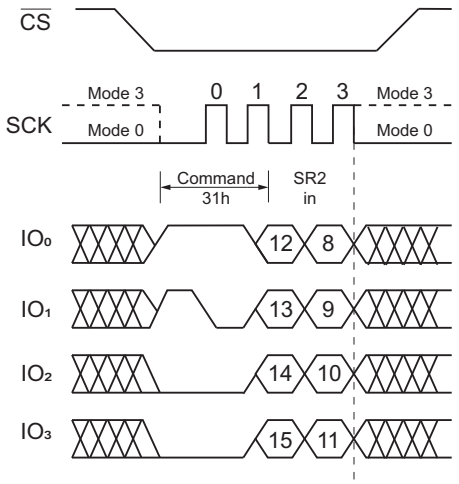

Figure 13. Write Status Register-2 Command (QPI Mode)

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8.8 Read Data (03h)

The Read Data command is to read data out from the device. The command is initiated by driving the $\overline{CS}$ pin low and then sending the command code 03h with following a 24-bit address (A23- A0) into the SI pin. After the address is received, the data byte of the addressed memory location is shifted out on the SO pin at the falling edge of SCK with most significant bit (MSB) first. The address is automatically incremented to the next higher address after byte of data is shifted out allowing for a continuous stream of data. This means that the entire memory can be accessed with a single command as long as the clock continues. The command is completed by driving $\overline{CS}$ high. The Read Data command sequence is shown in Figure 14. If a Read Data command is issued while an Erase, Program or Write Status Register cycle is in process (BUSY=1) the command is ignored and has no effect on the current cycle. The Read Data command allows clock rates from D.C to a maximum of f_R (see Section 9.6, AC Electrical Characteristics).

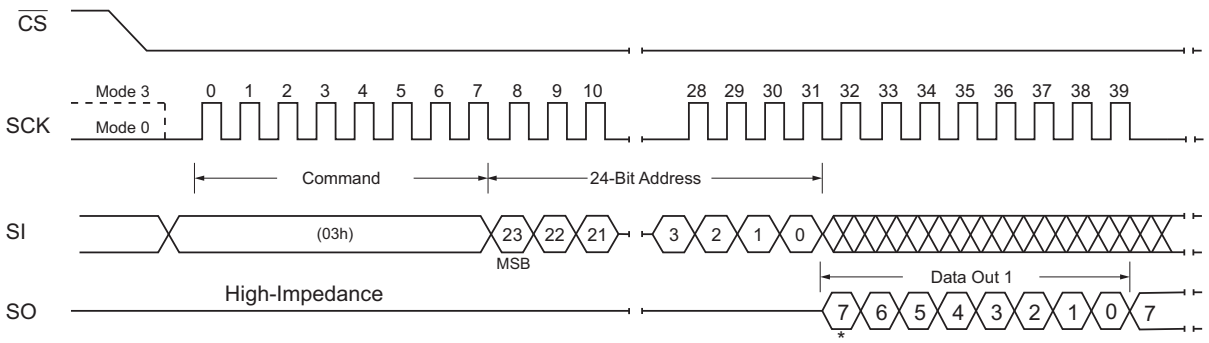

Figure 14. Read Data Command

8.9 Fast Read (0Bh)

The Fast Read command is high speed reading mode that it can operate at the highest possible frequency of FR. The address is latched on the rising edge of the SCK. After the 24-bit address, this is accomplished by adding dummy clocks, as shown in Figure 15. The dummy clocks means the internal circuits require time to set up the initial address. During the dummy clocks, the data value on the SO pin is a don't care. Data of each bit shifts out on the falling edge of SCK.

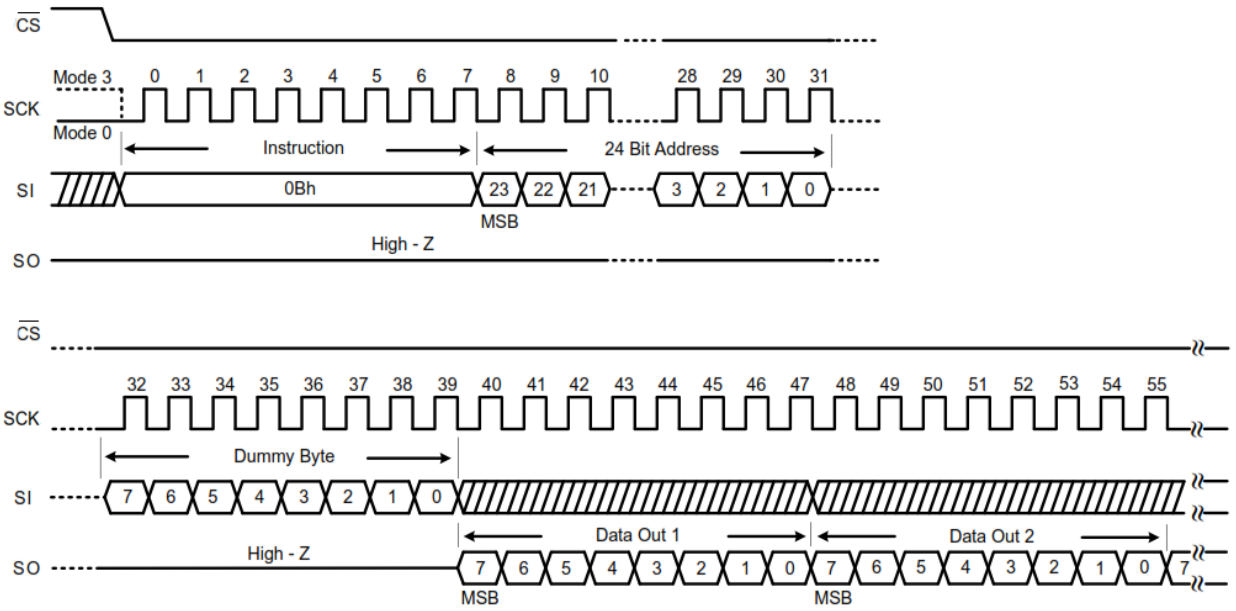

Figure 15. Fast Read Command (SPI Mode)

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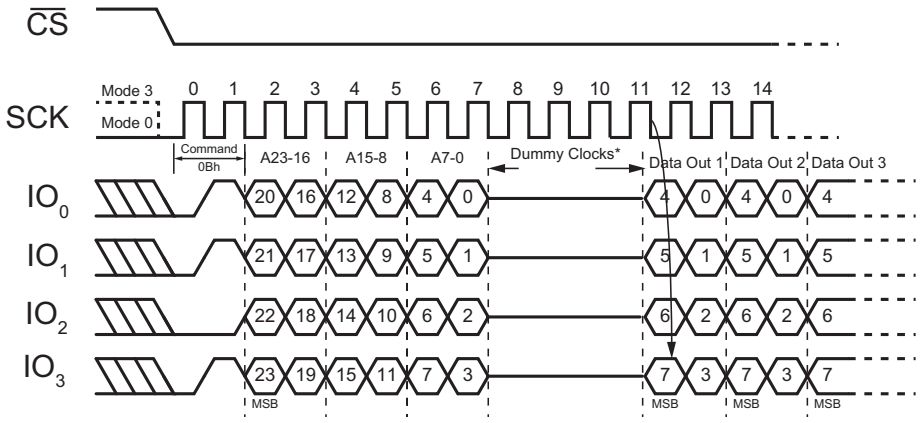
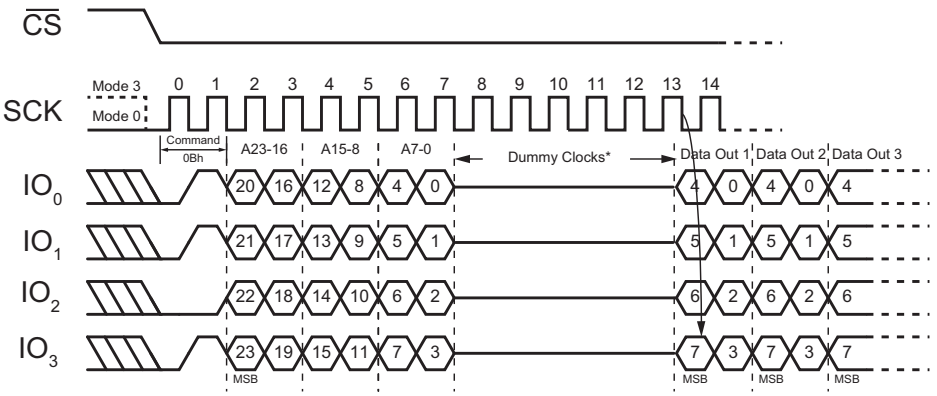
8.10 Fast Read in QPI Mode

When QPI mode is enabled, the number of dummy clock is configured by the Set Read Parameters (C0h) command to accommodate wide range applications with different needs for either maximum Fast Read frequency or minimum data access latency. Depending on the Read Parameter Bit P[4] and P[5] setting, the number of dummy clocks can be configured as either 4, or 6 or 8. The default number of dummy clocks upon power up or after a Reset command is four. (See Figure 15, Figure 16, and Figure 17).



* = “Set Read Parameters” command (C0h) can set the number of dummy clocks

Figure 16. Fast Read Command (QPI Mode, 80MHz)



* = “Set Read Parameters” command (C0h) can set the number of dummy clocks

Figure 17. Fast Read Command (QPI Mode, 104MHz)

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8.11 Fast Read Dual Output (3Bh)

By using two pins (IO_0 and IO_1, instead of just IO_0), The Fast Read Dual Output command allows data to be transferred from the AT25QL128A at twice the rate of standard SPI devices. The Fast Read Dual Output command is ideal for quickly downloading code from Flash to RAM upon power-up or for application that cache code-segments to RAM for execution.

The Fast Read Dual Output command can operate at the highest possible frequency of F_R (see Section 9.6, AC Electrical Characteristics). After the 24-bit address, this is accomplished by adding eight dummy clocks, as shown in Figure 18. The dummy clocks allow the internal circuits additional time for setting up the initial address. During the dummy clocks, the data value on the SO pin is a don't care. However, the IO_0 pin must be high-impedance before the falling edge of the first data out clock.

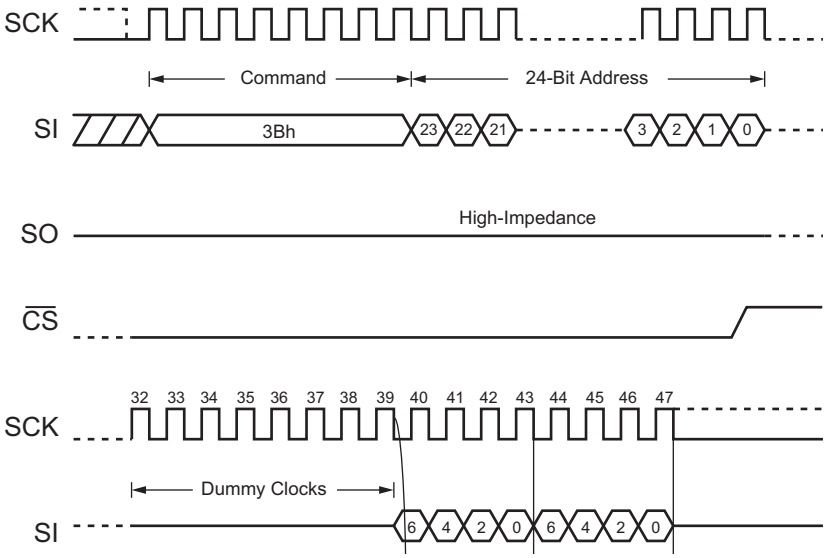

Figure 18. Fast Read Dual Output Command (SPI Mode)

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8.12 Fast Read Quad Output (6Bh)

By using four pins (IO_0, IO_1, IO_2, and IO_3), The Fast Read Quad Output command allows data to be transferred from the AT25QL128A at four times the rate of standard SPI devices. A Quad enable of Status Register-2 must be executed before the device can accept the Fast Read Quad Output command (Status Register bit QE must equal 1).

The Fast Read Quad Output command can operate at the highest possible frequency of F_R (see Section 9.6, AC Electrical Characteristics). This is accomplished by adding eight dummy clocks after the 24- bit address, as shown in Figure 19. The dummy clocks allow the internal circuits additional time for setting up the initial address. During the dummy clocks, the data value on the SO pin is a don't care. However, the IO_0 pin must be high-impedance before the falling edge of the first data out clock.

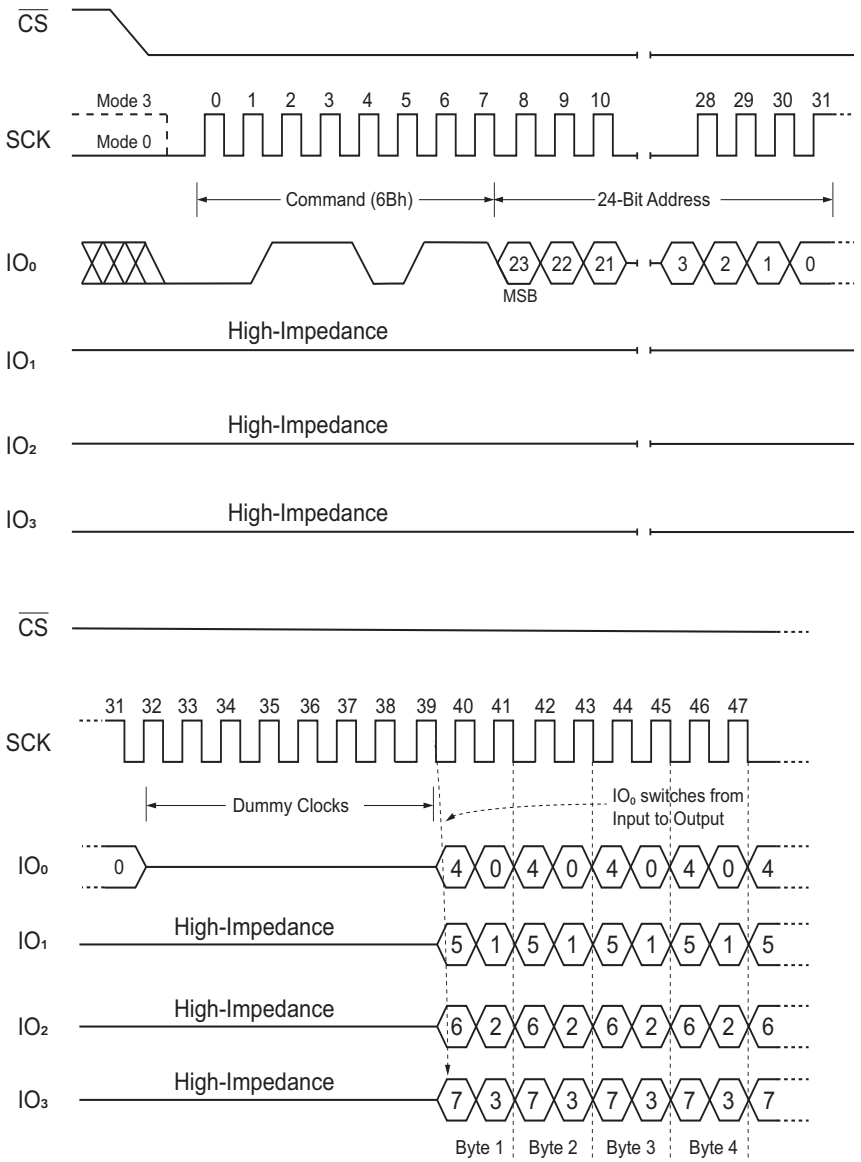

Figure 19. Fast Read Quad Output Command (SPI Mode)

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8.13 Fast Read Dual I/O (BBh)

The Fast Read Dual I/O command reduces cycle overhead through double access using pins IO_0 and IO_1.

Continuous Read Mode

The Fast Read Dual I/O command can further reduce cycle overhead through setting the Mode bits (M7-0) after the input Address bits (A23-0). The upper nibble of the Mode (M7-4) controls the length of the next Fast Read Dual I/O command through the inclusion or exclusion of the first byte command code. The lower nibble bits of the Mode (M3-0) are don't care (X), However, the IO pins must be high-impedance before the falling edge of the first data out clock.

If the Mode bits (M7-0) equal Ax hex, the next Fast Dual I/O command (after $\overline{CS}$ is raised and then lowered) does not require the command (BBh) code, as shown in Figure 20 and Figure 21. This reduces the command sequence by eight clocks and allows the address to be immediately entered after $\overline{CS}$ is asserted low. If Mode bits (M7-0) are any value other Ax hex, the next command (after $\overline{CS}$ is raised and then lowered) requires the first byte command code, thus returning to normal operation. A Mode Bit Reset can be used to reset Mode Bits (M7-0) before issuing normal commands.

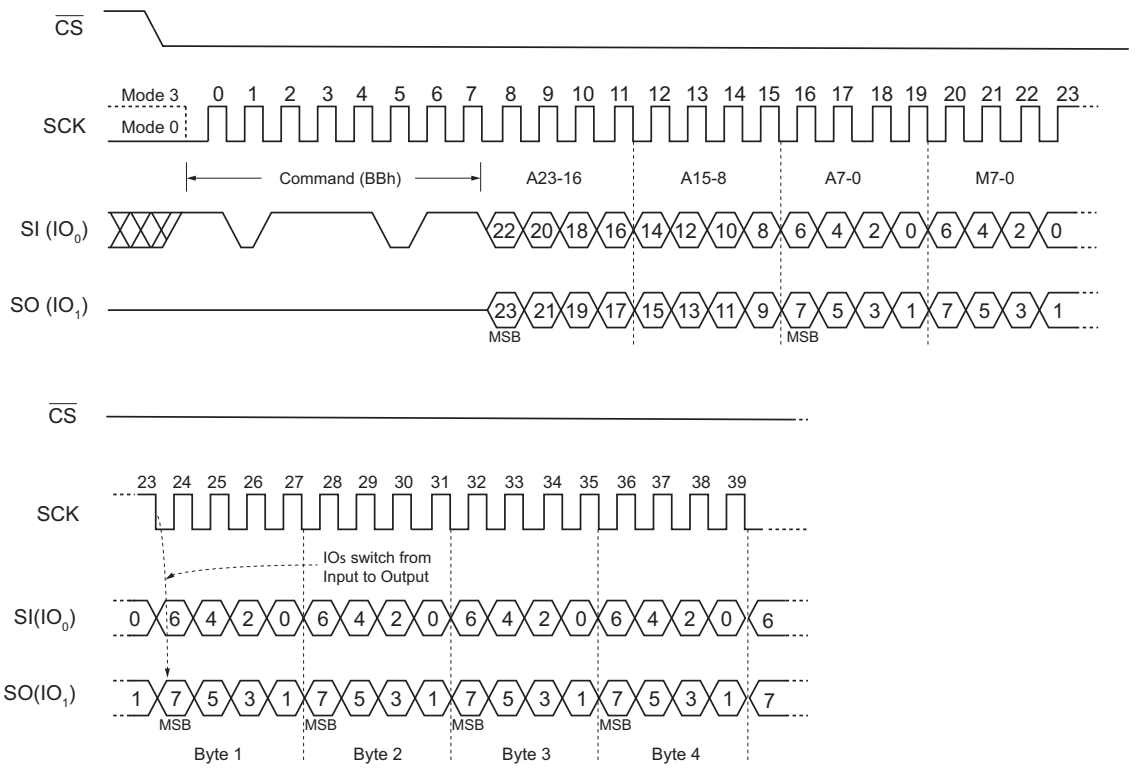

Figure 20. Fast Read Dual I/O Command (initial command or previous M7-0≠ Axh)

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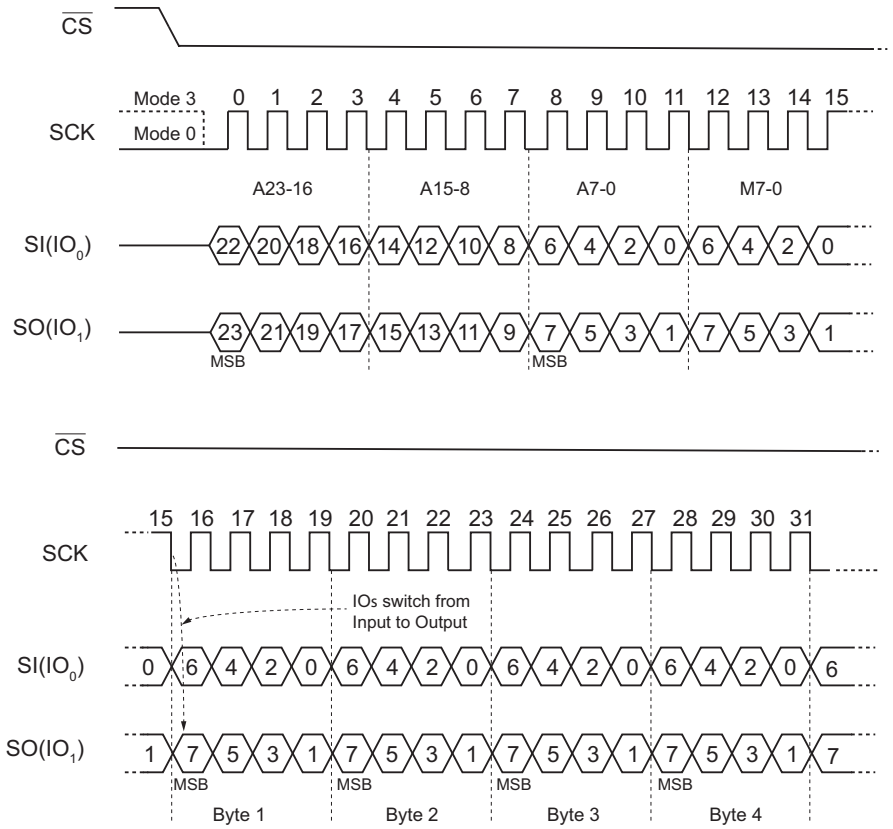

Figure 21. Fast Read Dual I/O Command (previous M7-0 = Axh)

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8.14 Fast Read Quad I/O (EBh)

The Fast Read Quad I/O command reduces cycle overhead through quad access using four IO pins: IO_0, IO_1, IO_2, and IO_3. The Quad Enable bit (QE) of Status Register-2 must be set to enable the Fast read Quad I/O Command.

Continuous Read Mode

The Fast Read Quad I/O command can further reduce command overhead through setting the Mode bits (M7-0) with following the input Address bits (A23-0), as shown in Figure 22. The upper nibble of the Mode (M7-4) controls the length of the next Fast Read Quad I/O command through the inclusion or exclusion of the first byte command code. The lower nibble bits of the Mode (M3-0) are don't care (X). However, the IO pins must be high-impedance before the falling edge of the first data out clock.

If the Mode bits (M7-0) equal Ax hex, then the next Fast Read Quad I/O command (after $\overline{CS}$ is raised and then lowered) does not require the EBh command code, as shown in Figure 23. This reduces the command sequence by eight clocks and allows the address to be immediately entered after $\overline{CS}$ is asserted low. If the Mode bits (M7-0) are any value other than Ax hex, the next command (after $\overline{CS}$ is raised and then lowered) requires the first byte command code, thus retuning normal operation. A Mode Bit Reset can be used to reset Mode Bits (M7-0) before issuing normal commands.

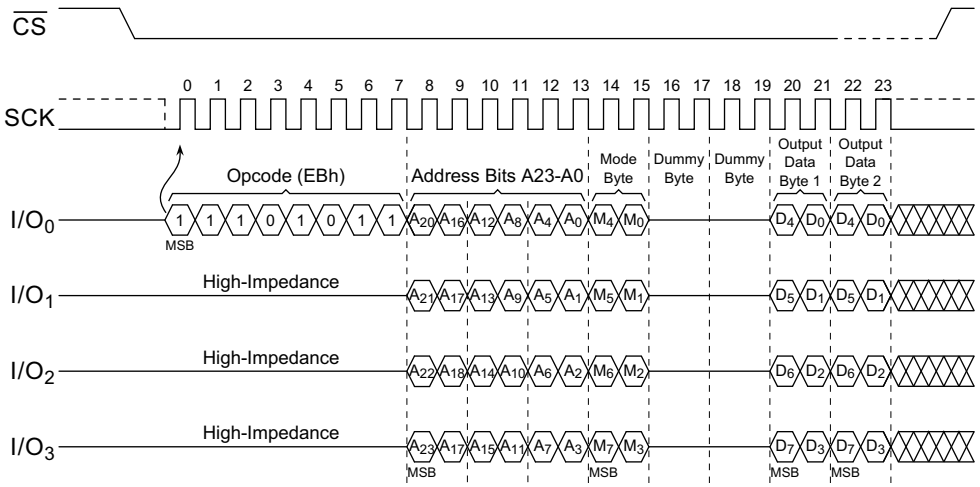

Figure 22. Fast Read Quad I/O Command (Initial command or previous M7-0 ≠ Axh, SPI mode)

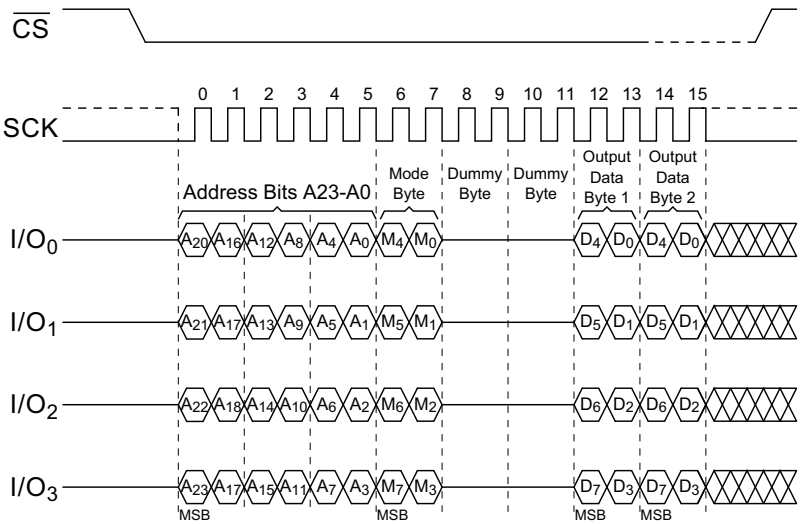

Figure 23. Fast Read Quad I/O Command (previous M7-0 = Axh, SPI mode)

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Wrap Around in SPI Mode

The Fast Read Quad I/O command can also be used to access specific portion within a page by issuing a Set Burst with Wrap (77h) command prior Fast Read Quad I/O (EBh) command. The Set Burst with Wrap (77h) command can either enable or disable the Wrap Around feature for the following Fast Read Quad I/O command.

When Wrap Around is enabled, the data being accessed can be limited to an 8/16/32/64-byte section of a 256-byte page. The output data starts at the initial address specified in the command, once it reaches the ending boundary of the 8/16/32/64-byte section, the output wraps around to the beginning boundary automatically until $\overline{CS}$ is pulled high to terminate the command.

The Burst with Wrap feature allows applications that use cache to quickly fetch a critical address and then fill the cache afterwards within a fixed length (8/16/32/64-byte) of data without issuing multiple read commands. (See Section 8.32.)

Fast Read Quad I/O in QPI Mode

When QPI mode in enabled, the number of dummy clocks is configured by the Set Read Parameters (C0h) command to accommodate a wide range applications with different needs for either maximum Fast Read frequency or minimum data access latency. Depending on the Read Parameter Bits P [4] and P [5] setting, the number of dummy clocks can be configured as either 4 or 6 or 8. The default number of dummy clocks upon power up or after a Reset (99h) command is 4.

The Continuous Read Mode feature is also available in QPI mode for Fast Read Quad I/O command. In QPI mode, the Continuous Read Mode bits M7-0 are also considered as dummy clocks. In the default setting, the data output follows the Continuous Read Mode bits immediately.

The Wrap Around feature is not available in QPI mode for Fast Read Quad I/O command. To perform a read operation with fixed data length wrap around in QPI mode, a Burst Read with Wrap (0Ch) command must be used. (See Section 8.33.)

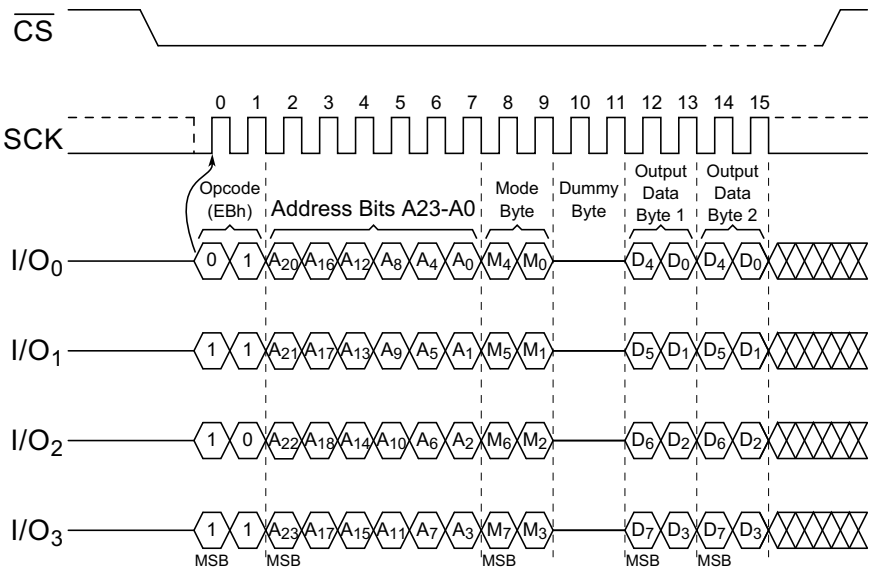

Figure 24. Fast Read Quad I/O Command (Initial command or previous M7-0 ≠ Axh, QPI mode, 80 MHz)

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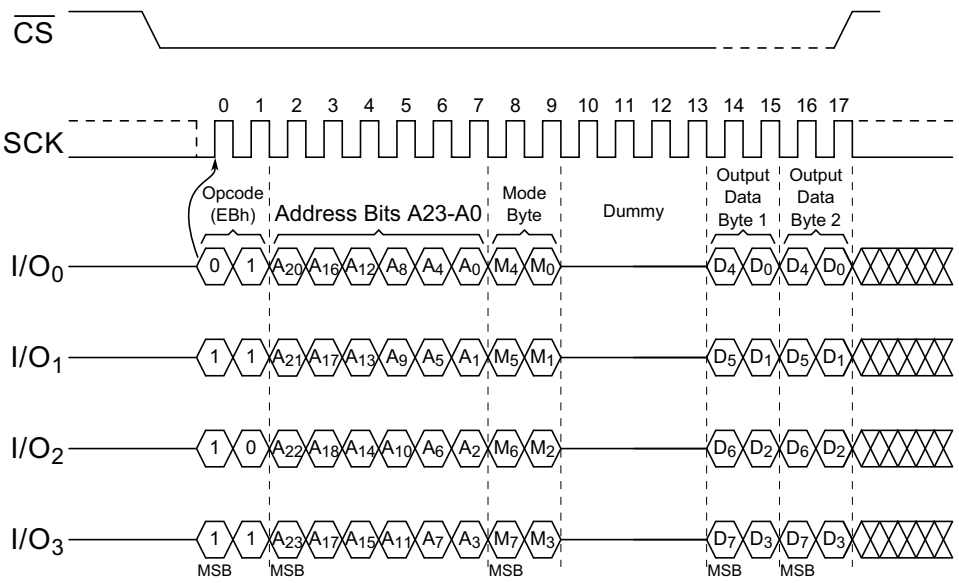

Figure 25. Fast Read Quad I/O Command (Initial command or previous M7-0 ≠ Axh, QPI mode, 133 MHz)

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8.15 Page Program (02h)

The Page Program command is for programming the memory to be 0. A Write Enable command must be issued before the device accept the Page Program Command (Status Register bit WEL=1). After the Write Enable (WREN) command has been decoded, the device sets the Write Enable Latch (WEL). The command is entered by driving the $\overline{CS}$ pin low and then sending the command code 02h with following a 24-bits address (A23-A0) and at least one data byte, into the SI pin. The $\overline{CS}$ pin must be driven low for the entire time of the command while data is being sent to the device. (See Figure 26 and Figure 27).

If an entire 256 byte page is to be programmed, the last address byte (the eight least significant address bits) must be set to 0. If the last address byte is not zero, and the number of clocks exceeds the remaining page length, the addressing wraps to the beginning of the page. In some cases, less than 256 bytes (a partial page) can be programmed without having any effect on other bytes within the same page. One condition to perform a partial page program is that the number of clocks cannot exceed the remaining page length. If more than 256 bytes are sent to the device, the addressing wraps to the beginning of the page and overwrites previously sent data.

The $\overline{CS}$ pin must be driven high after the eighth bit of the last byte has been latched. If this is not done, the Page Program command is not executed. After $\overline{CS}$ is driven high, the self-timed Page Program command is active for a time duration of t_{PP} (see Section 9.6, AC Electrical Characteristics). While the Page Program cycle is in progress, the Read Status Register command can still be accessed for checking the status of the BUSY bit. The BUSY bit is a 1 during the Page Program cycle and becomes a 0 when the cycle is finished and the device is ready to accept other commands again. When the BUSY bit is asserted, the Write Enable Latch (WEL) bit in the Status Register is cleared to 0.

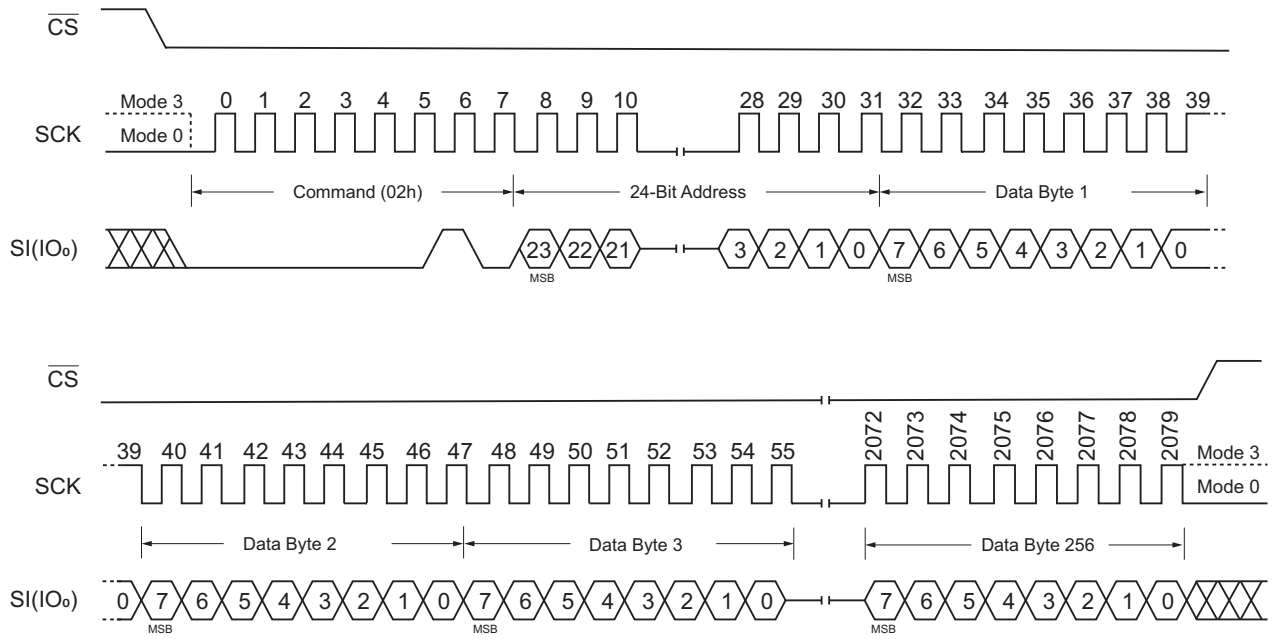

Figure 26. Page Program Command (SPI Mode)

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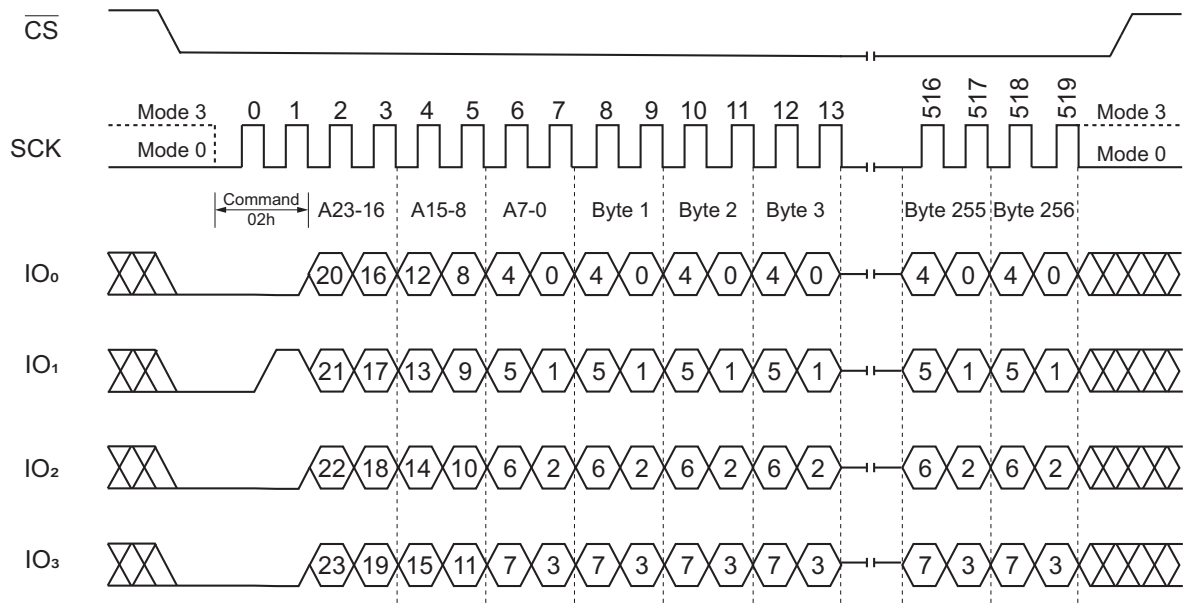

Figure 27. Page Program Command (QPI Mode)

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8.16 Quad Page Program (33h)

The Quad Page Program command is to program the memory as being 0 at previously erased memory areas. The Quad Page Program takes four pins: IO_0, IO_1, IO_2 and IO_3 as address and data input, which can improve programmer performance and the effectiveness of application of lower clock less than 5 MHz. A system using a faster clock speed does not get more benefit for the Quad Page Program because the required internal page program time is far more than the time data clock-in.

To use Quad Page Program, the Quad Enable bit must be set, A Write Enable command must be executed before the device accepts the Quad Page Program command (Status Register-1, WEL = 1). The command is initiated by driving the $\overline{CS}$ pin low then sending the command code 33h with following a 24-bit address (A23-A0) and at least one data, into the IO pins. The $\overline{CS}$ pin must be held low for the entire length of the command while data is being sent to the device. All other functions of Quad Page Program are perfectly same as standard Page Program. (See Figure 28 and Figure 29).

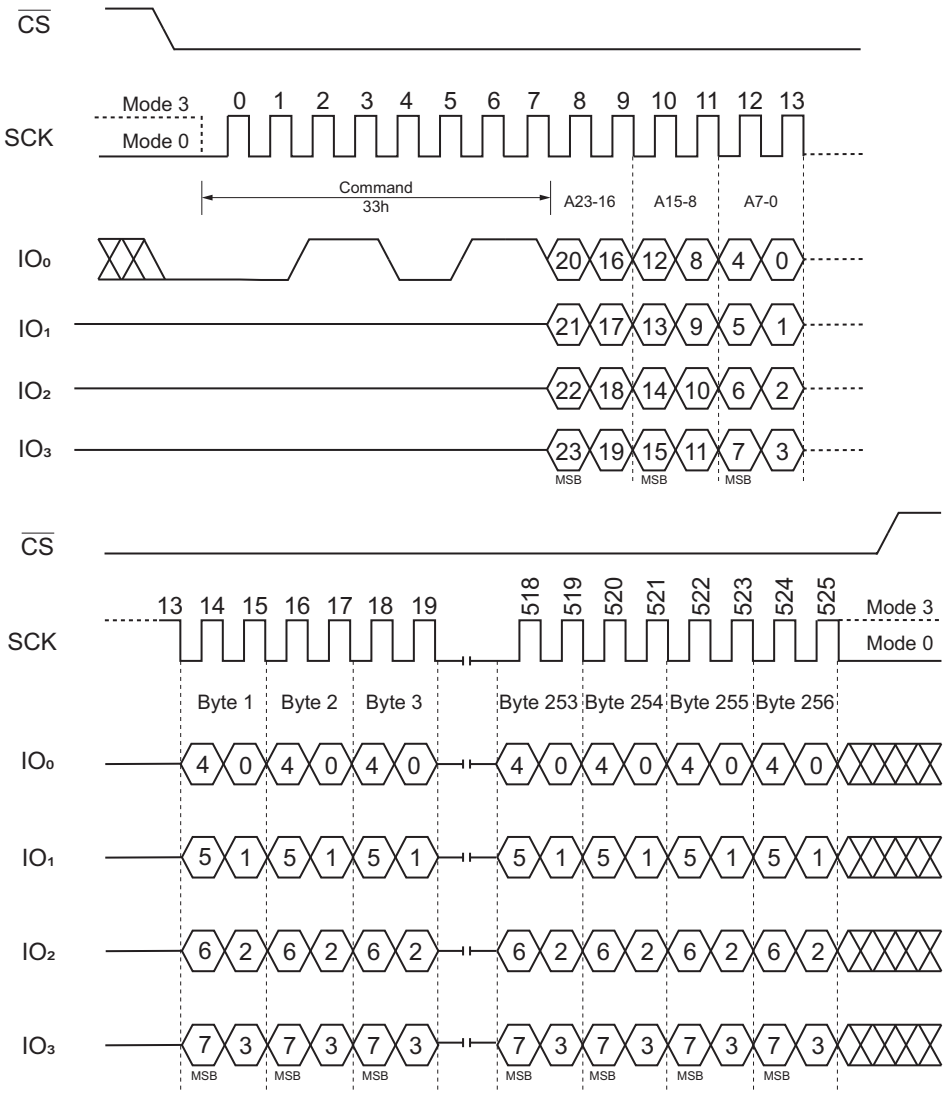

Figure 28. Quad Page Program Command (SPI mode)

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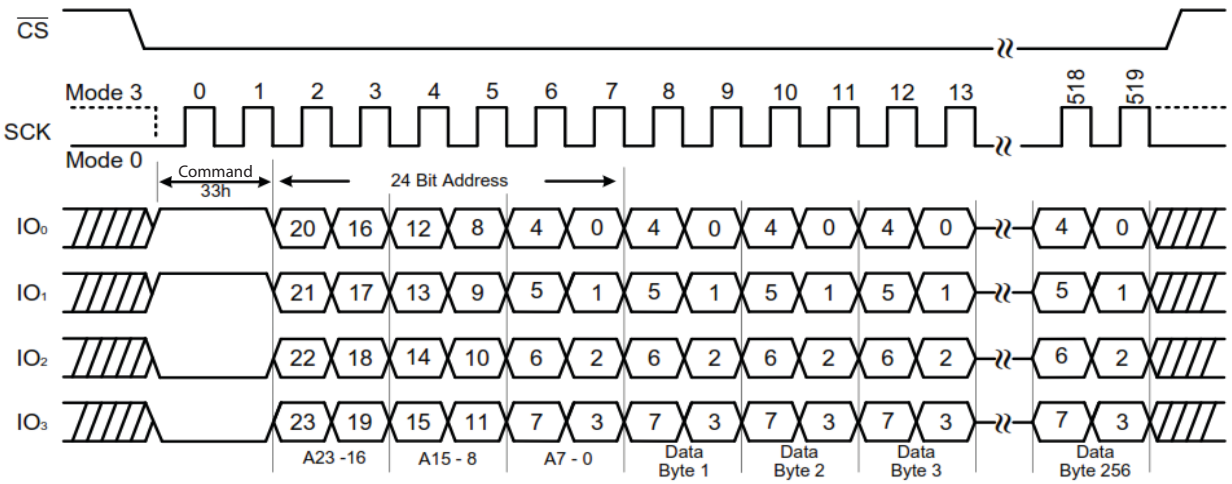

Figure 29. Quad Page Program Command (QPI mode)

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8.17 4 kbytes Block Erase (20h)

The Block Erase command is to erase the data of the selected block as being 1. The command is used for 4 kbytes block. The Write Enable command must be issued before issuing the Block Erase command. The command is initiated by driving the $\overline{CS}$ pin low and shifting the command code 20h followed a 24-bit block address (A23 - A0). (See Figure 30 and Figure 31.) The $\overline{CS}$ pin must go high after the eighth bit of the last byte has been latched in; otherwise, the Block Erase command is not executed. After $\overline{CS}$ goes high, the self-timed Block Erase command is active for a time duration of t_{SE} (see Section 9.6, AC Electrical Characteristics).

While the Block Erase cycle is in progress, the Read Status Register command can still be accessed for checking the status of the BUSY bit. The BUSY bit is a 1 during the Block Erase cycle and becomes a 0 when the cycle is finished and the device is ready to accept other commands again. When the BUSY bit is asserted, the Write Enable Latch (WEL) bit in the Status Register is cleared to 0.

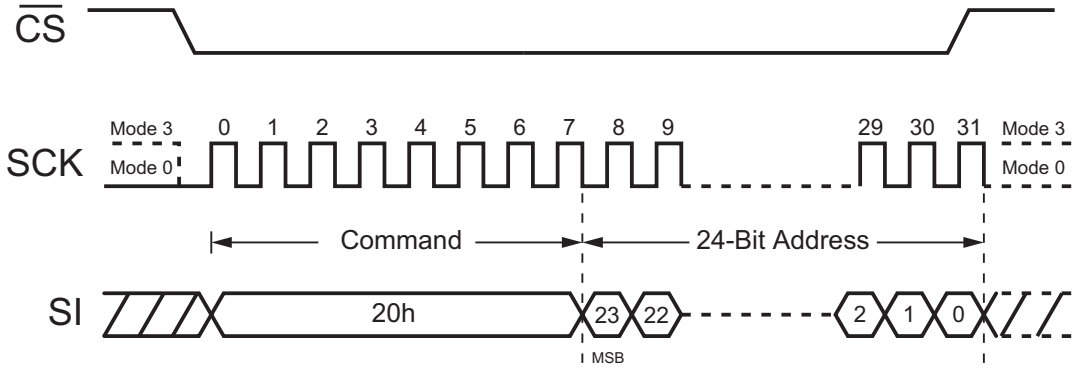

Figure 30. Block Erase Command (SPI Mode)

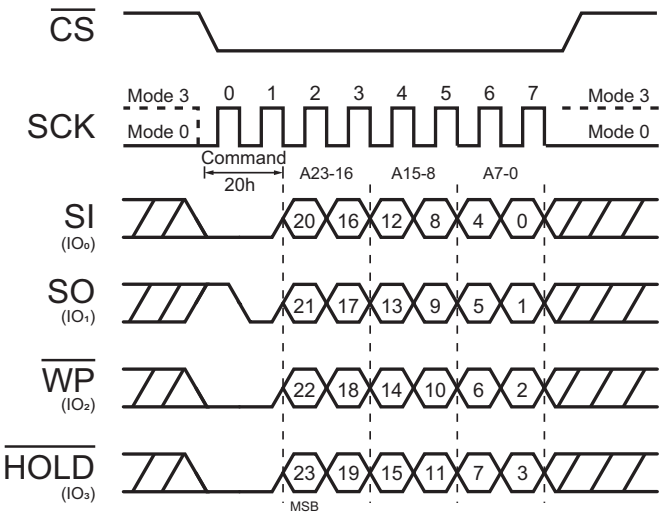

Figure 31. Block Erase Command (QPI Mode)

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8.18 32 kbytes Block Erase (52h)

The Block Erase command is to erase the data of the selected block as being 1. The command is used for 32 kbytes Block erase operation. A Write Enable command must be issued before the Block Erase Command. The command is initiated by driving the $\overline{CS}$ pin low and shifting the command code 52h followed a 24-bit block address (A23-A0). (See Figure 32 and Figure 33.) The $\overline{CS}$ pin must go high after the eighth bit of the last byte has been latched in, otherwise, the Block Erase command is not executed. After $\overline{CS}$ is driven high, the self-timed Block Erase command is active for a time duration of t_{BE1} (see Section 9.6, AC Electrical Characteristics).

While the Block Erase cycle is in progress, the Read Status Register command can still be read the status of the BUSY bit. The BUSY bit is a 1 during the Block Erase cycle and becomes a 0 when the cycle is finished and the device is ready to accept other commands again. When the BUSY bit is asserted, the Write Enable Latch (WEL) bit in the Status Register is cleared to 0.

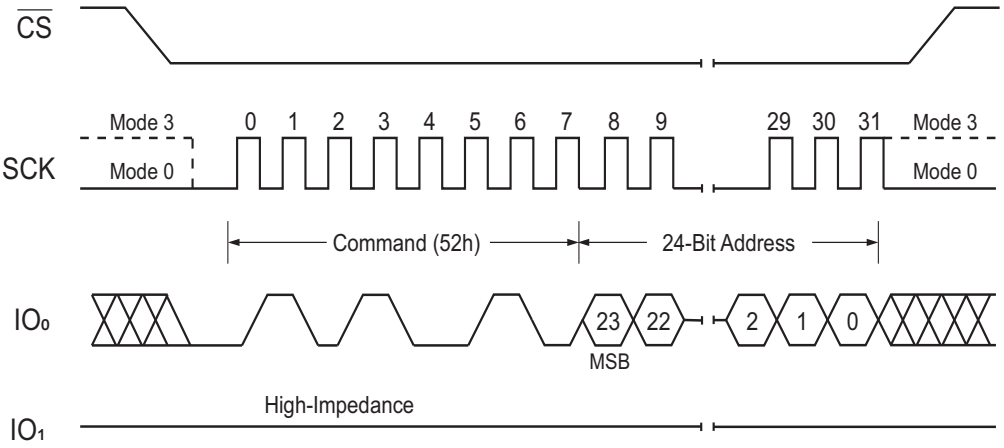

Figure 32. 32 kbytes Block Erase Command (SPI Mode)

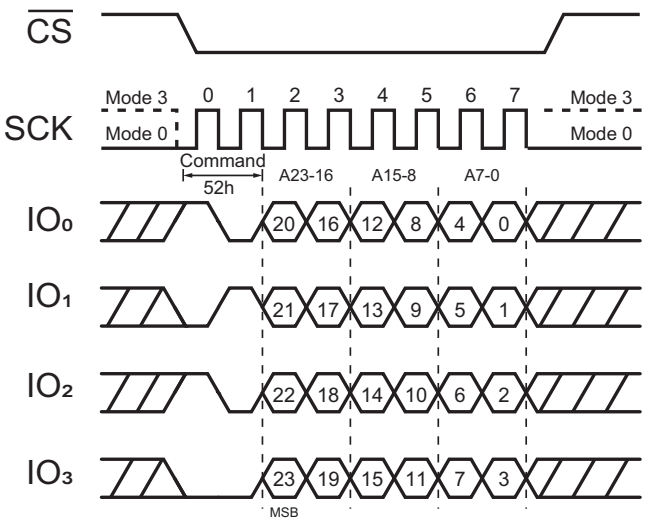

Figure 33. 32 kbytes Block Erase Command (QPI Mode)

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8.19 64 kbytes Block Erase (D8h)

The Block Erase command is to erase the data of the selected block as being 1. The command is used for 64 kbytes Block erase operation. A Write Enable command must be issued before issuing the Block Erase Command. The command is initiated by driving the $\overline{CS}$ pin low and shifting the command code D8h followed a 24-bit block address (A23-A0). (See Figure 34 and Figure 35.) The $\overline{CS}$ pin must go high after the eighth bit of the last byte has been latched in, otherwise, the Block Erase command is not executed. After $\overline{CS}$ is driven high, the self-timed Block Erase command is active for a time duration of t_{BE2} (see Section 9.6, AC Electrical Characteristics).

While the Block Erase cycle is in progress, the Read Status Register command can still be read the status of the BUSY bit. The BUSY bit is a 1 during the Block Erase cycle and becomes a 0 when the cycle is finished and the device is ready to accept other commands again. When the BUSY bit is asserted, the Write Enable Latch (WEL) bit in the Status Register is cleared to 0.

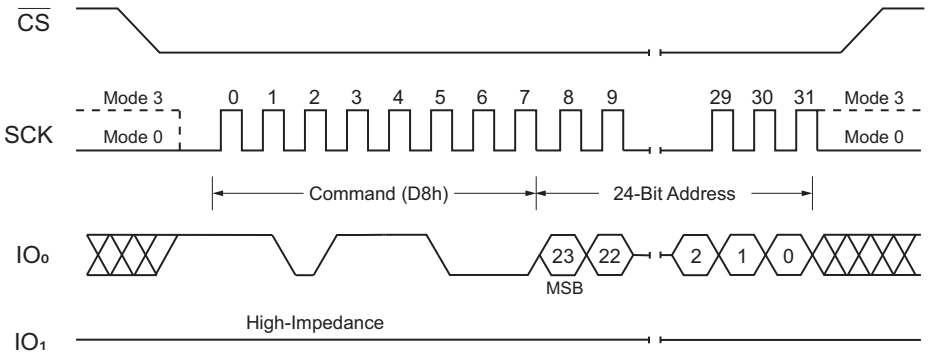

Figure 34. 64 kbytes Block Erase Command (SPI Mode)

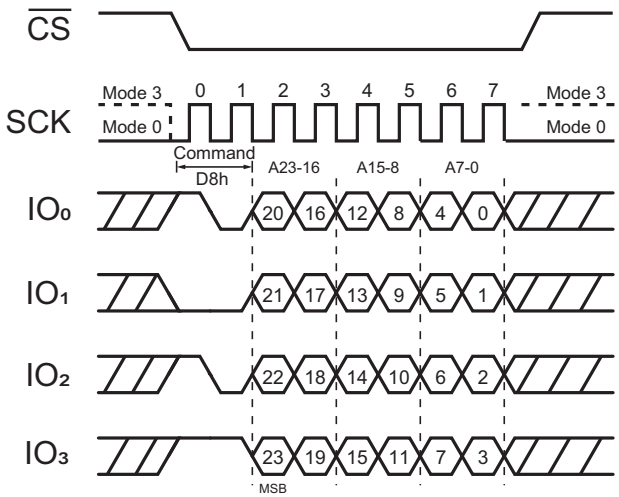

Figure 35. 64 kbytes Block Erase Command (QPI Mode)

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8.20 Chip Erase (C7h / 60h)

The Chip Erase command clears all bits in the device to be FFh (all 1s). A Write Enable command must be issued before issuing the Chip Erase command. The command is initiated by driving the $\overline{CS}$ pin low and shifting the command code C7h or 60h. (See Figure 36.) The $\overline{CS}$ pin must go high after the eighth bit of the last byte has been latched in, otherwise, the Chip Erase command is not executed. After $\overline{CS}$ is driven high, the self-timed Chip Erase command is active for a duration of t_{CE} (see Section 9.6, AC Electrical Characteristics).

While the Chip Erase cycle is in progress, the Read Status Register command can still be accessed to check the status of the BUSY bit. The BUSY bit is a 1 during the Chip Erase cycle and becomes a 0 when the cycle is finished and the device is ready to accept other commands again. When the BUSY bit is asserted, the Write Enable Latch (WEL) bit in the Status Register is cleared to 0.

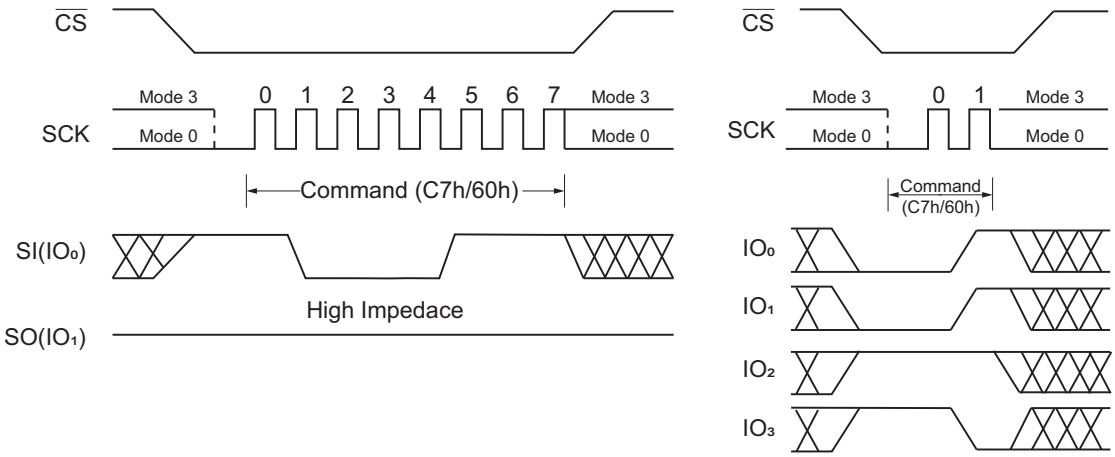

Figure 36. Chip Erase Command for SPI Mode (left) and QPI Mode (right)

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8.21 Erase / Program Suspend (75h)

The Erase/Program Suspend command allows the system to interrupt a Block Erase, Block Erase operation or a Page Program, Quad Data Input Page Program, Quad Page Program operation.

Erase Suspend is valid only during the Block or Block erase operation. The Write Status Register-1 (01h), Write Status Register-2 (31h) command and Erase commands (20h, 52h, D8h, C7h, 60h) are not allowed during Erase Suspend. During the Chip Erase operation, the Erase Suspend command is ignored.

Program Suspend is valid only during the Page Program, Quad Data Input Page Program or Quad Page Program operation. The Write Status Register-1 (01h), Write Status Register-2 (31h) command, Program commands (02h and 33h) and Erase Commands (20h, 52h, D8h, C7h, 60h) are not allowed during Program Suspend.

The Erase/Program Suspend command 75h is accepted by the device only if the SUS bit in the Status Register equals to 0 and the BUSY bit equals to 1 while a Block Erase or a Page Program operation is on-going. If the SUS bit equals to 1 or the BUSY bit equals to 0, the Suspend command is ignored by the device. A maximum of time of t_{SUS} (see Section 9.6, AC Electrical Characteristics) is required to suspend the erase or program operation. After Erase/Program Suspend, the SUS bit in the Status Register is set from 0 to 1 immediately, and the BUSY bit in the Status Register is cleared from 1 to 0 within t_{SUS}. For a previously resumed Erase/Program operation, it is also required that the Suspend command 75h is not issued earlier than a minimum of time of t_{SUS} following the preceding Resume command 7Ah.

A read operation from an 8-Mbit area (referred to as a physical block) that includes a suspended area might provide unreliable data. For the definition of the physical block and for the techniques to ensure high data integrity, see application note AN-500.

Unexpected power-off during the Erase/Program suspend state resets the device and releases the suspend state. SUS bit in the Status Register also resets to 0. The data within the page, or block that was being suspended can become corrupted. It is recommended for the user to implement system design techniques against the accidental power interruption and preserve data integrity during erase/program suspend state. (See Figure 37 and Figure 38).

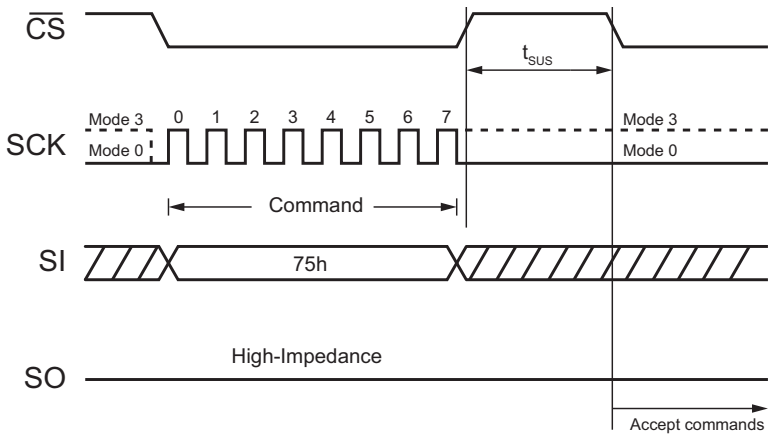

Figure 37. Erase Suspend command (SPI Mode)

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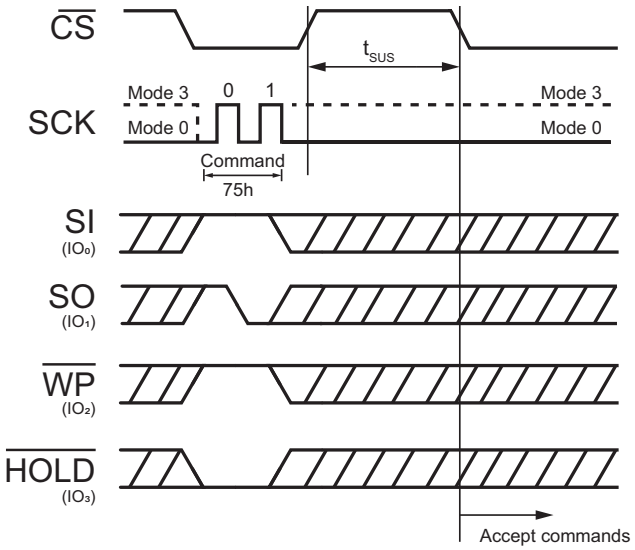

Figure 38. Erase Suspend command (QPI Mode)

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8.22 Erase / Program Resume (7Ah)

The Erase/Program Resume command 7Ah is to restart the Block Erase operation or the Page Program operation upon an Erase/Program Suspend. The Resume command 7Ah is accepted by the device only if the SUS bit in the Status Register equals to 1 and the BUSY bit equals to 0. After issued, hardware clears the SUS bit from 1 to 0 immediately, and sets the BUSY bit from 0 to 1 within 200ns and the Block completes either the erase operation, or the page completes the program operation. If the SUS bit equals to 0 or the BUSY bit equals to 1, the Resume command 7Ah is ignored by the device.

Resume command cannot be accepted if the previous Erase/Program Suspend operation was interrupted by unexpected power-off. It is also required that a subsequent Erase/Program Suspend command not to be issued within a minimum of time of t_{SUS} following a previous Resume command. (See Figure 39 and Figure 40).

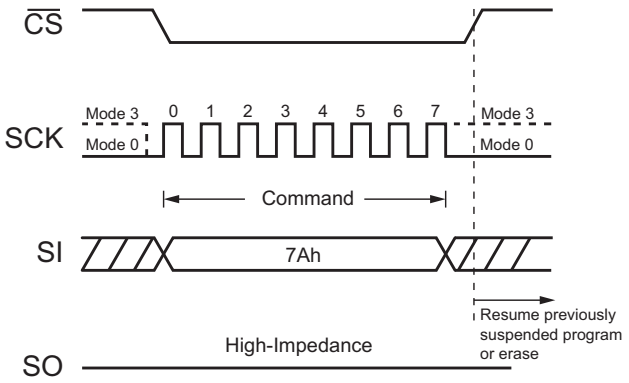

Figure 39. Erase / Program Resume command (SPI Mode)

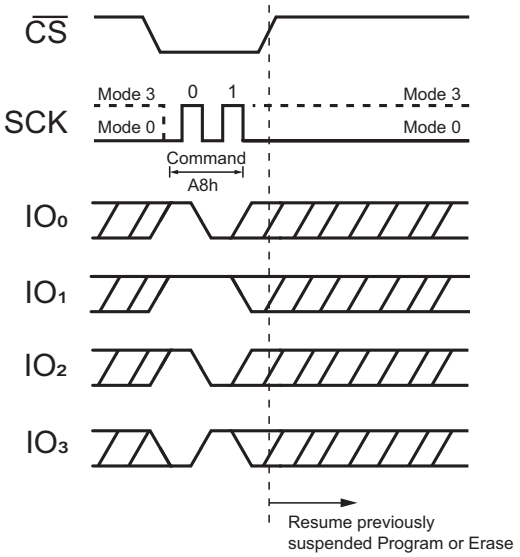

Figure 40. Erase / Program Resume command (QPI Mode)

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8.23 Deep Power-Down (B9h)

Executing the Deep Power-Down command is the best way to put the device in the lowest power consumption. The Deep Power-Down command reduces the standby current (from ICC1 to ICC2, as specified in Section 9.6, AC Electrical Characteristics). The command is entered by driving the $\overline{CS}$ pin low with following the command code B9h. (See Figure 41 and Figure 42.)

The $\overline{CS}$ pin must go high exactly at the byte boundary (the latest eighth bit of command code been latched-in); otherwise, the Deep Power-Down command is not executed. After $\overline{CS}$ goes high, it requires a delay of t_{DP} before the Deep Power-Down mode is entered. While in the Release Deep Power-Down / Device ID command, which restores the device to normal operation, is recognized. All other commands are ignored, including the Read Status Register command, which is always available during normal operation. Deep Power-Down Mode automatically stops at Power-Down, and the device always powers up in Standby Mode.

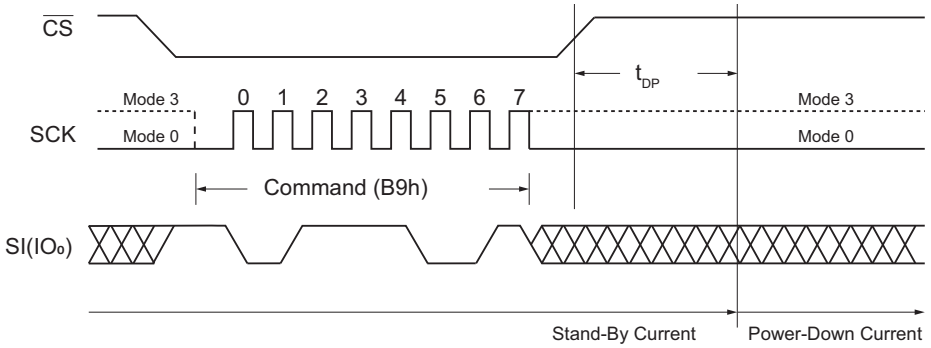

Figure 41. Deep Power-Down Command (SPI Mode)

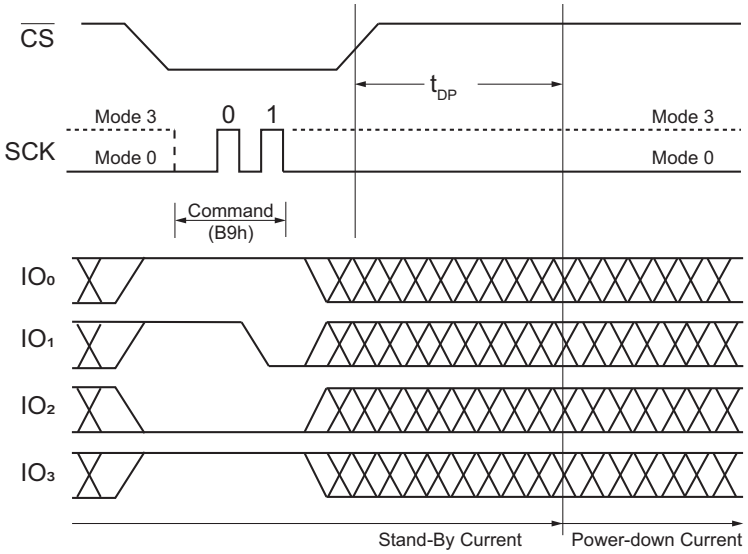

Figure 42. Deep Power-Down Command (QPI Mode)

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8.24 Release Deep Power-Down / Device ID (ABh)

The Release Deep Power-Down / Device ID command is a multi-purpose command. It can be used to release the device from the Deep Power-Down state or obtain the device identification (ID).

The command is issued by driving the $\overline{CS}$ pin low, sending the command code ABh and driving $\overline{CS}$ high, as shown in figure Figure 43 and Figure 44. Release from Deep Power-Down require the time duration of t_{RES1} (see Section 9.6, AC Electrical Characteristics) for re-work a normal operation and accepting other commands. The $\overline{CS}$ pin must keep high during the tRES1 time duration.

The Device ID can be read during SPI mode only. In other words, Device ID feature is not available in QPI mode for Release Deep Power-Down/Device ID command. To obtain the Device ID in SPI mode, command is initiated by driving the $\overline{CS}$ pin low and sending the command code ABh with following three dummy bytes. The Device ID bits are then shifted on the falling edge of SCK with most significant bit (MSB) first, as shown in Figure 45. After $\overline{CS}$ is driven high it must keep high for a time duration of t_{RES2} (see Section 9.6, AC Electrical Characteristics). The Device ID can be read continuously. The command is completed by driving $\overline{CS}$ high.

If the Release from Deep Power-Down /Device ID command is issued while an Erase, Program or Write cycle is in process (when BUSY equals 1) the command is ignored and has no effect on the current cycle.

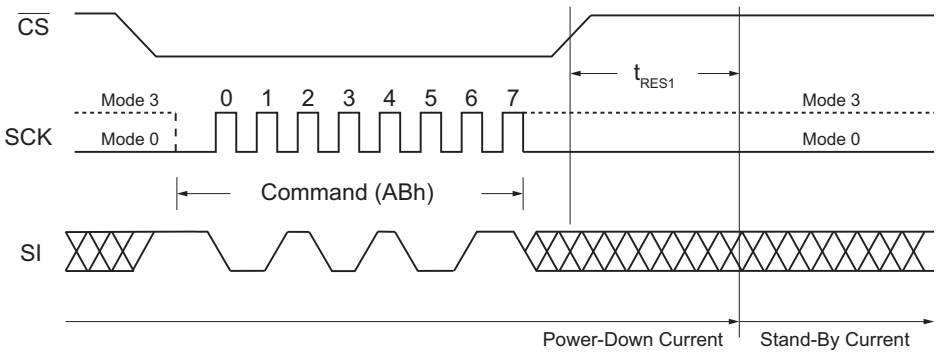

Figure 43. Release Power-Down Command (SPI Mode)

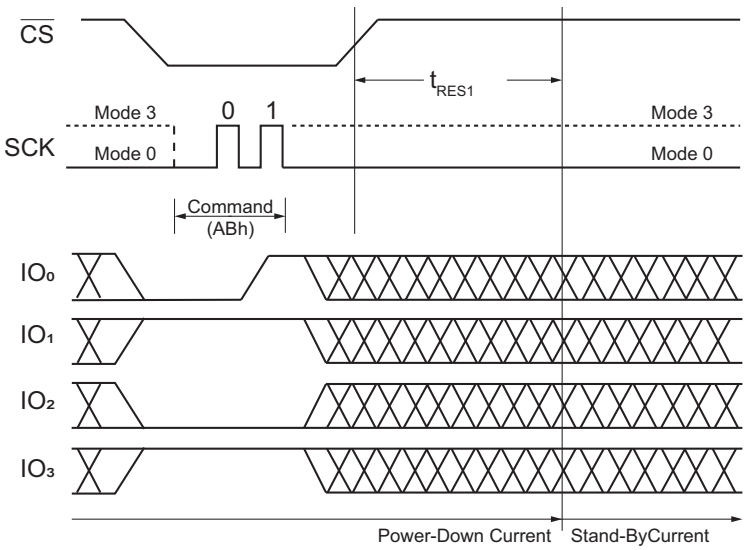

Figure 44. Release Power-Down Command (QPI Mode)

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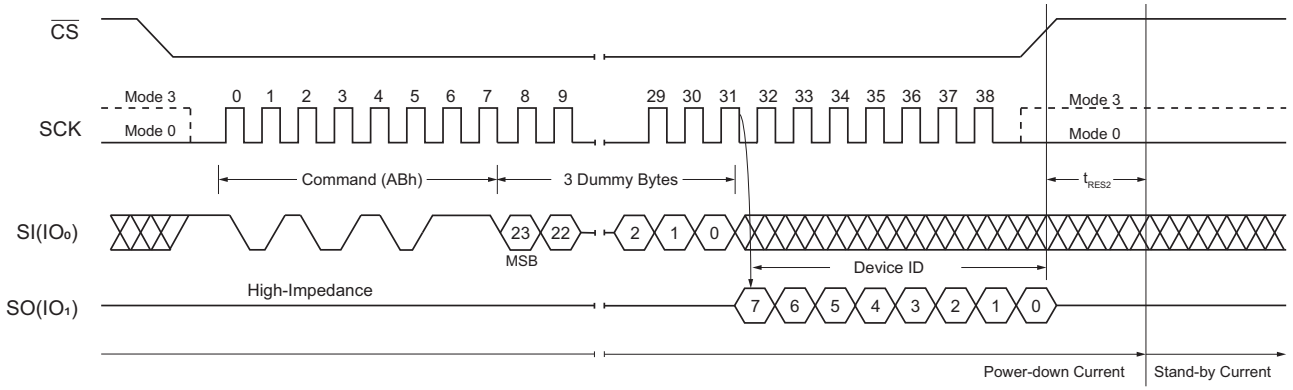

Figure 45. Release Power-Down / Device ID Command (SPI Mode)

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8.25 Read Manufacturer / Device ID Dual I/O (90h)

The Read Manufacturer/ Device ID Dual I/O command provides both the JEDEC assigned manufacturer ID and the specific device ID.

The Read Manufacturer/ Device ID command is very similar to the Fast Read Dual I/O command. The command is initiated by driving the $\overline{CS}$ pin low and shifting the command code 90h followed by a 24-bit address (A23-A0) of 000000h. After this, the Manufacturer ID for Renesas Electronics (1Fh) and the Device ID(17h) are shifted out on the falling edge of SCK with most significant bit (MSB) first, as shown in Figure 46 and Figure 47. If the 24-bit address is initially set to 000001h, the Device ID is read first and then followed by the Manufacturer ID. The Manufacturer and Device ID can be read continuously, alternating from one to the other. The command is completed by driving $\overline{CS}$ high.

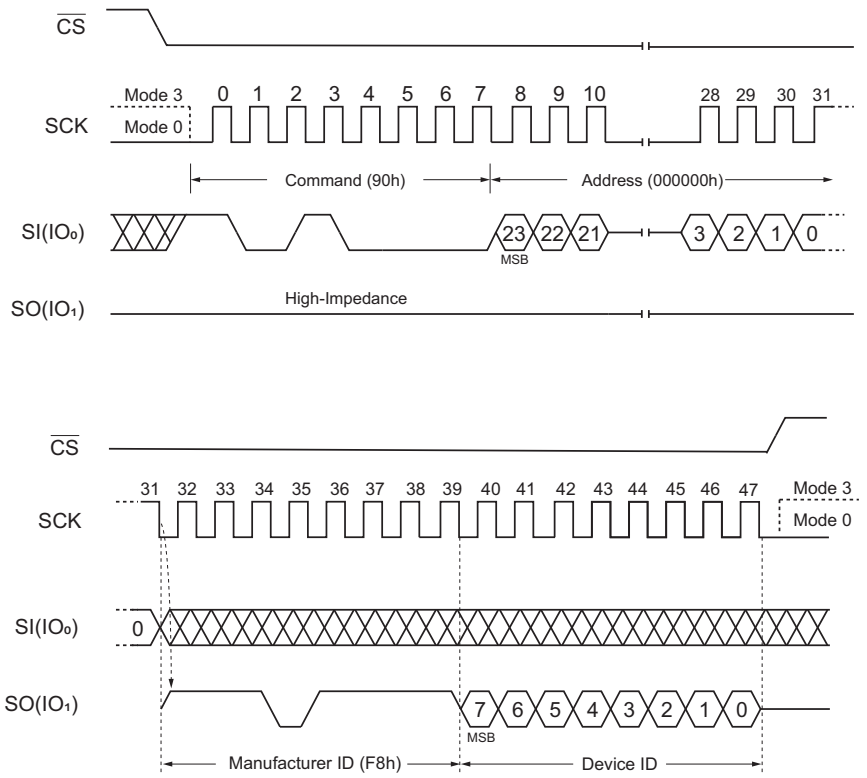

Figure 46. Read Manufacturer/ Device ID Command (SPI Mode)

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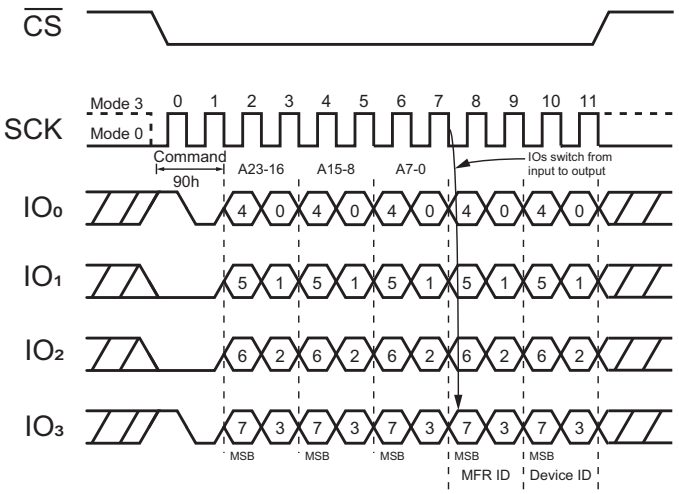

Figure 47. Read Manufacturer/ Device ID Command (QPI Mode)

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8.26 Read Manufacturer / Device ID Dual I/O (92h)

The Read Manufacturer/ Device ID Dual I/O command provides both the JEDEC assigned manufacturer ID and the specific device ID.

The Read Manufacturer/ Device ID command is very similar to the Fast Read Dual I/O command. The command is initiated by driving the $\overline{CS}$ pin low and shifting the command code 92h followed by a 24-bit address (A23-A0) of 000000h. After which, the Manufacturer ID for Renesas Electronics (1Fh) and the Device ID (17h) are shifted out on the falling edge of SCK with most significant bit (MSB) first, as shown in Figure 48. If the 24-bit address is initially set to 000001h, the Device ID is read first and then followed by the Manufacturer ID. The Manufacturer and Device ID can be read continuously, alternating from one to the other. The command is completed by driving $\overline{CS}$ high.

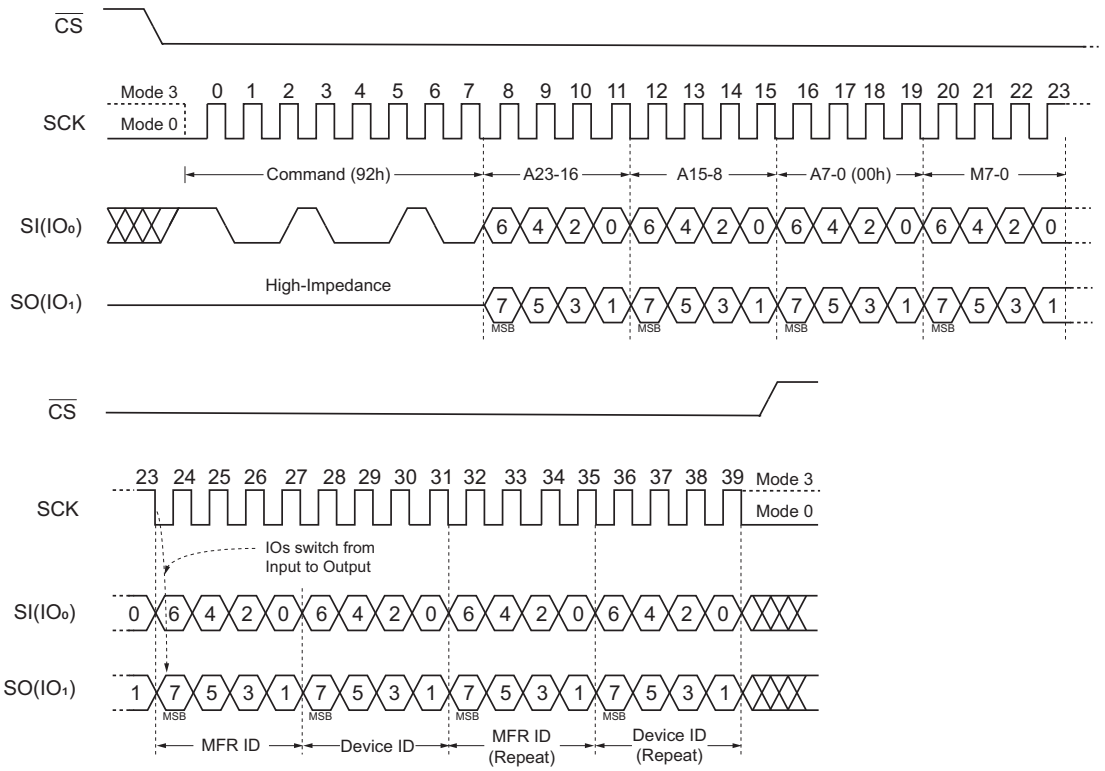

Figure 48. Read Dual Manufacturer/ Device ID Dual I/O Command (SPI Mode)

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8.27 Read Manufacturer / Device ID Quad I/O (94h)

The Read Manufacturer/ Device ID Quad I/O command provides both the JEDEC assigned manufacturer ID and the specific device ID.

The Read Manufacturer/ Device ID command is very similar to the Fast Read Quad I/O command. The command is initiated by driving the $\overline{CS}$ pin low and shifting the command code 94h followed by a 24-bit address (A23-A0) of 000000h. After which, the Manufacturer ID for Renesas Electronics (1Fh) and the Device ID (17h) are shifted out on the falling edge of SCK with most significant bit (MSB) first, as shown in Figure 49. If the 24-bit address is initially set to 000001h, the Device ID is read first and then followed by the Manufacturer ID. The Manufacturer and Device ID can be read continuously, alternating from one to the other. The command is completed by driving $\overline{CS}$ high.

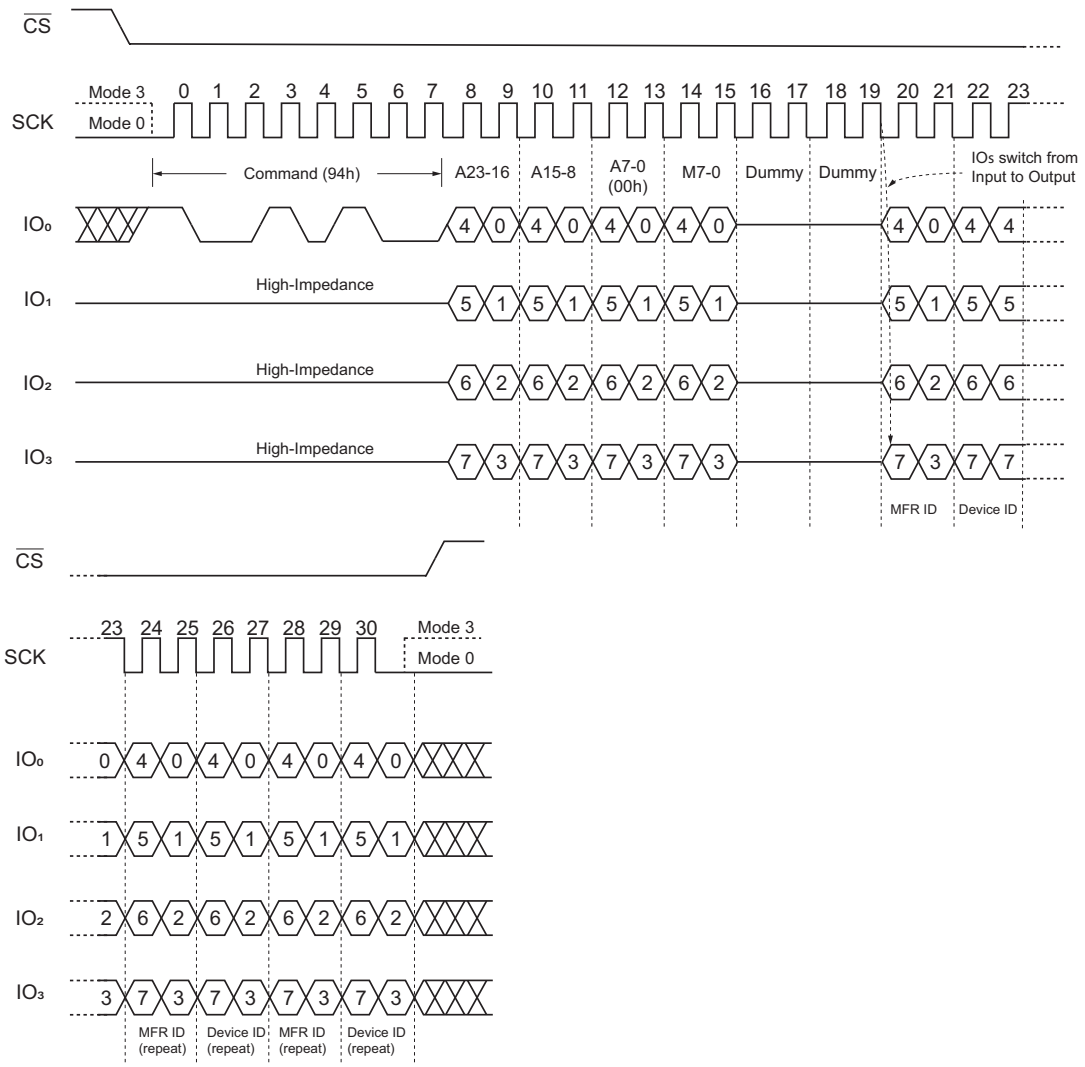

Figure 49. Read Quad Manufacturer/ Device ID Quad I/O Command (SPI Mode)

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8.28 JEDEC ID (9Fh)

For compatibility reasons, the AT25QL128A provides several commands to electronically determine the identity of the device. The Read JEDEC ID command is congruous with the JEDEC standard for SPI compatible serial flash memories that was adopted in 2003. The command is entered by driving the $\overline{CS}$ pin low with following the command code 9Fh. JEDEC assigned Manufacturer ID byte for Renesas Electronics (1Fh) and two Device ID bytes, Memory Type (ID-15-ID8) and Capacity (ID7-ID0) are then shifted out on the falling edge of SCK with most significant bit (MSB) first shown in Figure 50 and Figure 51. For memory type and capacity values refer to Manufacturer and Device Identification table. The JEDEC ID can be read continuously. The command is terminated by driving $\overline{CS}$ high.

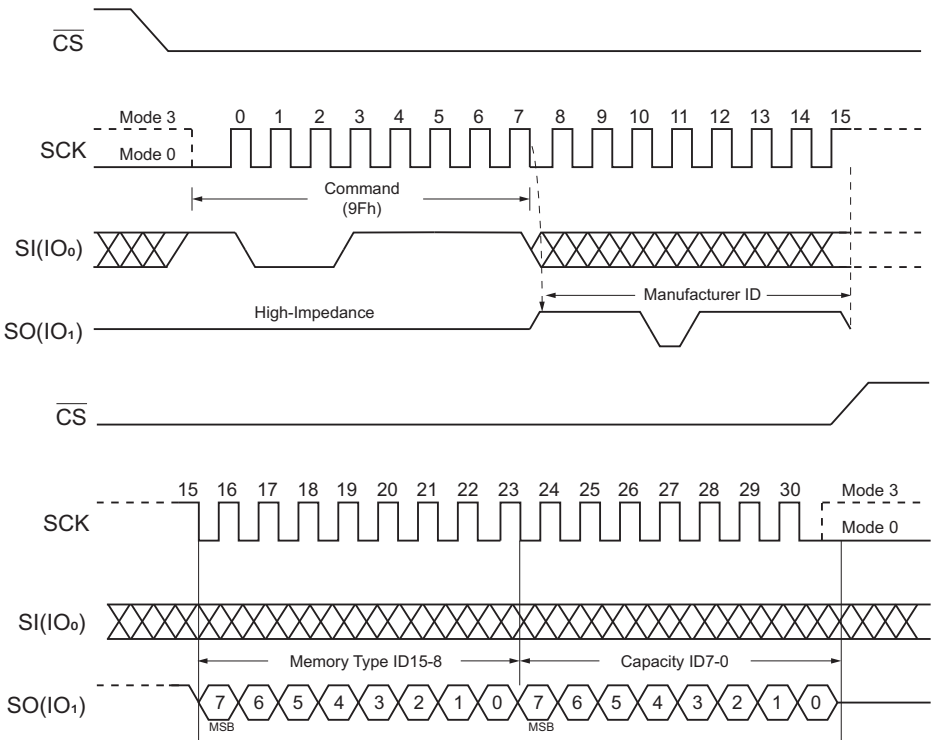

Figure 50. Read JEDEC ID Command (SPI Mode)

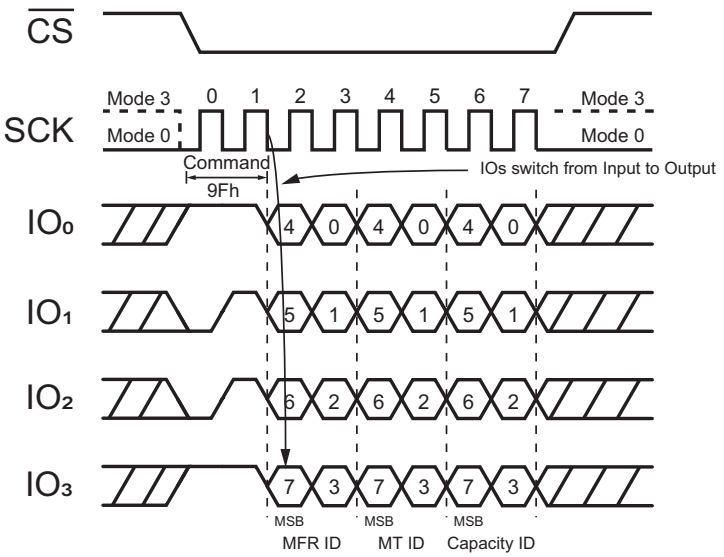

Figure 51. Read JEDEC ID Command (QPI Mode)

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8.29 Enable QPI (38h)

The AT25QL128A support both Standard/Dual/Quad Serial Peripheral interface (SPI) and Quad Peripheral Interface (QPI). However, SPI mode and QPI mode cannot be used at the same time. Enable QPI command is the only way to switch the device from SPI mode to QPI mode.

In order to switch the device to QPI mode, the Quad Enable (QE) bit in Status Register 2 must be set to 1 first, and an Enable QPI command must be issued. If the Quad Enable (QE) bit is 0, the Enable QPI command is ignored, and the device remains in SPI mode.

After power-up, the default state of the device is SPI mode. See the command Set Table 8 for all the commands supported in SPI mode and the command Set Table 10 for all the commands supported in QPI mode.

When the device is switched from SPI mode to QPI mode, the existing Write Enable and Program/Erase Suspend status, and the Wrap Length setting remains unchanged.

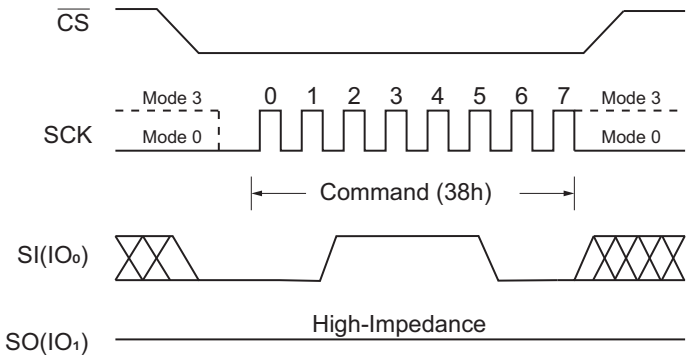

Figure 52. Enable QPI Command (SPI Mode only)

8.30 Disable QPI (FFh)

By issuing Disable QPI (FFh) command, the device is reset SPI mode. When the device is switched from QPI mode to SPI mode, the existing Write Enable Latch (WEL) and Program/Erase Suspend status, and the Wrap Length setting remains unchanged.

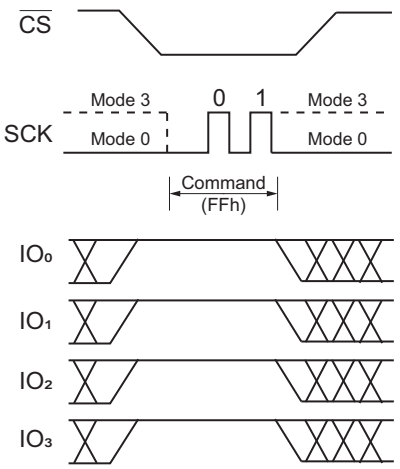

Figure 53. Disable QPI Command for QPI Mode

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8.31 Word Read Quad I/O (E7h)

The Quad I/O dramatically reduces command overhead allowing faster random access for code execution (XIP) directly from the Quad SPI. The Quad Enable bit (QE) of Status Register-2 must be set to enable the Word Read Quad I/O command. The lowest Address bit (A0) must equal 0 and only two dummy clocks are required before the data output.

Continuous Read Mode

The Word Read Quad I/O command can further reduce command overhead through setting the Continuous Read Mode bits (M7-0) after the input Address bits (A23-0), as shown in Figure 54. The upper nibble of the (M7-4) controls the length of the next Word Read Quad I/O command through the inclusion or exclusion of the first byte command code. The lower nibble bits of the (M[3:0]) are don't care (X). However, the IO pins must be high-impedance before the falling edge of the first data out clock.

If the Continuous Read Mode bits M[7-4] = Ah, then the next Fast Read Quad I/O command (after $\overline{CS}$ is raised and then lowered) does not require the E7h command code, as shown in Figure 55. This reduces the command sequence by eight clocks and allows the Read address to be immediately entered after $\overline{CS}$ is asserted low. If the Continuous Read Mode bits M[7:4] do not equal Ah (1010), the next command (after $\overline{CS}$ is raised and then lowered) requires the first byte command code, thus returning to normal operation.

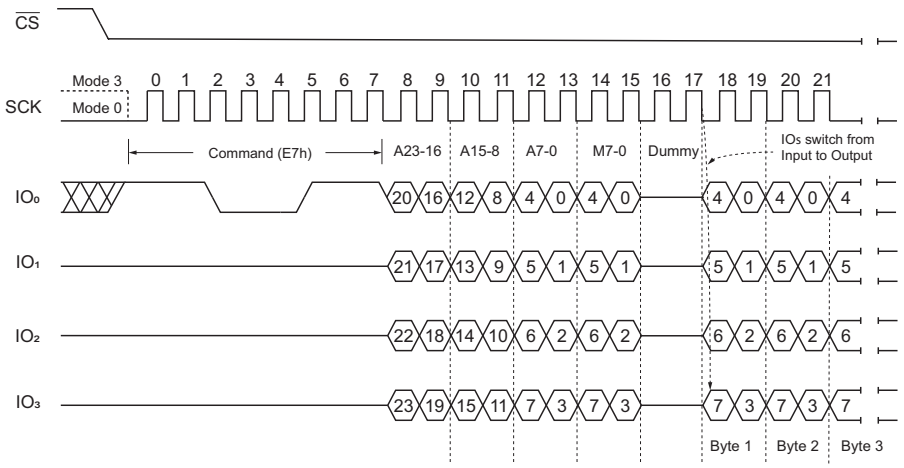

Figure 54. Word Read Quad I/O Command (Initial command or previous set M7-0 ≠ Axh, SPI Mode)

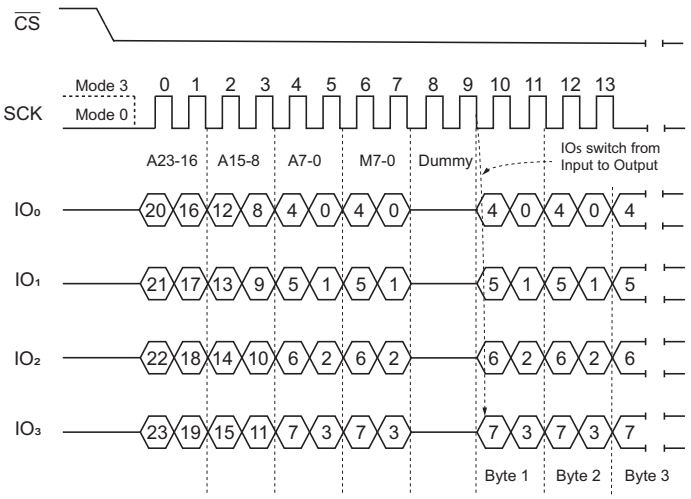

Figure 55. Word Read Quad I/O Command (Previous command set M7-0 = Axh, SPI Mode)

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Wrap Around in SPI Mode

The Word Read Quad I/O command can also be used to access a specific portion within a page by issuing a Set Burst with Wrap (77h) command before E7h. The Set Burst with Wrap (77h) command can either enable or disable the Wrap Around feature for the following E7h commands. When Wrap Around is enabled, the output data starts at the initial address specified in the command, once it reaches the ending boundary of the 8/16/32/64-byte section, the output wraps around to the beginning boundary automatically until $\overline{CS}$ is pulled high to terminate the command.

The Burst with Wrap feature allows applications that use cache to quickly fetch a critical address and then fill the cache afterwards within a fixed length (8/16/32/64 bytes) of data without issuing read commands.

The Set Burst with Wrap command allows three Wrap Bits, W6-4 to be set. The W4 bit is used to enable or disable the Wrap Around operation while W6-5 is used to specify the length of the wrap around section within a page.

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8.32 Set Burst with Wrap (77h)

The Set Burst with Wrap (77h) command is used in conjunction with Fast Read Quad I/O and Word Read Quad I/O commands to access a fixed length of 8/16/32/64-byte section within a 256-byte page. Certain applications can benefit from this feature and improve the overall system code execution performance. Before the device can accept the Set Burst with Wrap command, a Quad enable of Status Register-2 must be executed (Status Register bit QE must equal 1).

The Set Burst with Wrap command is initiated by driving the $\overline{CS}$ pin low and then shifting the command code 77h followed by 24 dummy bits and 8 Wrap Bits, W7-0. The command sequence is shown in Set Burst with Wrap Command Sequence. Wrap bit W7 and W3-0 are not used.

Table 12. Encoding of W[6:4] Bits

	W4 = 0		W4 = 1 (Default)	
	Wrap Around	Wrap Length	Wrap Around	Wrap Length
00	Yes	8-byte	No	N/A
01	Yes	16-byte	No	N/A
10	Yes	32-byte	No	N/A
11	Yes	64-byte	No	N/A

Once W6-4 is set by a Set Burst with Wrap command, the following Fast Read Quad I/O and Word Read Quad I/O commands use the W6-4 setting to access the 8/16/32/64-byte section within any page. To exit the Wrap Around function and return to normal read operation, another Set Burst with Wrap command must be issued to set W4 = 1. The default value of W4 upon power on is 1. In the case of a system Reset while W4 = 0, it is recommended that the controller issues a Set Burst with Wrap command or Reset (99h) command to reset W4 = 1 before any normal Read commands since AT25QL128A does not have a hardware Reset Pin.

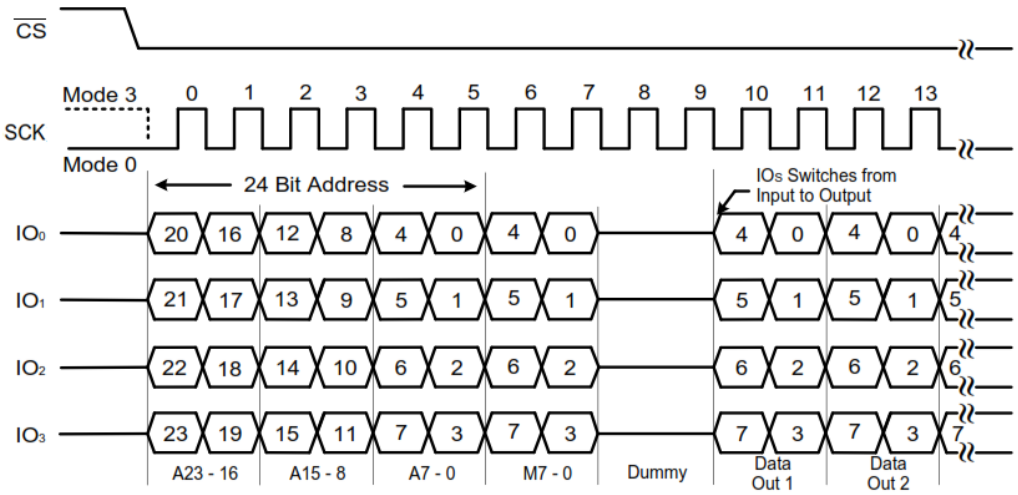

Figure 56. Set Burst with Wrap Command Sequence

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8.33 Burst Read with Wrap (0Ch)

The Burst Read with Wrap (0Ch) command provides an alternative way to perform the read operation with Wrap Around in QPI mode. The command is similar to the Fast Read (0Bh) command in QPI mode, except the addressing of the read operation wraps around to the beginning boundary of the Wrap Length once the ending boundary is reached.

The Wrap Length and the number of dummy of clocks can be configured by the Set Read Parameters (C0h) command.

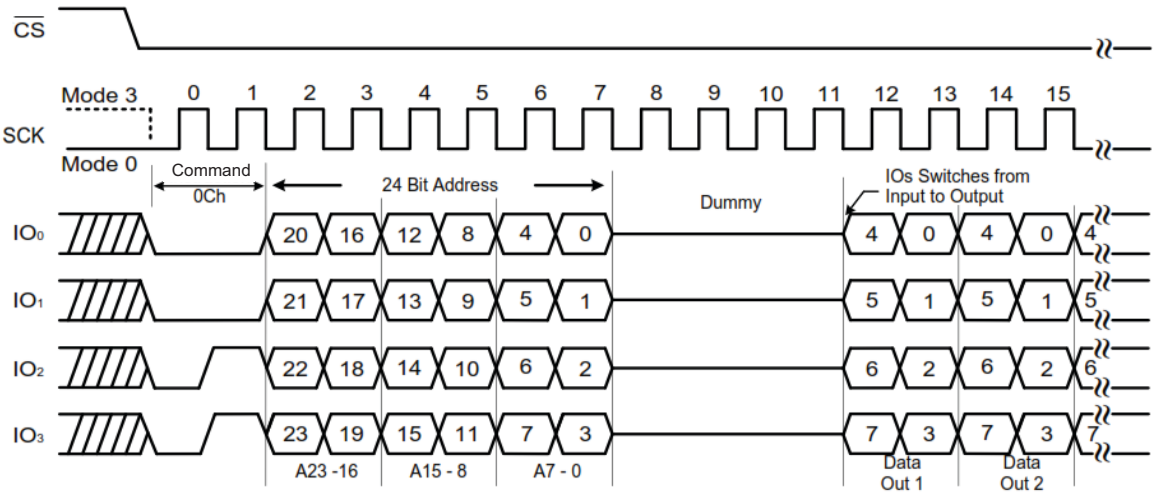

Figure 57. Burst Read with Wrap command (QPI Mode, 80MHz)

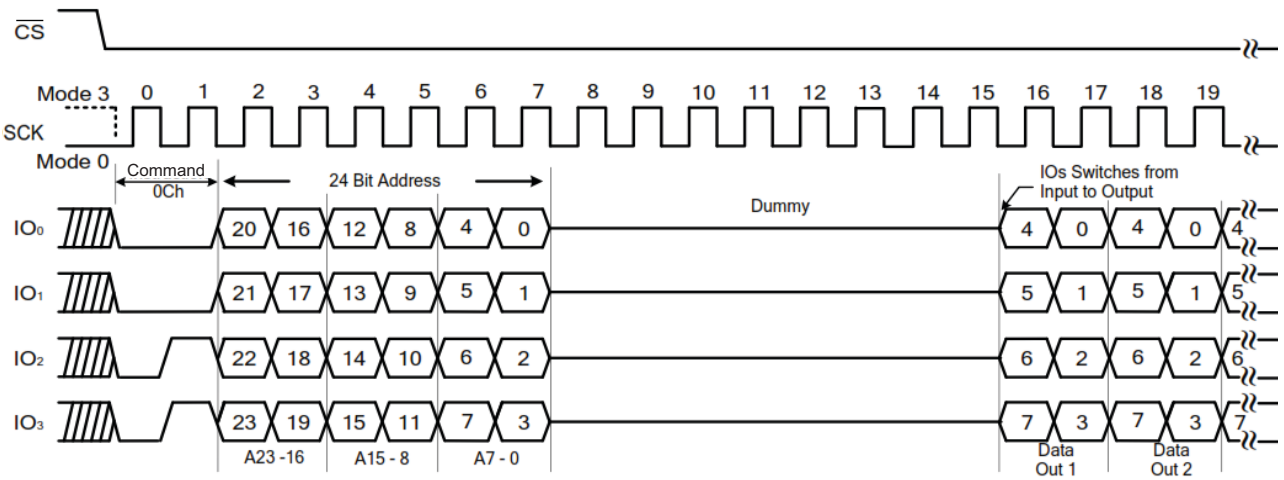

Figure 58. Burst Read with Wrap command (QPI Mode, 133 MHz)

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8.34 Set Read Parameters (C0h)

In QPI mode, to accommodate a wide range of applications with different needs for either maximum read frequency or minimum data access latency, Set Read Parameters (C0h) command can be used to configure the number of dummy clocks for Fast Read (0Bh), Fast Read Quad I/O (EBh) and Burst Read with Wrap (0Ch) commands, and to configure the number of bytes of Wrap Length for the Burst Read with Wrap (0Ch) command.

In Standard SPI mode, the Set Read Parameters (C0h) command is not accepted. The dummy clocks for various Fast Read commands in Standard/Dual/Quad SPI mode are fixed, see the specific command; for details, see Table 8, Table 9, Table 10, and Table 11. The Wrap Length is set by W6-5 bit in the Set Burst with Wrap (77h) command. This setting remains unchanged when the device is switched from Standard SPI mode to QPI mode.

The default Wrap Length after a power up or a Reset command is eight bytes, the default number of dummy clocks is four.

Table 13. Encoding of P[5:4] Bits

P5, P4	Dummy Clocks	Maximum Read Frequency
00	4	80 MHz
01	4	80 MHz
10	6	104 MHz
11	8	133 MHz

Table 14. Encoding of P[1:0] Bits

P1, P0	Wrap Length
0 0	8-byte
0 1	16-byte
1 0	32-byte
1 1	64-byte

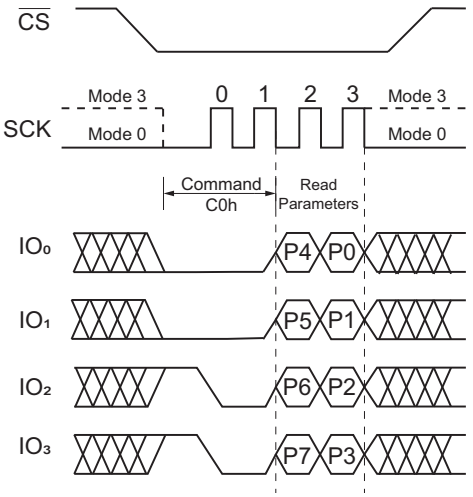

Figure 59. Set Read Parameters command (QPI Mode)

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8.35 Enable Reset (66h) and Reset (99h)

For eight-pin packages, the AT25QL128A provide a software Reset command instead of a dedicated RESET pin.

Once the Reset command is accepted, any on-going internal operations are terminated and the device returns to its default power-on state and loses all the current volatile settings, such as Volatile Status Register bits, Write Enable Latch (WEL) status, Program/Erase Suspend status, Continuous Read Mode bit setting, Read parameter setting and Wrap bit setting.

The Enable Reset (66h) and Reset (99h) commands can be issued in either SPI mode or QPI mode. To avoid accidental reset, both commands must be issued in sequence. Any other commands other than Reset (99h) after the Enable (66h) command disables the Reset Enable state. A new sequence of Enable Reset (66h) and Reset (99h) is needed to reset the device. Once the Reset command is accepted by the device, it takes approximately t_{RST} = 30 µs to reset. During this period, no command is accepted.

Data corruption can happen if there is an on-going or suspended internal Erase or Program operation when Reset command sequence is accepted by device. Check the BUSY bit and the SUS bit in the Status Register before issuing the Reset command sequence.

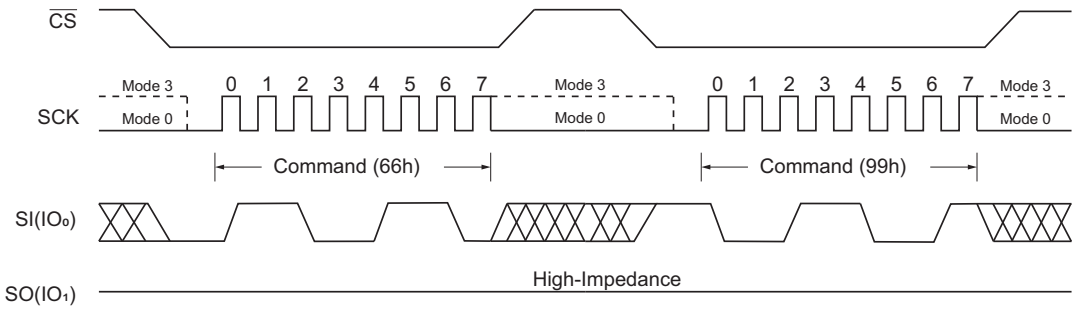

Figure 60. Enable Reset and Reset Command (SPI Mode)

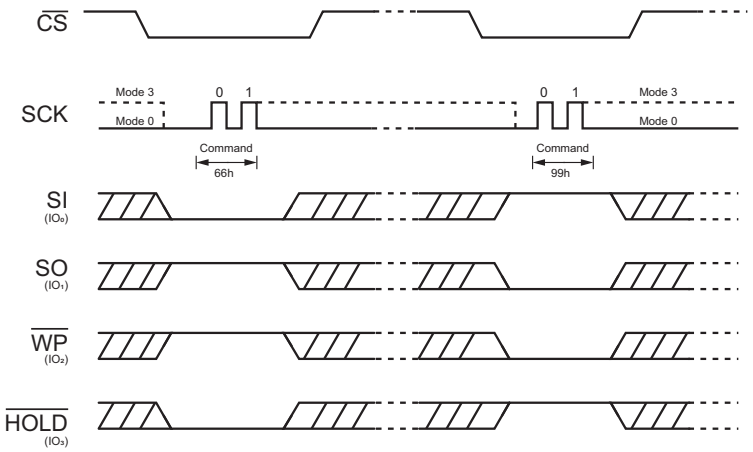

Figure 61. Enable Reset and Reset Command (QPI Mode)

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8.36 Read Serial Flash Discovery Parameter (5Ah)

The Read Serial Flash Discovery Parameter (SFDP) command allows reading the Serial Flash Discovery Parameter area (SFDP). This SFDP area is composed of 2048 read-only bytes containing operating characteristics and vendor specific information. The SFDP area is factory programmed. If the SFDP area is blank, the device is shipped with all the SFDP bytes at FFh. If only a portion of the SFDP area is written to, the portion not used is shipped with bytes in erased state (FFh). The command sequence for the read SFDP has the same structure as that of a Fast Read command. First, the device is selected by driving Chip Select ($\overline{CS}$) Low. Next, the 8-bit command code (5Ah) and the 24-bit address are shifted in, followed by 8 dummy clock cycles. The bytes of SFDP content are shifted out on the Serial Data Output (SO) starting from the specified address. Each bit is shifted out during the falling edge of Serial Clock (SCK). The command sequence is shown here. The Read SFDP command is terminated by driving Chip Select ($\overline{CS}$) High at any time during data output.

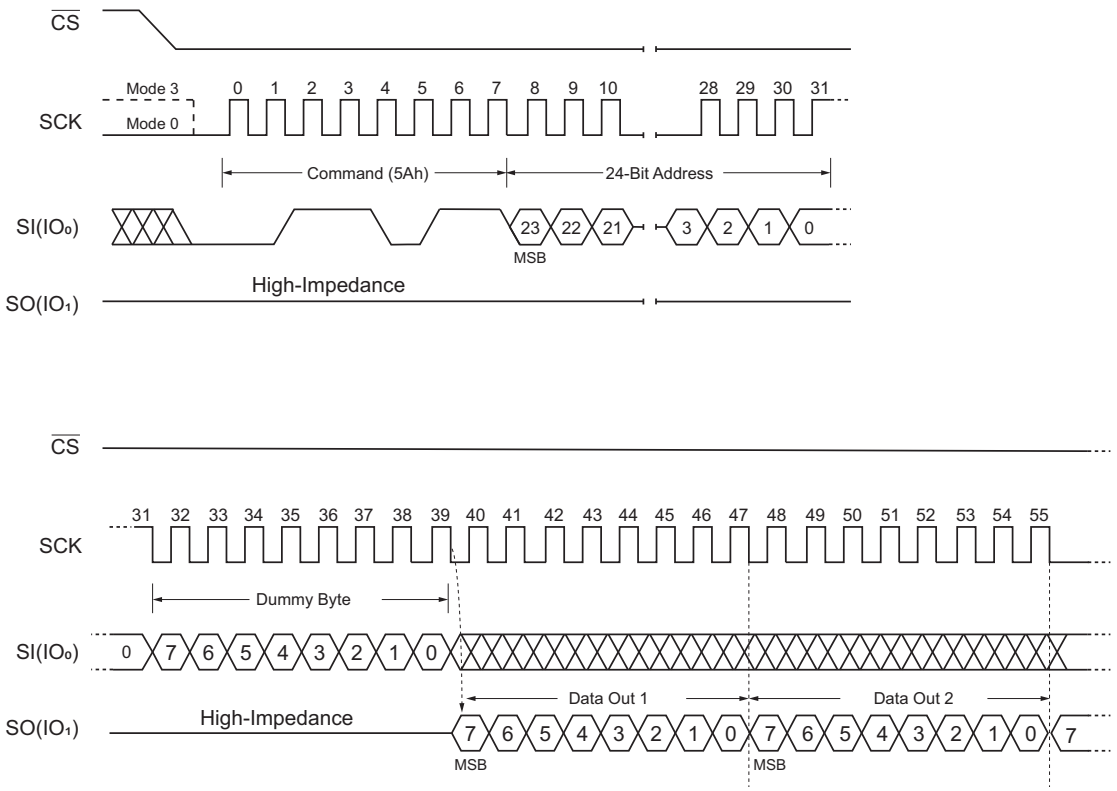

Figure 62. Read SFDP Register Command

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Table 15. SFDP Signature and Headers

Description	Comment	Address Byte	Bits	Data (binary)	Data (hex)
SFDP Signature		00h	07:00	0101 0011	53h
		01h	15:08	0100 0110	46h
		02h	23:16	0100 0100	44h
		03h	31:24	0101 0110	50h
SFDP Minor Revision	Start from 00h	04h	07:00	0000 0110	06h
SFDP Major Revision	Start from 01h	05h	15:08	0000 0001	01h
Number of Parameters Headers	Start from 00h	06h	23:16	0000 0001	01h
Reserved	FFh	07h	31:24	1111 1111	FFh
JEDEC Parameter ID (LSB)	JEDEC Parameter ID (LSB) = 00h	08h	07:00	0000 0000	00h
Parameter Table Minor Revision	Start from 00h	09h	15:08	0000 0110	06h
Parameter Table Major Revision	Start from 01h	0Ah	23:16	0000 0001	01h
Parameter Table Length (double words)	How many DWORDs in the parameter table	0Bh	31:24	0001 0000	10h
Parameter Table Pointer	Address of Renesas Electronics Parameter Table	0Ch	07:00	0011 0000	30h
		0Dh	15:08	0000 0000	00h
		0Eh	23:16	0000 0000	00h
JEDEC Parameter ID (MSB)	JEDEC Parameter ID (MSB):FFh	0Fh	31:24	1111 1111	FFh
JEDEC Parameter ID (LSB)	Renesas Electronics Manufacturer ID	10h	07:00	0001 1111	1Fh
Parameter Table Minor Revision	Start from 00h	11h	15:08	0000 0000	00h
Parameter Table Major Revision	Start from 01h	12h	23:16	0000 0001	01h
Parameter Table Length (double words)	How many DWORDs in the parameter table	13h	31:24	0000 0010	02h
Parameter Table Pointer (PTP)	Address of Renesas Electronics Parameter Table	14h	07:00	1000 0000	80h
		15h	15:08	0000 0000	00h
		16h	23:16	0000 0000	00h
Reserved	FFh	17h	31:24	0000 0001	01h

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Table 16. SFDP Parameters Table 1

Description	Comment	Address Byte	Bits	Data (binary)	Data (hex)
Erase Granularity	01: 4 kbytes available 11: 4 kbytes not available	30h	01:00	01	E5h
Write Granularity	0: 1 Byte 1: 64 bytes or larger		02	1	
Volatile Status Register Block Protect Bits	0: Nonvolatile status bit 1: Volatile status bit		03	0	
Volatile Status Register Write Enable Opcode	0: 50h Opcode to enable, if bit 3 = 1		04	0	
Reserved			07:05	111	
4 kbytes Erase Opccde	Opcode or FFh	31h	15:08	0010 0000	20h
Fast Dual Read Output (1 -1 -2)	0: Not supported, 1: Supported	32h	16	1	F1h
Number of Address Bytes	00: 3 Byte only 01: 3 or 4 Byte 10: 4 Byte only 11: Reserved		18:17	00	
Double Transfer Rate (DTR) Clocking	0: Not supported, 1: Supported		19	0	
Fast Dual I/O Read (1-2- 2)	0: Not supported, 1: Supported		20	1	
Fast Quad I/O Read (1-4-4)	0: Not supported, 1: Supported		21	1	
Fast Quad Output Read (1-1-4)	0: Not supported, 1: Supported		22	1	
Reserved	FFh		23	1	
Reserved	FFh	33h	31:24	1111 1111	FFh
Flash Memory Density		34h	07:00	1111 1111	FFh
		35h	15:08	1111 1111	FFh
		36h	23:16	1111 1111	FFh
		37h	31:24	0000 0111	07h
Fast Quad I/O (1-4-4) Number of dummy clocks	Number of dummy clocks	38h	04:00	00100	44h
Fast Quad I/O (1-4-4) Number of mode bits	Number of mode bits		07:05	010	
Fast Quad I/O (1-4-4) Read Opcode	Opcode or FFh	39h	15:08	1110 1011	EBh
Fast Quad Output (1-1-4) Number of dummy clocks	Number of dummy clocks	3Ah	20:16	01000	08h
Fast Quad Output (1-1-4) Number of mode bits	Number of mode bits		23:21	000	
Fast Quad Output (1-1-4) Read Opcode	Opcode or FFh	3Bh	31:24	0110 1011	6Bh
Fast Dual Output (1-1-2) Number of dummy clocks	Number of dummy clocks	3Ch	04:00	01000	08h
Fast Dual Output (1-1-2) Number of mode bits	Number of mode bits		07:05	000	
Fast Dual Output (1-1-2) Read Opcode	Opcode or FFh	3Dh	15:08	0011 1011	3Bh

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Table 16. SFDP Parameters Table 1 (Continued)

Description	Comment	Address Byte	Bits	Data (binary)	Data (hex)
Fast Dual I/O (1-2-2) Number of dummy clocks	Number of dummy clocks	3Eh	20:16	00000	80h
Fast Dual I/O (1-2-2) Number of mode bits	Number of mode bits		23:21	100	
Fast Dual I/O (1-2-2) Read Opcode	Opcode or FFh	3Fh	31:24	1011 1011	BBh
Fast Dual DPI (2-2-2)	0: Not supported, 1: Supported	40h	0	0	FEh
Reserved	FFh		03:01	111	
Fast Quad QPI (4-4-4)	0: Not supported, 1: Supported		04	1	
Reserved	FFh		07:05	111	
Reserved	FFh	41h	15:08	1111 1111	FFh
Reserved	FFh	42h	23:16	1111 1111	FFh
Reserved	FFh	43h	31:24	1111 1111	FFh
Reserved	FFh	44h	07:00	1111 1111	FFh
Reserved	FFh	45h	15:08	1111 1111	FFh
Fast Dual DPI (2-2-2) Number of dummy clocks	Number of dummy clocks	46h	20:16	0 0000	00h
Fast Dual DPI (2-2-2) Number of mode bits	Number of mode bits		23:21	000	
Fast Dual DPI(2-2-2) Read Opcode	Opcode or FFh	47h	31:24	1111 1111	FFh
Reserved	FFh	48h	07:00	1111 1111	FFh
Reserved	FFh	49h	15:08	1111 1111	FFh
Fast Quad QPI (4-4-4) Number of dummy clocks	Number of dummy clocks	4Ah	20:16	00010	42h
Fast Quadl QPI (4-4-4) Number of mode bits	Number of mode bits		23:21	010	
Fast Quad QPI(4-4-4) Read Opcode	Opcode or FFh	4Bh	31:24	1110 1011	EBh
Erase type-1 Size	4 kbytes = 2^0Ch 32 kbytes = 2^0Fh 64 kbytes = 2^10h; (2^Nbyte)	4Ch	07:00	0000 1100	0Ch
Erase type-1 Opcode	Opcode or FFh	4Dh	15:08	0010 0000	20h
Erase type-2 Size	4 kbytes = 2^0Ch 32 kbytes = 2^0Fh 64 kbytes = 2^10h; (2^Nbyte)	4Eh	23:16	0000 1111	0Fh
Erase type-2 Opcode	Opcode or FFh	4Fh	31:24	0101 0010	52h
Erase Type-3 Size	4 kbytes = 2^0Ch 32 kbytes = 2^0Fh 64 kbytes = 2^10h; (2^Nbyte)	50h	07:00	0001 0000	10h
Erase Type-3 Opcode	Opcode or FFh	51h	15:08	1101 1000	D8h
Erase Type-4 Size	4 kbytes = 2^0Ch 32 kbytes = 2^0Fh 64 kbytes = 2^10h; (2^Nbyte)	52h	23:16	0000 0000	00h
Erase Type-4 Opcode	Opcode or FFh	53h	31:24	1111 1111	FFh

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Table 16. SFDP Parameters Table 1 (Continued)

Description	Comment	Address Byte	Bits	Data (binary)	Data (hex)
Erase Maximum/Typical Ratio	Maximum = 2 * (COUNT + 1) * Typical	54h 55h 56h 57h	03:00	0011	33h 62h D5h 00h
Erase type-1 Typical time	Count or 00h		08:04	0 0011	
Erase type-1 Typical units	00b: 1ms 01b: 16ms 10b: 128ms 11b: 1s		10:09	01	
Erase type-2 Typical time	Count or 00h		15:11	0110 0	
Erase type-2 Typical units	00b: 1ms 01b: 16ms 10b: 128ms 11b: 1s		17:16	01	
Erase type-3 Typical time	Count or 00h		22:18	101 01	
Erase type-3 Typical units	00b: 1ms 01b: 16ms 10b: 128ms 11b: 1s		24:23	01	
Erase type-4 Typical time	Count or 00h		29:25	00 000	
Erase type-4 Typical units	00b: 1ms 01b: 16ms 10b: 128ms 11b: 1s		31:30	00	
Program Maximum/Typical Ratio	Maximum = 2 * (COUNT + 1) * Typical	58h	03:00	0100	84h
Page Size	2^N bytes		07:04	1000	
Program Page Typical time	Count or 00h	59h 5Ah 5Bh	12:08	0 1001	29h 01h CEh
Program Page Typical units	0: 8µs, 1: 64µs		13	1	
Program Byte Typical time, 1st byte	Count or 00h		17:14	01 00	
Program Byte Typical units, 1st byte	0: 1µs, 1: 8µs		18	0	
Program Additional Byte Typical time	Count or 00h		22:19	000 0	
Program Additional Byte Typical units	0: 1µs, 1: 8µs		23	0	
Erase Chip Typical time	Count or 00h		28:24	0 1110	
Erase Chip Typical units	00b: 16ms 01b: 256ms 10b: 4s 11b: 64s		30:29	10	
Reserved	1h		31	1	
Prohibited Op during Program Suspend	See datasheet	5Ch	03:00	11010	ECh
Prohibited Op during Erase Suspend	See datasheet		07:04	1110	

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Table 16. SFDP Parameters Table 1 (Continued)

Description	Comment	Address Byte	Bits	Data (binary)	Data (hex)
Reserved	1h	5Dh 5Eh 5Fh	08	1	A1h 07h 3Dh
Program Resume to Suspend time	Count of 64µs		12:09	0 000	
Program Suspend Maximum time	Count or 00h		17:13	11 101	
Program Suspend Maximum units	00b: 128ns, 01b: 1µs, 10b: 8µs, 11b: 64µs		19:18	01	
Erase Resume to Suspend time	Count of 64µs		23:20	0000	
Erase Suspend Maximum time	Count or 00h		28:24	1 1101	
Erase Suspend Maximum units	00b: 128ns, 01b: 1µs, 10b: 8µs, 11b: 64µs		30:29	01	
Suspend / Resume supported	0: Program and Erase suspend supported 1: not supported		31	0	
Program Resume Opcode	Opcode or FFh	60h	7:0	0111 1010	7Ah
Program Suspend Opcode	Opcode or FFh	61h	15:8	0111 0101	75h
Resume Opcode	Opcode or FFh	62h	23:16	0111 1010	7Ah
Suspend Opcode	Opcode or FFh	63h	31:24	0111 0101	75h
Reserved	11b	64h	01:00	11	F7h
Status Register Busy Polling	xxxxx1b: Opcode = 05h, bit 0 = 1 Busy, xxxx1xb: Opcode = 70h, bit 7 = 0 Busy, Others: reserved		07:02	1111 01	
Exit Deep Power-down time	Count or 00h	65h 66h 67h	12:08	0 0010	A2h D5h 5Ch
Exit Deep Power-down units	00b: 128ns, 01b: 1µs, 10b: 8µs, 11b: 64µs		14:13	01	
Exit Deep Power-down Opcode	Opcode or FFh		22:15	101 0101 1	
Enter Deep Power-down Opcode	Opcode or FFh		30:23	101 1100 1	
Deep Power-down Supported	0: Deep Power-down supported, 1: not supported		31	0	

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Table 16. SFDP Parameters Table 1 (Continued)

Description	Comment	Address Byte	Bits	Data (binary)	Data (hex)
Disable 4-4-4 Read Mode		68h 69h 6Ah	03:00	1001	19h F6h 1Ch
Enable 4-4-4 Read Mode			08:04	0 0001	
Fast Quad I/O Continuous (0-4-4) supported	0: not supported, 1: Quad I/O 0-4-4 supported		09	1	
Fast Quad I/O Continuous (0-4-4) Exit			15:10	1111 01	
Fast Quad I/O Continuous (0-4-4) Enter			19:16	1100	
Quad Enable Requirements (QER)			22:20	001	
HOLD or RESET Disable	0: not supported, 1: use Configuration register bit 4		23	0	
Reserved	FFh	6Bh	31;24	1111 1111	FFh
Status Register Opcode		6Ch	06:00	110 1000	E8h
Reserved	1h		07	1	
Soft Reset Opcodes		6Dh	13:08	01 0000	10h C0h
4-Byte Address Exit		6Eh	23:14	1100 0000 00	
4-Byte Address Enter		6Fh	31:24	1000 0000	80h

Table 17. SFDP Parameters Table 2

Description	Comment	Address (h) Byte	Bits	Data (b) (Bit)	Data (h) (Byte)
VCC Minimum Voltage	1650h: 1.65 V, 1700h: 1.70 V, 2300h: 2.30 V, 2500h: 2.50 V, 2700h: 2.70 V	80h 81h	15:0	0000 0000 0001 0111	00h 17h
VCC Maximum Voltage	1950h: 1.95 V, 3600h: 3.60 V, 4000h: 4.00 V, 4400h: 4.40 V	82h/83h	31:16	0000 0000 0010 0000	00h 20h
Array Protection Method	10b: use non-volatile status register	84h 85h	01:00	00	00h 00h
Power up Protection default	0: power up unprotected 1: power up protected		02	0	
Protection Disable Opcodes	011b: use status register		05:03	000	
Protection Enable Opcodes	011b: use status register		08:06	0 00	
Protection Read Opcodes	011b: use status register		11:09	000	
Protection Register Erase Opcode	00b: not supported, 01b: Opcodes 3Dh, 2Ah, 7Fh, CFh,		13:12	00	
Protection Register Program Opcode	00b: not supported 01b: Opcodes 3Dh, 2Ah, 7Fh, FCh		15:14	00	
Reserved	FFh	86h	23:16	1111 1111	FFh
Reserved	FFh	87h	31:24	1111 1111	FFh
Reserved	FFh	88h - FFh			Reserved

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8.37 Enter Secured OTP (B1h)

The Enter Secured OTP command is for entering the additional 4-kbit secured OTP mode. The additional 4-kbit secured OTP is independent from main array, which can be used to store unique serial number for system identifier. After entering the secured OTP mode, and then follow standard read or program, procedure to read out the data or update data. The secured OTP data cannot be updated again once it is locked down.

Please note that Write Status Register-1, Write Status Register-2 and Write Security Register commands are not acceptable during the access of secure OTP region. Once security OTP is locked down, only commands related with read are valid. The Enter Secured OTP command sequence is shown in Figure 63.

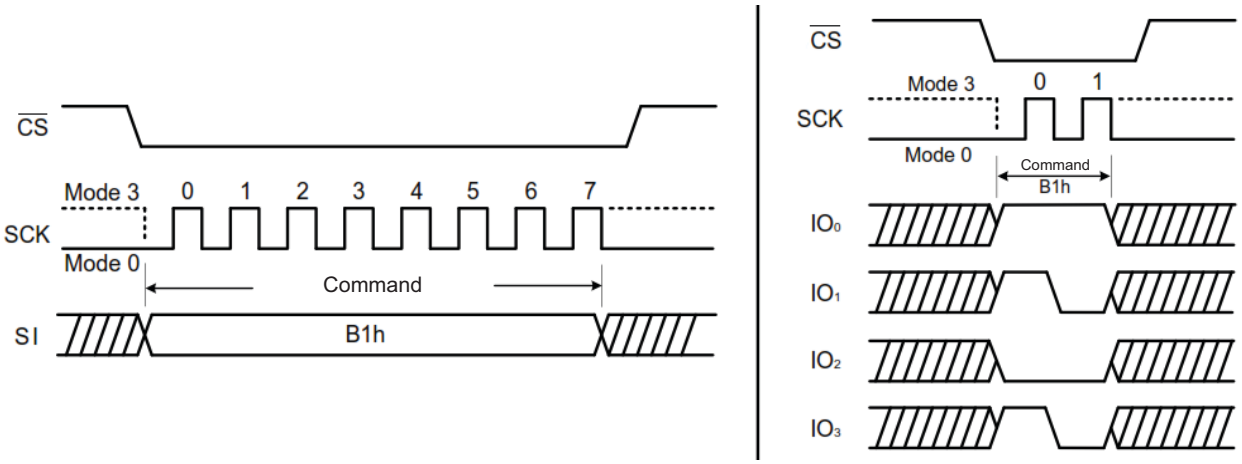

Figure 63. Enter Secured OTP Command for SPI Mode (left) and QPI Mode (right)

8.38 Exit Secured OTP (C1h)

The Exit Secured OTP command is for exiting the additional 4 kbit secured OTP mode. (See Figure 64.)

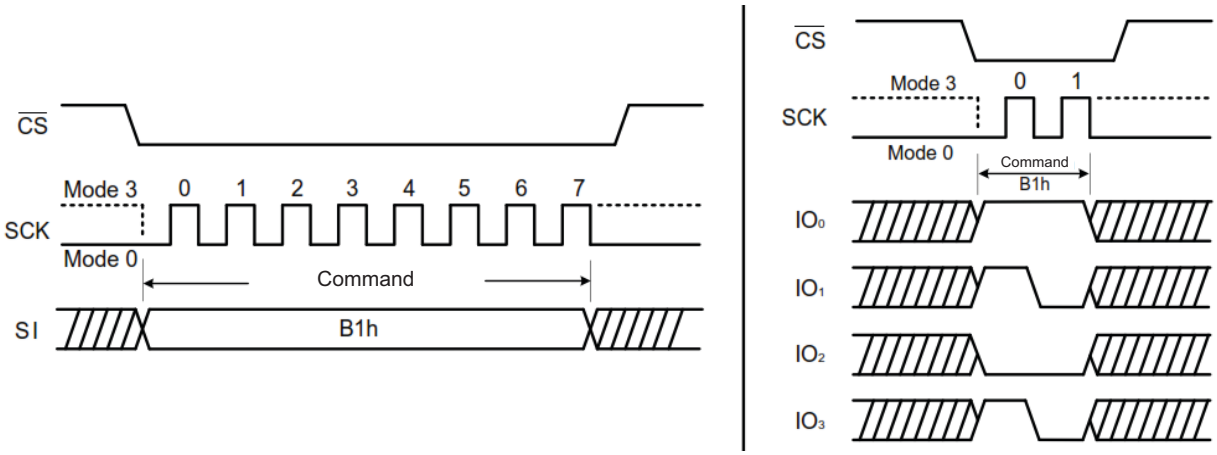

Figure 64. Exit Secured OTP Command for SPI Mode (left) and QPI Mode (right)

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8.39 Read Security Register (2Bh)

The Read Security Register can be read the value of Security Register bits at any time (even in program/erase/write status register-1 and write status register-2 condition) and continuously.

Secured OTP Indicator bit. The Secured OTP indicator bit shows the chip is locked by factory before ex-factory or not. When it is 0, it indicates non-factory lock, 1 indicates factory-lock.

Lock-Down Secured OTP (LDSO) bit. By writing Write Security Register command, the LDSO bit can be set to 1 for customer lock-down purpose. However, once the bit it set to 1 (Lock-down), the LDSO bit and the 4-kbit secured OTP area cannot be updated any more. While it is in 4-kbit secured OTP mode, array access is not allowed to write.

Table 18. Security Register Bit Assignments

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
x	x	x	x	x	x	LDSO (indicate if lock-down)	Secured OTP indicator bit
Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	0: no lock down 1: lock- down (cannot program/ erase OTP)	0: non factory lock 1: factory lock
Volatile bit	Volatile bit	Volatile bit	Volatile bit	Volatile bit	Volatile bit	Non Volatile bit	Non-Volatile bit

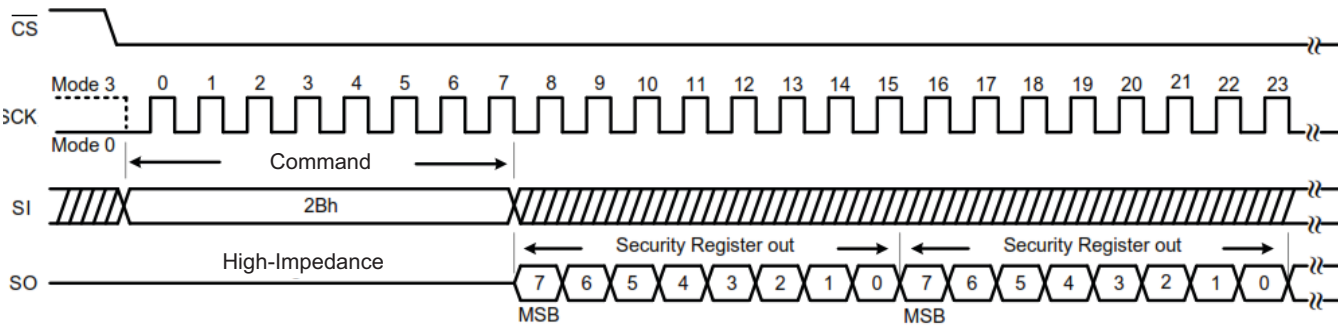

Figure 65. Read Security Register Command (SPI Mode)

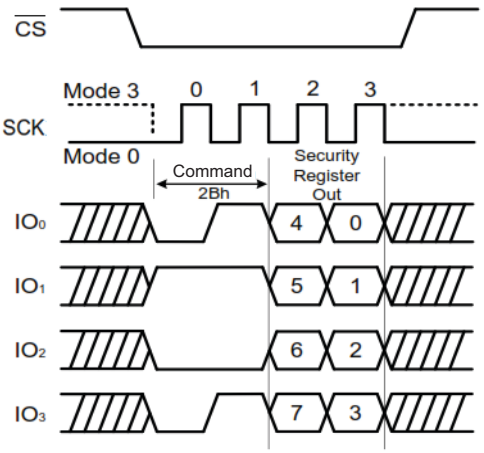

Figure 66. Read Security Register Command (QPI Mode)

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8.40 Write Security Register (2Fh)

The Write Security Register command is for changing the values of Security Register bits. Unlike Write Status Register, the Write Enable command is not required before writing Write Security Register command. The Write Security Register command can change the value of bit1 (LDSO bit) for customer to lock-down the 4-kbit secured OTP area. Once the LDSO bit is set to 1, the secured OTP area cannot be updated any more.

The $\overline{CS}$ must go high exactly at the boundary; otherwise, the command is rejected and not executed.

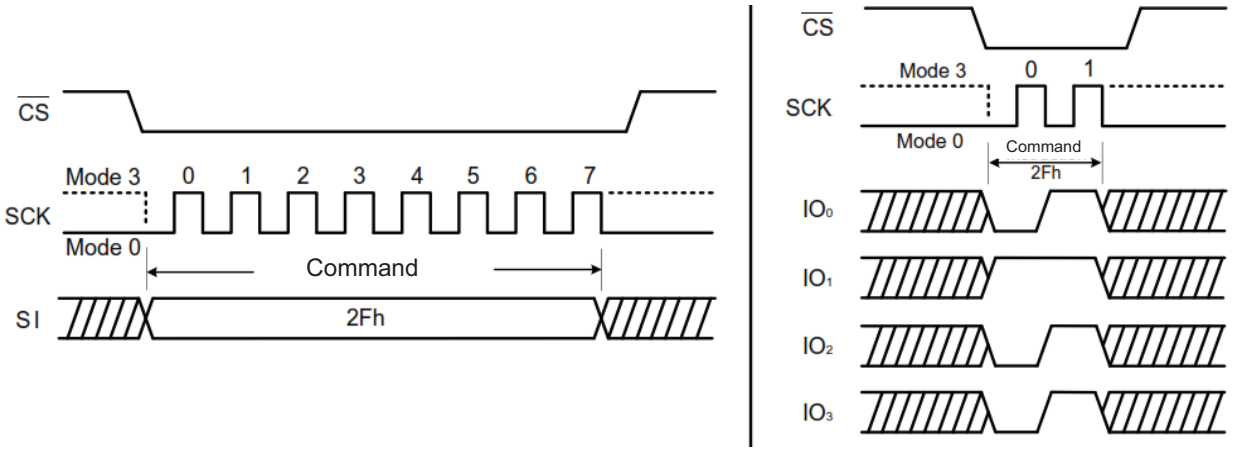

Figure 67. Write Security Register Command for SPI Mode (left) and QPI Mode (right)

8.41 4-kbit Secured OTP

This unique identifier provides a 4-kbit one-time-program area for setting device unique serial number that can be set by factory or system customer. See Table 19.

- Security register bit 0 indicates whether the chip is locked by factory or not.
- To program the 4 kbit secured OTP by entering 4 kbit secured OTP mode (with ENSO command) and going through normal program procedure, and then exiting 4 kbit secured OTP mode by writing EXSO command
- Customer can lock-down bit1 as 1. See Table 18 for security register bit definition and Table 19 for the address range definition.

Note. Once lock-down whatever by factory or customer, it cannot be changed any more. While in 4 kbit secured OTP mode, array access is not allowed to write.

Table 19. Addressing of Secured OTP Area

Address Range	Size	Standard	Customer Lock
000000 ~ 00000F	128 bits	ESN (Electrical Serial Number)	Determined by customer
000010 ~ 0001FF	3,968 bits	N/A	

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9. Electrical Characteristics

Table 20. Electrical Characteristics

Parameter	Symbol	Conditions	Range	Unit
Supply Voltage	VCC		-0.6 to VCC+0.4	V
Voltage Applied to Any Pin	VIO	Relative to Ground	-0.6 to VCC +0.4	V
Transient Voltage on any Pin	VIOT	<20 ns Transient Relative to Ground	-1.0 V to VCC +1.0 V	V
Storage Temperature	TSTG		-65 to +150	°C
Lead Temperature	TLEAD		See Note(2)	°C
Electrostatic Discharge Voltage	VESD	Human Body Model(3)	-2000 to +2000	V

Notes:

1. Stresses beyond those listed under Absolute Maximum Ratings can cause permanent damage to the device. The Absolute Maximum Ratings are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods can affect device reliability. Voltage extremes referenced in the Absolute Maximum Ratings are intended to accommodate short duration undershoot/overshoot conditions and does not imply or guarantee functional device operation at these levels for any extended period of time.
2. Compliant with JEDEC Standard J-STD-20C for small body Sn-Pb or Pb-free (Green) assembly and the European directive on restrictions on hazardous substances (RoHS) 2002/95/EU.
3. JEDEC Std JESD22-A114A (C1 = 100 pF, R1 = 1500 ohms, R2 = 500 Ohms).

9.1 Operating Ranges

Table 21. Operating Ranges

Parameter	Symbol	Conditions	Min	Max	Unit
Supply Voltage	VCC	f_R = 133 MHz (Single/Dual/Quad SPI) f_R = 50 MHz (Read Data 03h)	1.7	2.0	V
Ambient Operating Temperature	T_A	Industrial	-40	+85	°C

9.2 Endurance and Data Retention

Table 22. Endurance and Data Retention

Parameter	Condition	Min	Max	Unit
Erase/Program Cycles	4 kbytes block, 32/64 kbytes block or full chip	100,000		Cycles
Data Retention	Full temperature range		20	Years

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9.3 Power-up Timing and Write Inhibit Threshold

Table 23. Power-up and Write Inhibit Threshold

Parameter	Symbol	Min	Max	Unit
VCC (min) to $\overline{CS}$ Low	t_{VSL} [1]	15		µs
Time Delay Before Write Command	t_{PUW} [1]	1	10	ms
Write Inhibit Threshold Voltage	$V_{WI(}$ [1]	1.0	1.4	V

1. These parameters are characterized at -10C & +85C only

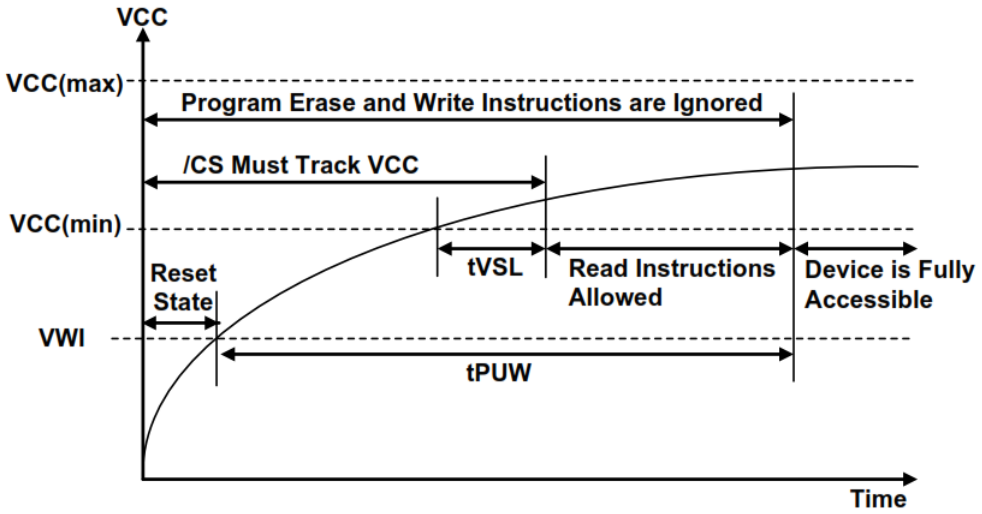

Figure 68. Power-Up Timing and Voltage Levels

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9.4 DC Electrical Characteristics

Table 24. DC Electrical Characteristics

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Input Capacitance	CIN [1]	VIN = 0 V[(2)]			6	pF
Output Capacitance	COUT [1]	VOUT = 0 V[(2)]			8	pF
Input Leakage	ILI				±2	µA
I/O Leakage	ILO				±2	µA
Standby Current	ICC1	$\overline{CS}$ = VCC, VIN = GND or VCC		10	70	µA
Power-Down Current	ICC2	$\overline{CS}$ = VCC, VIN = GND or VCC		2	20	µA
Current Read Data/ Dual/Quad 1 MHz [2]	ICC3	C = 0.1 VCC / 0.9 VCC IO = Open			7	mA
Current Read Data/ Dual/Quad 50 MHz [2]	ICC3	C = 0.1 VCC / 0.9 VCC IO = Open			15	mA
Current Read Data/ Dual/Quad 80 MHz [2]	ICC3	C = 0.1 VCC / 0.9 VCC IO = Open			18	mA
Current Read Data/ Dual/Quad 104 MHz [2]	ICC3	C = 0.1 VCC / 0.9 VCC IO = Open			20	mA
Current Read Data/ Dual/Quad 133 MHz [2]	ICC3	C = 0.1 VCC / 0.9 VCC IO = Open			27	mA
Current Write Status Register	ICC4	$\overline{CS}$ = VCC		10	20	mA
Current Page Program	ICC5	$\overline{CS}$ = VCC		15	25	mA
Current Block Erase	ICC6	$\overline{CS}$ = VCC		15	25	mA
Current Chip Erase	ICC7	$\overline{CS}$ = VCC		15	25	mA
Input Low Voltage	VIL		-0.5		VCC x 0.2	V
Input High Voltage	VIH		VCC x 0.8		VCC + 0.4	V
Output Low Voltage	VOL	IOL = 100 µA			0.2	V
Output High Voltage	VOH	IOH = -100 µA	VCC - 0.2			V

1. Tested on sample basis and specified through design and characterization data, TA = 25 ºC, VCC = 1.8 V.
2. Checked board pattern.

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9.5 AC Measurement Conditions

Table 25. AC Measurement Conditions

Parameter	Symbol	Min	Max	Unit
Load Capacitance	C_L		30	pF
Input Rise and Fall Times	T_R, T_F		5	ns
Input Pulse Voltages	V_{IN}	0.2 VCC to 0.8 VCC		V
Input Timing Reference Voltages	IN	0.3 VCC to 0.7 VCC		V
Output Timing Reference Voltages	OUT	0.5 VCC to 0.5 VCC		V

Output Hi-Z is defined as the point where data out is no longer driven.

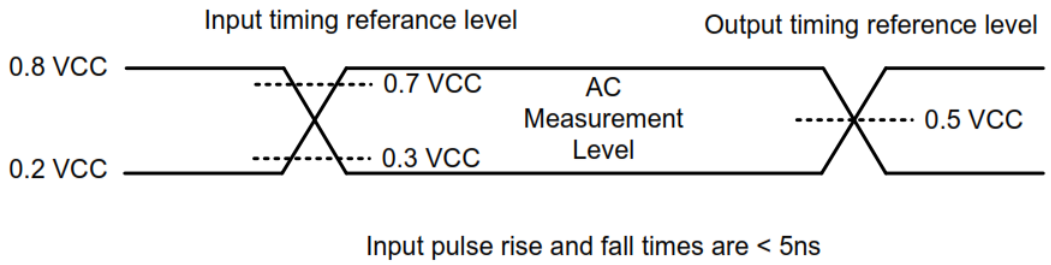

Figure 69. AC Measurement I/O Waveform

9.6 AC Electrical Characteristics

Table 26. AC Electrical Characteristics

Parameter [5]	Symbol	Alt	Min	Typ	Max	Unit
Clock frequency for all commands, except Read Data and Fast Read Data in SPI mode (03h, 0Bh) 1.7 V - 2.0 V VCC and industrial temperature	F_R	f_C	D.C.		133	MHz
Clock freq. Fast Read Data command in SPI mode (0Bh)	f_R		D.C.		104	MHz
Clock freq. Read Data command in SPI mode (03h)	f_R		D.C.		50	MHz
Clock High, Low Time except Read Data (03h)	t_{CLH}, t_{CLL} [1]		3.5			ns
Clock High, Low Time for Read Data (03h) commands	t_{CRLH},		8			ns
Clock Rise Time peak to peak	t_{CLCH} [2]		0.1			V/ns
Clock Fall Time peak to peak	t_{CHCL} [2]		0.1			V/ns
$\overline{CS}$ Active Setup Time relative to Clock	t_{SLCH}	t_{CSS}	5			ns
$\overline{CS}$ Not Active Hold Time relative to Clock	t_{CHSL}		5			ns
Data In Setup Time	t_{DVCH}	t_{DSU}	2			ns
Data In Hold Time	t_{CHDX}	t_{DH}	3			ns
$\overline{CS}$ Active Hold Time relative to Clock	t_{CHSH}		5			ns
$\overline{CS}$ Not Active Setup Time relative to Clock	t_{CHSH}		5			ns
$\overline{CS}$ Deselect Time (for Read commands/Write, Erase and Program commands)	t_{SHSL}	t_{CSH}	100			ns
Output Disable Time	t_{SHQZ} [2]	t_{DIS}			7	ns

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Table 26. AC Electrical Characteristics (Continued)

Parameter [5]	Symbol	Alt	Min	Typ	Max	Unit
Clock Low to Output Valid	t_{CLQV}	t_{V1}			6	ns
Clock Low to Output Valid (Except Main Read) [3]	t_{CLQV}	t_{V2}			7	ns
Output Hold Time	t_{CLQX}	t_{HO}	1.5			ns
$\overline{HOLD}$ Active Setup Time relative to Clock	t_{HLCH}		5			ns
$\overline{HOLD}$ Active Hold Time relative to Clock	t_{CHHH}		5			ns
$\overline{HOLD}$ Not Active Setup Time relative to Clock	t_{HHCH}		5			ns
$\overline{HOLD}$ Not Active Hold Time relative to Clock	t_{CHHL}		5			ns
$\overline{HOLD}$ to Output Low-Z	t_{HHQX} [2]	t_{LZ}			7	ns
$\overline{HOLD}$ to Output High-Z	t_{HLQZ} [2]	t_{HZ}			12	ns
Write Protect Setup Time Before $\overline{CS}$ Low	t_{WHSL} [4]		20			ns
Write Protect Setup Time After $\overline{CS}$ High	t_{SHWL} [4]		100			ns
$\overline{CS}$ High to Power-Down Mode	t_{DP} [2]				3	µs
$\overline{CS}$ High to Standby Mode without Electronic Signature Read	t_{RES1} [2]				3	µs
$\overline{CS}$ High to Standby Mode with Electronic Signature Read	t_{RES2} [2]				1.8	µs
$\overline{CS}$ High to next Command after Suspend	t_{SUS} [2]				30	µs
$\overline{CS}$ High to next Command after Reset	t_{RST} [2]				30	µs
Write Status Register Time	tw			5	15	ms
Byte Program Time	t_{BP}			5	150	µs
Page Program Time	t_{PP}			0.6	5	ms
Block Erase Time (4 kbytes)	t_{SE}			0.06	0.4	s
Block Erase Time (32 kbytes)	t_{BE1}			0.2	1.5	s
Block Erase Time (64 kbytes)	t_{BE2}			0.35	2.5	s
Chip Erase Time	t_{CE}			60	300	s

1. Clock high + Clock low must be less than or equal to 1/fc.
2. Value guaranteed by design and/or characterization, not 100% tested in production.
3. Contains: Read Status Register-1,2/ Read Manufacturer/Device ID, Dual, Quad/ Read JEDEC ID/ Read Security Register/ Read Serial Flash Discovery Parameter.
4. Only applicable as a constraint for a Write Status Register command when Sector Protect Bit is set to 1.
5. Commercial temperature only applies to Fast Read (FR). Industrial temperature applies to all other parameters.

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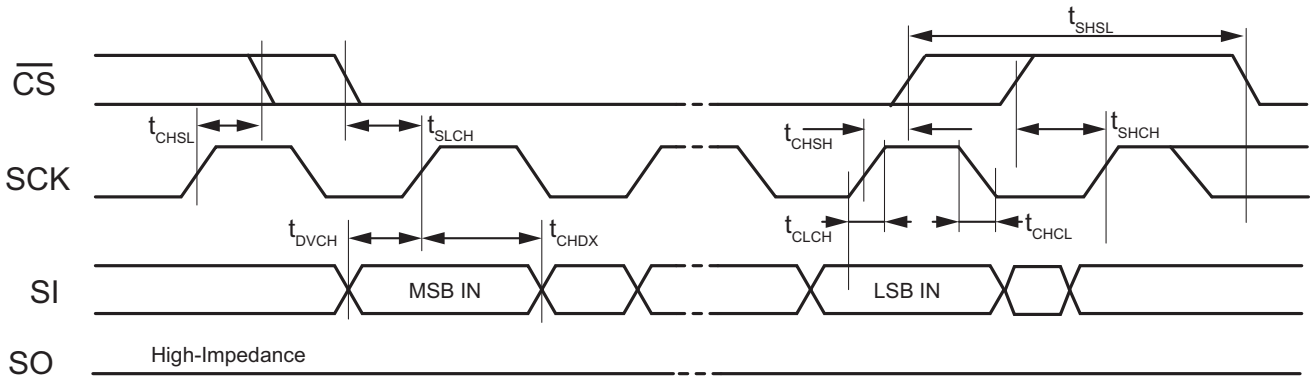
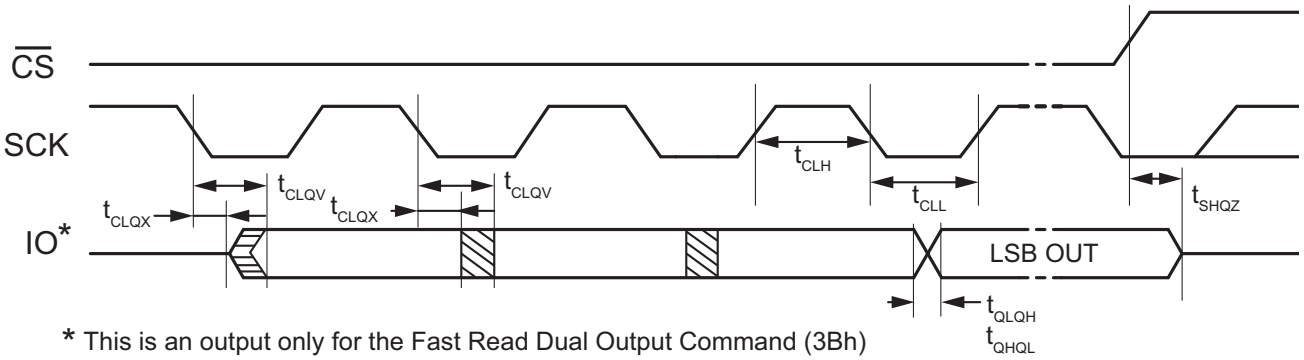
9.7 Input Timing

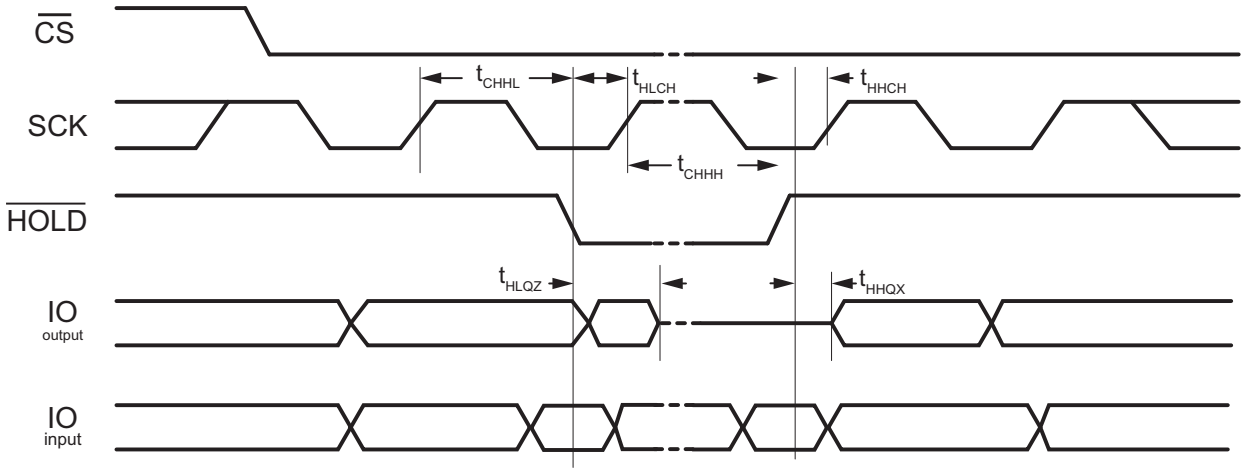


9.8 Output Timing



* This is an output only for the Fast Read Dual Output Command (3Bh)

9.9 $\overline{\text{Hold}}$ Timing



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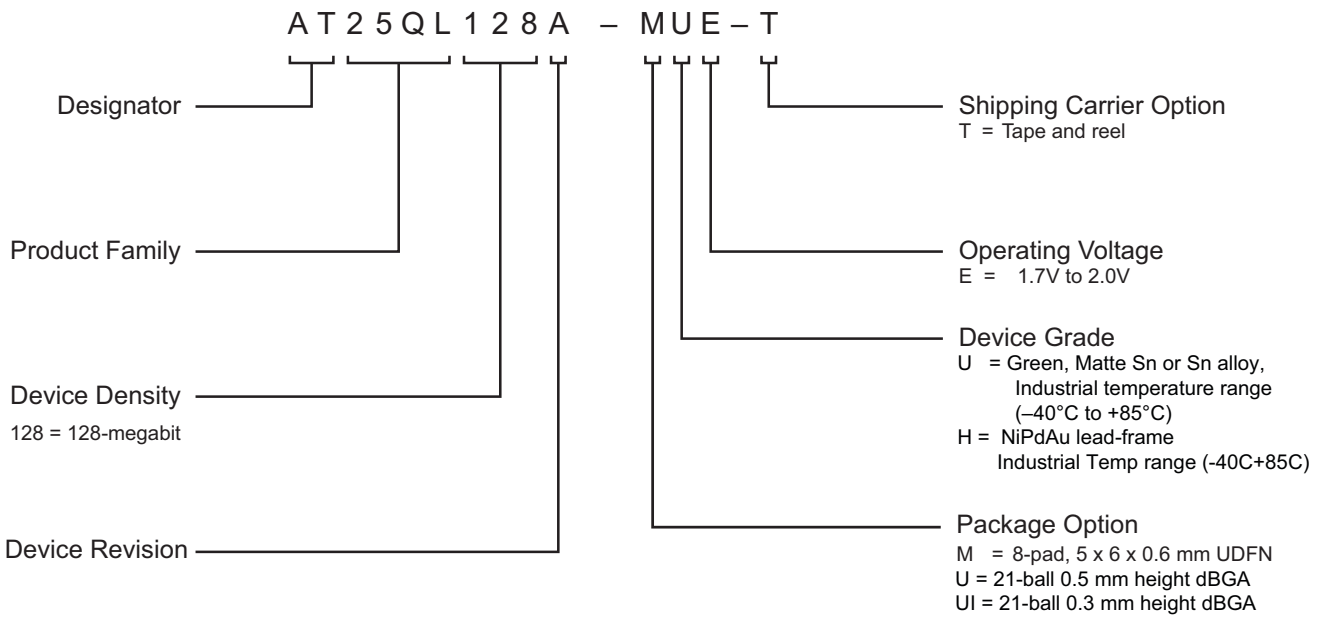
10. Ordering Information

10.1 Ordering Code Detail



Ordering Code [1]	Package	Lead Finish	Operating Voltage	Max. Freq. (MHz)	Operation Range
AT25QL128A-MHE-T	8 MA1	NiPdAu	1.7 V - 2.0 V	133 MHz	-40˚C to 85˚C (Industrial Temperature Range)
AT25QL128A-UUE-T	21-WLCSP	SnAgCu			
AT25QL128A-UIUE-T	21-WLCSP low profile				

1. The shipping carrier option code is not marked on the devices.

Package Type	Package Description
8 MA1	8-pad (5 x 6 x 0.6 mm body), Thermally Enhanced Plastic Ultra-Thin Dual Flat No-lead (UDFN)
U	21-ball, 0.5 mm height, die Ball Grid Array (dBGA)
UI	21-ball, 0.3 mm height, die Ball Grid Array (dBGA)

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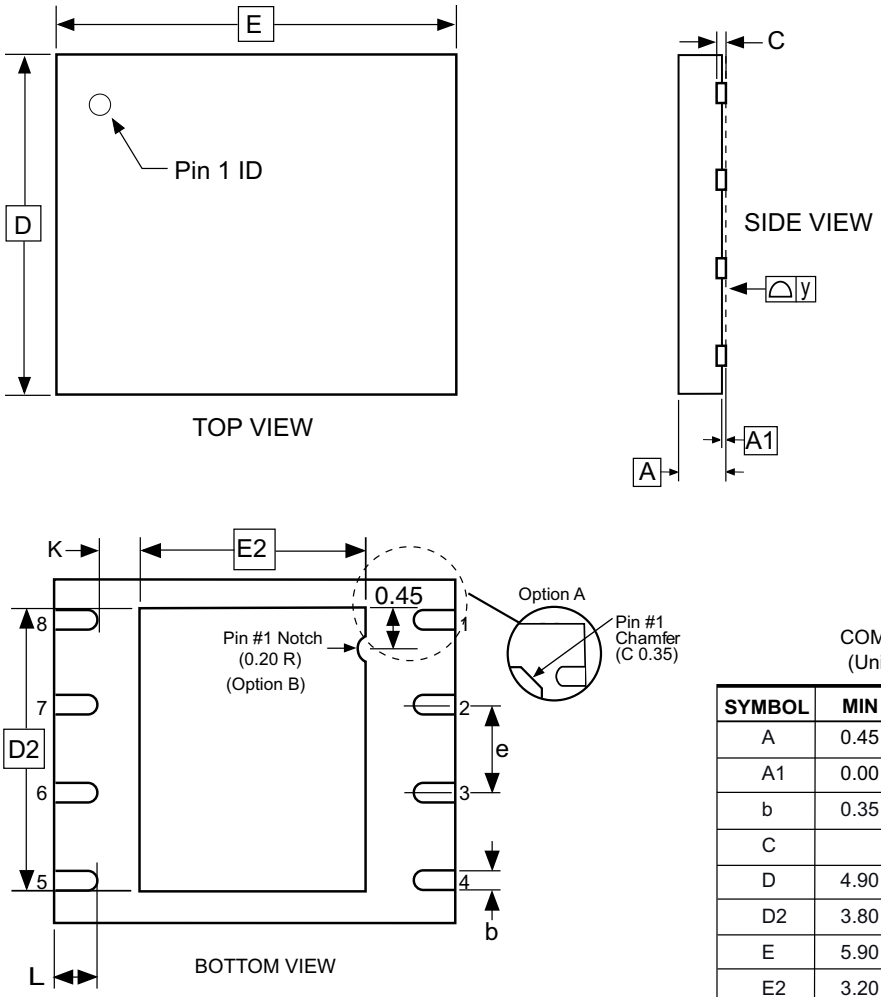
11. Packaging Information

11.1 8 MA1 – UDFN



COMMON DIMENSIONS
(Unit of Measure = mm)

SYMBOL	MIN	NOM	MAX	NOTE
A	0.45	0.55	0.60	
A1	0.00	0.02	0.05	
b	0.35	0.40	0.48	
C		0.152 REF		
D	4.90	5.00	5.10	
D2	3.80	4.00	4.20	
E	5.90	6.00	6.10	
E2	3.20	3.40	3.60	
e		1.27		
L	0.50	0.60	0.75	
y	0.00	–	0.08	
K	0.20	–	–	

Notes: 1. This package conforms to JEDEC reference MO-229, Saw Singulation.
2. The terminal #1 ID is a Laser-marked Feature.

4/15/08

	TITLE	GPC	REV.
RENESAS	8-pad (5 x 6 x 0.6 mm Body), Thermally Enhanced Plastic Ultra Thin Dual Flat No Lead Package (UDFN)	YFG	D

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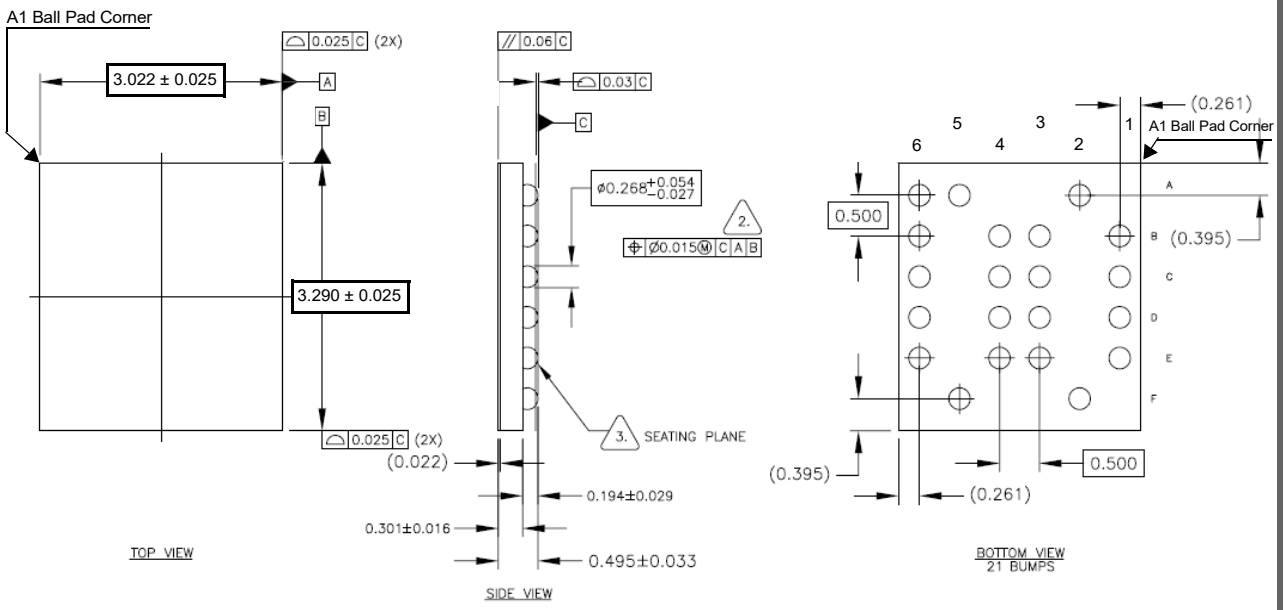
11.2 U (21-WLCSP)



8/1/16

	TITLE	GPC	DRAWING NO.	REV.
RENESAS	21-WLCSP, 21-ball, 3.02 x 3.29 x 0.50 mm body. 0.50 mm ball pitch (6x6 array), Wafer Level Chip Scale Package (WLCSP).	CAA	21WP	B

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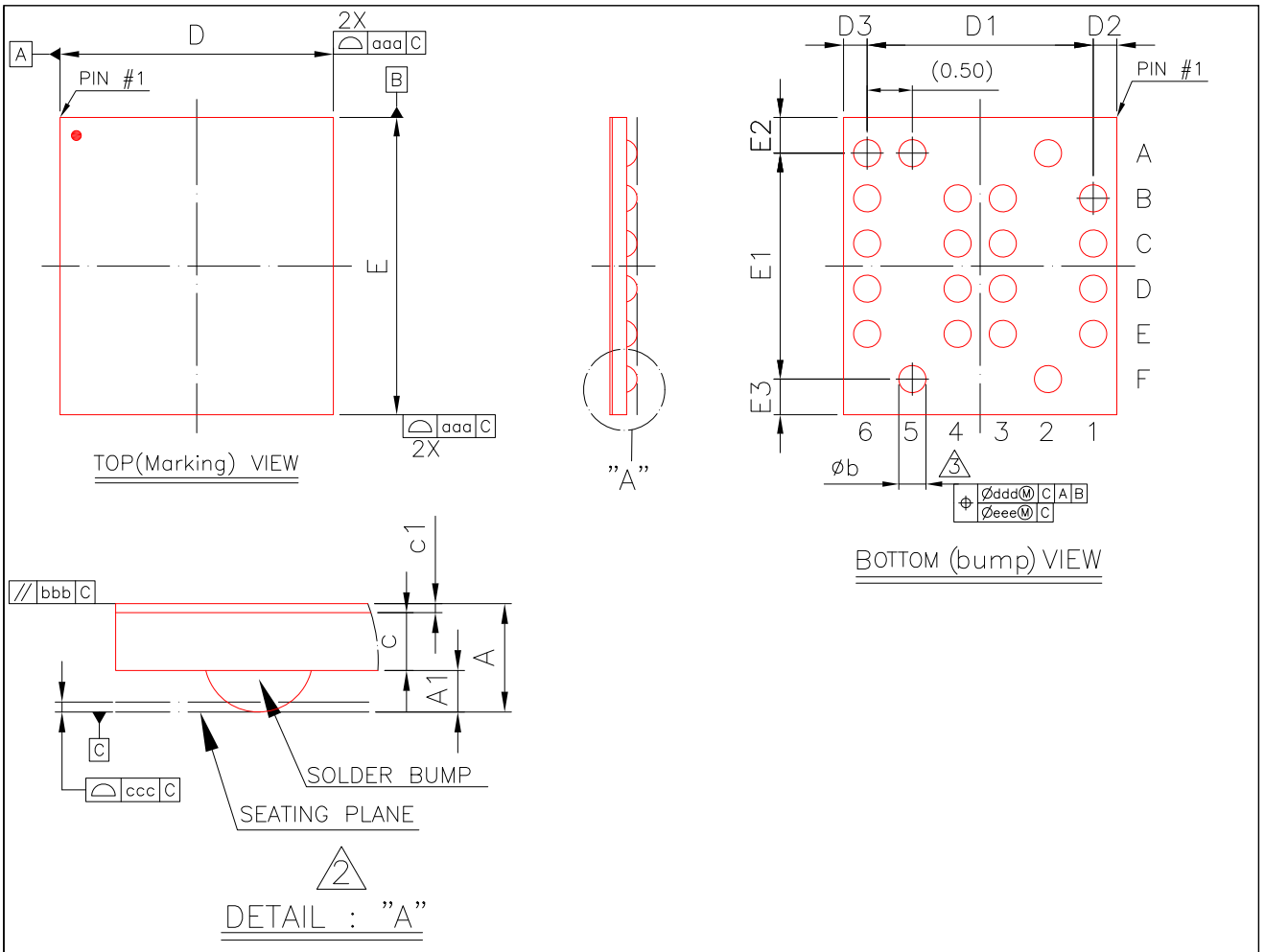
11.3 UI (21-WLCSP)



Symbol	Dimension in mm			Dimension in inch		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.270	0.300	0.330	0.0106	0.0118	0.0130
A1	0.100	0.115	0.130	0.0039	0.0045	0.0051
c	0.148	0.160	0.172	0.0058	0.0063	0.0068
c1	0.022	0.025	0.028	0.0009	0.0010	0.0011
D	2.997	3.022	3.047	0.1180	0.1190	0.1200
E	3.265	3.290	3.315	0.1285	0.1295	0.1305
b	0.270	0.300	0.330	0.0106	0.0118	0.0130
D1	---	2.500	---	---	0.0984	---
E1	---	2.500	---	---	0.0984	---
D2	---	0.261	---	---	0.0103	---
E2	---	0.395	---	---	0.0156	---
D3	---	0.261	---	---	0.0103	---
E3	---	0.395	---	---	0.0156	---
aaa	0.03			0.001		
bbb	0.10			0.004		
ccc	0.03			0.001		
ddd	0.05			0.002		
eee	0.05			0.002		

NOTE:
1. CONTROLLING DIMENSION : MILLIMETER.
2. PRIMARY DATUM C AND SEATING PLANE ARE DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BUMPS.
3. DIMENSION b IS MEASURED AT THE MAXIMUM SOLDER BUMP DIAMETER, PARALLEL TO PRIMARY DATUM C.
4. SPECIAL CHARACTERISTICS C CLASS: c.
5. MINIMUM BUMP PITCH 0.500 mm.
6. THE PIN1 DOT LOCATED AT THE TOP (MARKING)/ BACK (BUMP) VIEW OF DIE IS BASED ON WAFER NOTCH AT THE BOTTOM.
7. BALL PLACEMENT USE Cyclomax 0.2 mm SOLDER BALL.
8. DEVICE NAME: QL128A.
9. DIMENSION FOR Øb for both the UBM and bump diameter.

TITLE	DWG NO.	REV NO
21LD BSL–CF–WLCSP (3.022X3.29 mm) PACKAGE OUTLINE	PSA9096	A

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12. Revision History

Revision	Date	Change History
A	12/2016	Initial release of AT25QL128A data sheet.
B	02/2017	Update Note 1 on Table 8.1.
C	11/2017	Updated Table 1-1 (WP pin description). Updated 5.1 (Write Protect Features). Updated Tables 6-1 and 6-2. Restored Sector and Block Protect descriptions. Restored Status Register Memory Protection tables (Tables 6-3 and 6-4). Updated document status from Advanced to Complete. (Added Errata 11.1). Removed references to 133 MHz option. Removed RESET option from I/O3. Removed 26-WLCSP and 24-ball BGA package options. Removed references to ACC feature.
D	10/2018	Updated maximum operating frequency to 133 MHz throughout document. Updated 104 MHz → 133 MHz, 208 MHz → 266 MHz, and 416 MHz → 532 MHz in Section 1. Table 7-5. Updated the EBh (fast read quad I/O) and 0Ch (burst read with wrap) commands with a 133 MHz entry. Updated frequency in Figure 7-21 to 133 MHz. Updated Figure 7-50, Quad Word Read I/O. Updated Figure 7-54 to 133 MHz. Updated P5:P4 encoding in Section 7.33 Set Read Parameters, to include 133 MHz encoding. Update Table 8.6, DC Electrical Characteristics, to include 133 MHz ICC3. Update Table 8.7, AC Electrical Characteristics, to include 133 MHz timing. Clarified 03h and 0Bh command behavior. Updated row 4 of Table 8-7 from 4.5 to 3.5 ns. Reformatted all tables throughout document. Thorough technical edit of existing material. Updated current consumption in DPD mode from 3 µA to 2 µA. Updated ordering code information in Section 9.1 to show 133 MHz frequency. Updated table 8-2 in Section 8.1 to show 133 MHz. Removed Die in Wafer Form packaging option.
E	01/2021	Updated 21-WLCSP package dimensions and package ball out numbering and A1 ball location in Section 11.3. Reformatted and standardized all tables throughout document. Changed template to latest Adesto standard. Added part number AT25QL128A-UIUE-T (21-ball low profile WLCSP package) in Section 10. Added low-profile WLCSP package details in Section 11.4. Corrected descriptions for $\overline{WP}$ and $\overline{HOLD}$ pins in Table 2-1.
F	02/2022	Applied new corporate template to document. Removed the 8-lead 208-mil SOIC package option. Added physical block size information to Key Features list and Section 1 Introduction. Removed the 208-mil SOIC package option in Section 10 and Section 11. Added the following note to the description of the 75h command: “A read operation from an 8-Mbit area (referred to as a physical block) that includes a suspended area might provide unreliable data. For the definition of the physical block and for the techniques to ensure high data integrity, see application note AN-500.” Changed “AT25QL128A-SUE-T” to “AT25QL128A-MHE-T” in Section 10. Removed the “S” from Package Options in Section 10. Removed “AT25QL128A-SUE-T” from Ordering Code in Section 10. Removed “8S4” from Package Type in Section 10.

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12.1 Errata:

1. If Status Register-2 CMP bit is 0, and Status Register-1 bits {SEC,TB,BP2,BP1,BP} are {1,0,0,0,1}, addresses FFF000h-FFFFFFh *are protected* from any Program or Erase commands. However, this setting does *not* protect the rest of Sector 255 or the rest of Block 511 from 64 kbit or 32 kbit Block Erase commands. If a 64 kbit Block Erase Command is issued to Sector 255, addresses FF0000h-FFEFFFh *are* erased. If a 32 kbit Block Erase Command is issued to Block 511, addresses FF8000h-FFEFFFh *are* erased.

   Workaround: If this protection bit combination is used and the behavior described in Note 3 is required, avoid using 64 kbit or 32kbit Block Erase commands for this specific memory region.

2. If Status Register-2 CMP bit is 1, and Status Register-1 bits {SEC,TB,BP2,BP1,BP} are {1,1,0,0,1}, addresses 001000h-FFFFFFh *are protected* from any Program or Erase commands. However, this setting does *not* protect the rest of Sector 0 or the rest of Block 0 from 64 kbit or 32 kbit Block Erase commands. If a 64 kbit Block Erase Command is issued to Sector 0, addresses 000000h-000FFFh *are* erased. If a 32 kbit Block Erase Command is issued to Block 0, addresses 000000h-000FFFh *are* erased.

   Workaround: If this protection bit combination is used and the behavior described in Note 3 is required, avoid using 64 kbit or 32 kbit Block Erase commands for this specific memory region.

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