CD40106B CMOS Hex Schmitt-Trigger Inverters

1 Features

- Schmitt-Trigger Inputs
- Hysteresis Voltage (Typical):
  - 0.9 V at V_{DD} = 5 V
  - 2.3 V at V_{DD} = 10 V
  - 3.5 V at V_{DD} = 15 V
- Noise Immunity Greater Than 50%
- No Limit On Input Rise and Fall Times
- Standardized, Symmetrical Output Characteristics
- For Quiescent Current at 20 V
- Maximum Input Current Of 1 µA at 18 V Over Full Package Temperature Range:
  - 100 nA at 18 V and 25°C
- Low V_{DD} and V_{SS} Current During Slow Input Ramp
- 5-V, 10-V, and 15-V Parametric Ratings

2 Applications

- Wave and Pulse Shapers
- High-Noise-Environment Systems
- Monostable Multivibrators
- Astable Multivibrators

3 Description

The CD40106B device consists of six Schmitt-Trigger inputs. Each circuit functions as an inverter with Schmitt-Trigger input. The trigger switches at different points for positive- and negative-going signals. The difference between the positive-going voltage (V_P) and the negative-going voltages (V_N) is defined as hysteresis voltage (V_H).

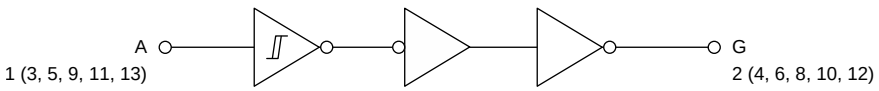
The CD40106B device is supplied in ceramic packaging (J) as well as standard packaging (D, N, NS, PW). All CD40106B devices are rated for –55°C to +125°C ambient temperature operation.

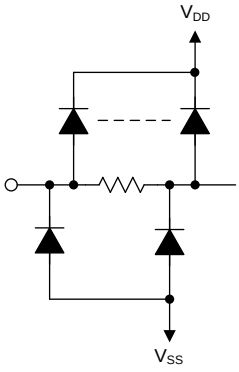
Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
CD40106BF	CDIP (14)	6.92 mm x 19.94 mm
CD40106BE	PDIP (14)	6.30 mm x 19.31 mm
CD40106BM	SOIC (14)	3.90 mm x 8.65 mm
CD40106BNSR	SO (14)	5.30 mm x 10.20 mm
CD40106BPWR	TSSOP (14)	4.40 mm x 5.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Logic Diagram





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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision E (September 2016) to Revision F **Page**

- Changed incorrect pin descriptions to match package drawing ... 3

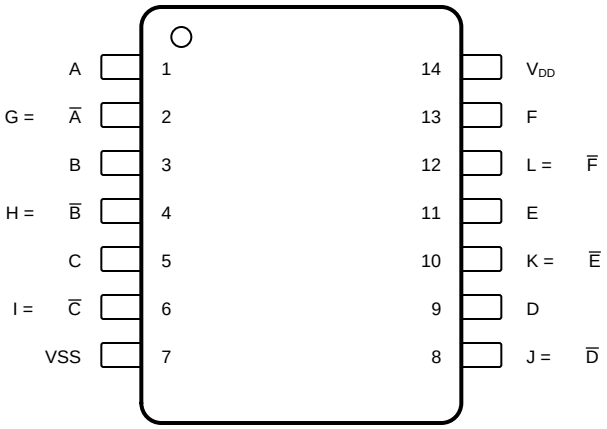
Changes from Revision D (August 2003) to Revision E **Page**

- Added *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section ... 1
- Added *Thermal Information* table ... 4

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5 Pin Configuration and Functions

D, J, N, NS, PW Packages
14-Pin SOIC, CDIP, PDIP, SO, TSSOP
Top View



Not to scale

Pin Functions

PIN		I/O	DESCRIPTION
NO.	NAME		
1	A	I	Channel A input
2	G = $\overline{A}$	O	Channel A inverted output
3	B	I	Channel B input
4	H = $\overline{B}$	O	Channel B inverted output
5	C	I	Channel C input
6	I = $\overline{C}$	O	Channel C inverted output
7	V_{SS}	—	Ground
8	J = $\overline{D}$	O	Channel D inverted output
9	D	I	Channel D input
10	K = $\overline{E}$	O	Channel E inverted output
11	E	I	Channel E input
12	L = $\overline{F}$	O	Channel F inverted output
13	F	I	Channel F input
14	V_{DD}	—	Power supply

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6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
DC supply voltage, V_{DD}(2)		–0.5	20	V
Input voltage, all inputs		–0.5	V_{DD} + 0.5	V
DC input current, any one input			±10	mA
Power dissipation, P_D	T_A = –55°C to +100°C		500	mW
	T_A = 100°C to 125°C(3)		200	
Device dissipation per output transistor			100	mW
Maximum junction temperature, T_J			150	°C
Storage temperature, T_{stg}		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Voltages referenced to V_{SS} terminal
(3) Derate linearity at 12 mW/°C

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

	MIN	MAX	UNIT
Supply voltage	3	18	V
Operating temperature, T_A	–55	125	°C

6.4 Thermal Information

THERMAL METRIC(1)		CD40106B				UNIT
		D (SOIC)	N (PDIP)	NS (SO)	PW (TSSOP)	
		14 PINS	14 PINS	14 PINS	14 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	86.1	51.3	83.5	114.1	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	44.3	38.6	41.5	39.1	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	40.6	31.2	42.2	56.9	°C/W
ψ_{JT}	Junction-to-top characterization parameter	11.6	23.4	13.1	3.1	°C/W
ψ_{JB}	Junction-to-board characterization parameter	40.3	31.3	41.8	56.2	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

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6.5 Electrical Characteristics: Static

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
I_{DD}max	Quiescent device current	V_{IN} = 0 or 5, V_{DD} = 5	T_A = –55°C			1	µA
			T_A = –40°C			1	
			T_A = 25°C		0.02	1	
			T_A = 85°C			30	
			T_A = 125°C			30	
		V_{IN} = 0 or 10, V_{DD} = 10	T_A = –55°C			2	
			T_A = –40°C			2	
			T_A = 25°C		0.02	2	
			T_A = 85°C			60	
			T_A = 125°C			60	
		V_{IN} = 0 or 15, V_{DD} = 15	T_A = –55°C			4	
			T_A = –40°C			4	
			T_A = 25°C		0.02	4	
			T_A = 85°C			120	
			T_A = 125°C			120	
		V_{IN} = 0 or 20, V_{DD} = 20	T_A = –55°C			20	
			T_A = –40°C			20	
			T_A = 25°C		0.04	20	
			T_A = 85°C			600	
			T_A = 125°C			600	
$V_P$min	Positive trigger threshold voltage	V_{DD} = 5	T_A = –55°C	2.2			V
			T_A = –40°C	2.2			
			T_A = 25°C	2.2	2.9		
			T_A = 85°C	2.2			
			T_A = 125°C	2.2			
		V_{DD} = 10	T_A = –55°C	4.6			
			T_A = –40°C	4.6			
			T_A = 25°C	4.6	5.9		
			T_A = 85°C	4.6			
			T_A = 125°C	4.6			
		V_{DD} = 15	T_A = –55°C	6.8			
			T_A = –40°C	6.8			
			T_A = 25°C	6.8	8.8		
			T_A = 85°C	6.8			
			T_A = 125°C	6.8			

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Electrical Characteristics: Static (continued)

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
$V_P$max	Positive trigger threshold voltage	V_{DD} = 5	T_A = –55°C			3.6	V
			T_A = –40°C			3.6	
			T_A = 25°C		2.9	3.6	
			T_A = 85°C			3.6	
			T_A = 125°C			3.6	
		V_{DD} = 10	T_A = –55°C			7.1	
			T_A = –40°C			7.1	
			T_A = 25°C		5.9	7.1	
			T_A = 85°C			7.1	
			T_A = 125°C			7.1	
		V_{DD} = 15	T_A = –55°C			10.8	
			T_A = –40°C			10.8	
			T_A = 25°C		8.8	10.8	
			T_A = 85°C			10.8	
			T_A = 125°C			10.8	
$V_N$min	Negative trigger threshold voltage	V_{DD} = 5	T_A = –55°C	0.9			V
			T_A = –40°C	0.9			
			T_A = 25°C	0.9	1.9		
			T_A = 85°C	0.9			
			T_A = 125°C	0.9			
		V_{DD} = 10	T_A = –55°C	2.5			
			T_A = –40°C	2.5			
			T_A = 25°C	2.5	3.9		
			T_A = 85°C	2.5			
			T_A = 125°C	2.5			
		V_{DD} = 15	T_A = –55°C	4			
			T_A = –40°C	4			
			T_A = 25°C	4	5.8		
			T_A = 85°C	4			
			T_A = 125°C	4			
$V_N$max	Negative trigger threshold voltage	V_{DD} = 5	T_A = –55°C			2.8	V
			T_A = –40°C			2.8	
			T_A = 25°C		1.9	2.8	
			T_A = 85°C			2.8	
			T_A = 125°C			2.8	
		V_{DD} = 10	T_A = –55°C			5.2	
			T_A = –40°C			5.2	
			T_A = 25°C		3.9	5.2	
			T_A = 85°C			5.2	
			T_A = 125°C			5.2	
		V_{DD} = 15	T_A = –55°C			7.4	
			T_A = –40°C			7.4	
			T_A = 25°C		5.8	7.4	
			T_A = 85°C			7.4	
			T_A = 125°C			7.4	

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Electrical Characteristics: Static (continued)

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
$V_H$min	Hysteresis voltage	V_{DD} = 5	T_A = –55°C	0.3			V
			T_A = –40°C	0.3			
			T_A = 25°C	0.3	0.9		
			T_A = 85°C	0.3			
			T_A = 125°C	0.3			
		V_{DD} = 10	T_A = –55°C	1.2			
			T_A = –40°C	1.2			
			T_A = 25°C	1.2	2.3		
			T_A = 85°C	1.2			
			T_A = 125°C	1.2			
		V_{DD} = 15	T_A = –55°C	1.6			
			T_A = –40°C	1.6			
			T_A = 25°C	1.6	3.5		
			T_A = 85°C	1.6			
			T_A = 125°C	1.6			
$V_H$max	Hysteresis voltage	V_{DD} = 5	T_A = –55°C			1.6	V
			T_A = –40°C			1.6	
			T_A = 25°C		0.9	1.6	
			T_A = 85°C			1.6	
			T_A = 125°C			1.6	
		V_{DD} = 10	T_A = –55°C			3.4	
			T_A = –40°C			3.4	
			T_A = 25°C		2.3	3.4	
			T_A = 85°C			3.4	
			T_A = 125°C			3.4	
		V_{DD} = 15	T_A = –55°C			5	
			T_A = –40°C			5	
			T_A = 25°C		3.5	5	
			T_A = 85°C			5	
			T_A = 125°C			5	
I_{OL}min	Output low (sink) current	V_O = 0.4, V_{IN} = 0 or 5, V_{DD} = 5	T_A = –55°C	0.64			mA
			T_A = –40°C	0.61			
			T_A = 25°C	0.51	1		
			T_A = 85°C	0.42			
			T_A = 125°C	0.36			
		V_O = 0.5, V_{IN} = 0 or 10, V_{DD} = 10	T_A = –55°C	1.6			
			T_A = –40°C	1.5			
			T_A = 25°C	1.3	2.6		
			T_A = 85°C	1.1			
			T_A = 125°C	0.9			
		V_O = 1.5, V_{IN} = 0 or 15, V_{DD} = 15	T_A = –55°C	4.2			
			T_A = –40°C	4			
			T_A = 25°C	3.4	6.8		
			T_A = 85°C	2.8			
			T_A = 125°C	2.4			

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Electrical Characteristics: Static (continued)

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
I_{OH}min	Output high (source) current	V_O = 4.6, V_{IN} = 0 or 5, V_{DD} = 5	T_A = –55°C	–0.64			mA
			T_A = –40°C	–0.61			
			T_A = 25°C	–0.51	–1		
			T_A = 85°C	–0.42			
			T_A = 125°C	–0.36			
		V_O = 2.5, V_{IN} = 0 or 5, V_{DD} = 5	T_A = –55°C	–2			
			T_A = –40°C	–1.8			
			T_A = 25°C	–1.6	–3.2		
			T_A = 85°C	–1.3			
			T_A = 125°C	–1.15			
		V_O = 9.5, V_{IN} = 0 or 10, V_{DD} = 10	T_A = –55°C	–1.6			
			T_A = –40°C	–1.5			
			T_A = 25°C	–1.3	–2.6		
			T_A = 85°C	–1.1			
			T_A = 125°C	–0.9			
		V_O = 13.5, V_{IN} = 0 or 15, V_{DD} = 15	T_A = –55°C	–4.2			
			T_A = –40°C	–4			
			T_A = 25°C	–3.4	–6.8		
			T_A = 85°C	–2.8			
			T_A = 125°C	–2.4			
V_{OL}max	Low-level output voltage	V_{IN} = 5, V_{DD} = 5	T_A = –55°C, –40°C, 25°C, 85°C, and 125°C		0	0.05	V
		V_{IN} = 10, V_{DD} = 10	T_A = –55°C, –40°C, 25°C, 85°C, and 125°C		0	0.05	
		V_{IN} = 15, V_{DD} = 15	T_A = –55°C, –40°C, 25°C, 85°C, and 125°C		0	0.05	
V_{OH}min	High-level output voltage	V_{IN} = 0, V_{DD} = 5	T_A = –55°C, –40°C, 25°C, 85°C, and 125°C	4.95	5		V
		V_{IN} = 0, V_{DD} = 10	T_A = –55°C, –40°C, 25°C, 85°C, and 125°C	9.95	10		
		V_{IN} = 0, V_{DD} = 15	T_A = –55°C, –40°C, 25°C, 85°C, and 125°C	14.95	15		
I_{IN}max	Input current	V_{IN} = 0 or 18, V_{DD} = 18	T_A = –55°C			±0.1	µA
			T_A = –40°C			±0.1	
			T_A = 25°C		±0.00001	±0.1	
			T_A = 85°C			±1	
			T_A = 125°C			±1	

6.6 Electrical Characteristics: Dynamic

at T_A = 25°C, input t_r, t_f = 20 ns, C_L = 50 pF, and R_L = 200 kΩ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PHL}, t_{PLH}	Propagation delay time	V_{DD} = 5		140	280	ns
		V_{DD} = 10		70	140	
		V_{DD} = 15		60	120	
t_{THL}, t_{TLH}	Transition time	V_{DD} = 5		100	200	ns
		V_{DD} = 10		50	100	
		V_{DD} = 15		40	80	
C_{IN}	Input capacitance	Any input		5	7.5	pF

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6.7 Typical Characteristics

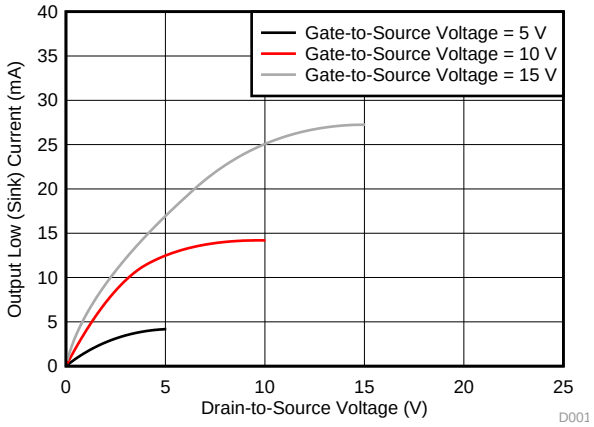


Figure 1. Typical Output Low (Sink) Current Characteristics

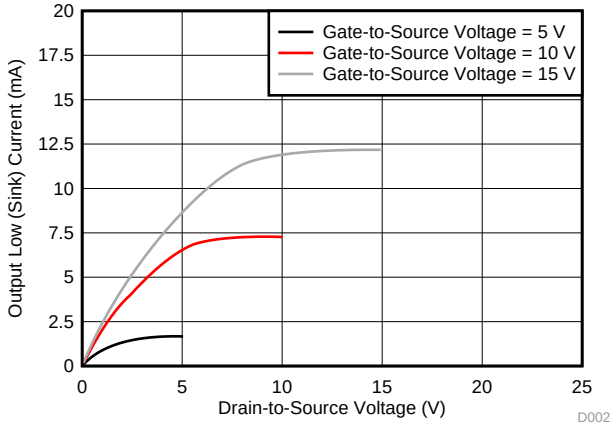


Figure 2. Minimum Output Low (Sink) Current Characteristics

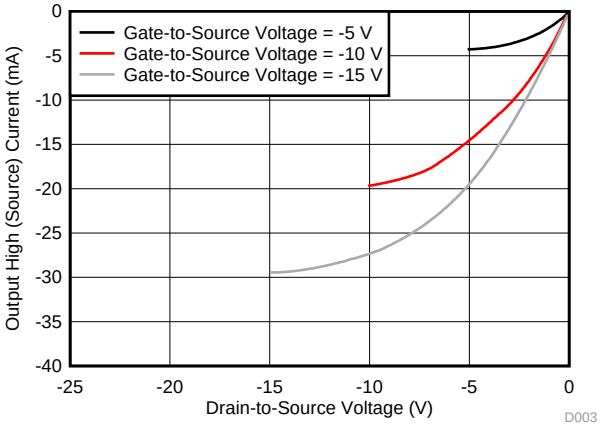


Figure 3. Typical Output High (Source) Current Characteristics

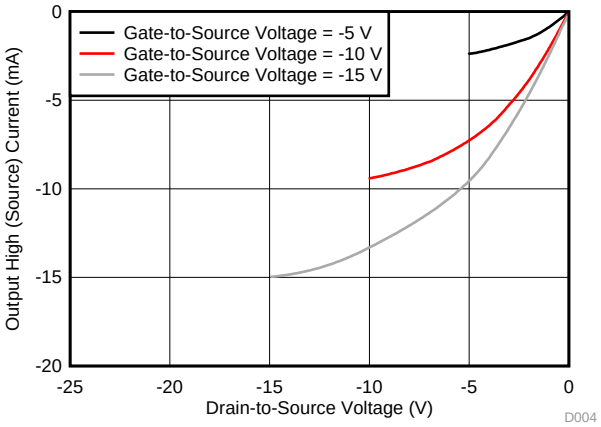


Figure 4. Minimum Output High (Source) Current Characteristics

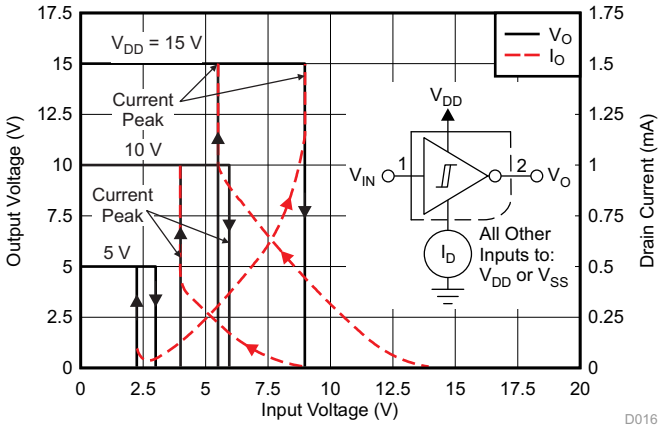


Figure 5. Typical Current and Voltage Transfer Characteristics

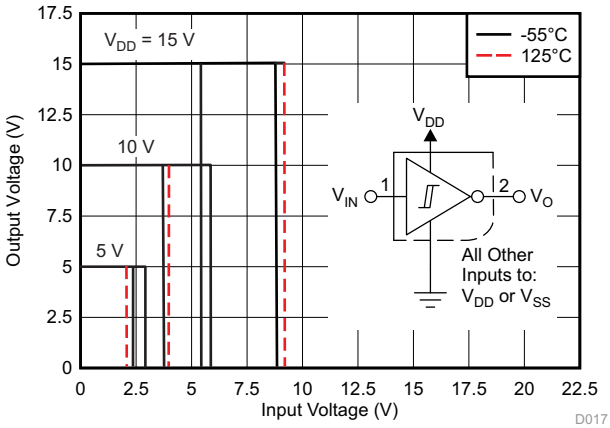


Figure 6. Typical Voltage Transfer Characteristics as a Function of Temperature

Typical Characteristics (continued)

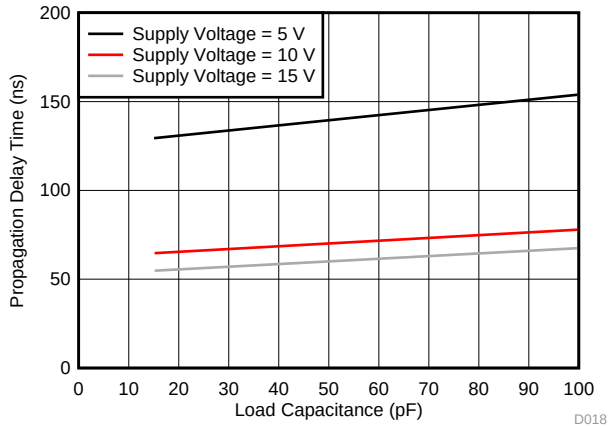


Figure 7. Typical Propagation Delay Time as a Function of Load Capacitance

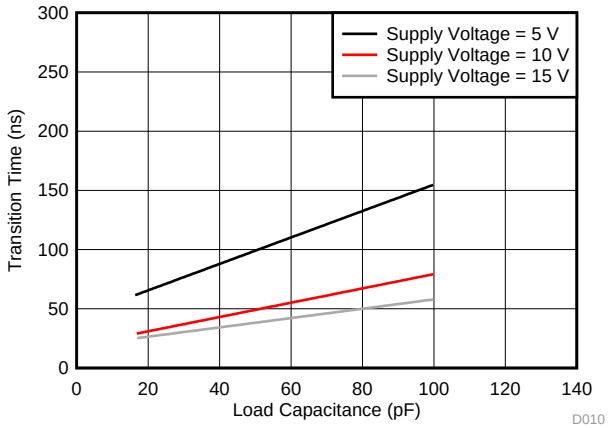


Figure 8. Typical Transition Time as a Function of Load Capacitance

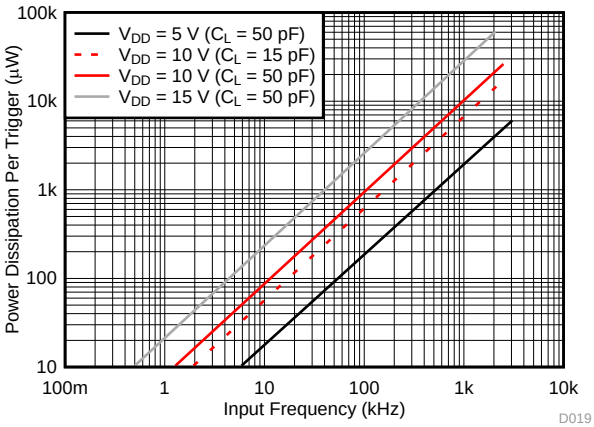


Figure 9. Typical Power Dissipation Per Trigger as a Function of Input Frequency

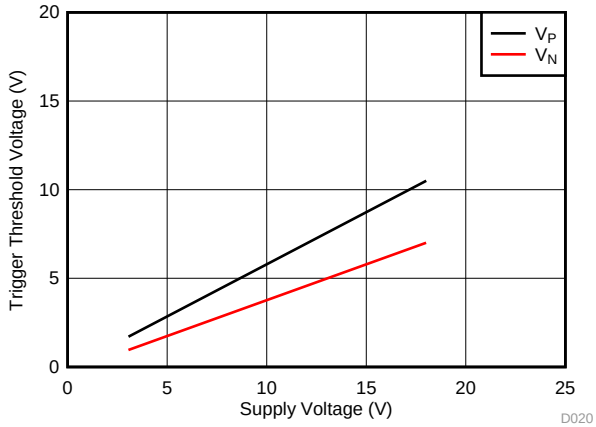


Figure 10. Typical Trigger Threshold Voltage as a Function of Supply Voltage

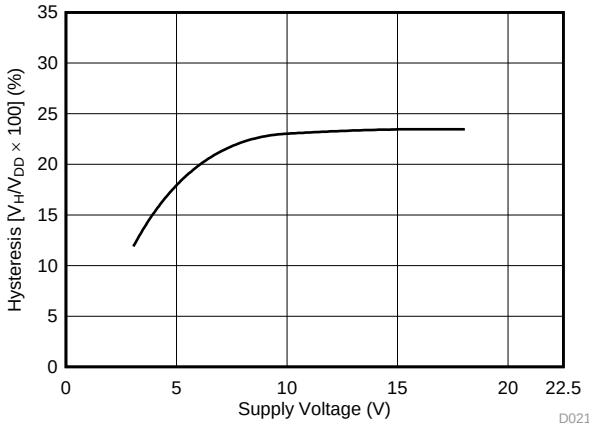


Figure 11. Typical Percent Hysteresis as a Function of Supply Voltage

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7 Parameter Measurement Information

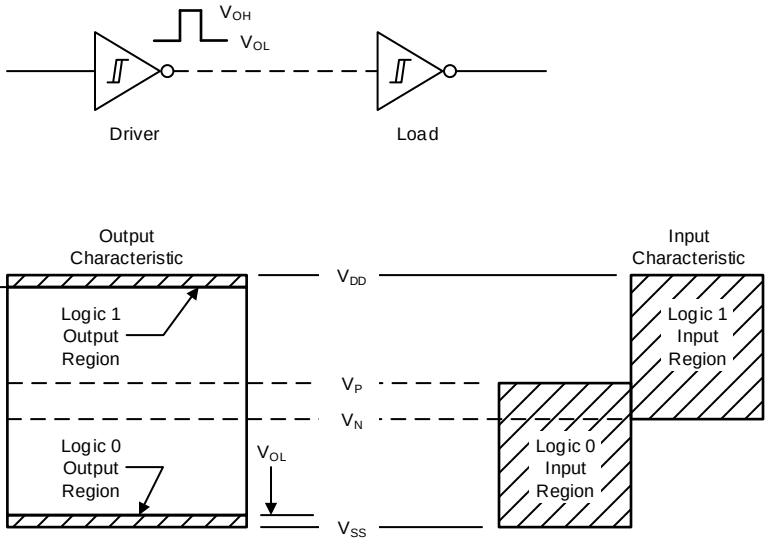
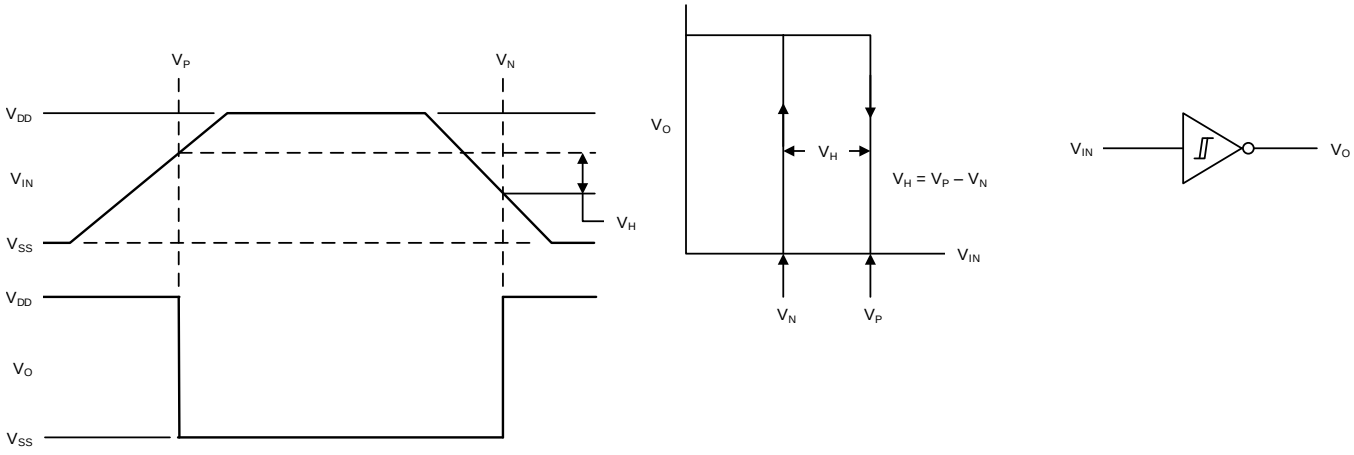


Figure 12. Input and Output Characteristics



a) Definition of V_P, V_N, and V_H b) Transfer Characteristics of 1 of 6 Gates

Figure 13. Hysteresis Definition, Characteristics, and Test Set-Up

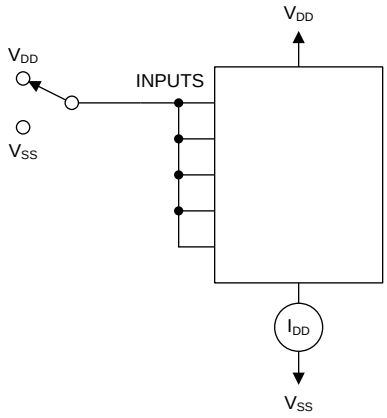


Figure 14. Quiescent Device Current Test Circuit

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Parameter Measurement Information (continued)

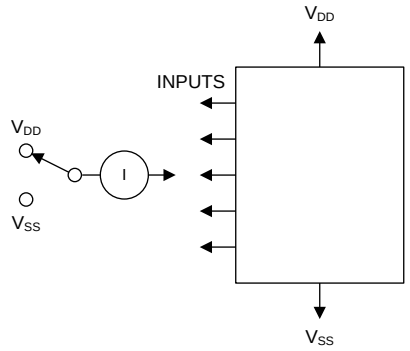


Figure 15. Input Current Test Circuit

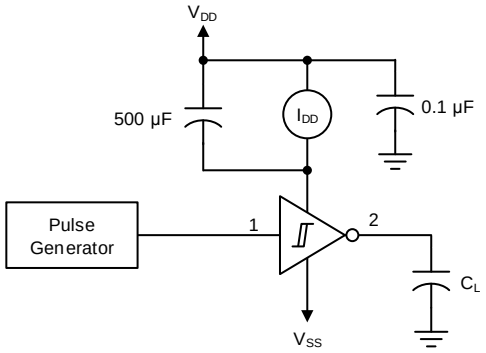


Figure 16. Dynamic Power Dissipation Test Circuit

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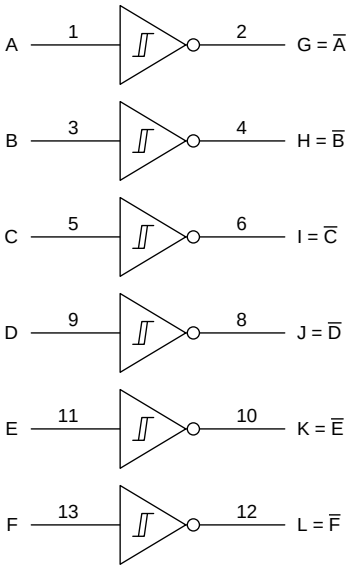
8 Detailed Description

8.1 Overview

The CD40106B device contains six independent inverters with schmitt trigger inputs.. They perform the Boolean function $Y = \overline{A}$ in positive logic.

Schmitt-Trigger inputs are designed to provide a minimum separation between positive and negative switching thresholds. This allows for noisy or slow inputs that would cause problems such as oscillation or excessive current consumption.

8.2 Functional Block Diagram



V_{DD} = Pin 14
V_{SS} = Pin 7

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8.3 Feature Description

The CD40106B has standardized symmetrical output characteristics and a wide operating voltage from 3 V to 18 V with quiescent current of 20 µA tested at 20 V. These devices have transition times of $t_{TLH} = t_{THL} = 50$ ns (typical) at 10 V. The operating temperature is from –55°C to +125°C. Schmitt trigger inputs on this device support slow or noisy input signals.

8.4 Device Functional Modes

Table 1 lists the functional modes of the CD40106B.

Table 1. Function Table

INPUT	OUTPUT
H	L
L	H

9 Application and Implementation

NOTE

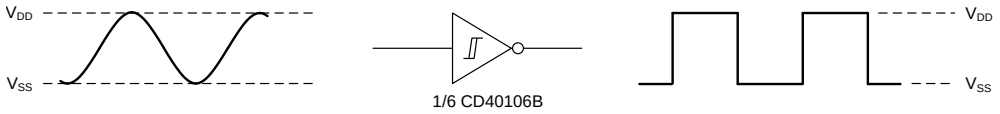
Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The CD40106B device is a Schmitt-Trigger input device that can be used for a multitude of inverting buffer type functions. The application shown here takes advantage of the Schmitt-Trigger inputs to produce a square wave output from a sine wave input.

9.2 Typical Applications

9.2.1 Wave Shaper



Frequency Range of Wave Shape
is from DC to 1 MHz.

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Figure 17. Wave Shaper Schematic

9.2.1.1 Design Requirements

Take care to avoid bus contention, because it can drive currents that would exceed maximum limits. Parallel output drive can create fast edges into light loads so consider routing and load conditions to prevent ringing.

9.2.1.2 Detailed Design Procedure

The recommended input conditions for Figure 17 includes specified high and low levels (see V_P and V_N in *Electrical Characteristics: Static*). Inputs are not overvoltage tolerant and must be below V_{CC} level because of the presence of input clamp diodes to VCC.

The recommended output condition for the CD40106B application includes specific load currents. Load currents must be limited so as to not exceed the total power (continuous current through VCC or GND) for the device. These limits are in the *Absolute Maximum Ratings*. Outputs must not be pulled above V_{CC}.

9.2.1.3 Application Curve

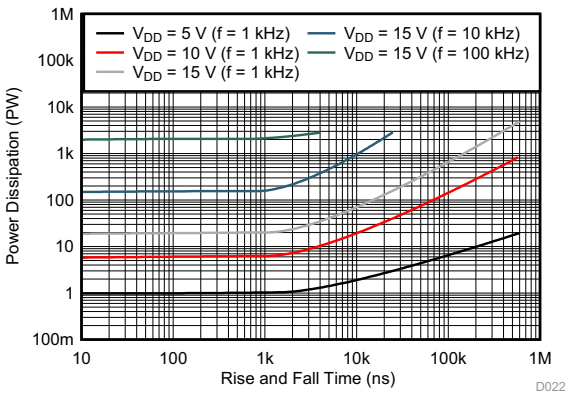


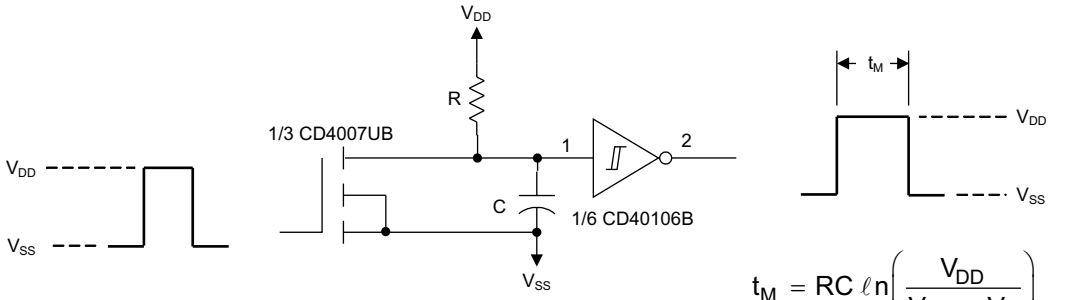
Figure 18. Typical Power Dissipation as a Function of Rise and Fall Times

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Typical Applications (continued)

9.2.2 Monostable Multivibrator

The timing of the monostable multivibrator circuit can be set by following the equations shown in Figure 19.



$$t_M = RC\,\ell n\left(\frac{V_{DD}}{V_{DD} - V_P}\right)$$

$50\ k\Omega \le R \le 1\ M\Omega$

$100\ pF \le C \le 1\ \mu F$

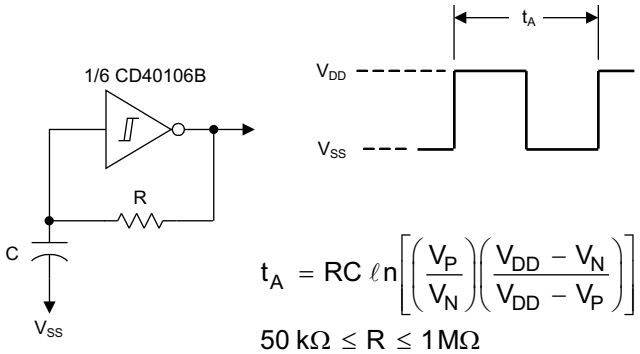
For the Range of R and C
Given $5\ \mu s < t_M < 1\ s$

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Figure 19. Monostable Multivibrator Schematic and Equations

9.2.3 Astable Multivibrator

The timing of the astable multivibrator circuit can be set by following the equations shown in Figure 20.



$$t_A = RC\,\ell n\left[\left(\frac{V_P}{V_N}\right)\left(\frac{V_{DD} - V_N}{V_{DD} - V_P}\right)\right]$$

$50\ k\Omega \le R \le 1\ M\Omega$

$100\ pF \le C \le 1\ \mu F$

For the Range of R and C
Given $2\ \mu s < t_A < 0.4\ s$

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Figure 20. Astable Multivibrator Schematic and Equations

10 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating located in the *Recommended Operating Conditions*. The V_{CC} terminal must have a good bypass capacitor to prevent power disturbance. A 0.1-µF capacitor is recommended to be used on the V_{CC} terminal, and it must be placed as close as possible to the pin for best results.

11 Layout

11.1 Layout Guidelines

When using multiple bit logic devices, inputs must never float. In many cases, functions or parts of functions of digital logic devices are unused, for example, when only two inputs of a triple-input AND gate are used or only three of the four buffer gates are used. Such inputs must not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. All unused inputs of digital logic devices must be connected to a high or low bias to prevent them from floating. The logic level that must be applied to any particular unused input depends on the function of the device. Generally they are tied to GND or V_{CC}, whichever makes more sense or is more convenient. Floating outputs are generally acceptable, unless the part is a transceiver.

11.2 Layout Example

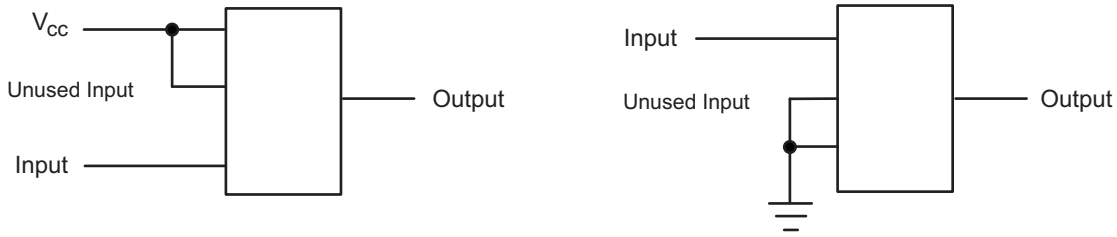


Figure 21. Layout Diagram

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Layout Example (continued)

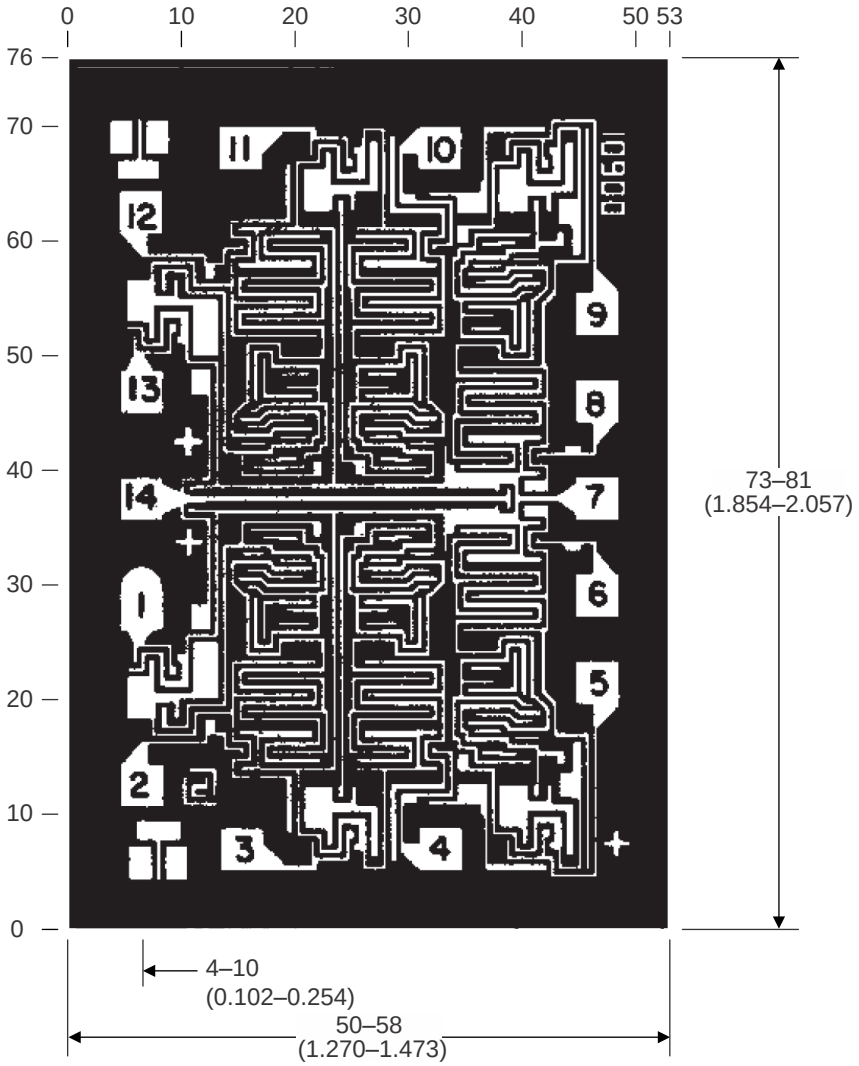


Figure 22. Dimensions and Pad Layout for CD40106BH

12 Device and Documentation Support

12.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.2 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.3 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

12.4 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
CD40106BE	ACTIVE	PDIP	N	14	25	RoHS & Green	NIPDAU	N / A for Pkg Type	-55 to 125	CD40106BE	Samples
CD40106BEE4	ACTIVE	PDIP	N	14	25	RoHS & Green	NIPDAU	N / A for Pkg Type	-55 to 125	CD40106BE	Samples
CD40106BF	ACTIVE	CDIP	J	14	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	CD40106BF	Samples
CD40106BF3A	ACTIVE	CDIP	J	14	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	CD40106BF3A	Samples
CD40106BM	ACTIVE	SOIC	D	14	50	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	CD40106BM	Samples
CD40106BM96	ACTIVE	SOIC	D	14	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	CD40106BM	Samples
CD40106BM96E4	ACTIVE	SOIC	D	14	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	CD40106BM	Samples
CD40106BM96G4	ACTIVE	SOIC	D	14	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	CD40106BM	Samples
CD40106BMG4	ACTIVE	SOIC	D	14	50	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	CD40106BM	Samples
CD40106BMT	ACTIVE	SOIC	D	14	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	CD40106BM	Samples
CD40106BNSR	ACTIVE	SO	NS	14	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	CD40106B	Samples
CD40106BPW	ACTIVE	TSSOP	PW	14	90	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	CM0106B	Samples
CD40106BPWR	ACTIVE	TSSOP	PW	14	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	CM0106B	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF CD40106B, CD40106B-MIL :

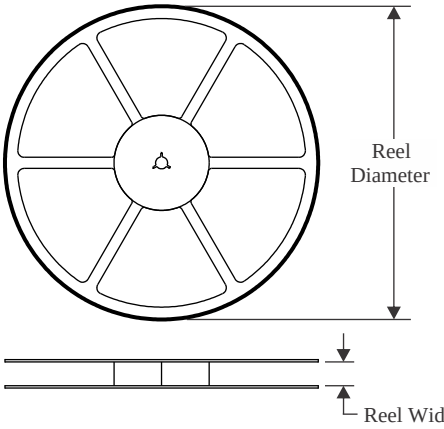
- Catalog : CD40106B
- Military : CD40106B-MIL

NOTE: Qualified Version Definitions:

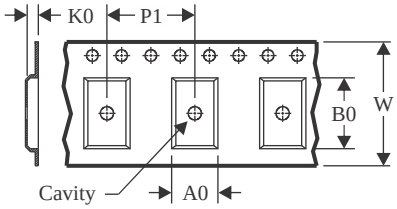
- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

TAPE AND REEL INFORMATION

REEL DIMENSIONS

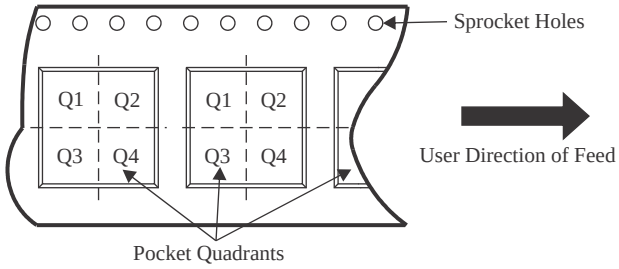


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

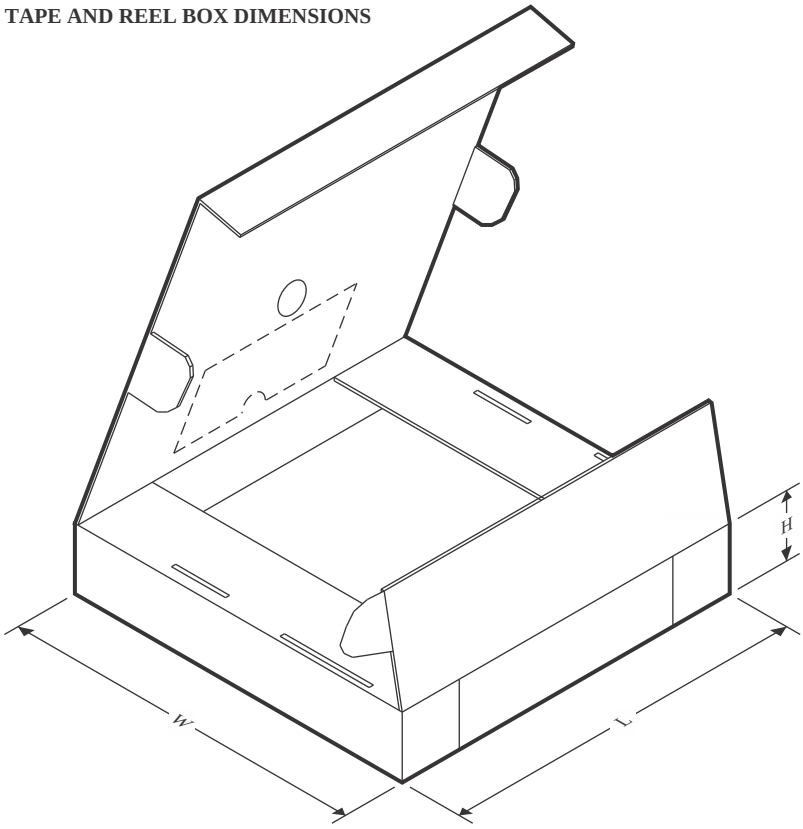
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CD40106BM96	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
CD40106BM96G4	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
CD40106BMT	SOIC	D	14	250	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
CD40106BNSR	SO	NS	14	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1
CD40106BPWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

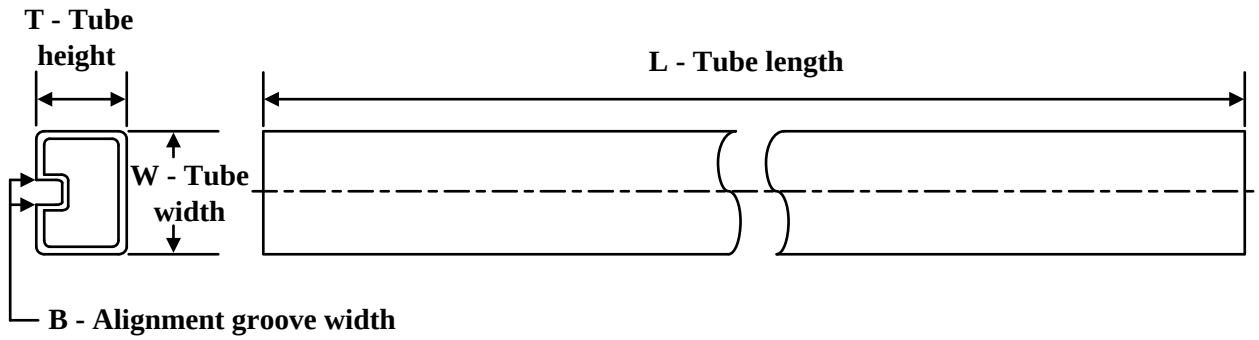
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CD40106BM96	SOIC	D	14	2500	356.0	356.0	35.0
CD40106BM96G4	SOIC	D	14	2500	356.0	356.0	35.0
CD40106BMT	SOIC	D	14	250	210.0	185.0	35.0
CD40106BNSR	SO	NS	14	2000	356.0	356.0	35.0
CD40106BPWR	TSSOP	PW	14	2000	356.0	356.0	35.0

TUBE



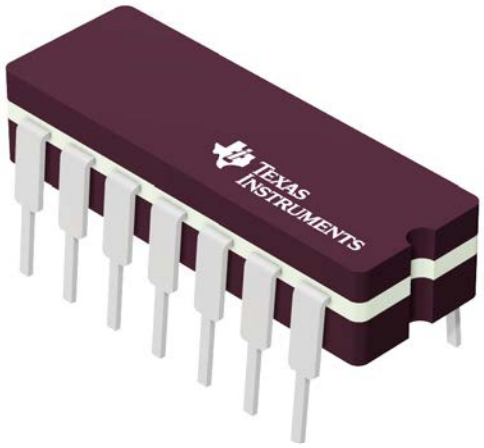
*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
CD40106BE	N	PDIP	14	25	506	13.97	11230	4.32
CD40106BE	N	PDIP	14	25	506	13.97	11230	4.32
CD40106BEE4	N	PDIP	14	25	506	13.97	11230	4.32
CD40106BEE4	N	PDIP	14	25	506	13.97	11230	4.32
CD40106BM	D	SOIC	14	50	506.6	8	3940	4.32
CD40106BMG4	D	SOIC	14	50	506.6	8	3940	4.32
CD40106BPW	PW	TSSOP	14	90	530	10.2	3600	3.5

GENERIC PACKAGE VIEW

J 14 CDIP - 5.08 mm max height

CERAMIC DUAL IN LINE PACKAGE



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

4040083-5/G

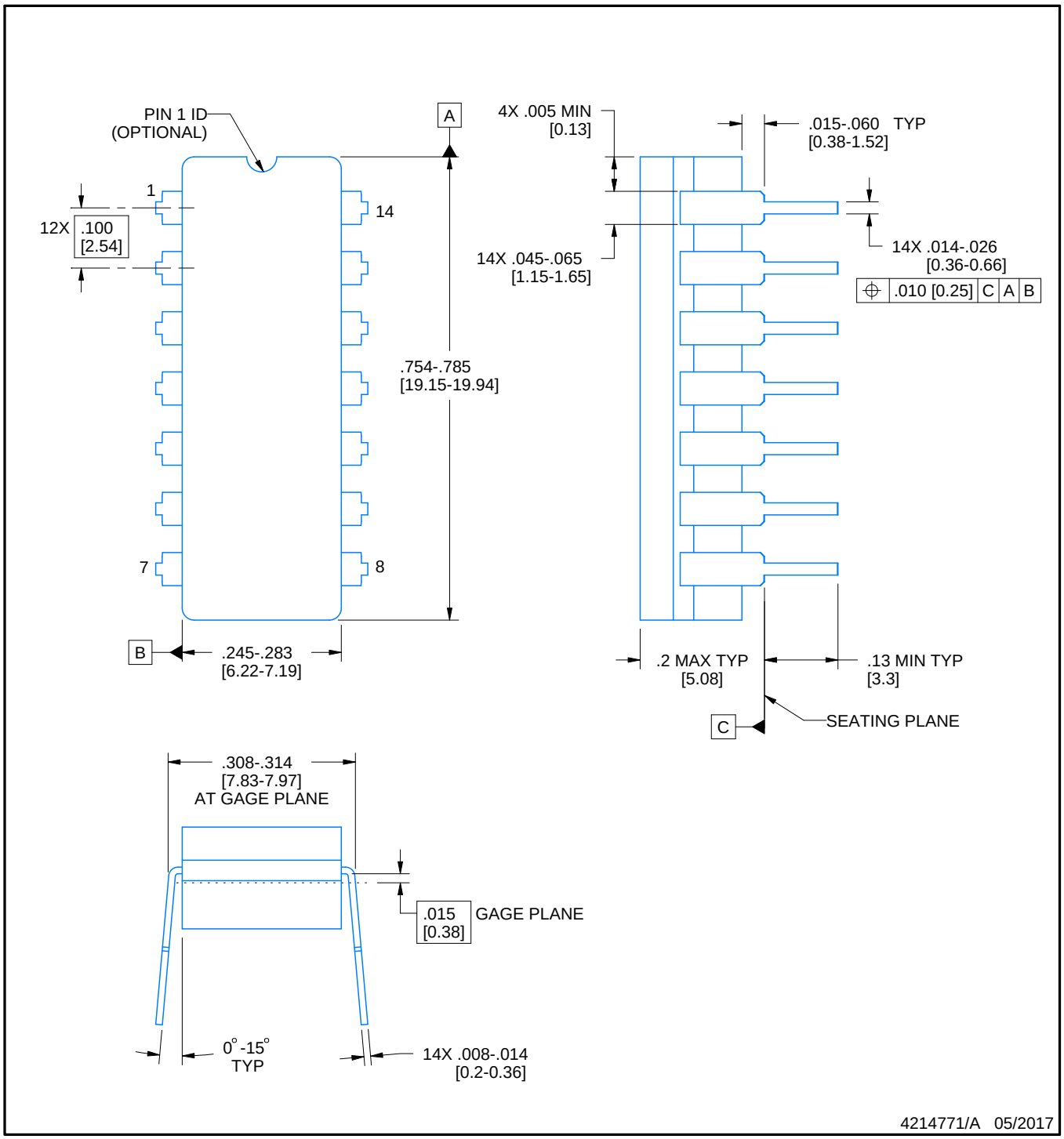


PACKAGE OUTLINE

J0014A

CDIP - 5.08 mm max height

CERAMIC DUAL IN LINE PACKAGE



NOTES:

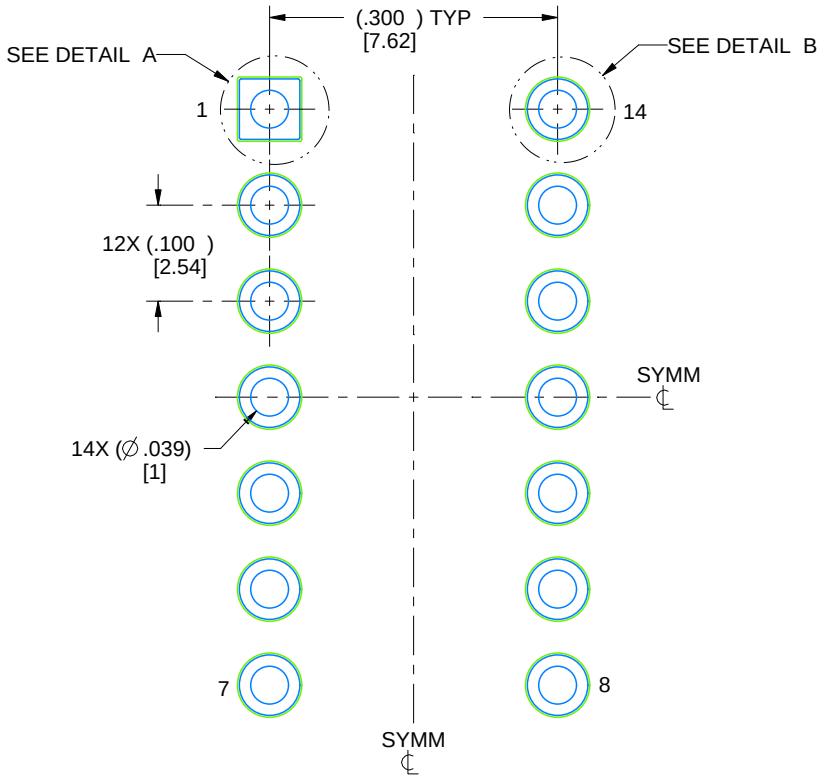
1. All controlling linear dimensions are in inches. Dimensions in brackets are in millimeters. Any dimension in brackets or parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This package is hermitically sealed with a ceramic lid using glass frit.
4. Index point is provided on cap for terminal identification only and on press ceramic glass frit seal only.
5. Falls within MIL-STD-1835 and GDIP1-T14.

EXAMPLE BOARD LAYOUT

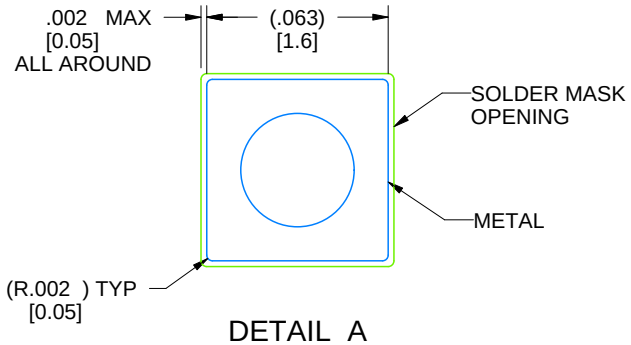
J0014A

CDIP - 5.08 mm max height

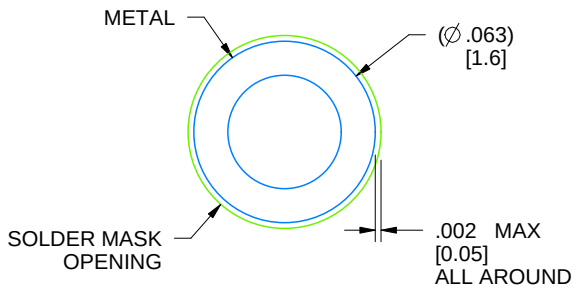
CERAMIC DUAL IN LINE PACKAGE



LAND PATTERN EXAMPLE
NON-SOLDER MASK DEFINED
SCALE: 5X



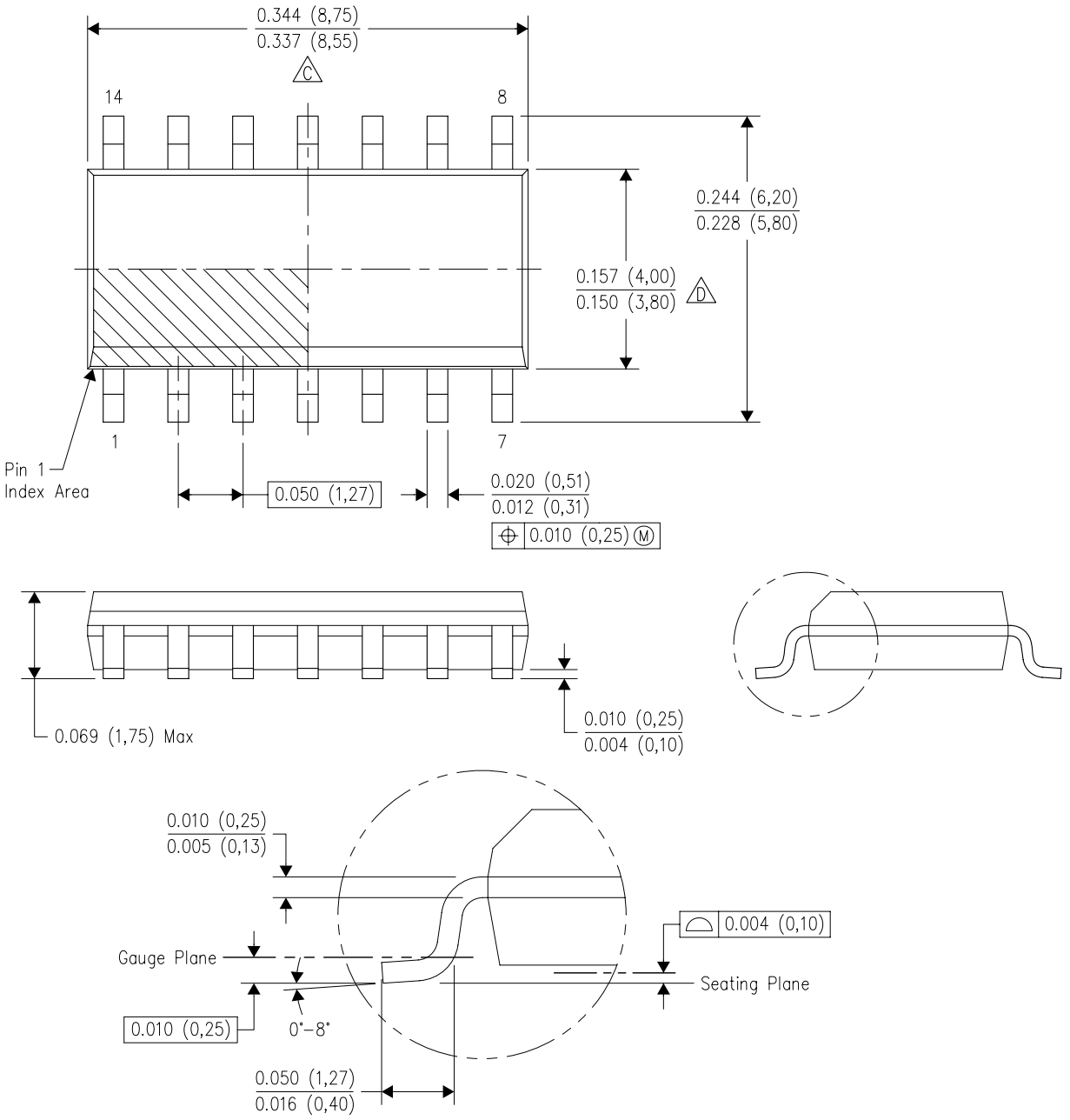
DETAIL A
SCALE: 15X



DETAIL B
13X, SCALE: 15X

4214771/A 05/2017

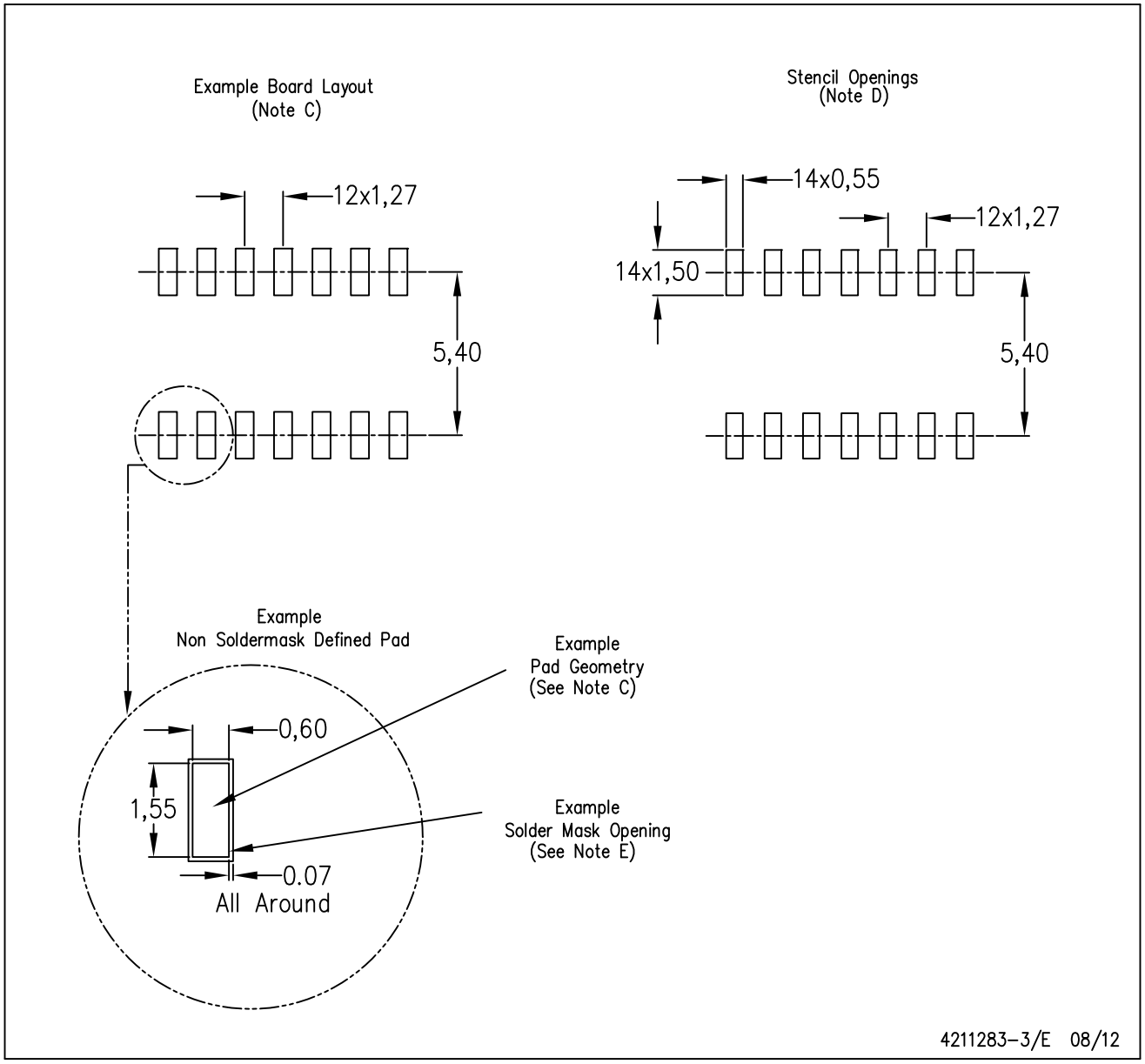
D (R–PDSO–G14) PLASTIC SMALL OUTLINE



4040047–5/M 06/11

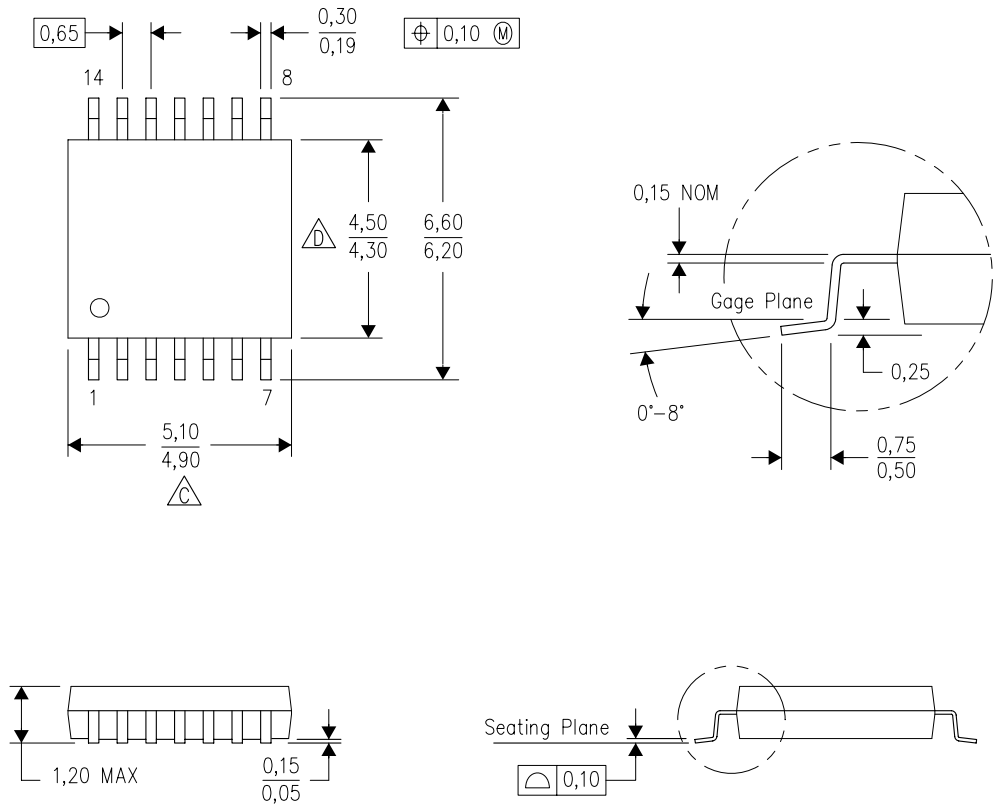
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AB.

D (R–PDSO–G14) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

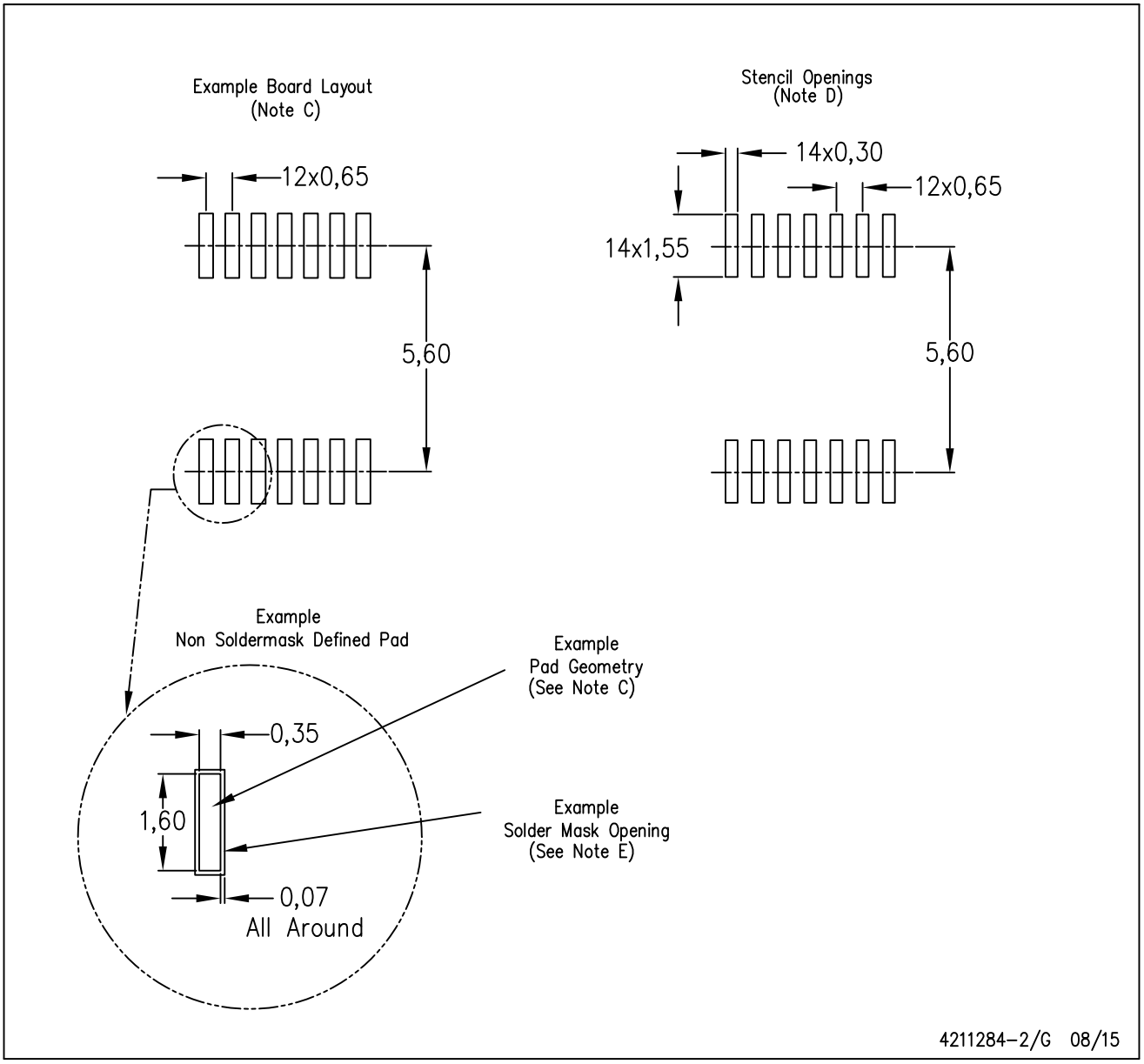
PW (R–PDSO–G14) PLASTIC SMALL OUTLINE



4040064–3/G 02/11

NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
E. Falls within JEDEC MO–153

PW (R–PDSO–G14) PLASTIC SMALL OUTLINE

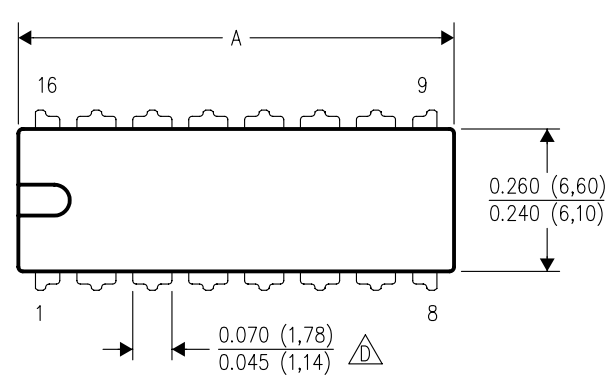


NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

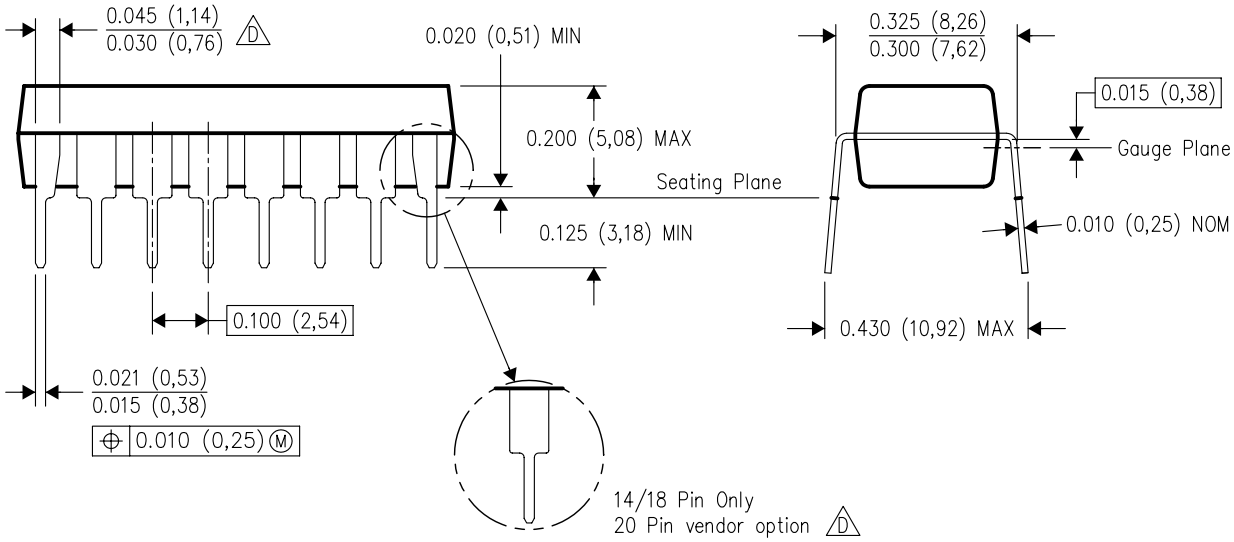
N (R–PDIP–T**)

PLASTIC DUAL–IN–LINE PACKAGE

16 PINS SHOWN



DIM \ PINS **	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS–001 VARIATION (C)	AA	BB	AC	AD



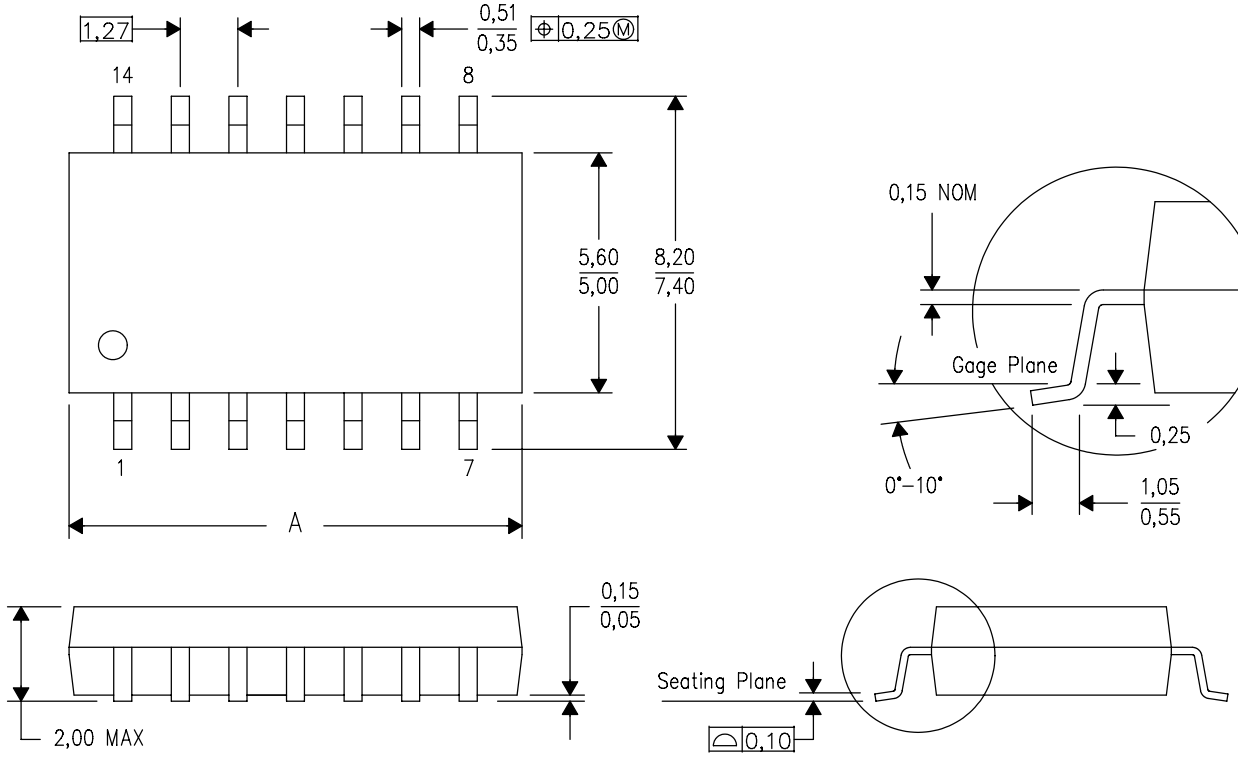
4040049/E 12/2002

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

MECHANICAL DATA

NS (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

14-PINS SHOWN



DIM \ PINS **	14	16	20	24
A MAX	10,50	10,50	12,90	15,30
A MIN	9,90	9,90	12,30	14,70

4040062/C 03/03

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

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