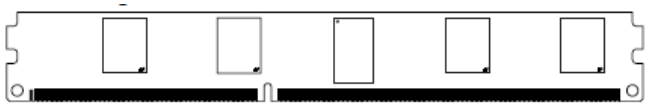
# 4GB / 8GB - WD4REV904G / WD4REV908G
# 8GB / 16GB - WD4REV808G / WD4REV816G

## Features:

- 288-pin Registered ECC for DDR4-1600, DDR4-1866, and DDR4-2133
- JEDEC standard $V_{DDL}$=1.2V (+/- 0.06V) power supply
- 4GB, 8GB and 16GB module
- Modules are built with x8 DDR4 SDRAM devices in FBGA-78 Pb-Free package
- Supports ECC error detection and correction
- Programmable CAS latency of 11, 13, and 15
- Adjustable data-output drive strength
- Bi-directional differential data strobe
- SPD (Serial Presence Detect) with EEPROM
- Fly-by topology
- All contacts are gold plated
- **ROHS compliant**

**Figure 1: Available profile**

**WD4REV904G / WDREV908G**
**Module height: 18.75mm (0.738in)**



**WD4REV808G / WD4REV816G**
**Module height: 18.75mm (0.738in)**

## Description:

The following specification covers the family of Registered ECC DDR4 modules using x8 FBGA SDRAMs. Please reference Figure 1 for available layout configurations and the product ordering guide on the final page of this specification for available options including speed grade and silicon manufacturer.

## Speed Grades:

| Speed Grade | Data Rate (MHz) | | | Clock/Data Rate | Latency | Module Speed |
|---|---|---|---|---|---|---|
| | CL11 | CL13 | CL15 | | | |
| -1600 | 1600 | - | - | 1.25ns/1600MTs | 11-11-11 | PC4-12800 |
| -1866 | 1600 | 1866 | - | 1.07ns/1866MTs | 13-13-13 | PC4-14990 |
| -2133 | 1600 | 1866 | 2133 | 0.93ns/2133MTs | 15-15-15 | PC4-17000 |

## Address Summary Table:

| | 4GB | 8GB | 8GB | 16GB |
|---|---|---|---|---|
| Module Configuration | 512M x 72 | 1024M x 72 | 1024M x 72 | 2048M x 72 |
| Device Configuration | 512M x8, 16 banks (9 components) | 1024M x8, 16 banks (9 components) | 512M x8, 16 banks (18 components) | 1024M x8, 16 banks (18 components) |
| Bank Address | BA0-BA1 | BA0-BA1 | BA0-BA1 | BA0-BA1 |
| Bank Group Address | BG0-BG1 | BG0-BG1 | BG0-BG1 | BG0-BG1 |
| Row Addressing | A0-A14 | A0-A15 | A0-A14 | A0-A15 |
| Column Addressing | A0-A9 | A0-A9 | A0-A9 | A0-A9 |
| Module rank | 1 | 1 | 2 | 2 |

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## Registered DIMM Pin Configurations

| Pin | Front | Pin | Back | Pin | Front | Pin | Back | Pin | Front | Pin | Back | Pin | Front | Pin | Back |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 1 | NC | 145 | NC | 40 | TDQS12_t, DQS12_t | 184 | VSS | 78 | EVENT_n | 222 | PARITY | 117 | DQ52 | 261 | VSS |
| 2 | VSS | 146 | VREFCA | 41 | TDQS12_c, DQS12_c | 185 | DQS3_c | 79 | A0 | 223 | VDD | 118 | VSS | 262 | DQ53 |
| 3 | DQ4 | 147 | VSS | 42 | VSS | 186 | DQS3_t | 80 | VDD | 224 | BA1 | 119 | DQ48 | 263 | VSS |
| 4 | VSS | 148 | DQ5 | 43 | DQ30 | 187 | VSS | 81 | BA0 | 225 | A10/AP | 120 | VSS | 264 | DQ49 |
| 5 | DQ0 | 149 | VSS | 44 | VSS | 188 | DQ31 | 82 | RAS_n/A16 | 226 | VDD | 121 | TDQS15_t, DQS15_t | 265 | VSS |
| 6 | VSS | 150 | DQ1 | 45 | DQ26 | 189 | VSS | 83 | VDD | 227 | RFU | 122 | TDQS15_c, DQS15_c | 266 | DQS6_c |
| 7 | TDQS9_t, DQS9_t | 151 | VSS | 46 | VSS | 190 | DQ27 | 84 | S0_n | 228 | WE_n/A14 | 123 | VSS | 267 | DQS6_t |
| 8 | TDQS9_c, DQS9_c | 152 | DQS0_c | 47 | CB4 | 191 | VSS | 85 | VDD | 229 | VDD | 124 | DQ54 | 268 | VSS |
| 9 | VSS | 153 | DQS0_t | 48 | VSS | 192 | CB5 | 86 | CAS_n/A15 | 230 | NC | 125 | VSS | 269 | DQ55 |
| 10 | DQ6 | 154 | VSS | 49 | CB0 | 193 | VSS | 87 | ODT0 | 231 | VDD | 126 | DQ50 | 270 | VSS |
| 11 | VSS | 155 | DQ7 | 50 | VSS | 194 | CB1 | 88 | VDD | 232 | A13 | 127 | VSS | 271 | DQ51 |
| 12 | DQ2 | 156 | VSS | 51 | TDQS17_t, DQS17_t | 195 | VSS | 89 | S1_n | 233 | VDD | 128 | DQ60 | 272 | VSS |
| 13 | VSS | 157 | DQ3 | 52 | TDQS17_c, DQS17_c | 196 | DQS8_c | 90 | VDD | 234 | A17 | 129 | VSS | 273 | DQ61 |
| 14 | DQ12 | 158 | VSS | 53 | VSS | 197 | DQS8_t | 91 | ODT1 | 235 | NC,C2 | 130 | DQ56 | 274 | VSS |
| 15 | VSS | 159 | DQ13 | 54 | CB6 | 198 | VSS | 92 | VDD | 236 | VDD | 131 | VSS | 275 | DQ57 |
| 16 | DQ8 | 160 | VSS | 55 | VSS | 199 | CB7 | 93 | C0,CS2_n,NC | 237 | NC,CS3_c,C1 | 132 | TDQS16_t, DQS16_t | 276 | VSS |
| 17 | VSS | 161 | DQ9 | 56 | CB2 | 200 | VSS | 94 | VSS | 238 | SA2 | 133 | TDQS16_c, DQS16_c | 277 | DQS7_c |
| 18 | TDQS10_t, DQS10_t | 162 | VSS | 57 | VSS | 201 | CB3 | 95 | DQ36 | 239 | VSS | 134 | VSS | 278 | DQS7_t |
| 19 | TDQS10_c, DQS10_c | 163 | DQS1_c | 58 | RESET_n | 202 | VSS | 96 | VSS | 240 | DQ37 | 135 | DQ62 | 279 | VSS |
| 20 | VSS | 164 | DQS1_t | 59 | VDD | 203 | CKE1 | 97 | DQ32 | 241 | VSS | 136 | VSS | 280 | DQ63 |
| 21 | DQ14 | 165 | VSS | 60 | CKE0 | 204 | VDD | 98 | VSS | 242 | DQ33 | 137 | DQ58 | 281 | VSS |
| 22 | VSS | 166 | DQ15 | 61 | VDD | 205 | RFU | 99 | TDQS13_t, DQS13_t | 243 | VSS | 138 | VSS | 282 | DQ59 |
| 23 | DQ10 | 167 | VSS | 62 | ACT_n | 206 | VDD | 100 | TDQS13_c, DQS13_c | 244 | DQS4_c | 139 | SA0 | 283 | VSS |
| 24 | VSS | 168 | DQ11 | 63 | BG0 | 207 | BG1 | 101 | VSS | 245 | DQS4_t | 140 | SA1 | 284 | VDDSPD |
| 25 | DQ20 | 169 | VSS | 64 | VDD | 208 | ALERT_n | 102 | DQ38 | 246 | VSS | 141 | SCL | 285 | SDA |
| 26 | VSS | 170 | DQ21 | 65 | A12/BC_n | 209 | VDD | 103 | VSS | 247 | DQ39 | 142 | VPP | 286 | VPP |
| 27 | DQ16 | 171 | VSS | 66 | A9 | 210 | A11 | 104 | DQ34 | 248 | VSS | 143 | VPP | 287 | VPP |
| 28 | VSS | 172 | DQ17 | 67 | VDD | 211 | A7 | 105 | VSS | 249 | DQ35 | 144 | RFU | 288 | VPP[4] |
| 29 | TDQS11_t, DQS11_t | 173 | VSS | 68 | A8 | 212 | VDD | 106 | DQ44 | 250 | VSS | | | | |
| 30 | TDQS11_c, DQS11_c | 174 | DQS2_c | 69 | A6 | 213 | A5 | 107 | VSS | 251 | DQ45 | | | | |
| 31 | VSS | 175 | DQS2_t | 70 | VDD | 214 | A4 | 108 | DQ40 | 252 | VSS | | | | |
| 32 | DQ22 | 176 | VSS | 71 | A3 | 215 | VDD | 109 | VSS | 253 | DQ41 | | | | |
| 33 | VSS | 177 | DQ23 | 72 | A1 | 216 | A2 | 110 | TDQS14_t, DQS14_t | 254 | VSS | | | | |
| 34 | DQ18 | 178 | VSS | 73 | VDD | 217 | VDD | 111 | TDQS14_c, DQS14_c | 255 | DQS5_c | | | | |
| 35 | VSS | 179 | DQ19 | 74 | CK0_t | 218 | CK1_t | 112 | VSS | 256 | DQS5_t | | | | |
| 36 | DQ28 | 180 | VSS | 75 | CK0_c | 219 | CK1_c | 113 | DQ46 | 257 | VSS | | | | |
| 37 | VSS | 181 | DQ29 | 76 | VDD | 220 | VDD | 114 | VSS | 258 | DQ47 | | | | |
| 38 | DQ24 | 182 | VSS | 77 | VTT | 221 | VTT | 115 | DQ42 | 259 | VSS | | | | |
| 39 | VSS | 183 | DQ25 | KEY | | | | 116 | VSS | 260 | DQ43 | | | | |

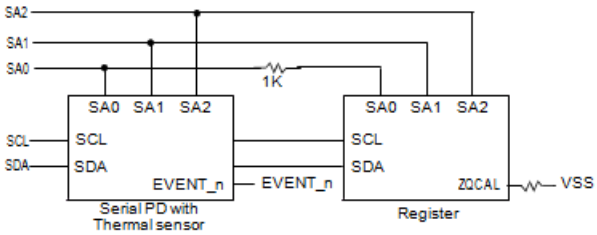

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## Pin Description

| Pin Name | Description | Pin Name | Description |
|---|---|---|---|
| A0–A17[1] | Register address input | SCL | I2C serial bus clock for SPD/TS and register |
| BA0, BA1 | Register bank select input | SDA | I2C serial bus data line for SPD/TS and register |
| BG0, BG1 | Register bank group select input | SA0–SA2 | I2C slave address select for SPD/TS and register |
| RAS_n[2] | Register row address strobe input | PAR | Register parity input |
| CAS_n[3] | Register column address strobe input | VDD | SDRAM core power supply |
| WE_n[4] | Register write enable input | VPP | SDRAM activating power supply |
| CS0_n, CS1_n, CS2_n, CS3_n | DIMM Rank Select Lines input | VREFCA | SDRAM command/address reference supply |
| CKE0, CKE1 | Register clock enable lines input | VSS | Power supply return (ground) |
| ODT0, ODT1 | Register on-die termination control lines input | VDDSPD | Serial SPD/TS positive power supply |
| ACT_n | Register input for activate input | ALERT_n | Register ALERT_n output |
| DQ0–DQ63 | DIMM memory data bus | RESET_n | Set Register and SDRAMs to a Known State |
| CB0–CB7 | DIMM ECC check bits | EVENT_n | SPD signals a thermal event has occurred |
| DQS0_t–DQS17_t | Data Buffer data strobes (positive line of differential pair) | VTT | SDRAM I/O termination supply |
| DQS0_c–DQS17_c | Data Buffer data strobes (negative line of differential pair) | RFU | Reserved for future use |
| CKO_t, CK1_t | Register clock input (positive line of differential pair) | | |
| CK0_c, CK1_c | Register clocks input (negative line of differential pair) | | |

Note:
1. Address A17 is only valid for 16GB x4 based SDRAMs
2. RAS_n is a multiplexed function with A16
3. CAS_n is a multiplexed function with A15
4. WE_n is a multiplexed function with A14

## On DIMM Thermal Sensor




## Temperature Sensor Characteristics

| Grade | Range | Temperature Sensor Accuracy | | | Units | NOTE |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| B | 75 < Ta < 95 | - | +/- 0.5 | +/- 1.0 | °C | - |
| | 40 < Ta < 125 | - | +/- 1.0 | +/- 2.0 | | - |
| | -20 < Ta < 125 | - | +/- 2.0 | +/- 3.0 | | - |
| Resolution | | 0.25 | | | °C /LSB | - |


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## Input/Output Functional Description

| Symbol | Type | Function |
|---|---|---|
| CK0_t, CK0_c, CK1_t, CK1_c | Input | Clock: CK_t and CK_c are differential clock inputs. All address and control input signals are sampled on the crossing of the positive edge of CK_t and negative edge of CK_c. |
| CKE0, CKE1 | Input | Clock Enable: CKE HIGH activates, and CKE LOW deactivates internal clock signals and device input buffers and output drivers. Taking CKE LOW provides Precharge Power-Down and Self-Refresh operation (all banks idle), or Active Power-Down (row Active in any bank). CKE is synchronous for Self-Refresh exit. After VREFCA and Internal DQ Vref have become stable during the power on and initialization sequence, they must be maintained during all operations (including Self-Refresh). CKE must be maintained high throughout read and write accesses. Input buffers, excluding CK_t, CK_c, ODT and CKE, are disabled during power-down. Input buffers, excluding CKE, are disabled during Self-Refresh. |
| CS0_n, CS1_n, CS2_n, CS3_n | Input | Chip Select: All commands are masked when CS_n is registered HIGH. CS_n provides for external Rank selection. CS_n is considered part of the command code. |
| C0, C1, C2 | Input | Chip ID: Chip ID is only used for 3DS for 2,4,8 high stack via TSV to select each slice of stacked component. Chip ID is considered part of the command code. |
| ODT0, ODT1 | Input | On Die Termination: ODT (registered HIGH) enables RTT_NOM termination resistance internal to the DDR4 SDRAM. When enabled, ODT is only applied to each DQ, DQS_t, DQS_c, TDQS_t and TDQS_c signal. The ODT pin will be ignored if MR1 is programmed to disable RTT_NOM. |
| ACT_n | Input | Activation Command Input : ACT_n defines the Activation command being entered along with CS_n. The input into RAS_n/A16, CAS_n/A15 and WE_n/A14 will be considered as Row Address A16, A15 and A14. |
| RAS_n/A16. CAS_n/A15. WE_n/A14 | Input | Command Inputs: RAS_n/A16, CAS_n/A15 and WE_n/A14 (along with CS_n) define the command being entered. Those pins have multi-function. For example, for activation with ACT_n Low, these are Addresses like A16, A15 and A14 but for non-activation command with ACT_n High, these are Command pins for Read, Write and other command defined in command truth table |
| BG0 - BG1 | Input | Bank Group Inputs: BG0 - BG1 define which bank group an Active, Read, Write or Precharge command is being applied. BG0 also determines which mode register is to be accessed during an MRS cycle. |
| BA0 - BA1 | Input | Bank Address Inputs: BA0 - BA1 define to which bank an Active, Read, Write or Precharge command is being applied. Bank address also determines which mode register is to be accessed during a MRS cycle. |
| A0 - A17 | Input | Address Inputs: Provide the row address for ACTIVATE Commands and the column address for Read/Write commands to select one location out of the memory array in the respective bank. A10/AP, A12/BC_n, RAS_n/A16, CAS_n/A15 and WE_n/A14 have additional functions. See other rows. The address inputs also provide the opcode during Mode Register Set commands. A17 is only defined for 16 Gb x4 SDRAM configurations. |
| A10 / AP | Input | Auto-precharge: A10 is sampled during Read/Write commands to determine whether Autoprecharge should be performed to the accessed bank after the Read/Write operation. (HIGH: Autoprecharge; LOW: no Autoprecharge). A10 is sampled during a Precharge command to determine whether the Precharge applies to one bank (A10 LOW) or all banks (A10 HIGH). If only one bank is to be precharged, the bank is selected by bank addresses. |
| A12 / BC_n | Input | Burst Chop: A12/BC_n is sampled during Read and Write commands to determine if burst chop (on-the fly) will be performed. (HIGH, no burst chop; LOW: burst chopped). See command truth table for details. |
| RESET_n | CMOS Input | Active Low Asynchronous Reset: Reset is active when RESET_n is LOW, and inactive when RESET_n is HIGH. RESET_n must be HIGH during normal operation. |
| DQ | Input/ Output | Data Input/ Output: Bi-directional data bus. If CRC is enabled via Mode register then CRC code is added at the end of Data Burst. Any DQ from DQ0-DQ3 may indicate the internal Vref level during test via Mode Register Setting MR4 A4=High. Refer to vendor specific data sheets to determine which DQ is used. |
| DQS0_t-DQS17_t, DQS0_c-DQS17_c | Input/ Output | Data Strobe: output with read data, input with write data. Edge-aligned with read data, centered in write data. The data strobe DQS_t is paired with differential signals DQS_c, respectively, to provide differential pair signaling to the system during reads and writes. DDR4 SDRAM supports differential data strobe only and does not support single-ended. |
| PAR | Input | Command and Address Parity Input: DDR4 Supports Even Parity check in SDRAMs with MR setting. Once it's enabled via Register in MR5, then SDRAM calculates Parity with ACT_n, RAS_n/A16, CAS_n/A15, WE_n/A14, BG0-BG1, BA0-BA1, A17-A0. Input parity should be maintained at the rising edge of the clock and at the same time with command & address with CS_n LOW |


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## Input/Output functional Description (continued)

| Symbol | Type | Function |
|---|---|---|
| ALERT_N | Output (Input) | Alert: It has multi functions such as CRC error flag, Command and Address Parity error flag as Output signal. If there is error in CRC, then ALERT_n goes LOW for the period time interval and goes back HIGH. If there is error in Command Address Parity Check, then ALERT_n goes LOW for relatively long period until ongoing SDRAM internal recovery transaction is complete. During Connectivity Test mode this pin functions as an input.<br>Using this signal or not is dependent on the system. If the SDRAM ALERT_n pins are not connected to the ALERT_n pin on the edge connector is must still be connected to VDD on DIMM. |
| RFU | | Reserved for Future Use: No on DIMM electrical connection is present |
| NC | | No Connect: No on DIMM electrical connection is present |
| VDD[1] | Supply | Power Supply: 1.2 V ± 0.06 V |
| VSS | Supply | Ground |
| VTT | Supply | VDD/2 |
| VPP | Supply | SDRAM Activating Power Supply: 2.5V ( 2.375V min, 2.75V max) |
| VDDSPD | Supply | SPD and register supply voltage. Register requires the nominal voltage to be 2.5V. |
| VREFCA | Supply | Reference voltage for CA |

Note:
1. For PC4 VDD is 1.2V. For PC4L VDD is TBD

## Registering Clock Driver Specification

## Timing and Capacitance values

| Symbol | Parameter | Conditions | $T_C$ = TBD<br>$V_{DD}$ = 1.2 ± 0.06V | | Units | Notes |
|---|---|---|---|---|---|---|
| | | | Min | Max | | |
| fclock | Input Clock Frequency | Application frequency | 625 | 1080 | MHz | |
| $t_{CH}/t_{CL}$ | Pulse duration, CK_t, CK_c HIGH or LOW | | 0.4 | - | $t_{CK}$ | |
| $t_{ACT}$ | Inputs active time4 before RESET is taken HIGH | DCKE0/1 = LOW and $\overline{DCS0/1}$ = HIGH | 16 | - | $t_{CK}$ | |
| $t_{PDM}$ | Propagation delay, single bit switching | CK_t/ CK_c to output | 1 | 1.3 | ns | |
| $t_{DIS}$ | Output disable time(1/2-Clock pre-launch) | CK_t/ CK_c to output float | 0.5*tCK + tQSK1(min) | - | $t_{CK}$ | |
| $t_{EN}$ | Output enable time(1/2-Clock pre-launch) | CK_t/ CK_c to output driving | 0.5*tCK - tQSK1(max) | - | $t_{CK}$ | |
| $C_{IN}$(DATA) | Data Input Capacitance | | 0.8 | 1.1 | pF | |
| $C_{IN}$(CLOCK) | Data Input Capacitance | | 0.8 | 1.1 | | |
| $C_{IN}$(RST) | Reset Input Capacitance | | 0.5 | 2.0 | | |


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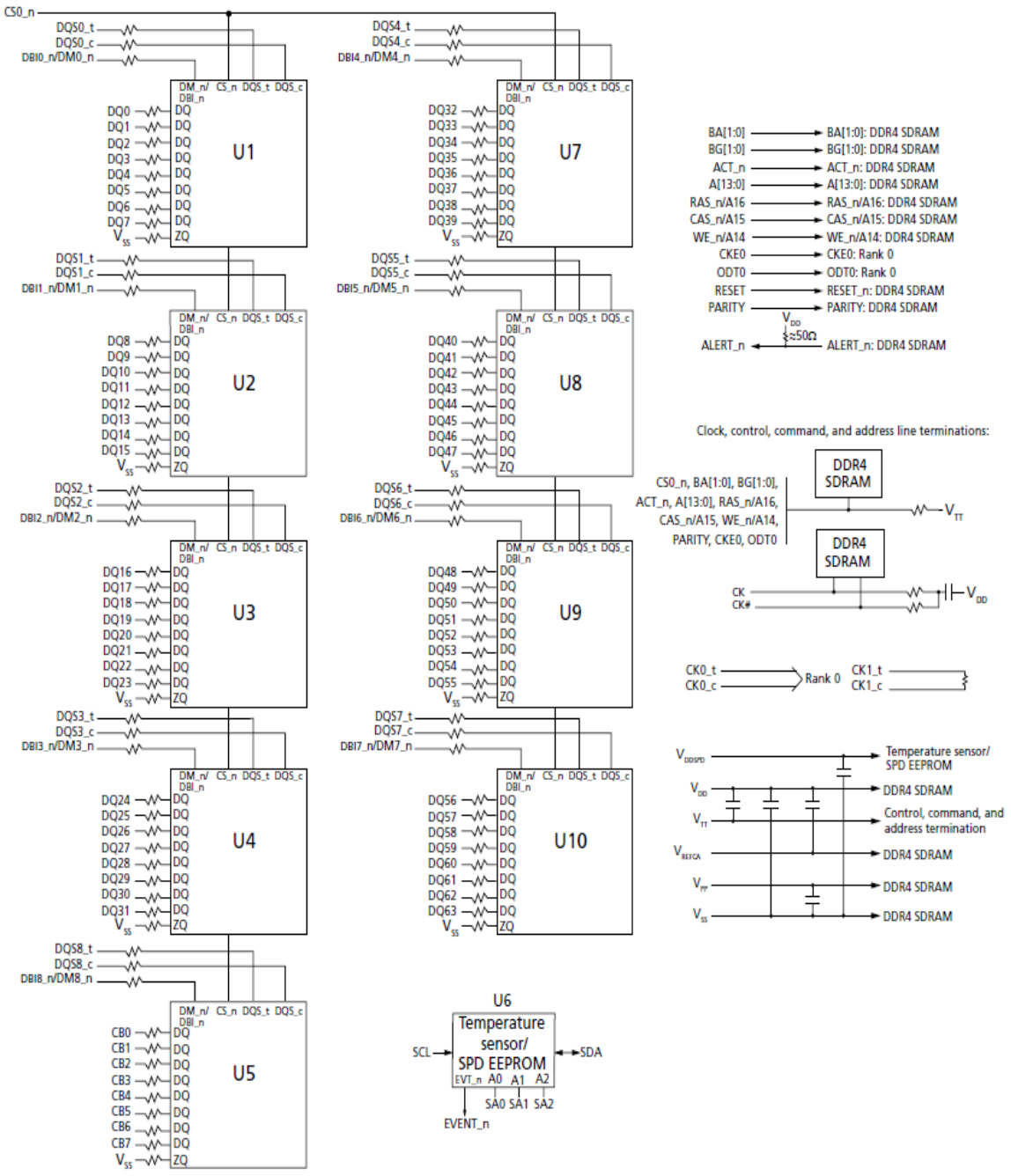
## Clock Driver Characteristics

| Symbol | Parameter | Conditions | $T_C$ = TBD<br>$V_{DD}$ = 1.2 ± 0.06V | | Units | Notes |
|---|---|---|---|---|---|---|
| | | | Min | Max | | |
| $t_{jit}$ (cc) | Cycle-to-cycle period jitter | | 0 | 0.025 x tCK | ps | |
| $t_{STAB}$ | Stabilization time | | - | 5 | us | |
| $t_{CKsk}$ | Clock Output skew | | - | 10 | ps | |
| $t_{jit}$(per) | Yn Clock Period jitter | | -0.025 * tCK | 0.025 * tCK | ps | |
| $t_{jit}$(hper) | Half period jitter | | -0.032 * tCK | 0.032 * tCK | ps | |
| $t_{Qsk1}$ | Qn Output to clock tolerance (Standard 1/2 -Clock Pre-Launch) | | -0.125 * tCK | 0.125 * tCK | ps | |
| $t_{dynoff}$ | Maximum re-driven dynamic clock off-set | | - | 50 | ps | |


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## Functional Block Diagram:

4GB 512Mx72 / 8GB 1Gx72 REG ECC DIMM (Populated as 1 rank x8 organization)

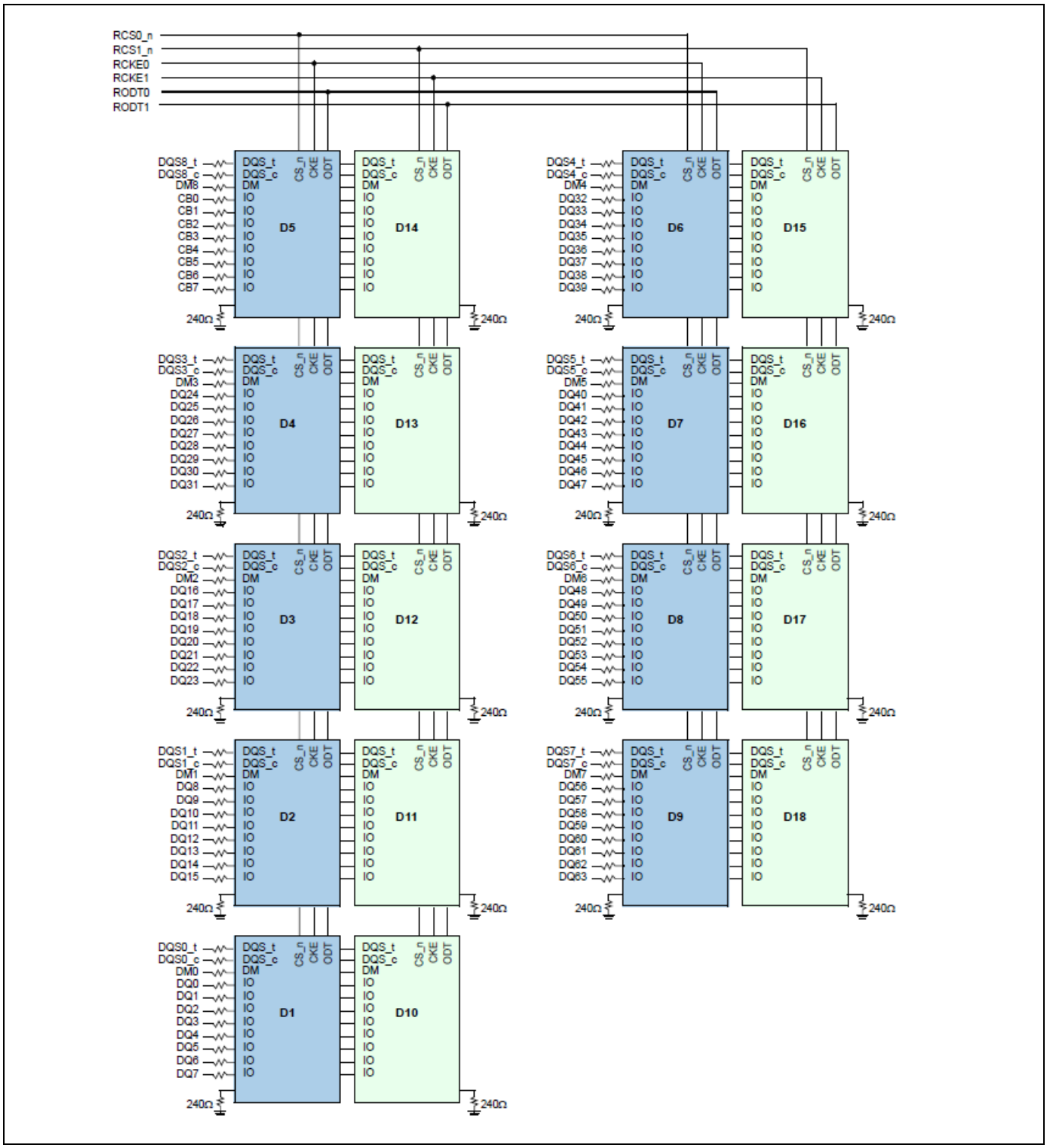



Note: 1. The ZQ ball on each DDR4 component is connected to an external 240Ω ±1% resistor that is tied to ground. It is used for the calibration of the component's ODT and output driver.


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**Functional Block Diagram:** (continued)

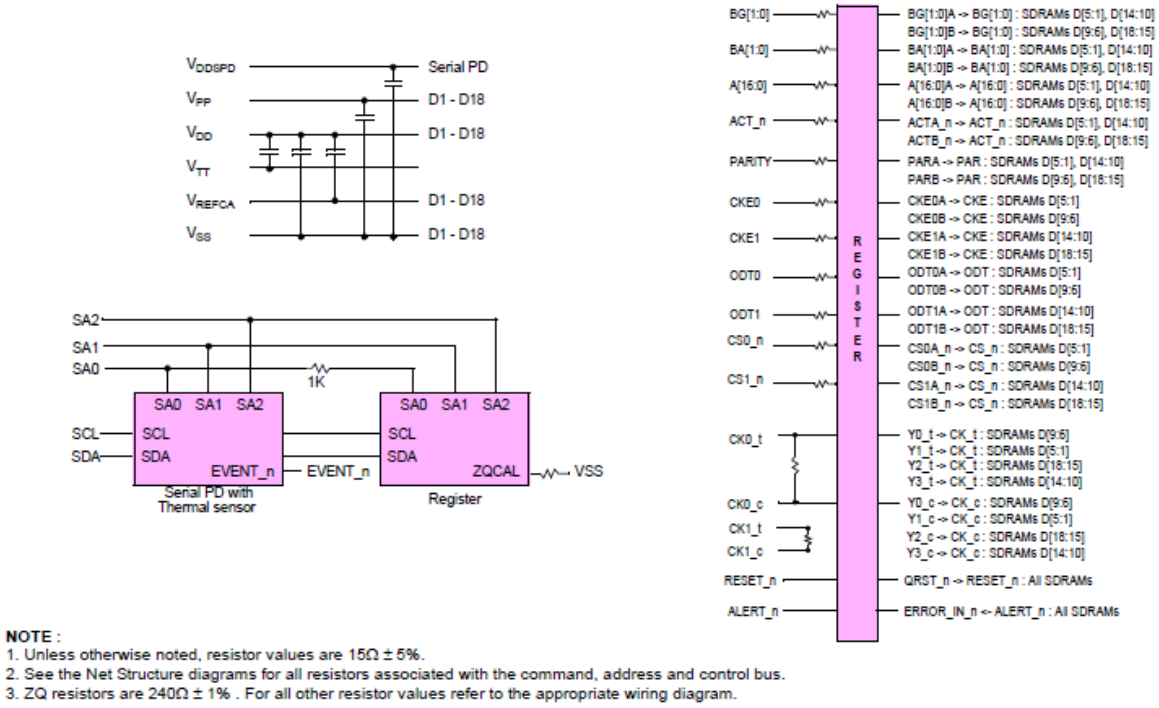
8GB 1Gx72 / 16GB 2Gx72 REG ECC DIMM (Populated as 2 rank x8 organization)





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**Functional Block Diagram:** (continued)




**NOTE** :
1. Unless otherwise noted, resistor values are 15Ω ± 5%.
2. See the Net Structure diagrams for all resistors associated with the command, address and control bus.
3. ZQ resistors are 240Ω ± 1% . For all other resistor values refer to the appropriate wiring diagram.


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## Absolute Maximum DC Ratings

| Symbol | Parameter | Min | Max | Units | Note |
|---|---|---|---|---|---|
| $V_{DD}$ | Voltage on $V_{DD}$ pin relative to $V_{SS}$ | -0.3 | 1.5 | V | 1,3 |
| $V_{DDQ}$ | Voltage on $V_{DDQ}$ relative to $V_{SS}$ | -0.3 | 1.5 | V | 1,3 |
| $V_{PP}$ | Voltage on any $V_{PP}$ pin relative to $V_{SS}$ | -0.3 | 3.0 | V | 4 |
| $V_{IN}$, $V_{OUT}$ | Voltage on any pin except VREFCA to $V_{SS}$ | -0.3 | 1.5 | V | 1 |
| $T_{STG}$ | Storage Temperature | -55 | +100 | °C | 1,2 |

Note:

1. Stress greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. Storage Temperature is the case surface temperature on the center/top side of the DRAM. For measurement conditions, please refer to JEDEC51-2 standard.
3. $V_{DD}$ and $V_{DDQ}$ must be within 300mV of each other at all times and VREFCA must not be greater than 0.6 x $V_{DDQ}$, when $V_{DD}$ and $V_{DDQ}$ are less than 500mV; VREFCA may be equal to or less than 300mV.
4. $V_{PP}$ must be equal or greater than $V_{DD}/V_{DDQ}$ at all times.

## Recommended DC Operating Conditions

| Symbol | Parameter | Min | Typical | Max | Units | Note |
|---|---|---|---|---|---|---|
| VDD | Supply Voltage | 1.14 | 1.2 | 1.26 | V | 1,2,3 |
| VDDq | Supply Voltage for Output | 1.14 | 1.2 | 1.26 | V | 1,2,3 |
| VPP | SDRAM Power Supply | 2.375 | 2.5 | 2.75 | V | 3 |

Note:

1. Under all conditions $V_{DDQ}$ must be less than or equal to $V_{DD}$.
2. $V_{DDQ}$ tracks with $V_{DD}$. AC parameters are measured with $V_{DD}$ and $V_{DDQ}$ tied together.
3. DC bandwidth is limited to 20MHz.

## AC & DC Logic Input Levels for Single Ended Signals

| Symbol | Parameter | DDR4-1600/1866/2133 | | Units | Note |
|---|---|---|---|---|---|
| | | Min | Max | | |
| $V_{IH.CA}$ (DC75) | DC Input Logic high | VREFCA +0.075 | VDD | V | |
| $V_{IL.CA}$ (DC75) | DC Input Logic low | $V_{SS}$ | VREFCA +0.075 | V | |
| $V_{IH.CA}$ (AC100) | AC Input Logic high | $V_{REF}$ + 0.1 | Note 2 | V | 1 |
| $V_{IL.CA}$ (AC100) | AC Input Logic low | Note 2 | $V_{REF}$ + 0.1 | V | 1 |
| $V_{REFCA}$(DC) | Reference Voltage for ADD, CMD inputs | 0.49*$V_{DD}$ | 0.51*$V_{DD}$ | V | 2,3 |

Note:

1. See "Overshoot and Undershoot Specifications" on section.
2. The AC peak noise on $V_{REFCA}$ may not $V_{REFCA}$ to deviate from $V_{REFCA}$(DC) by more than ± 1% $V_{DD}$ (for reference: approx. ± 12mV).
3. For reference: approx. $V_{DD}/2$ ± 12mV).

## Thermal Characteristics

| Symbol | Parameter/Condition | Value | Units | Notes |
|---|---|---|---|---|
| $T_C$ | Commercial operating case temperature | 0 to 85 | °C | 1, 2, 3 |
| $T_C$ | | >85 to 95 | °C | 1, 2, 3, 4 |
| $T_{OPER}$ | Normal operating temperature range | 0 to 85 | °C | 5 |
| $T_{OPER}$ | Extended temperature operating range (optional) | >85 to 95 | °C | 5 |


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Note:

1. Maximum operating case temperature: $T_C$ is measured in the center of the package.
2. A thermal solution must be designed to ensure the DRAM device does not exceed the maximum $T_C$ during operation.
3. Device functionality is not guaranteed if the DRAM device exceeds the maximum $T_C$ during operation.
4. If $T_C$ exceeds 85°C, the DRAM must be refreshed externally at 2X refresh, which is a 3.9µs interval refresh rate.
5. The refresh rate must double when 85°C < $T_{OPER}$ ≤ 95°C.

## AC and DC Input Measurement Levels: $V_{REF}$ Tolerances

The DC tolerance limits and ac-noise limits for the reference voltages $V_{REFCA}$ is illustrated in Figure 1. It shows a valid reference voltage $V_{REF}$ (t) as a function of time ($V_{REF}$ stands for $V_{REFCA}$).

$V_{REF}$(DC) is the linear average of $V_{REF}$(t) over a very long period of time (e.g. 1 sec). This average has to meet the min/max requirement in Table X. Furthermore $V_{REF}$(t) may temporarily deviate from $V_{REF}$(DC) by no more than ± 1% VDD.

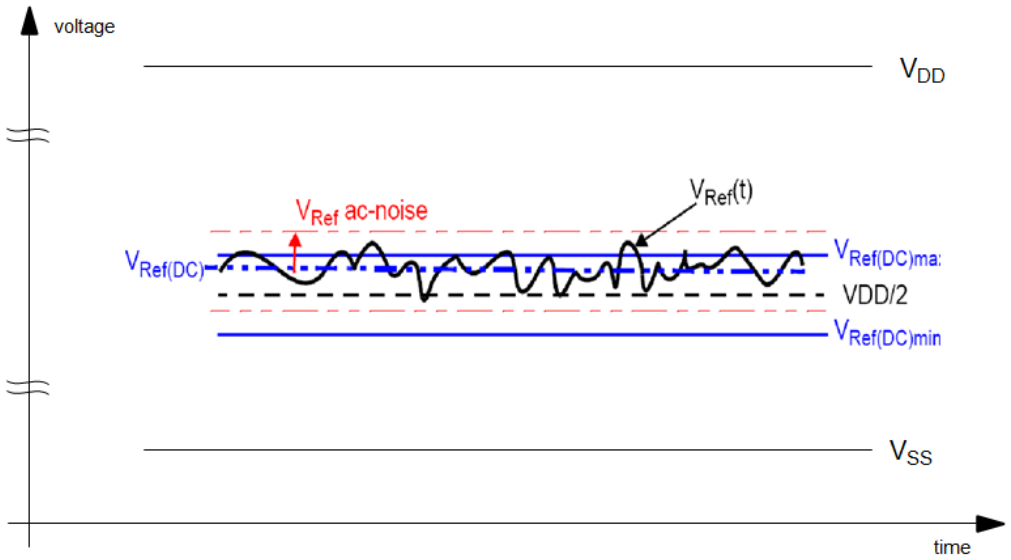



**Figure 2: Illistration for $V_{REF}$(DC) tolerance and $V_{REF}$ AC-noise limits**

The voltage levels for setup and hold time measurements $V_{IH}$(AC), $V_{IH}$(DC), $V_{IL}$(AC) and $V_{IL}$(DC) are dependent on $V_{REF}$. "$V_{REF}$" shall be understood as $V_{REF}$(DC), as defined in Figure 1.

This clarifies that DC-variations of $V_{REF}$ affect the absolute voltage a signal must reach to achieve a valid high or low level and therefore the time to which setup and hold is measured. System timing and voltage budgets need to account for $V_{REF}$(DC) deviations from the optimum position within the data-eye of the input signals.

This also clarifies that the DRAM setup/hold specification and derating values need to include time and voltage associated with $V_{REF}$ AC-noise. Timing and voltage effects due to AC-noise on $V_{REF}$ up to the specified limit (+/-1% of $V_{DD}$) are included in DRAM timings and their associated deratings.


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## AC and DC Logic Input Levels for Differential Signals

Differential Signals Definition

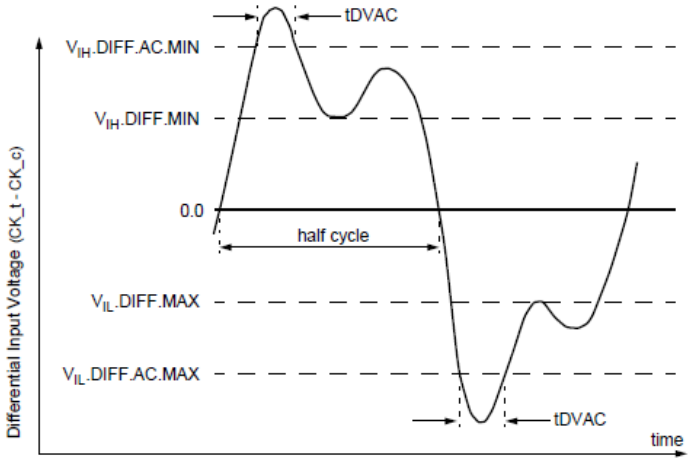



**Figure 3: Definition of differential ac-swing and 'time above ac-level" $t_{DVAC}$**

Note:

1. Differential signal rising edge from VIL.DIFF.MAX to VIH.DIFF.MIN must be monotonic slope
2. Differential signal falling edge from VIH.DIFF.MIN to VIL.DIFF.MAX must be monotonic slope

## Differential swing requirements for clock (CK_t – CK_c)

| Symbol | Parameter | DDR4-1600/1866/2133 | | Unit | Note |
|---|---|---|---|---|---|
| | | Min | Max | | |
| $V_{IHdiff}$ | differential input high | +0.150 | Note 3 | V | 1 |
| $V_{ILdiff}$ | differential input low | Note 3 | -0.150 | V | 1 |
| $V_{IHdiff}$(AC) | differential input high ac | 2 x ($V_{IH}$(AC) - $V_{REF}$) | Note 3 | V | 2 |
| $V_{IHdiff}$(AC) | differential input low ac | Note 3 | 2 x ($V_{IL}$(AC) - $V_{REF}$) | V | 2 |

Note:

1. Used to define a differential signal slew-rate.
2. For CK_t - CK_c use $V_{IH.CA}$/$V_{IL.CA}$(AC) of ADD/CMD and $V_{REFCA}$.
3. These value are not defined; however, the differential signal CK_t - CK_c, need to be written within the respective limits ($V_{IH.CA}$(DC) max, $V_{IL.CA}$(DC) for single-ended signals as well as the limitations for overshoot and undershoot.

## Allowed time before ringback (tDVAC) for CK_t – CK-c

| Slew Rate (V/ns) | tDVAC [ps] @\|$V_{IH/LDIFF}$(AC)\| = 200mV | |
|---|---|---|
| | Min | Max |
| >4.0 | 120 | - |
| 4.0 | 115 | - |
| 3.0 | 110 | - |
| 2.0 | 105 | - |
| 1.8 | 100 | - |
| 1.6 | 95 | - |
| 1.4 | 90 | - |
| 1.2 | 85 | - |
| 1.0 | 80 | - |
| <1.0 | 80 | - |


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## Electrical Characteristics and AC Timings:

### Timing Parameters by Speed Grade

| Speed | | DDR4-1600 | | DDR4-1866 | | DDR4-2133 | | Units | NOTE |
|---|---|---|---|---|---|---|---|---|---|
| Parameter | Symbol | MIN | MAX | MIN | MAX | MIN | MAX | | |
| Minimum Clock Cycle Time (DLL off mode) | tCK (DLL_OFF | 8 | - | 8 | - | 8 | - | ns | 22 |
| Average Clock Period | tCK(avg) | 1.25 | <1.5 | 1.071 | <1.25 | 0.938 | <1.071 | ns | 35,36 |
| Average high pulse width | tCH(avg) | 0.48 | 0.52 | 0.48 | 0.52 | 0.48 | 0.52 | tCK(avg) | |
| Average low pulse width | tCL(avg) | 0.48 | 0.52 | 0.48 | 0.52 | 0.48 | 0.52 | tCK(avg) | |
| Absolute Clock Period | tCK(abs) | tCK(avg)min + tJIT(per)min _ to t | tCK(avg)m ax + tJIT(per)m ax_tot | tCK(avg)min + tJIT(per)min _ to t | tCK(avg)m ax + tJIT(per)m ax_tot | tCK(avg)min + tJIT(per)min _ to t | tCK(avg)m ax + tJIT(per)m ax_tot | tCK(avg) | |
| Absolute clock HIGH pulse width | tCH(abs) | 0.45 | - | 0.45 | - | 0.45 | - | tCK(avg) | 23 |
| Absolute clock LOW pulse width | tCL(abs) | 0.45 | - | 0.45 | - | 0.45 | - | tCK(avg) | 24 |
| Clock Period Jitter- total | JIT(per)_tot | -63 | 63 | -54 | 54 | -47 | 47 | ps | 23 |
| Clock Period Jitter- deterministic | JIT(per)_dj | -31 | 31 | -27 | 27 | -23 | 23 | ps | 26 |
| Clock Period Jitter during DLL locking period | tJIT(per, lck) | -50 | 50 | -43 | 43 | -38 | 38 | ps | |
| Cycle to Cycle Period Jitter | JIT(cc)_total | 125 | | 107 | | 94 | | ps | 25 |
| Cycle to Cycle Period Jitter deterministic | tJIT(cc)_dj | 63 | | 54 | | 47 | | ps | 26 |
| Cycle to Cycle Period Jitter during DLL locking period | tJIT(cc, lck) | 100 | | 86 | | 75 | | ps | |
| Duty Cycle Jitter | tJIT(duty) | TBD | TBD | TBD | TBD | TBD | TBD | ps | |
| Cumulative error across 2 cycles | tERR(2per) | -92 | 92 | -79 | 79 | -69 | 69 | ps | |
| Cumulative error across 3 cycles | tERR(3per) | -109 | 109 | -94 | 94 | -82 | 82 | ps | |
| Cumulative error across 4 cycles | tERR(4per) | -121 | 121 | -104 | 104 | -91 | 91 | ps | |
| Cumulative error across 5 cycles | tERR(5per) | -131 | 131 | -112 | 112 | -98 | 98 | ps | |
| Cumulative error across 6 cycles | tERR(6per) | -139 | 139 | -119 | 119 | -104 | 104 | ps | |
| Cumulative error across 7 cycles | tERR(7per) | -145 | 145 | -124 | 124 | -109 | 109 | ps | |
| Cumulative error across 8 cycles | tERR(8per) | -151 | 151 | -129 | 129 | -113 | 113 | ps | |
| Cumulative error across 9 cycles | tERR(9per) | -156 | 156 | -134 | 134 | -117 | 117 | ps | |
| Cumulative error across 10 cycles | tERR(10per) | -160 | 160 | -137 | 137 | -120 | 120 | ps | |
| Cumulative error across 11 cycles | tERR(11per) | -164 | 164 | -141 | 141 | -123 | 123 | ps | |
| Cumulative error across 12 cycles | tERR(12per) | -168 | 168 | -144 | 144 | -126 | 126 | ps | |
| Cumulative error across 13 cycles | tERR(13per) | -172 | 172 | -147 | 147 | -129 | 129 | ps | |
| Cumulative error across 14 cycles | tERR(14per) | -175 | 175 | -150 | 150 | -131 | 131 | ps | |
| Cumulative error across 15 cycles | tERR(15per) | -178 | 178 | -152 | 152 | -133 | 133 | ps | |
| Cumulative error across 16 cycles | tERR(16per) | -180 | 189 | -155 | 155 | -135 | 135 | ps | |
| Cumulative error across 17 cycles | tERR(17per) | -183 | 183 | -157 | 157 | -137 | 137 | ps | |
| Cumulative error across 18 cycles | tERR(18per) | -185 | 185 | -159 | 159 | -139 | 139 | ps | |
| Cumulative error across n = 13, 14 . . . 49, 50 cycles | tERR(nper) | $^{t}$ERR(nper)min = ((1 + 0.68ln(n)) * $^{t}$JIT(per)_total min)<br>$^{t}$ERR(nper)max = ((1 + 0.68ln(n)) * $^{t}$JIT(per)_total max) | | | | | | ps | |
| Command and Address setup time to CK_t, CK_c referenced to Vih(ac) / Vil(ac) levels | tIS(base) | 115 | - | 100 | - | 80 | - | ps | |
| Command and Address setup time to CK_t, CK_c referenced to Vref levels | tIS(Vref) | 215 | - | 200 | - | 180 | - | ps | |
| Command and Address hold time to CK_t, CK_c referenced to Vih(dc) / Vil(dc) levels | tIH(base) | 140 | - | 125 | - | 105 | - | ps | |
| Command and Address hold time to CK_t, CK_c referenced to Vref levels | tIH(Vref) | 215 | - | 200 | - | 180 | - | ps | |
| Control and Address Input pulse width for each input | tIPW | 600 | - | 525 | - | 460 | - | ps | |


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| Speed | | DDR4-1600 | | DDR4-1866 | | DDR4-2133 | | Units | NOTE |
|---|---|---|---|---|---|---|---|---|---|
| Parameter | Symbol | MIN | MAX | MIN | MAX | MIN | MAX | | |
| CAS_n to CAS_n command delay for same bank group | tCCD_L | 5 | - | 5 | - | 6 | - | nCK | 34 |
| CAS_n to CAS_n command delay for different bank group | tCCD_S | 4 | - | 4 | - | 4 | - | nCK | 34 |
| ACTIVATE to ACTIVATE Command delay to different bank group for 2KB page size | tRRD_S(2K) | Max(4nCK,6ns) | - | Max(4nCK,5.3ns) | - | Max(4nCK,5.3ns) | - | nCK | 34 |
| ACTIVATE to ACTIVATE Command delay to different bank group for 2KB page size | tRRD_S(1K) | Max(4nCK,5ns) | - | Max(4nCK,4.2ns) | - | Max(4nCK,3.7ns) | - | nCK | 34 |
| ACTIVATE to ACTIVATE Command delay to different bank group for 1/2KB page size | tRRD_S(1/2K) | Max(4nCK,5ns) | - | Max(4nCK,4.2ns) | - | Max(4nCK,3.7ns) | - | nCK | 34 |
| ACTIVATE to ACTIVATE Command delay to same bank group for 2KB page size | tRRD_L(2K) | Max(4nCK,7.5ns) | - | Max(4nCK,6.4ns) | - | Max(4nCK,6.4ns) | - | nCK | 34 |
| ACTIVATE to ACTIVATE Command delay to same bank group for 1KB page size | tRRD_L(1K) | Max(4nCK,6ns) | - | Max(4nCK,5.3ns) | - | Max(4nCK,5.3ns) | - | nCK | 34 |
| ACTIVATE to ACTIVATE Command delay to same bank group for 1/2KB page size | tRRD_L(1/2K) | Max(4nCK,6ns) | - | Max(4nCK,5.3ns) | - | Max(4nCK,5.3ns) | - | nCK | 34 |
| Four activate window for 2KB page size | tFAW_2K | Max(28nCK,35ns) | - | Max(28nCK,30ns) | - | Max(28nCK,30ns) | - | ns | 34 |
| Four activate window for 1KB page size | tFAW_1K | Max(20nCK,25ns) | - | Max(20nCK,23ns) | - | Max(20nCK,21ns) | - | ns | 34 |
| Four activate window for 1/2KB page size | tFAW_1/2K | Max(16nCK,20ns) | - | Max(16nCK,17ns) | - | Max(16nCK,15ns) | - | ns | 34 |
| Delay from start of internal write transaction to internal read command for different bank group | tWTR_S | max(2nCK,2.5ns) | - | max(2nCK,2.5ns) | - | max(2nCK,2.5ns) | - | | 1,2,34 |
| Delay from start of internal write transaction to internal read command for same bank group | tWTR_L | max(4nCK,7.5ns) | - | max(4nCK,7.5ns) | - | max(4nCK,7.5ns) | - | | 1,34 |
| Internal READ Command to PRECHARGE Command delay | tRTP | max(4nCK,7.5ns) | - | max(4nCK,7.5ns) | - | max(4nCK,7.5ns) | - | | |
| WRITE recovery time | tWR | 15 | - | 15 | - | 15 | - | ns | 1 |
| Write recovery time when CRC and DM are enabled | tWR_CRC_DM | tWR+max (4nCK,3.75ns) | - | tWR+max (5nCK,3.75ns) | - | tWR+max (5nCK,3.75s) | - | ns | 1, 28 |
| delay from start of internal write transaction to internal read command for different bank group with both CRC and DM enabled | tWTR_SCRC_DM | tWTR_S+max (4nCK,3.75ns) | - | tWTR_S+max (5nCK,3.75ns) | - | tWTR_S+max (5nCK,3.75ns) | - | ns | 2, 29, 34 |
| delay from start of internal write transaction to internal read command for same bank group with both CRC and DM enabled | tWTR_LCRC_DM | tWTR_L+max (4nCK,3.75ns) | - | tWTR_L+max (5nCK,3.75ns) | - | tWTR_L+max (5nCK,3.75ns) | - | ns | 3,30, 34 |
| DLL locking time | tDLLK | 597 | - | 597 | - | 768 | - | nCK | |
| Mode Register Set command cycle time | tMRD | 8 | - | 8 | - | 8 | - | nCK | |
| Mode Register Set command update delay | tMOD | max(24nCK,15ns) | - | max(24nCK,1 5ns) | - | max(24nCK,15ns) | - | | |
| Multi-Purpose Register Recovery Time | tMPRR | 1 | - | 1 | - | 1 | - | nCK | 33 |
| Multi-Purpose Register Write Recovery Time | tWR_MPR | tMOD (min) + AL + PL | - | tMOD (min) + AL + PL | - | tMOD (min) + AL + PL | - | - | |
| Auto precharge write recovery + precharge time | tDAL(min) | Programmed WR + roundup ( tRP / tCK(avg)) | | | | | | nCK | |
| CS_n to Command Address Latency | tCAL | 3 | - | 4 | - | 4 | - | nCK | |
| DQS_t,DQS_c to DQ skew, per group, per access | tDQSQ | - | TBD | - | TBD | - | TBD | tCK(avg)/2 | 13,18 |
| DQS_t,DQS_c to DQ Skew deterministic, per group, per access | tDQSQ | - | TBD | - | TBD | - | TBD | tCK(avg)/2 | 14,16,18 |
| DQ output hold time from DQS_t,DQS_c | tQH | TBD | - | TBD | - | TBD | - | tCK(avg)/2 | 13,17,18 |
| DQ output hold time deterministic from DQS_t, DQS_c | tQH | TBD | - | TBD | - | TBD | - | UI | 14,16.18 |


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| Speed | | DDR4-1600 | | DDR4-1866 | | DDR4-2133 | | Units | NOTE |
|---|---|---|---|---|---|---|---|---|---|
| Parameter | Symbol | MIN | MAX | MIN | MAX | MIN | MAX | | |
| DQS_t,DQS_c to DQ Skew total, per group, per access; DBI enabled | tDQSQ | - | TBD | - | TBD | - | TBD | UI | 13,19 |
| DQ output hold time total from DQS_t, DQS_c; DBI enabled | tQH | TBD | - | TBD | - | TBD | - | UI | 13,19 |
| DQ to DQ offset , per group, per access referenced to DQS_t, | tDQSQ | TBD | TBD | TBD | TBD | TBD | TBD | UI | 15,16 |
| DQS_t, DQS_c differential READ Pre-amble (2 clock preamble) | tRPRE | 0.9 | TBD | 0.9 | TBD | 0.9 | TBD | tCK | |
| DQS_t, DQS_c differential READ Postamble | tRPST | TBD | TBD | TBD | TBD | TBD | TBD | tCK | |
| DQS_t,DQS_c differential output high time | tQSH | 0.4 | - | 0.4 | - | 0.4 | - | tCK | 21 |
| DQS_t,DQS_c differential output low time | tQSL | 0.4 | - | 0.4 | - | 0.4 | - | tCK | 20 |
| DQS_t, DQS_c differential WRITE Preamble | tWPRE | 0.9 | - | 0.9 | - | 0.9 | - | tCK | |
| DQS_t, DQS_c differential WRITE Postamble | tWPST | TBD | TBD | TBD | TBD | TBD | TBD | tCK | |
| DQS_t and DQS_c low-impedance time (Referenced from RL-1) | tLZ(DQS) | -450 | 225 | -390 | 195 | -360 | 180 | ps | |
| DQS_t and DQS_c high-impedance time (Referenced from RL+BL/2) | tHZ(DQS) | - | 225 | - | 195 | - | 180 | ps | |
| DQS_t, DQS_c differential input low pulse width | tDQSL | 0.46 | 0.54 | 0.46 | 0.54 | 0.46 | 0.54 | tCK | |
| DQS_t, DQS_c differential input high pulse width | tDQSH | 0.46 | 0.54 | 0.46 | 0.54 | 0.46 | 0.54 | tCK | |
| DQS_t, DQS_c rising edge to CK_t, CK_c rising edge (1 clock | tDQSS | -0.27 | 0.27 | -0.27 | 0.27 | -0.27 | 0.27 | tCK | |
| DQS_t, DQS_c falling edge setup time to CK_t, CK_c rising edge | tDSS | 0.18 | - | 0.18 | - | 0.18 | - | tCK | |
| DQS_t, DQS_c falling edge hold time from CK_t, CK_c rising edge | tDSH | 0.18 | - | 0.18 | - | 0.18 | - | tCK | |
| Command path disable delay upon MPSM entry | tMPED | tMOD(min) + tCPDED(min) | - | tMOD(min) + tCPDED(min) | - | tMOD(min) + tCPDED(min) | - | | |
| Valid clock requirement after MPSM entry | tCKMPE | tMOD(min) + tCPDED(min) | - | tMOD(min) + tCPDED(min) | - | tMOD(min) + tCPDED(min) | - | | |
| Valid clock requirement before MPSM exit | tCKMPX | tCKSRX(min) | | tCKSRX(min) | | tCKSRX(min) | | | |
| Exit MPSM to commands not requiring a locked DLL | tXMP | TBD | | TBD | | TBD | | | |
| Exit MPSM to commands requiring a locked DLL | tXMPDLL | tXMP(min) + tXSDLL(min) | | tXMP(min) + tXSDLL(min) | | tXMP(min) + tXSDLL(min) | | | |
| CS setup time to CKE | tMPX_S | TBD | - | TBD | - | TBD | - | | |
| CS hold time to CKE | tMPX_H | TBD | - | TBD | - | TBD | - | | |
| Power-up and RESET calibration time | tZQinit | 1024 | - | 1024 | - | 1024 | - | nCK | |
| Normal operation Full calibration time | tZQoper | 512 | - | 512 | - | 512 | - | nCK | |
| Normal operation Short calibration time | tZQCS | 128 | - | 128 | - | 128 | - | nCK | |
| Exit Reset from CKE HIGH to a valid command | tXPR | max (5nCK,tRFC(min) + 10ns) | - | max (5nCK,tRFC (min)+ 10ns) | - | max (5nCK,tRFC (min)+ 10ns) | - | | |
| Exit Self Refresh to commands not requiring a locked DLL | tXS | tRFC(min)+1 0ns | - | tRFC(min)+1 0ns | - | tRFC(min)+ 1 0ns | - | | |
| SRX to commands not requiring a locked DLL in Self Refresh ABORT | tXS_ABORT (min) | tRFC4(min)+ 10ns | - | tRFC4(min) + 10ns | - | tRFC4(min) + 10ns | - | | |
| Exit Self Refresh to ZQCL,ZQCS and MRS (CL,CWL,WR,RTP and Gear Down) | tXS_FAST (min) | tRFC4(min)+ 10ns | - | tRFC4(min) + 10ns | - | tRFC4(min) + 10ns | - | | |
| Exit Self Refresh to commands requiring a locked DLL | tXSDLL | tDLLK(min) | - | tDLLK(min) | - | tDLLK(min) | - | | |


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| Speed | | DDR4-1600 | | DDR4-1866 | | DDR4-2133 | | Units | NOTE |
|---|---|---|---|---|---|---|---|---|---|
| Parameter | Symbol | MIN | MAX | MIN | MAX | MIN | MAX | | |
| Minimum CKE low width for Self-refresh entry to exit timing | tCKESR | tCKE(min)+1 nCK | - | tCKE(min)+1 nCK | - | tCKE(min)+1 nCK | - | | |
| Minimum CKE low width for Self-refresh entry to exit timing with CA Pari- ty enabled | tCKESR_ PAR | tCKE(min)+ 1nCK+PL | - | tCKE(min)+ 1nCK+PL | - | tCKE(min)+ 1nCK+PL | - | | |
| Valid Clock Requirement after Self Refresh Entry (SRE) or Power-Down Entry (PDE) | tCKSRE | max(5nCK,10 ns) | - | max(5nCK,10 ns) | - | max(5nCK,10 ns) | - | | |
| Valid Clock Requirement after Self Refresh Entry (SRE) or Power-Down when CA Parity is enabled | tCKSRE_PA R | max (5nCK,10ns) +PL | - | max (5nCK,10ns) +PL | - | max (5nCK,10ns) +PL | - | | |
| Valid Clock Requirement before Self Refresh Exit (SRX) or Power-Down Exit (PDX) or Reset Exit | tCKSRX | max(5nCK,10 ns) | - | max(5nCK,10 ns) | - | max(5nCK,10 ns) | - | | |
| Exit Power Down with DLL on to any valid command; Exit Precharge Power Down with DLL frozen to commands not requiring a locked | tXP | max (4nCK,6ns) | - | max (4nCK,6ns) | - | max (4nCK,6ns) | - | | |
| CKE minimum pulse width | tCKE | max (3nCK, 5ns) | - | max (3nCK, 5ns) | - | max (3nCK, 5ns) | - | | 31,32 |
| Command pass disable delay | tCPDED | 4 | - | 4 | - | 4 | - | nCK | |
| Power Down Entry to Exit Timing | tPD | tCKE(min) | 9*tREFI | tCKE(min) | 9*tREFI | tCKE(min) | 9*tREFI | | 6 |
| Timing of ACT command to Power Down entry | tACTPDEN | 1 | - | 1 | - | 2 | - | nCK | 7 |
| Timing of PRE or PREA command to Power Down entry | tPRPDEN | 1 | - | 1 | - | 2 | - | nCK | 7 |
| Timing of RD/RDA command to Power Down entry | tRDPDEN | RL+4+1 | - | RL+4+1 | - | RL+4+1 | - | nCK | |
| Timing of WR command to Power Down entry (BL8OTF, BL8MRS, BC4OTF) | tWRPDEN | WL+4+(tWR/ tCK(avg)) | - | WL+4+(tWR/ tCK(avg)) | - | WL+4+(tWR/ tCK(avg)) | - | nCK | 4 |
| Timing of WRA command to Power Down entry (BL8OTF, BL8MRS, BC4OTF) | tWRAPDEN | WL+4+WR+1 | - | WL+4+WR+1 | - | WL+4+WR+1 | - | nCK | 5 |
| Timing of WR command to Power Down entry (BC4MRS) | tWRPBC4D EN | WL+2+(tWR/ tCK(avg)) | - | WL+2+(tWR/ tCK(avg)) | - | WL+2+(tWR/ tCK(avg)) | - | nCK | 4 |
| Timing of WRA command to Power Down entry (BC4MRS) | tWRAPBC4 DEN | WL+2+WR+1 | - | WL+2+WR+1 | - | WL+2+WR+1 | - | nCK | 5 |
| Timing of REF command to Power Down entry | tREFPDEN | 1 | - | 1 | - | 2 | - | nCK | 7 |
| Timing of MRS command to Power Down entry | tMRSPDEN | tMOD(min) | - | tMOD(min) | - | tMOD(min) | - | | |
| Mode Register Set command cycle time in PDA mode | tMRD_PDA | max(16nCK,1 0ns) | | max(16nCK,1 0ns) | | max(16nCK,1 0ns) | | | |
| Mode Register Set command update delay in PDA mode | tMOD_PDA | tMOD | | tMOD | | tMOD | | | |
| Asynchronous RTT turn-on delay (Power-Down with DLL frozen) | tAONAS | 1.0 | 9.0 | 1.0 | 9.0 | 1.0 | 9.0 | ns | |
| Asynchronous RTT turn-off delay (Power-Down with DLL frozen) | tAOFAS | 1.0 | 9.0 | 1.0 | 9.0 | 1.0 | 9.0 | ns | |
| RTT dynamic change skew | tADC | 0.3 | 0.7 | 0.3 | 0.7 | 0.3 | 0.7 | tCK(avg) | |
| First DQS_t/DQS_n rising edge after write leveling mode is programmed | tWLMRD | 40 | - | 40 | - | 40 | - | nCK | 12 |
| DQS_t/DQS_n delay after write leveling mode is programmed | tWLDQSEN | 25 | - | 25 | - | 25 | - | nCK | 12 |
| Write leveling setup time from rising CK_t, CK_c crossing to rising DQS_t/ DQS_n crossing | tWLS | 0.13 | - | 0.13 | - | 0.13 | - | tCK(avg) | |
| Write leveling hold time from rising DQS_t/DQS_n crossing to rising CK_t, CK_ crossing | tWLH | 0.13 | - | 0.13 | - | 0.13 | - | tCK(avg) | |
| Write leveling output delay | tWLO | 0 | 9.5 | 0 | 9.5 | 0 | 9.5 | ns | |
| Write leveling output error | tWLOE | | | | | | | ns | |


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| Speed | | DDR4-1600 | | DDR4-1866 | | DDR4-2133 | | Units | NOTE |
|---|---|---|---|---|---|---|---|---|---|
| Parameter | Symbol | MIN | MAX | MIN | MAX | MIN | MAX | | |
| Commands not guaranteed to be executed during this time | tPAR_UNKNOWN | - | PL | - | PL | - | PL | | |
| Delay from errant command to ALERT_n assertion | tPAR_ALERT_ON | - | PL+6ns | - | PL+6ns | - | PL+6ns | | |
| Pulse width of ALERT_n signal when asserted | tPAR_ALERT_PW | 48 | 96 | 56 | 112 | 64 | 128 | nCK | |
| Time from when Alert is asserted till controller must start providing DES commands in Persistent CA parity mode | tPAR_ALERT_RSP | - | 43 | - | 50 | - | 57 | nCK | |
| Parity Latency | PL | 4 | | 4 | | 4 | | nCK | |
| CRC error to ALERT_n latency | tCRC_ALERT | 3 | 13 | 3 | 13 | 3 | 13 | ns | |
| CRC ALERT_n pulse width | CRC_ALERT_PW | 6 | 10 | 6 | 10 | 6 | 10 | nCK | |
| tRFC1 (min) | 2Gb | 160 | - | 160 | - | 160 | - | ns | 34 |
| | 4Gb | 260 | - | 260 | - | 260 | - | ns | 34 |
| | 8Gb | 350 | - | 350 | - | 350 | - | ns | 34 |
| | 16Gb | TBD | - | TBD | - | TBD | - | ns | 34 |
| tRFC2 (min) | 2Gb | 110 | - | 110 | - | 110 | - | ns | 34 |
| | 4Gb | 160 | - | 160 | - | 160 | - | ns | 34 |
| | 8Gb | 260 | - | 260 | - | 260 | - | ns | 34 |
| | 16Gb | TBD | - | TBD | - | TBD | - | ns | 34 |
| tRFC4 (min) | 2Gb | 90 | - | 90 | - | 90 | - | ns | 34 |
| | 4Gb | 110 | - | 110 | - | 110 | - | ns | 34 |
| | 8Gb | 160 | - | 160 | - | 160 | - | ns | 34 |
| | 16Gb | TBD | - | TBD | - | TBD | - | ns | 34 |

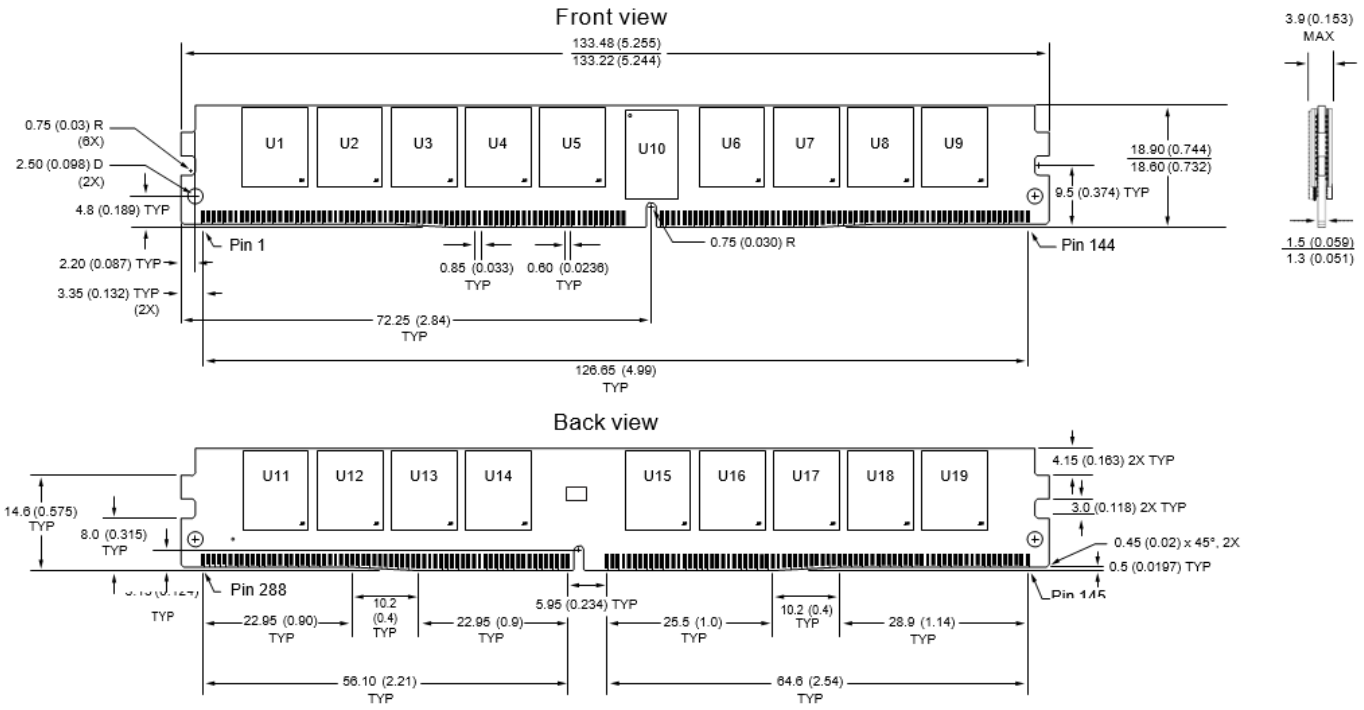
Note:

1. Start of internal write transaction is defined as follows :
   For BL8 (Fixed by MRS and on-the-fly) : Rising clock edge 4 clock cycles after WL. For BC4 (on-the-fly) : Rising clock edge 4 clock cycles after WL.
   For BC4 (fixed by MRS) : Rising clock edge 2 clock cycles after WL.
2. A separate timing parameter will cover the delay from write to read when CRC and DM are simultaneously enabled
3. Commands requiring a locked DLL are: READ (and RAP) and synchronous ODT commands.
4. tWR is defined in ns, for calculation of tWRPDEN it is necessary to round up tWR/tCK to the next integer.
5. WR in clock cycles as programmed in MR0.
6. tREFI depends on TOPER.
7. CKE can be registered low while operations such as row activation, precharge, autoprecharge or refresh are in progress, but power down IDD spec will not be applied until finishing those operations.
8. For these parameters, the DDR4 SDRAM device supports tnPARAM[nCK]=RU{tPARAM[ns]/tCK(avg)[ns]}, which is in clock cycles assuming all input clock jitter specifications are satisfied
9. When CRC and DM are both enabled, tWR_CRC_DM is used in place of tWR.
10. When CRC and DM are both enabled tWTR_S_CRC_DM is used in place of tWTR_S.
11. When CRC and DM are both enabled tWTR_L_CRC_DM is used in place of tWTR_L.
12. The max values are system dependent.
13. DQ to DQS total timing per group where the total includes the sum of deterministic and random timing terms for a specified BER. BER spec and measurement method are tbd.
14. The deterministic component of the total timing. Measurement method tbd.
15. DQ to DQ static offset relative to strobe per group. Measurement method tbd.
16. This parameter will be characterized and guaranteed by design.
17 When the device is operated with the input clock jitter, this parameter needs to be derated by the actual tjit(per)_total of the input clock. (output deratings are relative to the SDRAM input clock). Example tbd.
18. DRAM DBI mode is off.
19. DRAM DBI mode is enabled. Applicable to x8 and x16 DRAM only.
20. tQSL describes the instantaneous differential output low pulse width on DQS_t - DQS_c, as measured from on falling edge to the next consecutive rising edge
21. tQSH describes the instantaneous differential output high pulse width on DQS_t - DQS_c, as measured from on falling edge to the next consecutive rising edge
22. There is no maximum cycle time limit besides the need to satisfy the refresh interval tREFI
23. tCH(abs) is the absolute instantaneous clock high pulse width, as measured from one rising edge to the following falling edge
24. tCL(abs) is the absolute instantaneous clock low pulse width, as measured from one falling edge to the following rising edge
25. Total jitter includes the sum of deterministic and random jitter terms for a specified BER. BER target and measurement method are tbd.
26. The deterministic jitter component out of the total jitter. This parameter is characterized and guaranteed by design.
27. This parameter must be even number of clocks


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28. When CRC and DM are both enabled, tWR_CRC_DM is used in place of tWR.
29. When CRC and DM are both enabled tWTR_S_CRC_DM is used in place of tWTR_S.
30. When CRC and DM are both enabled tWTR_L_CRC_DM is used in place of tWTR_L.
31. After CKE is registered LOW, CKE signal level shall be maintained below VILDC for tCKE specification ( Low pulse width ).
32. After CKE is registered HIGH, CKE signal level shall be maintained above VIHDC for tCKE specification ( HIGH pulse width ).
33. Defined between end of MPR read burst and MRS which reloads MPR or disables MPR function.
34. Parameters apply from tCK(avg)min to tCK(avg)max at all standard JEDEC clock period values as stated in the Speed Bin Tables.
35. This parameter must keep consistency with Speed-Bin Tables shown in section 10.
36. DDR4-1600 AC timing apply if DRAM operates at lower than 1600 MT/s data rate. UI=tCK(avg).min/2

**Physical Dimensions:**




Notes: 1. All dimensions are in millimeters (inches); MAX/MIN or typical (TYP) where noted.
2. The dimensional diagram is for reference only.


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## Ordering Guide:

*DDR4-1600, 1866, 2133, x8, Registered ECC VLP DIMM*

**WD4REV** $\mathcal{V}\,\mathcal{WWW}\,\mathcal{XX}\,\mathcal{Y}\,\mathcal{Zz}$ - $\mathcal{AAA}$

| | |
|---|---|
| W | Wintec |
| D4 | 1.2V DDR4 SDRAM |
| REV | Registered ECC, 288-pin VLP DIMM<br>Very Low Profile (0.738" / 18.75mm height) |

| $\mathcal{V}$ # DRAM IC | | $\mathcal{WWW}$ | | $\mathcal{XX}$ Speed | |
|---|---|---|---|---|---|
| 8 | 18 | 04G | 4GB | 18 | 1866 |
| 9 | 9 | 08G | 8GB | 21 | 2133 |
| | | 16G | 16GB | | |

| $\mathcal{Y}$ Register | | $\mathcal{Zz}$ DRAM | | Die | |
|---|---|---|---|---|---|
| M | Montage | S | Samsung | A | A-Die |
| I | Inphi | M | Micron | B | B-Die |
| | | | | C | C-Die |
| | | | | D | D-Die |
| | | | | E | E-Die |

| Capacity | Part Number | Module Speed | DRAM Configuration | Components | Rank |
|---|---|---|---|---|---|
| 4GB | WD4REV904G21MSE | 2133@CL15 | 512Mx8 | 9 | 1 |
| 8GB | WD4REV908G21MSC | 2133@CL15 | 1Gx8 | 9 | 1 |
| 8GB | WD4REV808G21MSE | 2133@CL15 | 512Mx8 | 18 | 2 |
| 16GB | WD4REV816G21MSC | 2133@CL15 | 1G x8 | 18 | 2 |

**Orderable Example:**

WD4REV904G21MSE
288-Pin DDR4 4GB 1.2V 512Mx8 2133MTs @ CL15 REG ECC DIMM 1.23"

WD4REV908G21MSC
288-Pin DDR4 8GB 1.2V 1024Mx8 2133MTs @ CL15 REG ECC DIMM 1.23"

WD4REV816G21MSC
288-Pin DDR4 16GB 1.2V 1024Mx8 2133MTs @ CL15 REG ECC DIMM 1.23"


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## Revision History:

Revision 2.00
- Initial Release

Revision 2.01
- Corrected part number on page 1

Revision 2.02
- Updated contact information

Revision 2.03
- Put in placeholder for 1Rx8 dimensions

Revision 2.04
- 1Rx8 dimensions

Revision 2.05
- Added 1Rx8 capacities and configurations

Revision 2.06
- Cleaned up document
- Added Operating Temperature

Revision 2.07
- Added C-die

## About Wintec Industries, Inc.

Wintec, founded in 1988, is headquartered in Newark, California. Wintec, a leading third-party memory module manufacturer, specializes in a variety of module design and manufacturing, such as memory module, flash module, Handspring module, modem module, game module, etc. Besides a complete line of DDR, SDR, and EDO/FPM legacy memory modules, Wintec also distribute CPU, motherboard, peripherals, PC software, and consumer Flash products (such as MMC, SD, SMC, Compact Flash, PC Card, etc.). With excellent design engineering and manufacturing capability, Wintec provides a wide range of design and manufacturing services for our valuable customers from concept design to final product delivery. Wintec is ISO9001-certified.

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