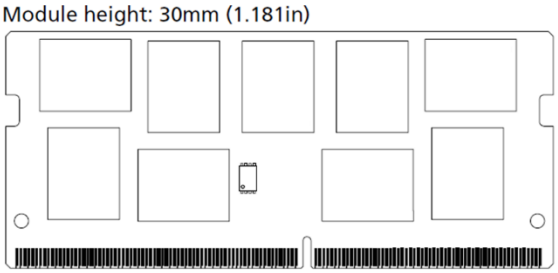
4GB - WD4SE9004G
8GB - WD4SE8008G / WD4SE9008G
16GB - WD4SE8016G

Features:

- 260-pin SODIMM Unbuffered ECC for DDR4-1866, DDR4-2133, DDR4-2400, and DDR4-2666
- JEDEC standard V_{DDL}=1.2V (+/- 0.06V) power supply
- 4GB, 8GB and 16GB modules
- Modules are built with x8 DDR4 SDRAM devices in FBGA-78 Pb-Free package
- Supports ECC error detection and correction
- Programmable CAS latency of 13, 15, 17 and 19
- Adjustable data-output drive strength
- Bi-directional differential data strobe
- SPD (Serial Presence Detect) with EEPROM
- Fly-by topology
- All contacts are gold plated
- Halogen Free
- **ROHS compliant**

Figure 1: Available profile

Standard:



Description:

The following specification covers the family of DDR4 Unbuffered ECC SODIMM modules using x8 FBGA SDRAMs. Please reference Figure 1 for available layout configurations and the product ordering guide on the final page of this specification for available options including speed grade and silicon manufacturer.

Speed Grades:

Speed Grade	Data Rate (MHz)				Clock/Data Rate	Latency	Module Speed
	CL13	CL15	CL17	CL19			
-1866	1866	-	-	-	1.07ns/1866MTs	13-13-13	PC4-14990
-2133	1866	2133	-	-	0.93ns/2133MTs	15-15-15	PC4-17000
-2400	1866	2133	2400	-	0.83ns/2400MTs	17-17-17	PC4-19200
-2666	1866	2133	2400	2666	0.75ns/2666MTs	19-19-19	PC4-21300

Address Summary Table:

	4GB	8GB	8GB	16GB
Device Configuration	4Gb 512M x 8, 16 banks (9 components)	8Gb 1024M x 8, 16 banks (9 components)	4Gb 512M x 8, 16 banks (18 components)	8Gb 1024M x 8, 16 banks (18 components)
Device bank group address	4 BG[1:0]	4 BG[1:0]	4 BG[1:0]	4 BG[1:0]
Device bank address per group	4 BA[1:0]	4 BA[1:0]	4 BA[1:0]	4 BA[1:0]
Row Addressing	A0-A14	A0-A15	A0-A14	A0-A15
Column Addressing	A0-A9	A0-A9	A0-A9	A0-A9
Module rank address	CS_n[1:0]	CS_n[1:0]	CS_n[1:0]	CS_n[1:0]
Module rank	1	1	2	2

***Specifications are for reference purposes only and are subject to change by Wintec without notice.**

Wintec Industries, Inc., reserves the right to change datasheets and/or products without any notice.
© 2020 Wintec Industries, Inc.

260-Pin x72 SODIMM Pin Configuration:

260-Pin DDR4 SODIMM Front								260-Pin DDR4 SODIMM Back							
Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol
1	V_{SS}	67	DQ29	133	A1	199	DM5_n/ BI5_n	2	V_{SS}	68	V_{SS}	134	EVENT_n, NF	200	DQS5_t
3	DQ5	69	V_{SS}	135	V_{DD}	201	V_{SS}	4	DQ4	70	DQ24	136	V_{DD}	202	V_{SS}
5	V_{SS}	71	DQ25	137	CK0_t	203	DQ46	6	V_{SS}	72	V_{SS}	138	CK1_t/NF	204	DQ47
7	DQ1	73	V_{SS}	139	CK0_c	205	V_{SS}	8	DQ0	74	DQS3_c	140	CK1_c/NF	206	V_{SS}
9	V_{SS}	75	DM3_n / BI3_n	141	V_{DD}	207	DQ42	10	V_{SS}	76	DQS3_t	142	V_{DD}	208	DQ43
11	DQS0_c	77	V_{SS}	143	PARITY	209	V_{SS}	12	DM0_n/ BI0_n	78	V_{SS}	144	A0	210	V_{SS}
13	DQS0_t	79	DQ30	145	BA1	211	DQ52	14	V_{SS}	80	DQ31	146	A10/AP	212	DQ53
15	V_{SS}	81	V_{SS}	147	V_{DD}	213	V_{SS}	16	DQ6	82	V_{SS}	148	V_{DD}	214	V_{SS}
17	DQ7	83	DQ26	149	CS0_n	215	DQ49	18	V_{SS}	84	DQ27	150	BA0	216	DQ48
19	V_{SS}	85	V_{SS}	151	WE_n/ A14	217	V_{SS}	20	DQ2	86	V_{SS}	152	RAS_n/ A16	218	V_{SS}
21	DQ3	87	CB5/NC	153	V_{DD}	219	DQS6_c	22	V_{SS}	88	CB4/NC	154	V_{DD}	220	DM6_n/ DBI6_n
23	V_{SS}	89	V_{SS}	155	ODT0	221	DQS6_t	24	DQ12	90	V_{SS}	156	CAS_n/ A15	222	V_{SS}
25	DQ13	91	CB1/NC	157	CS1_n	223	V_{SS}	26	V_{SS}	92	CB0/NC	158	A13	224	DQ54
27	V_{SS}	93	V_{SS}	159	V_{DD}	225	DQ55	28	DQ8	94	V_{SS}	160	V_{DD}	226	V_{SS}
29	DQ9	95	DQS8_c	161	ODT1	227	V_{SS}	30	V_{SS}	96	DM8_n/ DBI_n/NC	162	C0/ CS2_n/NC	228	DQ50
31	V_{SS}	97	DQS8_t	163	V_{DD}	229	DQ51	32	DQS1_c	98	V_{SS}	164	V_{REFCA}	230	V_{SS}
33	DM1_n/ DBI_n	99	V_{SS}	165	C1, CS3_n, NC	231	V_{SS}	34	DQS1_t	100	CB6/NC	166	SA2	232	DQ60
35	V_{SS}	101	CB2/NC	167	V_{SS}	233	DQ61	36	V_{SS}	102	V_{SS}	168	V_{SS}	234	V_{SS}
37	DQ15	103	V_{SS}	169	DQ37	235	V_{SS}	38	DQ14	104	CB7/NC	170	DQ36	236	DQ57
39	V_{SS}	105	CB3/NC	171	V_{SS}	237	DQ56	40	V_{SS}	106	V_{SS}	172	V_{SS}	238	V_{SS}
41	DQ10	107	V_{SS}	173	DQ33	239	V_{SS}	42	DQ11	108	RESET_n	174	DQ32	240	DQS7_c
43	V_{SS}	109	CKE0	175	V_{SS}	241	DM7_n/ DBI7_	44	V_{SS}	110	CKE1	176	V_{SS}	242	DQS7_t
45	DQ21	111	V_{DD}	177	DQS4_c	243	V_{SS}	46	DQ20	112	V_{DD}	178	DM4_n/ DBI4_n	244	V_{SS}
47	V_{SS}	113	BG1	179	DQS4_t	245	DQ62	48	V_{SS}	114	ACT_n	180	V_{SS}	246	DQ63
49	DQ17	115	BG0	181	V_{SS}	247	V_{SS}	50	DQ16	116	ALERT_n	182	DQ39	248	V_{SS}
51	V_{SS}	117	V_{DD}	183	DQ38	249	DQ58	52	V_{SS}	118	V_{DD}	184	V_{SS}	250	DQ59
53	DQS2_c	119	A12	185	V_{SS}	251	V_{SS}	54	DM2_n/ DBI2_n	120	A11	186	DQ35	252	V_{SS}
55	DQS2_t	121	A9	187	DQ34	253	SCL	56	V_{SS}	122	A7	188	V_{SS}	254	SDA
57	V_{SS}	123	V_{DD}	189	V_{SS}	255	V_{DDSPD}	58	DQ22	124	V_{DD}	190	DQ45	256	SA0
59	DQ23	125	A8	191	DQ44	257	V_{PP}	60	V_{SS}	126	A5	192	V_{SS}	258	V_{TT}
61	V_{SS}	127	A6	193	V_{SS}	259	V_{PP}	62	DQ18	128	A4	194	DQ41	260	SA1
63	DQ19	129	V_{DD}	195	DQ40	–	–	64	V_{SS}	130	V_{DD}	196	V_{SS}	–	–
65	V_{SS}	131	A3	197	V_{SS}	–	–	66	DQ28	132	A2	198	DQS5_c	–	–

Wintec Industries, Inc., reserves the right to change datasheets and/or products without any notice.
© 2020 Wintec Industries, Inc.

Pin Descriptions

The pin description table below is a comprehensive list of all possible pins for DD4 modules. All pins listed may not be supported on this module. See functional Block Diagram for pins specific to this module.

Symbol	Type	Description
Ax	Input	**Address inputs:** Provide the row address for ACTIVATE commands and the column address for READ/WRITE commands in order to select one location out of the memory array in the respective bank. (A10/AP, A12/BC_n, WE_n/A14, CAS_n/A15, and RAS_n/A16 have additional functions; see individual entries in this table.) The address inputs also provide the opcode during the MODE REGISTER SET command. A17 is only defined for x4 SDRAM.
A10/AP	Input	**Auto precharge:** A10 is sampled during READ and WRITE commands to determine whether an auto precharge should be performed on the accessed bank after a READ or WRITE operation. (HIGH = auto precharge; LOW = no auto precharge.) A10 is sam- pled during a PRECHARGE command to determine whether the precharge applies to one bank (A10 LOW) or all banks (A10 HIGH). If only one bank is to be precharged, the bank is selected by the bank group and bank addresses.
A12/BC_n	Input	**Burst chop:** A12/BC_n is sampled during READ and WRITE commands to determine if burst chop (on-the-fly) will be performed. (HIGH = no burst chop; LOW = burst-chop- ped.) See Command Truth Table in the DDR4 component data sheet.
ACT_n	Input	**Command input:** ACT_n defines the ACTIVATE command being entered along with CS_n. The input into RAS_n/A16, CAS_n/A15, and WE_n/A14 are considered as row ad- dress A16, A15, and A14. See Command Truth Table.
BAx	Input	**Bank address inputs:** Define the bank (with a bank group) to which an ACTIVATE, READ, WRITE, or PRECHARGE command is being applied. Also determine which mode register is to be accessed during a MODE REGISTER SET command.
BGx	Input	**Bank group address inputs:** Define the bank group to which a REFRESH, ACTIVATE, READ, WRITE, or PRECHARGE command is being applied. Also determine which mode register is to be accessed during a MODE REGISTER SET command. BG[1:0] are used in the x4 and x8 configurations. x16-based SDRAM only has BG0.
C0, C1, C2 (RDIMM/LRDIMM only)	Input	**Chip ID:** These inputs are used only when devices are stacked; that is, 2H, 4H, and 8H stacks for x4 and x8 configurations using through-silicon vias (TSVs). These pins are not used in the x16 configuration. Some DDR4 modules support a traditional DDP package, which uses CS1_n, CKE1, and ODT1 to control the second die. All other stack configurations, such as a 4H or 8H, are assumed to be single-load (master/slave) type configurations where C0, C1, and C2 are used as chip ID selects in conjunction with a single CS_n, CKE, and ODT. Chip ID is considered part of the command code.
CKx_t CKx_c	Input	**Clock:** Differential clock inputs. All address, command, and control input signals are sampled on the crossing of the positive edge of CK_t and the negative edge of CK_c.
CKEx	Input	**Clock enable:** CKE HIGH activates, and CKE LOW deactivates the internal clock signals, device input buffers, and output drivers. Taking CKE LOW provides PRECHARGE POWER-DOWN and SELF REFRESH operations (all banks idle), or active power-down (row active in any bank). CKE is asynchronous for self-refresh exit. After V_{REFCA} has be- come stable during the power-on and initialization sequence, it must be maintained during all operations (including SELF REFRESH). CKE must be maintained HIGH throughout read and write accesses. Input buffers (excluding CK_t, CK_c, ODT, RE- SET_n, and CKE) are disabled during power-down. Input buffers (excluding CKE and RESET#) are disabled during self-refresh.

Wintec Industries, Inc., reserves the right to change datasheets and/or products without any notice.
© 2020 Wintec Industries, Inc.

Pin Descriptions (continued)

Symbol	Type	Description
CSx_n	Input	**Chip select:** All commands are masked when CS_n is registered HIGH. CS_n provides external rank selection on systems with multiple ranks. CS_n is considered part of the command code. (CS2_n and CS3_n are not used on UDIMMs.)
ODTx	Input	**On-die termination:** ODT (registered HIGH) enables termination resistance internal to the DDR4 SDRAM. When enabled, ODT (R_{TT}) is applied only to each DQ, DQS_t, DQS_c, DM_n/DBI_n/TDQS_t, and TDQS_c signal for x4 and x8 configurations (when the TDQS function is enabled via the mode register). For the x16 configuration, R_{TT} is applied to each DQ, DQSU_t, DQSU_c, DQSL_t, DQSL_c, UDM_n, and LDM_n signal. The ODT pin will be ignored if the mode registers are programmed to disable R_{TT}.
PARITY	Input	**Parity for command and address:** This function can be enabled or disabled via the mode register. When enabled in MR5, the DRAM calculates parity with ACT_n, RAS_n/ A16, CAS_n/A15, WE_n/A14, BG[1:0], BA[1:0], A[16:0]. Input parity should be maintained at the rising edge of the clock and at the same time as command and address with CS_n LOW.
RAS_n/A16 CAS_n/A15 WE_n/A14	Input	**Command inputs:** RAS_n/A16, CAS_n/A15, and WE_n/A14 (along with CS_n) define the command and/or address being entered and have multiple functions. For example, for activation with ACT_n LOW, these are addresses like A16, A15, and A14, but for a non-activation command with ACT_n HIGH, these are command pins for READ, WRITE, and other commands defined in Command Truth Table.
RESET_n	CMOS Input	**Active LOW asynchronous reset:** Reset is active when RESET_n is LOW and inactive when RESET_n is HIGH. RESET_n must be HIGH during normal operation.
SAx	Input	**Serial address inputs:** Used to configure the temperature sensor/SPD EEPROM ad- dress range on the I^2C bus.
SCL	Input	**Serial clock for temperature sensor/SPD EEPROM:** Used to synchronize communication to and from the temperature sensor/SPD EEPROM on the I^2C bus.
DQx, CBx	I/O	**Data input/output and check bit input/output:** Bidirectional data bus. DQ represents DQ[3:0], DQ[7:0], and DQ[15:0] for the x4, x8, and x16 configurations, respectively. If cyclic redundancy checksum (CRC) is enabled via the mode register, the CRC code is added at the end of the data burst. Any one or all DQ0, DQ1, DQ2, or DQ3 may be used for monitoring of internal V_{REF} level during test via mode register setting MR[4] A[4] = HIGH; training times change when enabled.
DM_n/DBI_n/ TDQS_t (DMU_n, DBIU_n), (DML_n/ DBIl_n)	I/O	**Input data mask and data bus inversion:** DM_n is an input mask signal for write data. Input data is masked when DM_n is sampled LOW coincident with that input da- ta during a write access. DM_n is sampled on both edges of DQS. DM is multiplexed with the DBI function by the mode register A10, A11, and A12 settings in MR5. For a x8 device, the function of DM or TDQS is enabled by the mode register A11 setting in MR1. DBI_n is an input/output identifying whether to store/output the true or inverted data. If DBI_n is LOW, the data will be stored/output after inversion inside the DDR4 device and not inverted if DBI_n is HIGH. TDQS is only supported in x8 SDRAM configurations. (TDQS is not valid for UDIMMs.)
SDA	I/O	**Serial Data:** Bidirectional signal used to transfer data in or out of the EEPROM or EE- PROM/TS combo device.

Wintec Industries, Inc., reserves the right to change datasheets and/or products without any notice.
© 2020 Wintec Industries, Inc.

Pin Descriptions (Continued)

Symbol	Type	Description
DQS_t DQS_c DQSU_t DQSU_c DQSL_t DQSL_c	I/O	**Data strobe:** Output with read data, input with write data. Edge-aligned with read data centered-aligned with write data. For x16 configurations, DQSL corresponds to the data on DQ[7:0], and DQSU corresponds to the data on DQ[15:8]. For the x4 and x8 configurations, DQS corresponds to the data on DQ[3:0] and DQ[7:0], respectively. DDR4 SDRAM supports a differential data strobe only and does not support a single-ended data strobe.
ALERT_n	Output	**Alert output:** Possesses functions such as CRC error flag and command and address parity error flag as output signal. If a CRC error occurs, ALERT_n goes LOW for the period time interval and returns HIGH. If an error occurs during a command address parity check, ALERT_n goes LOW until the on-going DRAM internal recovery transaction is complete. During connectivity test mode, this pin functions as an input. Use of this signal is system dependent. If not connected as signal, ALERT_n pin must be connected to V_{DD} on DIMMs.
EVENT_n	Output	**Temperature event:** The EVENT_n pin is asserted by the temperature sensor when critical temperature thresholds have been exceeded. This pin has no function (NF) on modules without temperature sensors.
TDQS_t TDQS_c (x8 DRAM-based RDIMM only)	Output	**Termination data strobe:** When enabled via the mode register, the DRAM device enables the same R_{TT} termination resistance on TDQS_t and TDQS_c that is applied to DQS_t and DQS_c. When the TDQS function is disabled via the mode register, the DM/ TDQS_t pin provides the data mask (DM) function, and the TDQS_c pin is not used. The TDQS function must be disabled in the mode register for both the x4 and x16 configurations. The DM function is supported only in x8 and x16 configurations. DM, DBI, and TDQS are a shared pin and are enabled/disabled by mode register settings. For more information about TDQS, see the DDR4 DRAM component data sheet. (TDQS_t and TDQS_c are not valid for UDIMMs.)
V_{DD}	Supply	**Module power supply:** 1.21V (TYP).
V_{PP}	Supply	**DRAM activating power supply:** 2.5V –0.125V / +0.250V.
V_{REFCA}	Supply	Reference voltage for control, command, and address pins.
V_{SS}	Supply	Ground.
V_{TT}	Supply	Power supply for termination of address, command, and control $V_{DD}/2$.
V_{DDSPD}	Supply	Power supply used to power the I^2C bus for SPD.
RFU	–	Reserved for future use.
NC	–	**No connect:** No internal electrical connection is present.
NF	–	**No function:** May have internal connection present but has no function.

Wintec Industries, Inc., reserves the right to change datasheets and/or products without any notice.
© 2020 Wintec Industries, Inc.

DQ Map

Component-to-Module DQ Map, Front side

Component Reference Number	Module DQ	IC DQ	Module Pin Number	Component Reference Number	Module DQ	IC DQ	Module Pin Number
U1	0	1	8	U2	16	5	50
	1	3	7		17	7	49
	2	0	20		18	4	62
	3	2	21		19	6	63
	4	5	4		20	1	46
	5	7	3		21	3	45
	6	4	16		22	0	58
	7	6	17		23	2	59
U3	32	3	174	U4	48	3	216
	33	1	173		49	1	215
	34	0	187		50	2	228
	35	2	186		51	0	229
	36	5	170		52	7	211
	37	7	169		53	5	212
	38	6	183		54	6	224
	39	4	182		55	4	225
U5	8	1	28	U6	24	3	70
	9	3	29		25	1	71
	10	2	41		26	2	83
	11	0	42		27	0	84
	12	5	24		28	7	66
	13	7	25		29	5	67
	14	4	38		30	6	79
	15	6	37		31	4	80
U7	40	1	195	U8	56	3	237
	41	3	194		57	1	236
	42	0	207		58	2	249
	43	2	208		59	0	250
	44	7	191		60	7	232
	45	5	190		61	5	233
	46	4	203		62	6	245
	47	6	204		63	4	246

Wintec Industries, Inc., reserves the right to change datasheets and/or products without any notice.
© 2020 Wintec Industries, Inc.

Component-to-Module DQ Map, Front side (Continued)

Component Reference Number	Module DQ	IC DQ	Module Pin Number
U9	CB0	1	92
	CB1	3	91
	CB2	2	101
	CB3	0	105
	CB4	5	88
	CB5	7	87
	CB6	4	100
	CB7	6	104

Wintec Industries, Inc., reserves the right to change datasheets and/or products without any notice.
© 2020 Wintec Industries, Inc.

Component-to-Module DQ Map, Back side

Component Reference	Module DQ	IC DQ	Module Pin Number	Component Reference	Module DQ	IC DQ	Module Pin Number
U11	0	0	8	U12	16	4	50
	1	2	7		17	6	49
	2	1	20		18	5	62
	3	3	21		19	7	63
	4	4	4		20	0	47
	5	6	3		21	2	45
	6	5	16		22	1	58
	7	7	17		23	3	59
U13	32	2	174	U14	48	2	216
	33	0	173		49	0	215
	34	1	187		50	3	228
	35	3	186		51	1	229
	36	4	170		52	6	211
	37	6	169		53	4	212
	38	7	183		54	7	224
	39	5	182		55	5	225

Component Reference	Module DQ	IC DQ	Module Pin Number	Component Reference	Module DQ	IC DQ	Module Pin Number
U15	8	0	28	U16	24	2	70
	9	2	29		25	0	71
	10	3	41		26	1	83
	11	1	42		27	3	84
	12	4	24		28	4	66
	13	6	25		29	6	67
	14	5	38		30	7	79
	15	7	37		31	5	80
U17	40	0	195	U18	56	2	237
	41	2	194		57	0	236
	42	1	207		58	3	249
	43	3	208		59	1	250
	44	6	191		60	6	232
	45	4	190		61	4	233
	46	5	203		62	7	245
	47	7	204		63	5	246

Wintec Industries, Inc., reserves the right to change datasheets and/or products without any notice.
© 2020 Wintec Industries, Inc.

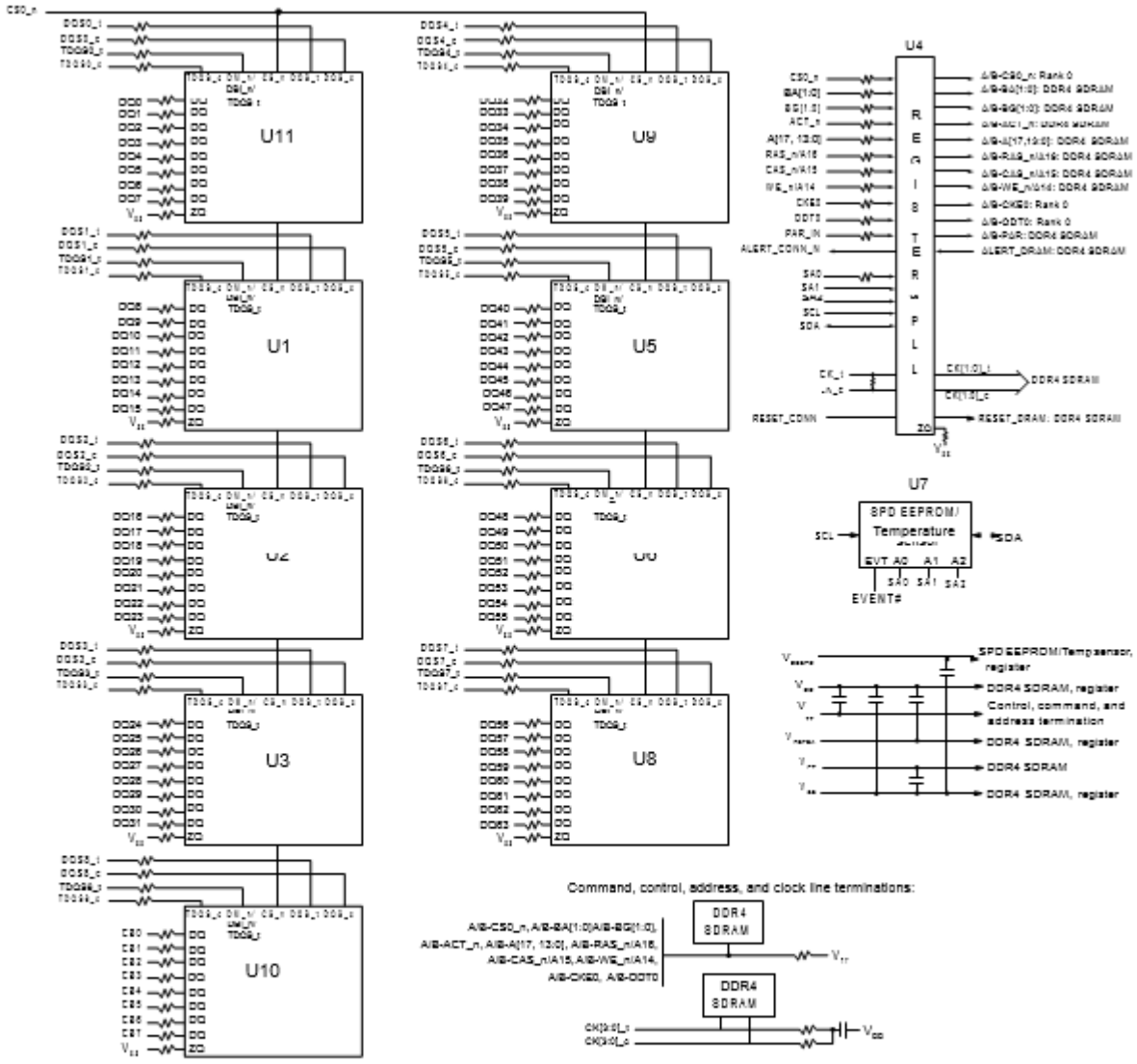
Component-to-Module DQ Map, Back side (Continued)

Component Reference Number	Module DQ	IC DQ	Module Pin Number
U19	CB0	0	92
	CB1	2	91
	CB2	3	101
	CB3	1	105
	CB4	4	88
	CB5	6	87
	CB6	5	100
	CB7	7	104

Wintec Industries, Inc., reserves the right to change datasheets and/or products without any notice.
© 2020 Wintec Industries, Inc.

Functional Block Diagram:

One Rank 512MB x 72 (4GB), 1GB x 72 (8GB) DDR4 ECC SODIMM

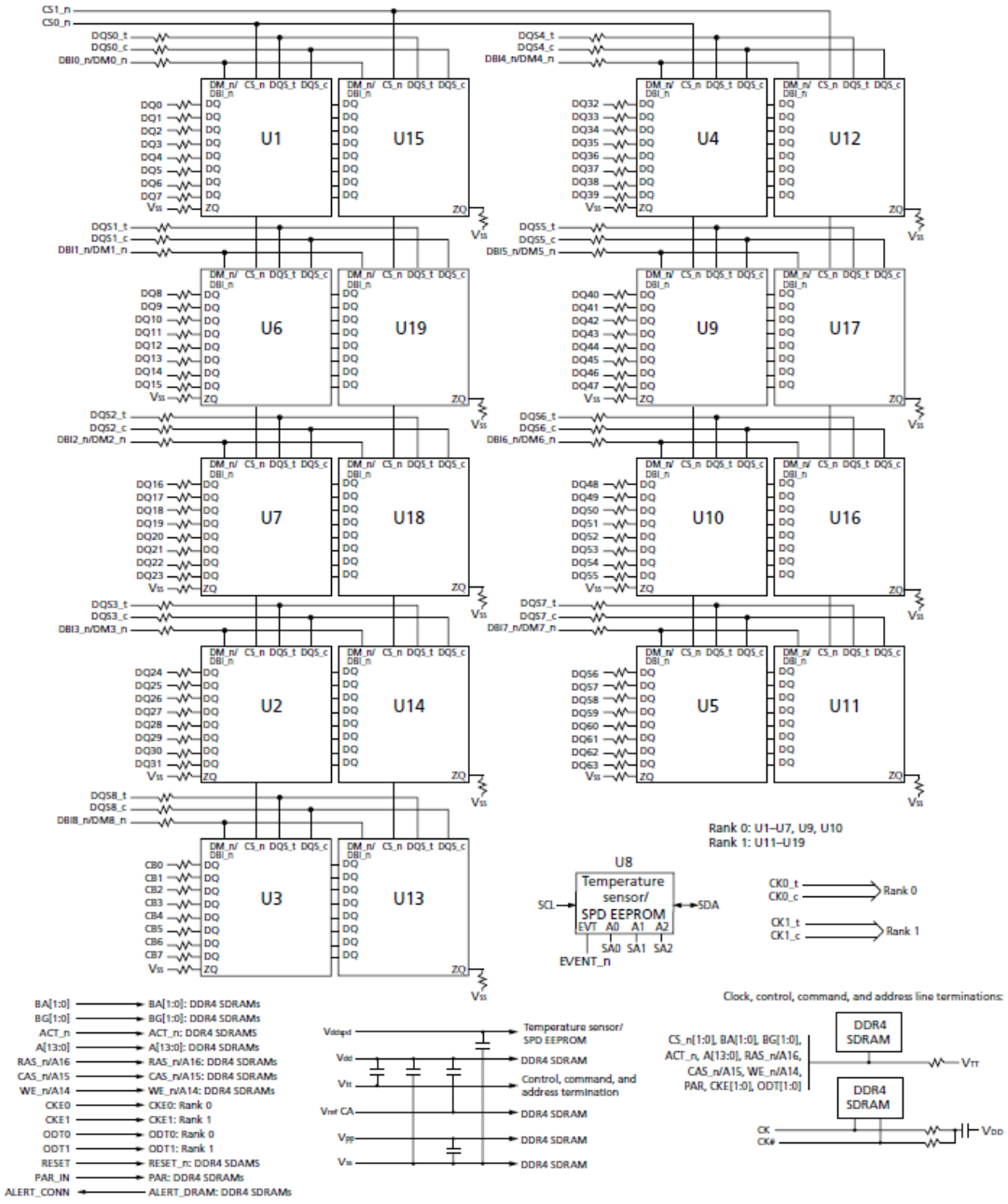


Note: 1. The ZQ ball on each DDR4 component is connected to an external 240Ω ±1% resistor that is tied to ground. It is used for the calibration of the component's ODT and output driver.

Wintec Industries, Inc., reserves the right to change datasheets and/or products without any notice.
© 2020 Wintec Industries, Inc.

Functional Block Diagram (continued):

Two Rank 512MB x 72 (8GB), 1GB x 72 (16GB) DDR4 ECC SODIMM



Note: 1. The ZQ ball on each DDR4 component is connected to an external 240Ω ±1% resistor that is tied to ground. It is used for the calibration of the component's ODT and output driver.

Wintec Industries, Inc., reserves the right to change datasheets and/or products without any notice.
© 2020 Wintec Industries, Inc.

Temperature Sensor with SPD EEPROM

The temperature sensor continuously monitors the module's temperature and can be read back at any time over the I^2C bus shared with the serial presence-detect (SPD) EEPROM.

Temperature Sensor with SPD EEPROM Operating Conditions

Parameter/Condition	Symbol	Min	Max	Units
Supply voltage	V_{DDSPD}	2.2	2.75	V
Input low voltage: logic 0; all inputs	V_{IL}	-0.5	$V_{DDSPD} \times 0.3$	V
Input high voltage: logic 1; all inputs	V_{IH}	$V_{DDSPD} \times 0.7$	$V_{DDSPD} + 0.5$	V
Output low voltage: 3mA sink current $V_{DDSPD} > 2V$	V_{OL}	–	0.4	V
Input leakage current: (SCL, SDA) $V_{IN} = V_{DDSPD}$ or V_{SSSPD}	I_{LI}	–	±5	µA
Output leakage current: $V_{OUT} = V_{DDSPD}$ or V_{SSSPD}, SDA in High-Z	I_{LO}	–	±5	µA

Temperature Sensor EEPROM Serial Interface Timing

Parameter/Condition	Symbol	Min	Max	Units
Clock frequency	^{f}SCL	10	1000	kHz
Clock pulse width HIGH time	$^{t}HIGH$	260	–	ns
Clock pulse width LOW time	^{t}LOW	500	–	ns
Detect clock LOW timeout	$^{t}TIMEOUT$	25	35	ms
SDA rise time	^{t}R	–	120	ns
SDA fall time	^{t}F	–	120	ns
Data-in setup time	$^{t}SU:DAT$	50	–	ns
Data-in hold time	$^{t}HD:DI$	0	–	ns
Data out hold time	$^{t}HD:DAT$	0	350	ns
Start condition setup time	$^{t}SU:STA$	260	–	ns
Start condition hold time	$^{t}HD:STA$	260	–	ns
Stop condition setup time	$^{t}SU:STO$	260	–	ns
Time the bus must be free before a new transition can start	^{t}BUF	500	–	ns
Write time	^{t}W	–	5	ms
Warm power cycle time off	$^{t}POFF$	1	–	ms
Time from power on to first command	$^{t}INIT$	10	–	ms

Wintec Industries, Inc., reserves the right to change datasheets and/or products without any notice.
© 2020 Wintec Industries, Inc.

Electrical Specifications:

Exposure to stresses greater than these absolute maximum rating conditions for extended periods may affect reliability of the module.

Absolute Maximum Ratings

Symbol	Parameter	Min	Max	Units	Note
V_{DD}	Voltage on V_{DD} pin relative to V_{SS}	-0.3	1.5	V	1,3
V_{DDQ}	Voltage on V_{DDQ} relative to V_{SS}	-0.3	1.5	V	1,3
V_{PP}	Voltage on any V_{PP} pin relative to V_{SS}	-0.3	3.0	V	4
V_{IN}, V_{OUT}	Voltage on any pin except VREFCA to V_{SS}	-0.3	1.5	V	1
T_{STG}	Storage Temperature	-55	+100	°C	1,2

Note:

1. Stress greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. Storage Temperature is the case surface temperature on the center/top side of the DRAM. For measurement conditions, please refer to JEDEC51-2 standard.
3. V_{DD} and V_{DDQ} must be within 300mV of each other at all times and VREFCA must not be greater than 0.6 x V_{DDQ}, when V_{DD} and V_{DDQ} are less than 500mV; VREFCA may be equal to or less than 300mV.
4. V_{PP} must be equal or greater than V_{DD}/V_{DDQ} at all times.

Recommended DC Operating Conditions

Symbol	Parameter	Min	Typical	Max	Units	Note
VDD	Supply Voltage	1.14	1.2	1.26	V	1,2,3
VDDq	Supply Voltage for Output	1.14	1.2	1.26	V	1,2,3
VPP	SDRAM Power Supply	2.375	2.5	2.75	V	3

Note:

1. Under all conditions V_{DDQ} must be less than or equal to V_{DD}.
2. V_{DDQ} tracks with V_{DD}. AC parameters are measured with V_{DD} and V_{DDQ} tied together.
3. DC bandwidth is limited to 20MHz.

AC & DC Logic Input Levels for Single Ended Signals

Symbol	Parameter	DDR4-1866/2133/2400/2666		Units	Note
		Min	Max		
$V_{IH.CA}$ (DC75)	DC Input Logic high	VREFCA +0.075	VDD	V	
$V_{IL.CA}$ (DC75)	DC Input Logic low	V_{SS}	VREFCA +0.075	V	
$V_{IH.CA}$ (AC100)	AC Input Logic high	V_{REF} + 0.1	Note 2	V	1
$V_{IL.CA}$ (AC100)	AC Input Logic low	Note 2	V_{REF} + 0.1	V	1
V_{REFCA}(DC)	Reference Voltage for ADD, CMD inputs	0.49*V_{DD}	0.51*V_{DD}	V	2,3

Note:

1. See "Overshoot and Undershoot Specifications" on section.
2. The AC peak noise on V_{REFCA} may not V_{REFCA} to deviate from V_{REFCA}(DC) by more than ± 1% V_{DD} (for reference: approx. ± 12mV).
3. For reference: approx. $V_{DD}/2$ ± 12mV).

Wintec Industries, Inc., reserves the right to change datasheets and/or products without any notice.
© 2020 Wintec Industries, Inc.

Thermal Characteristics

Symbol	Parameter/Condition	Value	Units	Notes
T_C	Commercial operating case temperature	0 to 85	°C	1, 2, 3
T_C		>85 to 95	°C	1, 2, 3, 4
T_{OPER}	Normal operating temperature range	0 to 85	°C	5
T_{OPER}	Extended temperature operating range (optional)	>85 to 95	°C	5

Note:

1. Maximum operating case temperature: T_C is measured in the center of the package.
2. A thermal solution must be designed to ensure the DRAM device does not exceed the maximum T_C during operation.
3. Device functionality is not guaranteed if the DRAM device exceeds the maximum T_C during operation.
4. If T_C exceeds 85°C, the DRAM must be refreshed externally at 2X refresh, which is a 3.9µs interval refresh rate.
5. The refresh rate must double when 85°C < T_{OPER} ≤ 95°C.

AC and DC Input Measurement Levels: V_{REF} Tolerances

The DC tolerance limits and ac-noise limits for the reference voltages V_{REFCA} is illustrated in Figure 2. It shows a valid reference voltage V_{REF} (t) as a function of time (V_{REF} stands for V_{REFCA}).

V_{REF}(DC) is the linear average of V_{REF}(t) over a very long period of time (e.g. 1 sec). This average has to meet the min/max requirement in Table X. Furthermore V_{REF}(t) may temporarily deviate from V_{REF}(DC) by no more than ± 1% VDD.

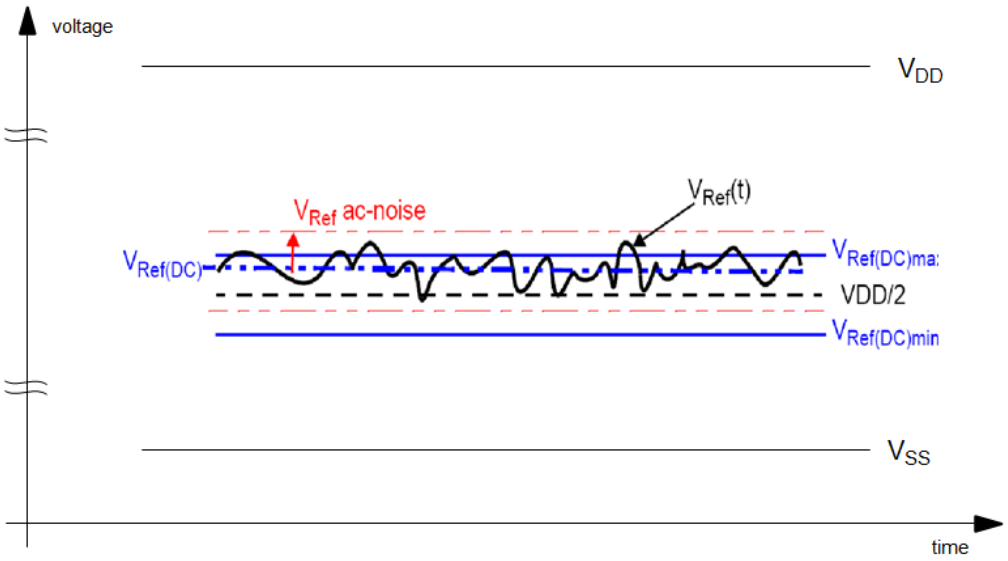


Figure 2: Illistration for V_{REF}(DC) tolerance and V_{REF} AC-noise limits

Wintec Industries, Inc., reserves the right to change datasheets and/or products without any notice.
© 2020 Wintec Industries, Inc.

The voltage levels for setup and hold time measurements V_{IH}(AC), V_{IH}(DC), V_{IL}(AC) and V_{IL}(DC) are dependent on V_{REF}.

"V_{REF}" shall be understood as V_{REF}(DC), as defined in Figure 2.

This clarifies that DC-variations of V_{REF} affect the absolute voltage a signal has to reach to achieve a valid high or low level and therefore the time to which setup and hold is measured. System timing and voltage budgets need to account for V_{REF}(DC) deviations from the optimum position within the data-eye of the input signals.

This also clarifies that the DRAM setup/hold specification and derating values need to include time and voltage associated with V_{REF} AC-noise. Timing and voltage effects due to AC-noise on V_{REF} up to the specified limit (+/-1% of V_{DD}) are included in DRAM timings and their associated deratings.

AC and DC Logic Input Levels for Differential Signals

Differential Signals Definition

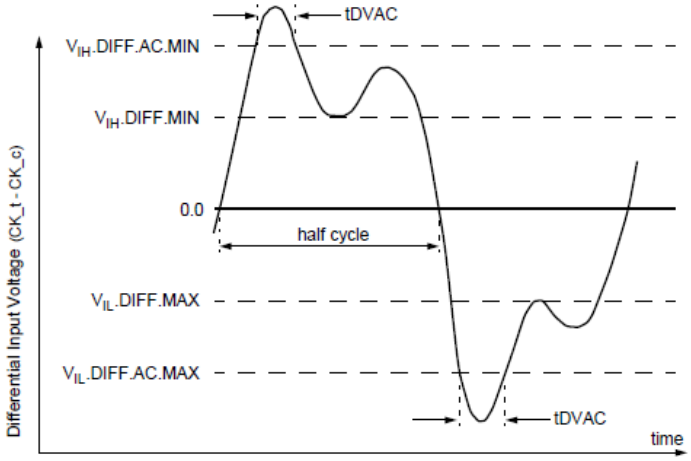


Figure 3: Definition of differential ac-swing and 'time above ac-level" t_{DVAC}

Note:

1. Differential signal rising edge from VIL.DIFF.MAX to VIH.DIFF.MIN must be monotonic slope
2. Differential signal falling edge from VIH.DIFF.MIN to VIL.DIFF.MAX must be monotonic slope

Wintec Industries, Inc., reserves the right to change datasheets and/or products without any notice.
© 2020 Wintec Industries, Inc.

Differential swing requirements for clock (CK_t – CK_c)

Symbol	Parameter	DDR4-1866/2133/2400		DDR4-2666		Unit	Note
		Min	Max	Min	Max		
V_{IHdiff}	differential input high	+0.150	Note 3	0.120	Note 3	V	1
V_{ILdiff}	differential input low	Note 3	-0.150	Note 3	-0.120	V	1
V_{IHdiff}(AC)	differential input high ac	2 x (V_{IH}(AC) - V_{REF})	Note 3	2 x (V_{IH}(AC) - V_{REF})	Note 3	V	2
V_{IHdiff}(AC)	differential input low ac	Note 3	2 x (V_{IL}(AC) -V_{REF})	Note 3	2 x (V_{IL}(AC) -V_{REF})	V	2

Note:

1. Used to define a differential signal slew-rate.
2. For CK_t - CK_c use $V_{IH.CA}$/$V_{IL.CA}$(AC) of ADD/CMD and V_{REFCA}.
3. These values are not defined; however, the differential signal CK_t - CK_c, need to be written within the respective limits ($V_{IH.CA}$(DC) max, $V_{IL.CA}$(DC) for single-ended signals as well as the limitations for overshoot and undershoot.

Allowed time before Ring-back (tDVAC) for CK_t – CK-c

Slew Rate (V/ns)	tDVAC [ps] @|$V_{IH/LDIFF}$(AC)| = 200mV		tDVAC [ps] @|$V_{IH/LDIFF}$(AC)| = TBDmV	
	Min	Max	Min	Max
>4.0	120	-	TBD	-
4.0	115	-	TBD	-
3.0	110	-	TBD	-
2.0	105	-	TBD	-
1.8	100	-	TBD	-
1.6	95	-	TBD	-
1.4	90	-	TBD	-
1.2	85	-	TBD	-
1.0	80	-	TBD	-
<1.0	80	-	TBD	-

Wintec Industries, Inc., reserves the right to change datasheets and/or products without any notice.
© 2020 Wintec Industries, Inc.

Electrical Characteristics and AC Timing Parameter

Timing Parameters by Speed Grade

Speed	DDR4-1866	DDR4-2133	DDR4-2400	DDR4-2666	Unit
	13-13-13	15-15-15	17-17-17	19-19-19	
tCK(min)	1.071	0.938	0.833	0.750	ns
CAS Latency	13	15	17	19	nCK
tRCD(min)	13.92	14.06	14.16	14.25	ns
tRP(min)	13.92	14.06	14.16	14.25	ns
tRAS(min)	34	33	32	32	ns
tRC(min)	47.92	47.06	46.16	46.25	ns

DDR4-1866 Speed Bins and Operating Conditions

Speed Bin				DDR4-1866		Unit	NOTE
CL-nRCD-nRP				13-13-13			
Parameter			Symbol	min	max		
Internal read command to first data			tAA	13.92	18.00	ns	10
Internal read command to first data with read DBI enabled			tAA_DBI	tAA(min) + 2nCK	tAA(max) +2nCK	ns	10
ACT to internal read or write delay time			tRCD	13.92	-	ns	10
PRE command period			tRP	13.92	-	ns	10
ACT to PRE command period			tRAS	34	9 x tREFI	ns	10
ACT to ACT or REF command period			tRC	47.92	-	ns	10
	Normal	Read DBI					
CWL = 9	CL = 9	CL = 11	tCK(AVG)	Reserved		ns	1,2,3,4,9
	CL = 10	CL = 12	tCK(AVG)	1.5	1.6	ns	1,2,3,4,9
CWL = 9,11	CL = 10	CL = 12	tCK(AVG)	Reserve		ns	4
	CL = 11	CL = 13	tCK(AVG)	1.25	<1.5	ns	1,2,3,4,6
	CL = 12	CL = 14	tCK(AVG)	1.25	<1.5	ns	1,2,3,6
CWL = 10,12	CL = 12	CL = 14	tCK(AVG)	Reserve		ns	1,2,3,4
	CL = 13	CL = 15	tCK(AVG)	1.071	<1.25	ns	1,2,3,4
	CL = 14	CL = 16	tCK(AVG)	1.071	<1.25	ns	1,2,3
Supported CL Settings				9,11,12,13,14		nCK	
Supported CL Settings with read DBI				11,13,14,15,16		nCK	
Supported CWL Settings				9,10,11,12		nCK	

Wintec Industries, Inc., reserves the right to change datasheets and/or products without any notice.
© 2020 Wintec Industries, Inc.

DDR4-2133 Speed Bins and Operating Conditions

Speed Bin				DDR4-2133		Unit	NOTE
CL-nRCD-nRP				15-15-15			
Parameter			Symbol	min	max		
Internal read command to first data			tAA	14.06 (13.75)[5]	18.00	ns	10
Internal read command to first data with read DBI enabled			tAA_DBI	tAA(min) + 3nCK	tAA(max) + 3nCK	ns	10
ACT to internal read or write delay time			tRCD	14.06 (13.75)[5]	-	ns	10
PRE command period			tRP	14.06 (13.75)[5]	-	ns	10
ACT to PRE command period			tRAS	33	9 x tREFI	ns	10
ACT to ACT or REF command period			tRC	47.06 (46.75)[5]	-	ns	10
	Normal	Read DBI					
CWL = 9	CL = 9	CL = 11	tCK(AVG)	Reserved		ns	1,2,3,4,9
	CL = 10	CL = 12	tCK(AVG)	1.5	1.6	ns	1,2,3,4,9
CWL = 9,11	CL = 11	CL = 13	tCK(AVG)	1.25	<1.5	ns	1,2,3,4,7
	CL = 12	CL = 14	tCK(AVG)	1.25	<1.5	ns	1,2,3,7
CWL = 10,12	CL = 13	CL = 15	tCK(AVG)	1.071	<1.25	ns	1,2,3,4,7
	CL = 14	CL = 16	tCK(AVG)	1.071	<1.25	ns	1,2,3,7
CWL = 11,14	CL = 14	CL = 17	tCK(AVG)	Reserved		ns	1,2,3,4
	CL = 15	CL = 18	tCK(AVG)	0.938	<1.071	ns	1,2,3,4
	CL = 16	CL = 19	tCK(AVG)	0.938	<1.071	ns	1,2,3
Supported CL Settings				9,11.12,13,14,15,16		nCK	
Supported CL Settings with read DBI				11,13,14,15,16,18,19		nCK	
Supported CWL Settings				9,10,11,12,14		nCK	

Wintec Industries, Inc., reserves the right to change datasheets and/or products without any notice.
© 2020 Wintec Industries, Inc.

DDR4-2400 Speed Bins and Operating Conditions

Speed Bin				DDR4-2400		Unit	NOTE
CL-nRCD-nRP				17-17-17			
Parameter			Symbol	min	max		
Internal read command to first data			tAA	14.16 (13.75)[5]	18.00	ns	10
Internal read command to first data with read DBI enabled			tAA_DBI	tAA(min) + 3nCK	tAA(max) + 3nCK	ns	10
ACT to internal read or write delay time			tRCD	14.16 (13.75)[5]	-	ns	10
PRE command period			tRP	14.16 (13.75)[5]	-	ns	10
ACT to PRE command period			tRAS	32	9 x tREFI	ns	10
ACT to ACT or REF command period			tRC	46.16 (45.75)[5]	-	ns	10
	Normal	Read DBI					
CWL = 9	CL = 9	CL = 11	tCK(AVG)	Reserved		ns	1,2,3,4,9
	CL = 10	CL = 12	tCK(AVG)	1.5	1.6	ns	1,2,3,4,9
CWL = 9,11	CL = 10	CL = 12	tCK(AVG)	Res		ns	4
	CL = 11	CL = 13	tCK(AVG)	1.25	<1.5	ns	1,2,3,4,8
	CL = 12	CL = 14	tCK(AVG)	1.25	<1.5	ns	1,2,3,8
CWL = 10,12	CL = 12	CL = 14	tCK(AVG)	Reserved		ns	4
	CL = 13	CL = 15	tCK(AVG)	1.071	<1.25	ns	1,2,3,4,8
	CL = 14	CL = 16	tCK(AVG)	1.071	<1.25	ns	1,2,3,8
CWL = 11,14	CL = 14	CL = 17	tCK(AVG)	Reserved		ns	4
	CL = 15	CL = 18	tCK(AVG)	0.938	<1.071	ns	1,2,3,4,8
	CL = 16	CL = 19	tCK(AVG)	0.938	<1.071	ns	1,2,3,8
CWL = 12,16	CL = 15	CL = 18	tCK(AVG)	Reserved		ns	1,2,3,4
	CL = 16	CL = 19	tCK(AVG)	Reserved		ns	1,2,3,4
	CL = 17	CL = 20	tCK(AVG)	0.833	<0.938		
	CL = 18	CL = 21	tCK(AVG)	0.833	<0.938	ns	1,2,3
Supported CL Settings				10,11,12,13,14,15,16,17,18		nCK	
Supported CL Settings with read DBI				12,13,14,15,16,18,19,20,21		nCK	
Supported CWL Settings				9,10,11,12,14,16		nCK	

Wintec Industries, Inc., reserves the right to change datasheets and/or products without any notice.
© 2020 Wintec Industries, Inc.

DDR4-2666 Speed Bins and Operating Conditions

Speed Bin				DDR4-2666		Unit	NOTE
CL-nRCD-nRP				19-19-19			
Parameter			Symbol	min	max		
Internal read command to first data			tAA	14.25 (13.75)[5,12]	18.00	ns	10
Internal read command to first data with read DBI enabled			tAA_DBI	tAA(min) + 3nCK	tAA(max) + 3nCK	ns	10
ACT to internal read or write delay time			tRCD	14.25 (13.75)[5]	-	ns	10
PRE command period			tRP	14.25 (13.75)[5]	-	ns	10
ACT to PRE command period			tRAS	32	9 x tREFI	ns	10
ACT to ACT or REF command period			tRC	46.25 (45.75)[5]	-	ns	10
	Normal	Read DBI					
CWL = 9	CL = 9	CL = 11	tCK(AVG)	Reserved		ns	1,2,3,4,9
	CL = 10	CL = 12	tCK(AVG)	1.5	1.6	ns	1,2,3,4,9
CWL = 9,11	CL = 10	CL = 12	tCK(AVG)	Reserved		ns	4
	CL = 11	CL = 13	tCK(AVG)	1.25	<1.5	ns	1,2,3,4,8
	CL = 12	CL = 14	tCK(AVG)	1.25	<1.5	ns	1,2,3,8
CWL = 10,12	CL = 12	CL = 14	tCK(AVG)	Reserved		ns	4
	CL = 13	CL = 15	tCK(AVG)	1.071	<1.25	ns	1,2,3,4,8
	CL = 14	CL = 16	tCK(AVG)	1.071	<1.25	ns	1,2,3,8
CWL = 11,14	CL = 14	CL = 17	tCK(AVG)	Reserved		ns	4
	CL = 15	CL = 18	tCK(AVG)	0.937	<1.071	ns	1,2,3,4,8
	CL = 16	CL = 19	tCK(AVG)	0.937	<1.071	ns	1,2,3,8
CWL = 12,16	CL = 15	CL = 18	tCK(AVG)	Reserved		ns	1,2,3,4
	CL = 16	CL = 19	tCK(AVG)	Reserved		ns	1,2,3,4
	CL = 17	CL = 20	tCK(AVG)	0.833	<0.937		
	CL = 18	CL = 21	tCK(AVG)	0.833	<0.937	ns	1,2,3
CWL = 14,18	CL = 17	CL = 20	tCK(AVG)	Reserved		ns	1,2,3,4
	CL = 18	CL = 21	tCK(AVG)	Reserved		ns	1,2,3,4
	CL = 19	CL = 22	tCK(AVG)	0.75	<0.833		
	CL = 20	CL = 23	tCK(AVG)	0.75	<0.833	ns	1,2,3
Supported CL Settings				10,11,12,13,14,15,16,17,18,19,20		nCK	
Supported CL Settings with read DBI				12,13,14,15,16,18,19,20,21,22,23		nCK	
Supported CWL Settings				9,10,11,12,14,16,18		nCK	

Wintec Industries, Inc., reserves the right to change datasheets and/or products without any notice.
© 2020 Wintec Industries, Inc.

1. The CL setting and CWL setting result in tCK(avg).MIN and tCK(avg).MAX requirements. When making a selection of tCK(avg), both need to be fulfilled: Requirements from
CL setting as well as requirements from CWL setting.
2. tCK(avg).MIN limits: Since CAS Latency is not purely analog - data and strobe output are synchronized by the DLL - all possible intermediate frequencies may not be
guaranteed. An application should use the next smaller JEDEC standard tCK(avg) value (1.5, 1.25, 1.071, 0.938 or 0.833 ns) when calculating CL [nCK] = tAA [ns] /
tCK(avg) [ns], rounding up to the next 'Supported CL', where tAA = 12.5ns and tCK(avg) = 1.3 ns should only be used for CL = 10 calculation.
3. tCK(avg).MAX limits: Calculate tCK(avg) = tAA.MAX / CL SELECTED and round the resulting tCK(avg) down to the next valid speed bin (i.e. 1.5ns or 1.25ns or 1.071 ns or
0.938 ns or 0.833 ns). This result is tCK(avg).MAX corresponding to CL SELECTED.
4. 'Reserved' settings are not allowed. User must program a different value.
5. 'Optional' settings allow certain devices in the industry to support this setting, however, it is not a mandatory feature. Refer to supplier's data sheet and/or the DIMM SPD
information if and how this setting is supported.
6. Any DDR4-1866 speed bin also supports functional operation at lower frequencies as shown in the table which are not subject to Production Tests but verified by Design/
Characterization.
7. Any DDR4-2133 speed bin also supports functional operation at lower frequencies as shown in the table which are not subject to Production Tests but verified by Design/
Characterization.
8. Any DDR4-2400 speed bin also supports functional operation at lower frequencies as shown in the table which are not subject to Production Tests but verified by Design/
Characterization.
9. Any DDR4-2666 speed bin also supports functional operation at lower frequencies as shown in the table which are not subject to Production Tests but verified by Design/
Characterization.
10. Parameters apply from tCK(avg)min to tCK(avg)max at all standard JEDEC clock period values as stated in the Speed Bin Tables.

Wintec Industries, Inc., reserves the right to change datasheets and/or products without any notice.
© 2020 Wintec Industries, Inc.

AC Timing Parameters by Speed Grade

Speed		DDR4-1866		DDR4-2133		DDR4-2400		DDR4-2666		Units	NOTE
Parameter	Symbol	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX		
Clock Timing											
Minimum Clock Cycle Time (DLL off mode)	tCK (DLL_OFF	8	20	8	20	8	20	8	20	ns	-
Average Clock Period	tCK(avg)	1.071	<1.25	0.937	<1.071	0.833	<0.937	0.750	<0.833	ns	35,36
Average high pulse width	tCH(avg)	0.48	0.52	0.48	0.52	0.48	0.52	0.48	0.52	tCK(avg)	
Average low pulse width	tCL(avg)	0.48	0.52	0.48	0.52	0.48	0.52	0.48	0.52	tCK(avg)	
Absolute Clock Period	tCK(abs)	tCK(avg)min + tJIT(per)min_ to t	tCK(avg)max + tJIT(per)max_tot	tCK(avg)min + tJIT(per)min_ to t	tCK(avg)max + tJIT(per)max_tot	tCK(avg)min + tJIT(per)min_ to t	tCK(avg)max + tJIT(per)max_tot	tCK(avg)min + tJIT(per)min_to t	tCK(avg)max + tJIT(per)max_tot	tCK(avg)	
Absolute clock HIGH pulse width	tCH(abs)	0.45	-	0.45	-	0.45	-	0.45	-	tCK(avg)	23
Absolute clock LOW pulse width	tCL(abs)	0.45	-	0.45	-	0.45	-	0.45	-	tCK(avg)	24
Clock Period Jitter- total	JIT(per)_tot	-54	54	-47	47	-42	42	-38	38	ps	23
Clock Period Jitter- deterministic	JIT(per)_dj	-27	27	-23	23	-21	21	-19	19	ps	26
Clock Period Jitter during DLL locking period	tJIT(per, lck)	-43	43	-38	38	-33	33	-30	30	ps	
Cycle to Cycle Period Jitter	(cc)_total	-	107	-	94	-	83	-	75	ps	25
Cycle to Cycle Period Jitter during DLL locking period	tJIT(cc, lck)	-	86	-	75	-	67	-	60	ps	
Duty Cycle Jitter	tJIT(duty)	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	ps	
Cumulative error across 2 cycles	tERR(2per)	-79	79	-69	69	-61	61	-55	55	ps	
Cumulative error across 3 cycles	tERR(3per)	-94	94	-82	82	-73	73	-66	66	ps	
Cumulative error across 4 cycles	tERR(4per)	-104	104	-91	91	-81	81	-73	73	ps	
Cumulative error across 5 cycles	tERR(5per)	-112	112	-98	98	-87	87	-78	78	ps	
Cumulative error across 6 cycles	tERR(6per)	-119	119	-104	104	-92	92	-83	83	ps	
Cumulative error across 7 cycles	tERR(7per)	-124	124	-109	109	-97	97	-87	87	ps	
Cumulative error across 8 cycles	tERR(8per)	-129	129	-113	113	-101	101	-91	91	ps	
Cumulative error across 9 cycles	tERR(9per)	-134	134	-117	117	-104	104	-94	94	ps	
Cumulative error across 10 cycles	tERR(10per)	-137	137	-120	120	-107	107	-96	96	ps	
Cumulative error across 11 cycles	tERR(11per)	-141	141	-123	123	-110	110	-99	99	ps	
Cumulative error across 12 cycles	tERR(12per)	-144	144	-126	126	-112	112	-101	101	ps	
Cumulative error across 13 cycles	tERR(13per)	-147	147	-129	129	-114	114	-103	103	ps	
Cumulative error across 14 cycles	tERR(14per)	-150	150	-131	131	-116	116	-104	104	ps	
Cumulative error across 15 cycles	tERR(15per)	-152	152	-133	133	-118	118	-106	106	ps	
Cumulative error across 16 cycles	tERR(16per)	-155	155	-135	135	-120	120	-108	108	ps	
Cumulative error across 17 cycles	tERR(17per)	-157	157	-137	137	-122	122	-110	110	ps	
Cumulative error across 18 cycles	tERR(18per)	-159	159	-139	139	-124	124	-112	112	ps	
Cumulative error across n = 13, 14 . . . 49, 50 cycles	tERR(nper)	^{t}ERR(nper)min = ((1 + 0.68ln(n)) * ^{t}JIT(per)_total min) ^{t}ERR(nper)max = ((1 + 0.68ln(n)) * ^{t}JIT(per)_total max)								ps	
Command and Address setup time to CK_t, CK_c referenced to Vih(ac) / Vil(ac) levels	tIS(base)	100	-	80	-	62	-	TBD	-	ps	
Command and Address setup time to CK_t, CK_c referenced to Vref levels	tIS(Vref)	200	-	180	-	162	-	TBD	-	ps	
Command and Address hold time to CK_t, CK_c referenced to Vih(dc) / Vil(dc) levels	tIH(base)	125	-	105	-	87	-	TBD	-	ps	
Command and Address hold time to CK_t, CK_c referenced to Vref levels	tIH(Vref)	200	-	180	-	162	-	TBD	-	ps	
Control and Address Input pulse width for each input	tIPW	525	-	460	-	410	-	385	-	ps	

Wintec Industries, Inc., reserves the right to change datasheets and/or products without any notice.
© 2020 Wintec Industries, Inc.

Timing Parameters by Speed Grade (continued)

Speed		DDR4-1866		DDR4-2133		DDR4-2400		DDR4-2666		Units	NOTE
Parameter	Symbol	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX		
Command and Address Timing											
CAS_n to CAS_n command delay for same bank group	tCCD_L	max(5 nCK, 5.355 ns)	-	max(5 nCK, 5.625 ns)	-	max(5 nCK 5 ns)	-	max(5 nCK,5 ns)	-	nCK	34
CAS_n to CAS_n command delay for different bank group	tCCD_S	4	-	4	-	4	-	4	-	nCK	34
ACTIVATE to ACTIVATE Command delay to different bank group for 2KB page size	tRRD_S(2K)	Max(4nCK,5.3ns)	-	Max(4nCK,5.3ns)	-	Max(4nCK,5.3ns)	-	Max(4nCK,5.3ns)	-	nCK	34
ACTIVATE to ACTIVATE Command delay to different bank group for 2KB page size	tRRD_S(1K)	Max(4nCK,4.2ns)	-	Max(4nCK,3.7ns)	-	Max(4nCK,3.3ns)	-	Max(4nCK,3.3ns)	-	nCK	34
ACTIVATE to ACTIVATE Command delay to different bank group for 1/2KB page size	tRRD_S(1/2K)	Max(4nCK,4.2ns)	-	Max(4nCK,3.7ns)	-	Max(4nCK,3.3ns)	-	Max(4nCK,3.3ns)	-	nCK	34
ACTIVATE to ACTIVATE Command delay to same bank group for 2KB page size	tRRD_L(2K)	Max(4nCK,6.4ns)	-	Max(4nCK,6.4ns)	-	Max(4nCK,6.4ns)	-	Max(4nCK,6.4ns)	-	nCK	34
ACTIVATE to ACTIVATE Command delay to same bank group for 1KB page size	tRRD_L(1K)	Max(4nCK,5.3ns)	-	Max(4nCK,5.3ns)	-	Max(4nCK,4.9ns)	-	Max(4nCK,4.9ns)	-	nCK	34
ACTIVATE to ACTIVATE Command delay to same bank group for 1/2KB page size	tRRD_L(1/2K)	Max(4nCK,5.3ns)	-	Max(4nCK,5.3ns)	-	Max(4nCK,4.9ns)	-	Max(4nCK,4.9ns)	-	nCK	34
Four activate window for 2KB page size	tFAW_2K	Max(28nCK,30ns)	-	Max(28nCK,30ns)	-	Max(28nCK, 30ns)	-	Max(28nCK, 30ns)	-	ns	34
Four activate window for 1KB page size	tFAW_1K	Max(20nCK,23ns)	-	Max(20nCK,21ns)	-	Max(20nCK, 21ns)	-	Max(20nCK, 21ns)	-	ns	34
Four activate window for 1/2KB page size	tFAW_1/2K	Max(16nCK,17ns)	-	Max(16nCK,15ns)	-	Max(16nCK, 13ns)	-	Max(16nCK, 13ns)	-	ns	34
Delay from start of internal write transaction to internal read command for different bank group	tWTR_S	max(2nCK,2.5ns)	-	max(2nCK,2.5ns)	-	max (2nCK, 2.5ns)	-	max (2nCK, 2.5ns)	-		1,2,34
Delay from start of internal write transaction to internal read command for same bank group	tWTR_L	max(4nCK,7.5ns)	-	max(4nCK,7.5ns)	-	max (4nCK,7.5ns)	-	max (4nCK,7.5ns)	-		1,34
Internal READ Command to PRECHARGE Command delay	tRTP	max(4nCK,7.5ns)	-	max(4nCK,7.5ns)	-	max (4nCK,7.5ns)	-	max (4nCK,7.5ns)	-		
WRITE recovery time	tWR	15	-	15	-	15	-	15	-	ns	1
Write recovery time when CRC and DM are enabled	tWR_CRC_DM	tWR+max (5nCK,3.75ns)	-	tWR+max (5nCK,3.75s)	-	tWR+max (5nCK,3.75ns)	-	tWR+max (5nCK,3.75ns)	-	ns	1, 28
delay from start of internal write transaction to internal read command for different bank group with both CRC and DM enabled	tWTR_SCRC_DM	tWTR_S+ma x (5nCK,3.75ns)	-	tWTR_S+ma x (5nCK,3.75ns)	-	tWTR_S+max (5nCK,3.75ns)	-	tWTR_S+max (5nCK,3.75ns)	-	ns	2, 29, 34
delay from start of internal write transaction to internal read command for same bank group with both CRC and DM enabled	tWTR_LCRC_DM	tWTR_L+max (5nCK,3.75ns)	-	tWTR_L+max (5nCK,3.75ns)	-	tWTR_L+max (5nCK,3.75ns)	-	tWTR_L+max (5nCK,3.75ns)	-	ns	3,30, 34
DLL locking time	tDLLK	597	-	768	-	768	-	854	-	nCK	
Mode Register Set command cycle time	tMRD	8	-	8	-	8	-	8	-	nCK	
Mode Register Set command update delay	tMOD	max(24nCK,15ns)	-	max(24nCK,1 5ns)	-	max(24nCK,1 5ns)	-	max(24nCK, 15ns)	-		
Multi-Purpose Register Recovery Time	tMPRR	1	-	1	-	1	-	1	-	nCK	33
Multi-Purpose Register Write Recovery Time	tWR_MPR	tMOD (min) + AL + PL	-	tMOD (min) + AL + PL	-	tMOD (min) + AL + PL	-	tMOD (min) + AL + PL	-	-	
Auto precharge write recovery + precharge time	tDAL(min)	Programmed WR + roundup (tRP / tCK(avg))								nCK	
CS_n to Command Address Latency											
CS_n to Command Address Latency	tCAL	3	-	4	-	4	-	5	-	nCK	
DRAM Data Timing											
DQS_t,DQS_c to DQ skew, per group, per access	tDQSQ	-	0.16	-	0.16	-	0.16	-	0.18	tCK(avg)/2	13,18
DQ output hold time per group, per access from	tQH	0.76	-	0.76	-	0.74	-	0.74	-	tCK(avg)/2	13,17,18, 38,49

Wintec Industries, Inc., reserves the right to change datasheets and/or products without any notice.
© 2020 Wintec Industries, Inc.

Data Valid Window per device per UI: (tQH - tDQSQ) of each UI on a given DRAM	tDVWd	0.63	-	0.64	-	0.64	-	TBD	-	UI	17,18,39,49
Data Valid Window per device per UI: (tQH - tDQSQ) of each UI on a given DRAM Data Valid	tDVWp	0.66	-	0.69	-	0.72	-	0.72	-	UI	17,18,39,49
DQ low impedance time from CK_t, CK_c	tLZ(DQ)	-390	195	-390	180	-330	175	-310	170	ps	39
DQ high impedance time from CK_t, CK_c	tHZ(DQ)	-	195	-	180	-	175	-	170	ps	39

Speed		DDR4-1866		DDR4-2133		DDR4-2400		DDR4-2666		Units	NOTE
Parameter	Symbol	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX		
Data Strobe Timing											
DQS_t, DQS_c differential READ Pre-amble (2 clock preamble)	tRPRE	0.9	Note 44	0.9	Note 44	0.9	Note 44	0.9	Note 44	tCK	40
DQS_t, DQS_c differential READ Postamble	tRPST	0.33	Note 45	0.33	Note 45	0.33	Note 45	0.33	Note 45	tCK	
DQS_t,DQS_c differential output high time	tQSH	0.4	-	0.4	-	0.4	-	0.4	-	tCK	21
DQS_t,DQS_c differential output low time	tQSL	0.4	-	0.4	-	0.4	-	0.4	-	tCK	20
DQS_t, DQS_c differential WRITE Preamble	tWPRE	0.9	-	0.9	-	0.9	-	0.9	-	tCK	
DQS_t, DQS_c differential WRITE Postamble	tWPST	0.33	-	0.33	-	0.33	-	0.33	-	tCK	
DQS_t and DQS_c low-impedance time (Referenced from RL-1)	tLZ(DQS)	-390	195	-360	180	-300	175	-310	170	ps	
DQS_t and DQS_c high-impedance time (Referenced from RL+BL/2)	tHZ(DQS)	-	195	-	180	-	175	-	170	ps	
DQS_t, DQS_c differential input low pulse width	tDQSL	0.46	0.54	0.46	0.54	0.46	0.54	0.46	0.54	tCK	
DQS_t, DQS_c differential input high pulse width	tDQSH	0.46	0.54	0.46	0.54	0.46	0.54	0.46	0.54	tCK	
DQS_t, DQS_c rising edge to CK_t, CK_c rising edge (1 clock	tDQSS	-0.27	0.27	-0.27	0.27	-0.27	0.27	-0.27	0.27	tCK	
DQS_t, DQS_c falling edge setup time to CK_t, CK_c rising edge	tDSS	0.18	-	0.18	-	0.18	-	0.18	-	tCK	
DQS_t, DQS_c falling edge hold time from CK_t, CK_c rising edge	tDSH	0.18	-	0.18	-	0.18	-	0.18	-	tCK	
MPSM Timing											
Command path disable delay upon MPSM entry	tMPED	tMOD(min) + tCPDED(min)	-	tMOD(min) + tCPDED(min)	-	tMOD(min) + tCPDED(min)	-	TBD	-		
Valid clock requirement after MPSM entry	tCKMPE	tMOD(min) + tCPDED(min)	-	tMOD(min) + tCPDED(min)	-	tMOD(min) + tCPDED(min)	-	TBD	-		
Valid clock requirement before MPSM exit	tCKMPX	tCKSRX(min)	-	tCKSRX(min)	-	tCKSRX(min)	-	TBD	-		
Exit MPSM to commands not requiring a locked DLL	tXMP	tXS(min)	-	tXS(min)	-	tXS(min)	-	TBD	-		
Exit MPSM to commands requiring a locked DLL	tXMPDLL	tXMP(min) + tXSDLL(min)	-	tXMP(min) + tXSDLL(min)	-	tXMP(min) + tXSDLL(min)	-	TBD	-		
CS setup time to CKE	tMPX_S	tIS(min) + tIHL(min)	-	tIS(min) + tIHL(min)	-	tIS(min) + tIHL(min)	-	TBD	-		
Calibration Timing											
Power-up and RESET calibration time	tZQinit	1024	-	1024	-	1024	-	1024	-	nCK	
Normal operation Full calibration time	tZQoper	512	-	512	-	512	-	512	-	nCK	
Normal operation Short calibration time	tZQCS	128	-	128	-	128	-	128	-	nCK	
Reset/Self Refresh Timing											
Exit Reset from CKE HIGH to a valid command	tXPR	max (5nCK,tRFC(min) + 10ns)	-	max (5nCK,tRFC (min)+ 10ns)	-	max (5nCK,tRFC (min)+ 10ns)	-	max (5nCK,tRFC (min)+10ns)	-		
Exit Self Refresh to commands not requiring a locked DLL	tXS	tRFC(min)+1 0ns	-	tRFC(min)+1 0ns	-	tRFC(min)+ 1 0ns	-	tRFC(min)+ 10ns	-		

Wintec Industries, Inc., reserves the right to change datasheets and/or products without any notice.
© 2020 Wintec Industries, Inc.

SRX to commands not requiring a locked DLL in Self Refresh ABORT	tXS_ABORT (min)	tRFC4(min)+ 10ns	-	tRFC4(min) + 10ns	-	tRFC4(min) + 10ns	-	tRFC4(min) +10ns	-		
Exit Self Refresh to ZQCL,ZQCS and MRS (CL,CWL,WR,RTP and Gear Down)	tXS_FAST (min)	tRFC4(min)+ 10ns	-	tRFC4(min) + 10ns	-	tRFC4(min) + 10ns	-	tRFC4(min) +10ns	-		
Exit Self Refresh to commands requiring a locked DLL	tXSDLL	tDLLK(min)	-	tDLLK(min)	-	tDLLK(min)	-	tDLLK(min)	-		

Speed		DDR4-1866		DDR4-2133		DDR4-2400		DDR4-2666		Units	NOTE
Parameter	Symbol	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX		
Minimum CKE low width for Self-refresh entry to exit timing	tCKESR	tCKE(min)+1 nCK	-	tCKE(min)+1 nCK	-	tCKE(min)+1 nCK	-	tCKE(min)+ 1nCK	-		
Minimum CKE low width for Self-refresh entry to exit timing with CA Pari- ty enabled	tCKESR_ PAR	tCKE(min)+ 1nCK+PL	-	tCKE(min)+ 1nCK+PL	-	tCKE(min)+ 1nCK+PL	-	tCKE(min)+ 1nCK+PL	-		
Valid Clock Requirement after Self Refresh Entry (SRE) or Power-Down Entry (PDE)	tCKSRE	max(5nCK,10 ns)	-	max(5nCK,10 ns)	-	max(5nCK,10 ns)	-	max (5nCK,10ns)	-		
Valid Clock Requirement after Self Refresh Entry (SRE) or Power-Down when CA Parity is enabled	tCKSRE_PA R	max (5nCK,10ns) +PL	-	max (5nCK,10ns) +PL	-	max (5nCK,10ns) +PL	-	max (5nCK,10ns) +PL	-		
Valid Clock Requirement before Self Refresh Exit (SRX) or Power-Down Exit (PDX) or Reset Exit	tCKSRX	max(5nCK,10 ns)	-	max(5nCK,10 ns)	-	max(5nCK,10 ns)	-	max (5nCK,10ns)	-		
Power Down Timing											
Exit Power Down with DLL on to any valid command; Exit Precharge Power Down with DLL frozen to commands not requiring a locked	tXP	max (4nCK,6ns)	-	max (4nCK,6ns)	-	max (4nCK,6ns)	-	max (4nCK,6ns)	-		
CKE minimum pulse width	tCKE	max (3nCK, 5ns)	-	max (3nCK, 5ns)	-	max (3nCK, 5ns)	-	max (3nCK, 5ns)	-		31,32
Command pass disable delay	tCPDED	4	-	4	-	4	-	4	-	nCK	
Power Down Entry to Exit Timing	tPD	tCKE(min)	9*tREFI	tCKE(min)	9*tREFI	tCKE(min)	9*tREFI	tCKE(min)	9*tREFI		6
Timing of ACT command to Power Down entry	tACTPDEN	1	-	1	-	2	-	2	-	nCK	7
Timing of PRE or PREA command to Power Down entry	tPRPDEN	1	-	1	-	2	-	2	-	nCK	7
Timing of RD/RDA command to Power Down entry	tRDPDEN	RL+4+1	-	RL+4+1	-	RL+4+1	-	RL+4+1	-	nCK	
Timing of WR command to Power Down entry (BL8OTF, BL8MRS, BC4OTF)	tWRPDEN	WL+4+(tWR/ tCK(avg))	-	WL+4+(tWR/ tCK(avg))	-	WL+4+(tWR/ tCK(avg))	-	WL+4+(tWR /tCK(avg))	-	nCK	4
Timing of WRA command to Power Down entry (BL8OTF, BL8MRS, BC4OTF)	tWRAPDEN	WL+4+WR+1	-	WL+4+WR+1	-	WL+4+WR+1	-	WL+4+WR+ 1	-	nCK	5
Timing of WR command to Power Down entry (BC4MRS)	tWRPBC4D EN	WL+2+(tWR/ tCK(avg))	-	WL+2+(tWR/ tCK(avg))	-	WL+2+(tWR/ tCK(avg))	-	WL+2+(tWR /tCK(avg))	-	nCK	4
Timing of WRA command to Power Down entry (BC4MRS)	tWRAPBC4 DEN	WL+2+WR+1	-	WL+2+WR+1	-	WL+2+WR+1	-	WL+2+WR+ 1	-	nCK	5
Timing of REF command to Power Down entry	tREFPDEN	1	-	1	-	2	-	2	-	nCK	7
Timing of MRS command to Power Down entry	tMRSPDEN	tMOD(min)	-	tMOD(min)	-	tMOD(min)	-	tMOD(min)	-		
PDA Timing											
Mode Register Set command cycle time in PDA mode	tMRD_PDA	max(16nCK,1 0ns)		max(16nCK,1 0ns)		max(16nCK,1 0ns)		max(16nCK, 10ns)		nCK	
Mode Register Set command update delay in PDA mode	tMOD_PDA	tMOD		tMOD		tMOD		tMOD		nCK	
ODT Timing											
Asynchronous RTT turn-on delay (Power-Down with DLL frozen)	tAONAS	1.0	9.0	1.0	9.0	1.0	9.0	1.0	9.0	ns	
Asynchronous RTT turn-off delay (Power-Down with DLL frozen)	tAOFAS	1.0	9.0	1.0	9.0	1.0	9.0	1.0	9.0	ns	
RTT dynamic change skew	tADC	0.3	0.7	0.3	0.7	0.3	0.7	0.3	0.7	tCK(avg)	
Write Leveling Timing											
First DQS_t/DQS_n rising edge after write leveling mode is programmed	tWLMRD	40	-	40	-	40	-	40	-	nCK	12
DQS_t/DQS_n delay after write leveling mode is programmed	tWLDQSEN	25	-	25	-	25	-	25	-	nCK	12

Wintec Industries, Inc., reserves the right to change datasheets and/or products without any notice.
© 2020 Wintec Industries, Inc.

Write leveling setup time from rising CK_t, CK_c crossing to rising DQS_t/ DQS_n crossing	tWLS	0.13	-	0.13	-	0.13	-	0.13	-	tCK(avg)	
Write leveling hold time from rising DQS_t/DQS_n crossing to rising CK_t, CK_ crossing	tWLH	0.13	-	0.13	-	0.13	-	0.13	-	tCK(avg)	
Write leveling output delay	tWLO	0	9.5	0	9.5	0	9.5	0	9.5	ns	
Write leveling output error	tWLOE									ns	

Speed		DDR4-1866		DDR4-2133		DDR4-2400		DDR4-2666		Units	NOTE
Parameter	Symbol	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX		
CA Parity Timing											
Commands not guaranteed to be executed during this time	tPAR_UNKNOWN	-	PL	-	PL	-	PL	-	PL		
Delay from errant command to ALERT_n assertion	tPAR_ALERT_ON	-	PL+6ns	-	PL+6ns	-	PL+6ns	-	PL+6ns		
Pulse width of ALERT_n signal when asserted	tPAR_ALERT_PW	56	112	64	128	72	144	80	160	nCK	
Time from when Alert is asserted till controller must start providing DES commands in Persistent CA parity mode	tPAR_ALERT_RSP	-	50	-	57	-	64	-	71	nCK	
Parity Latency	PL	4		4		5		5		nCK	
CRC Error Reporting											
CRC error to ALERT_n latency	tCRC_ALERT	3	13	3	13	3	13	3	13	ns	
CRC ALERT_n pulse width	CRC_ALERT_PW	6	10	6	10	6	10	6	10	nCK	
tREFI											
tRFC1 (min)	2Gb	160	-	160	-	160	-	160	-	ns	34
	4Gb	260	-	260	-	260	-	260	-	ns	34
	8Gb	350	-	350	-	350	-	350	-	ns	34
	16Gb	550	-	550	-	550	-	550	-	ns	34
tRFC2 (min)	2Gb	110	-	110	-	110	-	110	-	ns	34
	4Gb	160	-	160	-	160	-	160	-	ns	34
	8Gb	260	-	260	-	260	-	260	-	ns	34
	16Gb	350	-	350	-	350	-	350	-	ns	34
tRFC4 (min)	2Gb	90	-	90	-	90	-	90	-	ns	34
	4Gb	110	-	110	-	110	-	110	-	ns	34
	8Gb	160	-	160	-	160	-	160	-	ns	34
	16Gb	260	-	260	-	260	-	260	-	ns	34

Note:

1. Start of internal write transaction is defined as follows :
   For BL8 (Fixed by MRS and on-the-fly) :
   Rising clock edge 4 clock cycles after WL.
   For BC4 (on-the-fly) : Rising clock edge 4
   clock cycles after WL.
   For BC4 (fixed by MRS) : Rising clock edge 2 clock cycles after WL.
2. A separate timing parameter will cover the delay from write to read when CRC and DM are simultaneously enabled
3. Commands requiring a locked DLL are: READ (and RAP) and synchronous ODT commands.
4. tWR is defined in ns, for calculation of tWRPDEN it is necessary to round up tWR/tCK to the next integer.
5. WR in clock cycles as programmed in MR0.
6. tREFI depends on TOPER.
7. CKE is allowed to be registered low while operations such as row activation, precharge, autoprecharge or refresh are in progress, but power down IDD spec will not be applied until finishing those operations.
8. For these parameters, the DDR4 SDRAM device supports tnPARAM[nCK]=RU{tPARAM[ns]/tCK(avg)[ns]}, which is in clock cycles assuming all input clock jitter specifications are satisfied

Wintec Industries, Inc., reserves the right to change datasheets and/or products without any notice.
© 2020 Wintec Industries, Inc.

9. When CRC and DM are both enabled, tWR_CRC_DM is used in place of tWR.
10. When CRC and DM are both enabled tWTR_S_CRC_DM is used in place of tWTR_S.
11. When CRC and DM are both enabled tWTR_L_CRC_DM is used in place of tWTR_L.
12. The max values are system dependent.
13. DQ to DQS total timing per group where the total includes the sum of deterministic and random timing terms for a specified BER. BER spec and measurement method are tbd.
14. The deterministic component of the total timing. Measurement method tbd.
15. DQ to DQ static offset relative to strobe per group. Measurement method tbd.
16. This parameter will be characterized and guaranteed by design.
17U When the device is operated with the input clock jitter, this parameter needs to be derated by the actual tjit(per)_total of the input clock. (output deratings are relative to the SDRAM input clock). Example tbd.
18. DRAM DBI mode is off.
19. DRAM DBI mode is enabled. Applicable to x8 and x16 DRAM only.
20. tQSL describes the instantaneous differential output low pulse width on DQS_t - DQS_c, as measured from on falling edge to the next consecutive rising edge
21. tQSH describes the instantaneous differential output high pulse width on DQS_t - DQS_c, as measured from on falling edge to the next consecutive rising edge
22. There is no maximum cycle time limit besides the need to satisfy the refresh interval tREFI
23. tCH(abs) is the absolute instantaneous clock high pulse width, as measured from one rising edge to the following falling edge
24. tCL(abs) is the absolute instantaneous clock low pulse width, as measured from one falling edge to the following rising edge
25. Total jitter includes the sum of deterministic and random jitter terms for a specified BER. BER target and measurement method are tbd.
26. The deterministic jitter component out of the total jitter. This parameter is characterized and guaranteed by design.
27. This parameter has to be even number of clocks
28. When CRC and DM are both enabled, tWR_CRC_DM is used in place of tWR.
29. When CRC and DM are both enabled tWTR_S_CRC_DM is used in place of tWTR_S.
30. When CRC and DM are both enabled tWTR_L_CRC_DM is used in place of tWTR_L.
31. After CKE is registered LOW, CKE signal level shall be maintained below VILDC for tCKE specification (Low pulse width).
32. After CKE is registered HIGH, CKE signal level shall be maintained above VIHDC for tCKE specification (HIGH pulse width).
33. Defined between end of MPR read burst and MRS which reloads MPR or disables MPR function.
34. Parameters apply from tCK(avg)min to tCK(avg)max at all standard JEDEC clock period values as stated in the Speed Bin Tables.
35. This parameter must keep consistency with Speed-Bin Tables .
36. DDR4-1866 AC timing apply if DRAM operates at lower than 1866 MT/s data rate. UI=tCK(avg).min/2
37. applied when DRAM is in DLL ON mode.
38. Assume no jitter on input clock signals to the DRAM
39. Value is only valid for RZQ/7 RONNOM = 34 ohms
40. 1tCK toggle mode with setting MR4:A11 to 0
41. 2tCK toggle mode with setting MR4:A11 to 1, which is valid for DDR4-2400/2666/3200 speed grade.
42. 1tCK mode with setting MR4:A12 to 0
43. 2tCK mode with setting MR4:A12 to 1, which is valid for DDR4-2400/2666/3200 speed grade.
44. The maximum read preamble is bounded by tLZ(DQS)min on the left side and tDQSCK(max) on the right side.
45. DQ falling signal middle-point of transferring from High too Low to first rising edge of DQS diff-signal cross-point
46. last falling edge of DQS diff-signal cross-point to DQ rising signal middle-point of transferring from Low to High
47. VrefDQ value must be set to either its midpoint or Vcent_DQ(midpoint) in order to capture DQ0 or DQL0 low level for entering PDA mode.
48. The maximum read postamble is bound by tDQSCK(min) plus tQSH(min) on the left side and tHZ(DQS)max on the right side.
49. Reference level of DQ output signal is specified with a midpoint as a widest part of Output signal eye which should be approximately 0.7 * VDDQ as a center level of the static single-ended output peak-to-peak swing with a driver impedance of 34 ohms and an effective test load of 50 ohms to VTT = VDDQ .
50. For MR7 commands, the minimum delay to a subsequent non-MRS command is 5nCK.

Wintec Industries, Inc., reserves the right to change datasheets and/or products without any notice.
© 2020 Wintec Industries, Inc.

IDD Specification Definition

Symbol	Description
IDD0	**Operating One Bank Active-Precharge Current (AL=0)** **CKE:** High; **External clock:** On; **tCK, nRC, nRAS, CL**: Refer to Component Datasheet for detail pattern; **BL:** 8[1]; **AL:** 0; **CS_n:** High between ACT and PRE; **Command, Address, Bank Group Address, Bank Address Inputs:** partially toggling; **Data IO:** VDDQ; **DM_n:** stable at 1; **Bank Activity:** Cycling with one bank active at a time: 0,0,1,1,2,2,... ; **Output Buffer and RTT:** Enabled in Mode Registers[2]; **ODT Signal:** stable at 0; **Pattern Details:** Refer to Component Datasheet for detail pattern
IDD0A	**Operating One Bank Active-Read-Precharge Current (AL=CL-1)** **AL = CL-1, Other conditions:** see IDD0
IPP0	**Operating One Bank Active-Precharge IPP Current Same condition with IDD0**
IDD1	**Operating One Bank Active-Read-Precharge Current (AL=0)** **CKE:** High; **External clock:** On; **tCK, nRC, nRAS, nRCD, CL**: Refer to Component Datasheet for detail pattern; **BL:** 8[1]; **AL:** 0; **CS_n**: High between ACT, RD and PRE; **Command, Address, Bank Group Address, Bank Address Inputs, Data IO:** partially toggling; **DM_n:** stable at 1; **Bank Activity:** Cycling with one bank active at a time: 0,0,1,1,2,2,... ; **Output Buffer and RTT:** Enabled in Mode Registers[2]; **ODT Signal:** stable at 0; **Pattern Details:** Refer to Component Datasheet for detail pattern
IDD1A	**Operating One Bank Active-Read-Precharge Current (AL=CL-1)** **AL = CL-1, Other conditions:** see IDD1
IPP1	**Operating One Bank Active-Read-Precharge IPP Current** **Same condition with IDD1**
IDD2N	**Precharge Standby Current (AL=0)** **CKE**: High; **External clock:** On; **tCK, CL**: Refer to Component Datasheet for detail pattern; **BL:** 8[1]; **AL:** 0; **CS_n**: stable at 1; **Command, Address, Bank Group Address, Bank Address Inputs:** partially toggling ; **Data IO:** VDDQ; **DM_n:** stable at 1; **Bank Activity:** all banks closed; **Output Buffer and RTT:** Enabled in Mode Registers[2]; **ODT Signal:** stable at 0; **Pattern Details:** Refer to Component Datasheet for detail pattern
IDD2NA	**Precharge Standby Current (AL=CL-1)** **AL = CL-1, Other conditions:** see IDD2N
IPP2N	**Precharge Standby IPP Current Same condition with IDD2N**
IDD2NT	**Precharge Standby ODT Current** **CKE**: High; **External clock:** On; **tCK, CL**: Refer to Component Datasheet for detail pattern; **BL:** 8[1]; **AL:** 0; **CS_n**: stable at 1; **Command, Address, Bank Group Address, Bank Address Inputs:** partially toggling ; **Data IO: VSSQ**; **DM_n:** stable at 1; **Bank Activity:** all banks closed; **Output Buffer and RTT:** Enabled in Mode Registers[2]; **ODT Signal:** toggling according ; **Pattern Details:** Refer to Component Datasheet for detail pattern
IDDQ2NT (Optional)	**Precharge Standby ODT IDDQ Current** Same definition like for IDD2NT, however measuring IDDQ current instead of IDD current
IDD2NL	**Precharge Standby Current with CAL enabled** Same definition like for IDD2N, CAL enabled[3]
IDD2NG	**Precharge Standby Current with Gear Down mode enabled** Same definition like for IDD2N, Gear Down mode enabled[3,5]
IDD2ND	**Precharge Standby Current with DLL disabled** Same definition like for IDD2N, DLL disabled[3]
IDD2N_par	**Precharge Standby Current with CA parity enabled** Same definition like for IDD2N, CA parity enabled[3]
IDD2P	**Precharge Power-Down Current CKE:** Low; **External clock:** On; **tCK, CL**: Refer to Component Datasheet for detail pattern; **BL:** 8[1]; **AL:** 0; **CS_n**: stable at 1; **Command, Address, Bank Group Address, Bank Address Inputs:** stable at 0; **Data IO:** VDDQ; **DM_n:** stable at 1;**Bank Activity:** all banks closed; **Output Buffer and RTT:** Enabled in Mode Registers[2];**ODT Signal:** stable at 0
IPP2P	**Precharge Power-Down IPP Current Same condition with IDD2P**

Wintec Industries, Inc., reserves the right to change datasheets and/or products without any notice.
© 2020 Wintec Industries, Inc.

Symbol	Description
IDD2Q	**Precharge Quiet Standby Current** **CKE**: High; **External clock:** On; **tCK, CL**: Refer to Component Datasheet for detail pattern; **BL:** 8[1]; **AL:** 0; **CS_n**: stable at 1; **Command, Address, Bank Group Address, Bank Address Inputs:** stable at 0; **Data IO:** VDDQ; **DM_n:** stable at 1;**Bank Activity:** all banks closed; **Output Buffer and RTT:** Enabled in Mode Registers[2]; **ODT Signal:** stable at 0
IDD3N	**Active Standby Current** **CKE: High; External clock: On; tCK, CL: Refer to Component Datasheet for detail pattern; BL: 81; AL: 0; CS_n: stable at 1; Command, Address, Bank Group Address, Bank Address Inputs: partially toggling ; Data IO: VDDQ; DM_n: stable at 1;Bank Activity: all banks open; Output Buffer and RTT: Enabled in Mode Registers2; ODT Signal: stable at 0; Pattern Details: Refer to Component Datasheet for detail pattern**
IDD3NA	**Active Standby Current (AL=CL-1)** **AL = CL-1, Other conditions: see IDD3N**
IPP3N	**Active Standby IPP Current** **Same condition with IDD3N**
IDD3P	**Active Power-Down Current** **CKE: Low; External clock: On; tCK, CL: s Refer to Component Datasheet for detail pattern; BL: 81; AL: 0; CS_n: stable at 1; Command, Address, Bank Group Address, Bank Address Inputs: stable at 0; Data IO: VDDQ; DM_n: stable at 1; Bank Activity: all banks open; Output Buffer and RTT: Enabled in Mode Registers2; ODT Signal: stable at 0**
IPP3P	**Active Power-Down IPP Current** **Same condition with IDD3P**
IDD4R	**Operating Burst Read Current** **CKE: High; External clock: On; tCK, CL: Refer to Component Datasheet for detail pattern; BL: 82; AL: 0; CS_n: High between RD; Command, Address, Bank Group Address, Bank Address Inputs: partially toggling ; Data IO: seamless read data burst with different data between one burst and the next one according ; DM_n: stable at 1; Bank Activity: all banks open, RD commands cycling through banks: 0,0,1,1,2,2,... ; Output Buffer and RTT: Enabled in Mode Registers2; ODT Signal: stable at 0; Pattern Details: Refer to Component Datasheet for detail pattern**
IDD4RA	**Operating Burst Read Current (AL=CL-1)** **AL = CL-1, Other conditions: see IDD4R**
IDD4RB	**Operating Burst Read Current with Read DBI** **Read DBI enabled3, Other conditions: see IDD4R**
IPP4R	**Operating Burst Read IPP Current** **Same condition with IDD4R**
IDDQ4R (Optional)	**Operating Burst Read IDDQ Current** **Same definition like for IDD4R, however measuring IDDQ current instead of IDD current**
IDDQ4RB (Optional)	**Operating Burst Read IDDQ Current with Read DBI** **Same definition like for IDD4RB, however measuring IDDQ current instead of IDD current**
IDD4W	**Operating Burst Write Current** **CKE: High; External clock: On; tCK, CL: Refer to Component Datasheet for detail pattern; BL: 81; AL: 0; CS_n: High between WR; Command, Address, Bank Group Address, Bank Address Inputs: partially toggling ; Data IO: seamless write data burst with different data between one burst and the next one ; DM_n: stable at 1; Bank Activity: all banks open, WR commands cycling through banks: 0,0,1,1,2,2,... ; Output Buffer and RTT: Enabled in Mode Registers2; ODT Signal: stable at HIGH; Pattern Details: Refer to Component Datasheet for detail pattern**
IDD4WA	**Operating Burst Write Current (AL=CL-1)** **AL = CL-1, Other conditions: see IDD4W**
IDD4WB	**Operating Burst Write Current with Write DBI** **Write DBI enabled3, Other conditions: see IDD4W**
IDD4WC	**Operating Burst Write Current with Write CRC** **Write CRC enabled3, Other conditions: see IDD4W**
IDD4W_par	**Operating Burst Write Current with CA Parity** **CA Parity enabled3, Other conditions: see IDD4W**
IPP4W	**Operating Burst Write IPP Current** **Same condition with IDD4W**
IDD5B	**Burst Refresh Current (1X REF)** **CKE: High; External clock: On; tCK, CL, nRFC: Refer to Component Datasheet for detail pattern; BL: 81; AL: 0; CS_n: High between REF; Command, Address, Bank Group Address, Bank Address Inputs: partially toggling ; Data IO: VDDQ; DM_n: stable at 1; Bank Activity: REF command every nRFC ; Output Buffer and RTT: Enabled in Mode Registers2; ODT Signal: stable at 0; Pattern Details: Refer to Component Datasheet for detail pattern**

Wintec Industries, Inc., reserves the right to change datasheets and/or products without any notice.
© 2020 Wintec Industries, Inc.

IPP5B	**Burst Refresh Write IPP Current (1X REF)** **Same condition with IDD5B**
IDD5F2	**Burst Refresh Current (2X REF)** **tRFC=tRFC_x2, Other conditions: see IDD5B**
IPP5F2	**Burst Refresh Write IPP Current (2X REF)** **Same condition with IDD5F2**
IDD5F4	**Burst Refresh Current (4X REF)** **tRFC=tRFC_x4, Other conditions:** see IDD5B
IPP5F4	**Burst Refresh Write IPP Current** **(4X REF) Same condition with IDD5F4**
IDD6N	**Self-Refresh Current: Normal Temperature Range** **T_{CASE}:** 0 - 85°C; **Low Power Array Self Refresh (LP ASR)** : Normal[4]; **CKE:** Low; **External clock:** Off; CK_t and CK_c#: LOW; **CL**: Refer to Component Datasheet for detail pattern; **BL:** 8[1]; **AL:** 0; **CS_n#, Command, Address, Bank Group Address, Bank Address, Data IO:** High; **DM_n:** stable at 1; **Bank Activity:** Self-Refresh operation; **Output Buffer and RTT:** Enabled in Mode Registers[2]; **ODT Signal:** MID- LEVEL
IPP6N	**Self-Refresh IPP Current: Normal** **Temperature Range Same condition with IDD6N**
IDD6E	**Self-Refresh Current: Extended Temperature Range**) **T_{CASE}:** 0 - 95°C; **Low Power Array Self Refresh (LP ASR)** : Extended[4]; **CKE:** Low; **External clock:** Off; CK_t and CK_c: LOW; **CL**: Refer to Component Datasheet for detail pattern; **BL:** 8[1]; **AL:** 0; **CS_n, Command, Address, Bank Group Address, Bank Address, Data** **IO:** High; **DM_n**:stable at 1; **Bank Activity:** Extended Temperature Self-Refresh operation; **Output Buffer and RTT:** Enabled in Mode Registers[2]; **ODT Signal:** MID-LEVEL
IPP6E	**Self-Refresh IPP Current: Extended** **Temperature Range Same condition with IDD6E**
IDD6R	**Self-Refresh Current: Reduced Temperature Range** **T_{CASE}:** 0 - 45°C; **Low Power Array Self Refresh (LP ASR)** : Reduced[4]; **CKE:** Low; **External clock:** Off; CK_t and CK_c#: LOW; **CL**: Refer to Component Datasheet for detail pattern; **BL:** 8[1]; **AL:** 0; **CS_n#, Command, Address, Bank Group Address, Bank Address, Data IO:** High; **DM_n**:stable at 1; **Bank Activity:** Extended Temperature Self-Refresh operation; **Output Buffer and RTT:** Enabled in Mode Registers[2]; **ODT Signal:** MID-LEVEL
IPP6R	**Self-Refresh IPP Current: Reduced Temperature** **Range Same condition with IDD6R**
IDD6A	**Auto Self-Refresh Current** **T_{CASE}:** 0 - 95°C; **Low Power Array Self Refresh (LP ASR)** : Auto[4]; **CKE:** Low; **External clock:** Off; CK_t and CK_c#: LOW; **CL**: Refer to Component Datasheet for detail pattern; **BL:** 8[1]; **AL:** 0; **CS_n#, Command, Address, Bank Group Address, Bank Address, Data IO:** High; **DM_n**:stable at 1; **Bank Activity:** Auto Self-Refresh operation; **Output Buffer and RTT:** Enabled in Mode Registers[2]; **ODT Signal:** MID-LEVEL
IPP6A	**Auto Self-Refresh IPP Current** **Same condition with IDD6A**
IDD7	**Operating Bank Interleave Read Current CKE:** High; **External clock:** On; **tCK, nRC, nRAS, nRCD, nRRD, nFAW, CL**: Refer to Component Datasheet for detail pattern; **BL:** 8[1]; **AL:** CL-1; **CS_n**: High between ACT and RDA; **Command, Address, Bank Group Address, Bank Address Inputs:** partially toggling ; **Data IO:** read data bursts with different data between one burst and the next one ; **DM_n:** stable at 1; **Bank Activity:** two times interleaved cycling through banks (0, 1, ...7) with different addressing; **Output Buffer and RTT:** Enabled in Mode Registers[2]; **ODT Signal:** stable at 0; **Pattern Details:** Refer to Component Datasheet for detail pattern
IPP7	**Operating Bank Interleave Read IPP** **Current Same condition with IDD7**
IDD8	**Maximum Power Down Current TBD**
IPP8	**Maximum Power Down IPP Current Same condition with IDD8**

Wintec Industries, Inc., reserves the right to change datasheets and/or products without any notice.
© 2020 Wintec Industries, Inc.

IDD Spec Table

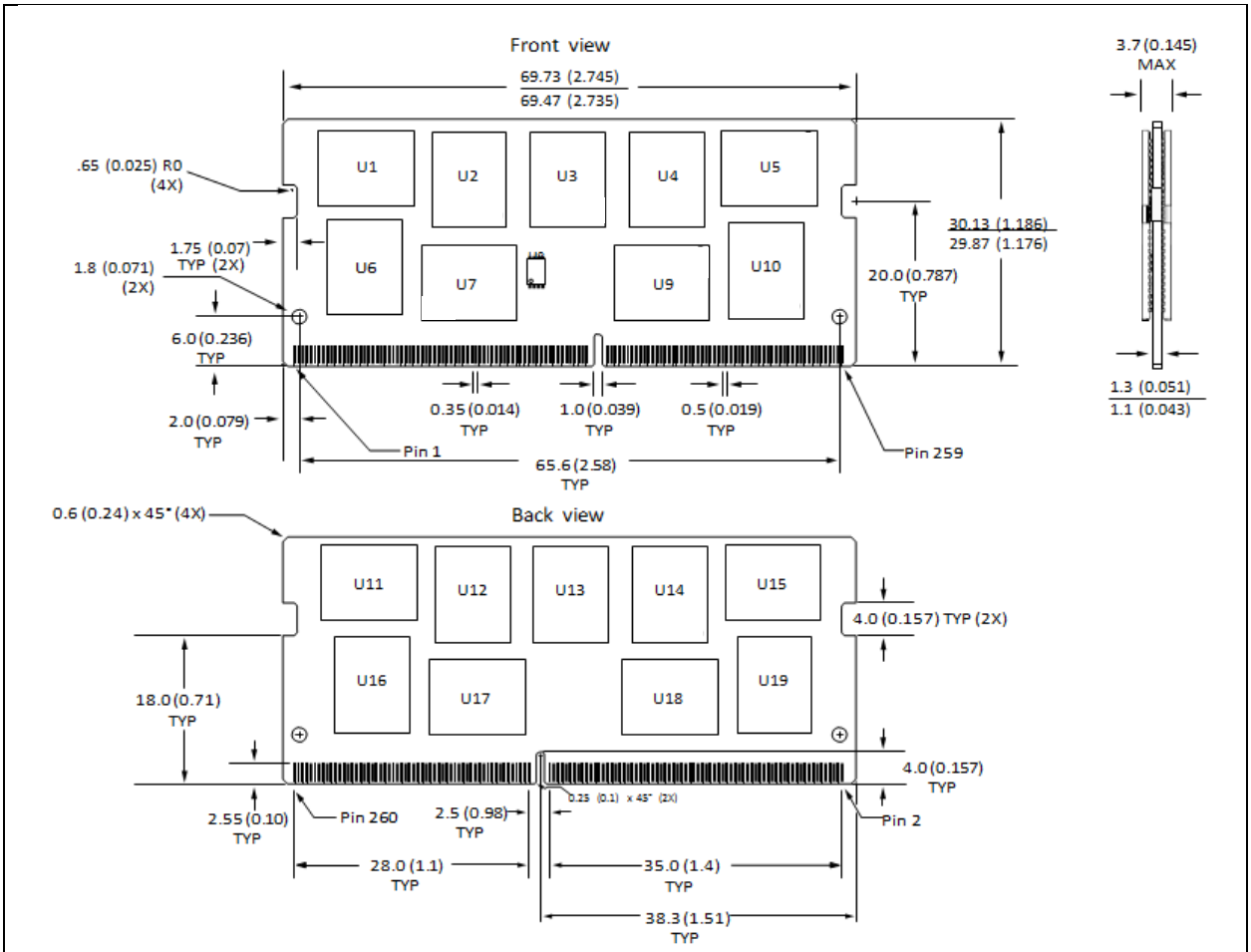
Symbol	8GB(1Gx72) Module						Unit
	DDR4-2133		DDR4-2400		DDR4-2666		
	15-15-15		17-17-17		19-19-19		
	VDD 1.2V	VPP 2.5V	VDD 1.2V	VPP 2.5V	VDD 1.2V	VPP 2.5V	
	IDD Max.	IPP Max.	IDD Max.	IPP Max.	IDD Max.	IPP Max.	
I_{DD0}	279	36	279	36	288	36	mA
I_{DD0A}	288	36	306	36	315	36	mA
I_{DD1}	396	36	405	36	405	36	mA
I_{DD1A}	423	36	432	36	459	36	mA
I_{DD2N}	198	27	207	27	207	27	mA
I_{DD2NA}	225	27	234	27	234	27	mA
I_{DD2NT}	225	27	234	27	234	27	mA
I_{DD2NL}	135	27	153	27	153	27	mA
I_{DD2NG}	198	27	207	27	207	27	mA
I_{DD2ND}	180	27	189	27	189	27	mA
I_{DD2N_par}	207	27	216	27	216	27	mA
I_{DD2P}	144	27	144	27	144	27	mA
I_{DD2Q}	180	27	189	27	189	27	mA
I_{DD3N}	324	27	324	27	324	27	mA
I_{DD3NA}	342	27	342	27	342	27	mA
I_{DD3P}	189	27	198	27	198	27	mA
I_{DD4R}	909	27	963	27	1116	27	mA
I_{DD4RA}	945	27	999	27	1170	27	mA
I_{DD4RB}	918	27	981	27	1125	27	mA
I_{DD4W}	756	27	801	27	909	27	mA
I_{DD4WA}	792	27	846	27	954	27	mA
I_{DD4WB}	756	27	810	27	918	27	mA
I_{DD4WC}	666	27	747	27	846	27	mA
I_{DD4W_par}	828	27	891	27	1008	27	mA
I_{DD5B}	1791	162	1791	162	1944	162	mA
I_{DD5F2}	1242	135	1251	135	1350	135	mA
I_{DD5F4}	1044	126	1053	126	1134	126	mA
I_{DD6N}	207	36	207	36	216	36	mA
I_{DD6E}	306	45	306	45	324	54	mA
I_{DD6R}	144	36	144	36	144	36	mA
I_{DD6A}	198	36	198	36	198	36	mA
I_{DD7}	1278	72	1287	81	1395	81	mA
I_{DD8}	99	27	99	27	99	27	mA

Wintec Industries, Inc., reserves the right to change datasheets and/or products without any notice.
© 2020 Wintec Industries, Inc.

Symbol	16GB(2Gx72) Module						Unit
	DDR4-2133		DDR4-2400		DDR4-2666		
	15-15-15		17-17-17		19-19-19		
	VDD 1.2V	VPP 2.5V	VDD 1.2V	VPP 2.5V	VDD 1.2V	VPP 2.5V	
	IDD Max.	IPP Max.	IDD Max.	IPP Max.	IDD Max.	IPP Max.	
I_{DD0}	477	63	486	63	516	63	mA
I_{DD0A}	486	63	513	63	545	63	mA
I_{DD1}	594	63	612	63	646	63	mA
I_{DD1A}	621	63	639	63	676	63	mA
I_{DD2N}	396	54	414	54	422	54	mA
I_{DD2NA}	450	54	468	54	498	54	mA
I_{DD2NT}	450	54	468	54	473	54	mA
I_{DD2NL}	270	54	306	54	323	54	mA
I_{DD2NG}	396	54	414	54	430	54	mA
I_{DD2ND}	360	54	378	54	383	54	mA
I_{DD2N_par}	414	54	432	54	440	54	mA
I_{DD2P}	288	54	288	54	297	54	mA
I_{DD2Q}	360	54	378	54	383	54	mA
I_{DD3N}	648	54	648	54	686	54	mA
I_{DD3NA}	684	54	684	54	737	54	mA
I_{DD3P}	378	54	396	54	409	54	mA
I_{DD4R}	1107	54	1170	54	1241	54	mA
I_{DD4RA}	1143	54	1206	54	1283	54	mA
I_{DD4RB}	1116	54	1188	54	1260	54	mA
I_{DD4W}	954	54	1008	54	1079	54	mA
I_{DD4WA}	990	54	1053	54	1139	54	mA
I_{DD4WB}	954	54	1017	54	1096	54	mA
I_{DD4WC}	864	54	954	54	1037	54	mA
I_{DD4W_par}	1026	54	1098	54	1184	54	mA
I_{DD5B}	1989	189	1998	189	2128	189	mA
I_{DD5F2}	1440	162	1458	162	1539	162	mA
I_{DD5F4}	1242	153	1260	153	1340	153	mA
I_{DD6N}	414	72	414	72	451	72	mA
I_{DD6E}	612	90	612	90	645	90	mA
I_{DD6R}	288	63	288	63	296	63	mA
I_{DD6A}	396	72	396	72	418	72	mA
I_{DD7}	1476	99	1494	104	1640	104	mA
I_{DD8}	198	54	198	54	206	54	mA

Wintec Industries, Inc., reserves the right to change datasheets and/or products without any notice.
© 2020 Wintec Industries, Inc.

Physical Dimensions
260-Pin DDR4 SODIMM 2-Rank



Notes:
1. All dimensions are in millimeters (inches); MAX/MIN or typical (TYP) where noted.
2. The dimensional diagram is for reference only.

Wintec Industries, Inc., reserves the right to change datasheets and/or products without any notice.
© 2020 Wintec Industries, Inc.

Ordering Guide:

DDR4-1866, 2133, 2400, 2666MTs, x8, ECC SODIMM

WD4SE *V (W)WWW XX Y Zz(R) - AAA*

W	Wintec
D4	1.2V DDR4 SDRAM
SE	Unbuffered ECC, X8, 9-Chips 1-rank,18-Chips 2-rank 260-Pin SODIMM Low Profile (1.181" / 29.99 mm)

V	# DRAM IC
8	18
9	9

WWWW	
004G	4GB
008G	8GB
016G	16GB

XX	Speed
18	1866
21	2133
24	2400
26	2666

Y	Latency
P	CL13
R	CL15
T	CL17
V	CL19

Zz	DRAM
S	Samsung
M	Micron

Die	
A	A-Die
B	B-Die
C	C-Die
D	D-Die
E	E-Die
F	F-Die

Capacity	Part Number	Module Speed	DRAM Configuration	Components	Rank
4GB	WD4SE9004G18PSE	1866@CL13	512M x 8	9	1
	WD4SE9004G21RSE	2133@CL15			
	WD4SE9004G24TSE	2400@CL17			
	WD4SE9004G26VSC	2666@CL19			
8GB	WD4SE9008G18PSB	1866@CL13	1G x 8	9	1
	WD4SE9008G21RSB	2133@CL15			
	WD4SE9008G24TSB	2400@CL17			
	WD4SE9008G26VSC	2666@CL19			
8GB	WD4SE8008G18PSE	1866@CL13	512M x 8	18	2
	WD4SE8008G21RSE	2133@CL15			
	WD4SE8008G24TSE	2400@CL17			
	WD4SE8008G24TSF	2400@CL17			
	WD4SE8008G26VSC	2666@CL19			
16GB	WD4SE8016G18PSB	1866@CL13	1G x 8	18	2
	WD4SE8016G21RSB	2133@CL15			
	WD4SE8016G24TSB	2400@CL17			
	WD4SE8016G26VSC	2666@CL19			

Orderable Examples:

WD4SE8008G24TSF
260 SODM 8GB DDR4-2400 512 X8 @ CL17 ECC 2Rx8 SAM F, RoHS

Wintec Industries, Inc., reserves the right to change datasheets and/or products without any notice.
© 2020 Wintec Industries, Inc.

Contact Us:
Wintec Industries OEM Group
8674 Thornton Avenue
Newark, CA 94560
Phone: 510-953-7400
Fax: 510-953-7414

oemsales@wintecind.com
http://www.wintecind.com/oem

Revision History:

Revision 2.00 (Sept 2015)
- Preliminary Release

Revision 2.01 (June 2016)
- Added Samsung E-die

Revision 2.02 (July 2016)
- Updated contact information

Revision 2.03 (August 2016)
- Added 1 Rank configuration

Revision 2.04 (September 2016)
- Corrected PNs in Ordering Guide

Revision 2.05 (September 2016)
- Added 1866-part numbers

Revision 2.06 (June 2017)
- Corrected DQ Map
- Add Speed Bins

Revision 2.07 (July 2017)
- Added IDD Table
- Corrected Voltage rating

Revision 2.08 (March 2018)
- Added new dies

Revision 2.09 (May 2018)
- Added SPD table

Revision 2.10 (June 2018)
- Added 2666MHz

About Wintec Industries, Inc.

Wintec, founded in 1988, is headquartered in Newark, California. Wintec, a leading third-party memory module manufacturer, specializes in a variety of module design and manufacturing, such as memory module, flash module, Handspring module, modem module, game module, etc. Besides a complete line of DDR, SDR, and EDO/FPM legacy memory modules, Wintec also distribute CPU, motherboard, peripherals, PC software, and consumer Flash products (such as MMC, SD, SMC, Compact Flash, PC Card, etc.). With excellent design engineering and manufacturing capability, Wintec provides a wide range of design and manufacturing services for our valuable customers from concept design to final product delivery. Wintec is ISO9001-certified.

Important Notice

Wintec Industries, Inc. makes no representations or warranties with respect to the contents of this User Guide and specifically disclaims any implied warranties of any product design for any particular purpose. Wintec Industries, Inc. reserves the rights to revise this publication and to make changes from time to time in the content hereof without obligation of Wintec Industries, Inc. to notify any person or organization of such revisions or changes.

Wintec Industries, Inc., reserves the right to change datasheets and/or products without any notice.
© 2020 Wintec Industries, Inc.