DS90CR483 / DS90CR484 48-Bit LVDS Channel Link SER/DES — 33 - 112 MHz

Check for Samples: DS90CR483, DS90CR484

FEATURES

- **Up to 5.38 Gbits/sec Bandwidth**
- **33 MHz to 112 MHz Input Clock Support**
- **LVDS SER/DES Reduces Cable and connector Size**
- **Pre-Emphasis Reduces Cable Loading Effects**
- **DC Balance Data Transmission Provided by Transmitter Reduces ISI Distortion**
- **Cable Deskew of +/−1 LVDS Data Bit Time (up to 80 MHz Clock Rate)**
- **5V Tolerant TxIN and Control Input Pins**
- **Flow Through Pinout for Easy PCB Design**
- **+3.3V Supply Voltage**
- **Transmitter Rejects Cycle-to-Cycle Jitter**
- **Conforms to ANSI/TIA/EIA-644-1995 LVDS Standard**
- **Both Devices are Available in 100 Lead TQFP Package**

DESCRIPTION

The DS90CR483 transmitter converts 48 bits of CMOS/TTL data into eight LVDS (Low Voltage Differential Signaling) data streams. A phase-locked transmit clock is transmitted in parallel with the data streams over a ninth LVDS link. Every cycle of the transmit clock 48 bits of input data are sampled and transmitted. The DS90CR484 receiver converts the LVDS data streams back into 48 bits of CMOS/TTL data. At a transmit clock frequency of 112MHz, 48 bits of TTL data are transmitted at a rate of 672Mbps per LVDS data channel. Using a 112MHz clock, the data throughput is 5.38Gbit/s (672Mbytes/s).

The multiplexing of data lines provides a substantial cable reduction. Long distance parallel single-ended buses typically require a ground wire per active signal (and have very limited noise rejection capability). Thus, for a 48-bit wide data and one clock, up to 98 conductors are required. With this Channel Link chipset as few as 19 conductors (8 data pairs, 1 clock pair and a minimum of one ground) are needed. This provides an 80% reduction in cable width, which provides a system cost savings, reduces connector physical size and cost, and reduces shielding requirements due to the cables' smaller form factor.

The 48 CMOS/TTL inputs can support a variety of signal combinations. For example, 6 8-bit words or 5 9-bit (byte + parity) and 3 controls.

The DS90CR483/DS90CR484 chipset is improved over prior generations of Channel Link devices and offers higher bandwidth support and longer cable drive with three areas of enhancement. To increase bandwidth, the maximum clock rate is increased to 112 MHz and 8 serialized LVDS outputs are provided. Cable drive is enhanced with a user selectable pre-emphasis feature that provides additional output current during transitions to counteract cable loading effects. Optional DC balancing on a cycle-to-cycle basis, is also provided to reduce ISI (Inter-Symbol Interference). With pre-emphasis and DC balancing, a low distortion eye-pattern is provided at the receiver end of the cable. A cable deskew capability has been added to deskew long cables of pair-to-pair skew of up to +/−1 LVDS data bit time (up to 80 MHz Clock Rate). These three enhancements allow cables 5+ meters in length to be driven.

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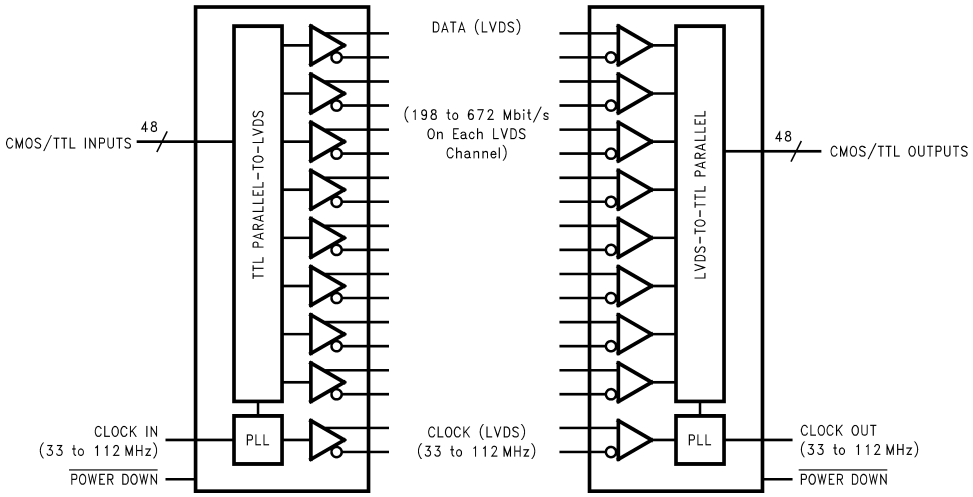
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DESCRIPTION (CONTINUED)

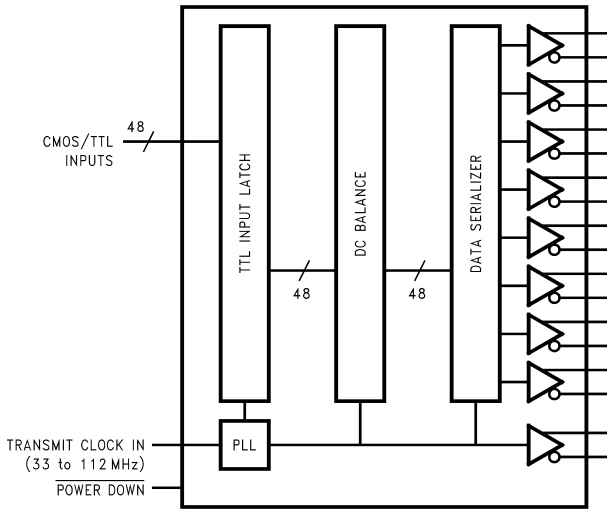
The chipset is an ideal means to solve EMI and cable size problems associated with wide, high speed TTL interfaces.

For more details, please refer to the APPLICATIONS INFORMATION section of this datasheet.

Generalized Block Diagrams

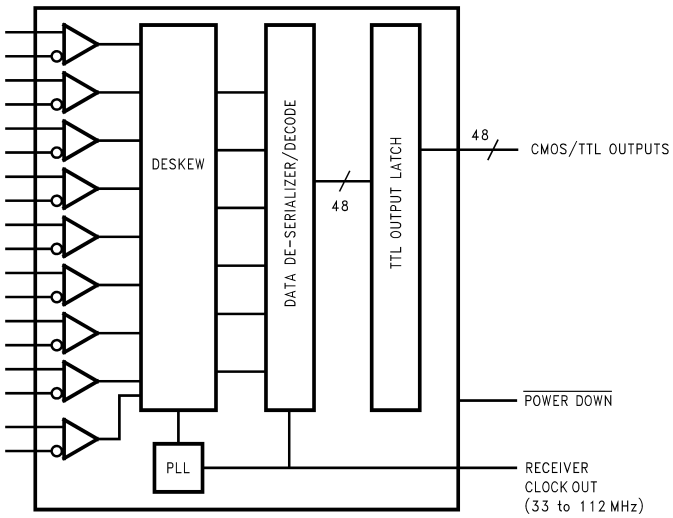


Generalized Transmitter Block Diagram



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Generalized Receiver Block Diagram



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings[1][2]

Supply Voltage (V_{CC})			−0.3V to +4V
CMOS/TTL Input Voltage			−0.3V to +5.5V
LVCMOS/TTL Output Voltage			−0.3V to (V_{CC} + 0.3V)
LVDS Receiver Input Voltage			−0.3V to +3.6V
LVDS Driver Output Voltage			−0.3V to +3.6V
LVDS Output Short Circuit Duration			Continuous
Junction Temperature			+150°C
Storage Temperature			−65°C to +150°C
Lead Temperature (Soldering, 4 sec.)	100L TQFP		+260°C
Maximum Package Power Dissipation Capacity @ 25°C	100 TQFP Package	DS90CR483VJD	2.3W
		DS90CR484VJD	2.3W
Package Derating		DS90CR483VJD	18.1mW/°C above +25°C
		DS90CR484VJD	18.1mW/°C above +25°C
ESD Rating		DS90CR483	
		(HBM, 1.5kΩ, 100pF)	> 6 kV
		(EIAJ, 0Ω, 200pF)	> 300 V
		DS90CR484	
		(HBM, 1.5kΩ, 100pF)	> 2 kV
		(EIAJ, 0Ω, 200pF)	> 200 V

(1) "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be ensured. They are not meant to imply that the device should be operated at these limits. "Electrical Characteristics" specify conditions for device operation.
(2) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/Distributors for availability and specifications.

Recommended Operating Conditions

	Min	Nom	Max	Units
Supply Voltage (V_{CC})	3.0	3.3	3.6	V
Operating Free Air Temperature (T_A)	−10	+25	+70	°C
Receiver Input Range	0		2.4	V
Supply Noise Voltage			100	mV_{p-p}

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Recommended Operating Conditions (continued)

	Min	Nom	Max	Units
Input Clock (TX)	33		112	MHz

Electrical Characteristics[1][2]

Over recommended operating supply and temperature ranges unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Units
CMOS/TTL DC SPECIFICATIONS							
V_{IH}	High Level Input Voltage			2.0			V
V_{IL}	Low Level Input Voltage			GND		0.8	V
V_{OH}	High Level Output Voltage	I_{OH} = −0.4 mA		2.7	3.3		V
		I_{OH} = −2mA		2.7	2.85		V
V_{OL}	Low Level Output Voltage	I_{OL} = 2 mA			0.1	0.3	V
V_{CL}	Input Clamp Voltage	I_{CL} = −18 mA			−0.79	−1.5	V
I_{IN}	Input Current	V_{IN} = 0.4V, 2.5V or V_{CC}			+1.8	+15	µA
		V_{IN} = GND		−15	0		µA
I_{OS}	Output Short Circuit Current	V_{OUT} = 0V				−120	mA
LVDS DRIVER DC SPECIFICATIONS							
$\|V_{OD}\|$	Differential Output Voltage	R_L = 100Ω		250	345	450	mV
ΔV_{OD}	Change in V_{OD} between Complimentary Output States					35	mV
V_{OS}	Offset Voltage			1.125	1.25	1.375	V
ΔV_{OS}	Change in V_{OS} between Complimentary Output States					35	mV
I_{OS}	Output Short Circuit Current	V_{OUT} = 0V, R_L = 100Ω			−3.5	−5	mA
I_{OZ}	Output TRI-STATE Current	$\overline{PD}$ = 0V, V_{OUT} = 0V or V_{CC}			±1	±10	µA
LVDS RECEIVER DC SPECIFICATIONS							
V_{TH}	Differential Input High Threshold	V_{CM} = +1.2V				+100	mV
V_{TL}	Differential Input Low Threshold			−100			mV
I_{IN}	Input Current	V_{IN} = +2.4V, V_{CC} = 3.6V				±10	µA
		V_{IN} = 0V, V_{CC} = 3.6V				±10	µA
TRANSMITTER SUPPLY CURRENT							
ICCTW	Transmitter Supply Current Worst Case	R_L = 100Ω, C_L = 5 pF, BAL = High, Worst Case Pattern (Figure 1 Figure 2)	f = 33 MHz		91.4	140	mA
			f = 66 MHz		106	160	mA
			f = 112 MHz		155	210	mA
ICCTZ	Transmitter Supply Current Power Down	$\overline{PD}$ = Low			5	50	µA
		Driver Outputs in TRI-STATE during power down Mode					
RECEIVER SUPPLY CURRENT							
ICCRW	Receiver Supply Current Worst Case	C_L = 8 pF, BAL = High, Worst Case Pattern (Figure 1 Figure 3)	f = 33 MHz		125	150	mA
			f = 66 MHz		200	210	mA
			f = 112 MHz		250	280	mA
ICCRZ	Receiver Supply Current Power Down	$\overline{PD}$ = Low Receiver Outputs stay low during power down mode.			20	100	µA

(1) Typical values are given for V_{CC} = 3.3V and T_A = +25°C.
(2) Current into device pins is defined as positive. Current out of device pins is defined as negative. Voltages are referenced to ground unless otherwise specified (except V_{TH}, V_{TL}, V_{OD} and ΔV_{OD}).

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Recommended Transmitter Input Characteristics

Over recommended operating supply and temperature ranges unless otherwise specified.

Symbol	Parameter	Min	Typ	Max	Units
TCIT	TxCLK IN Transition Time (Figure 4)	1.0	2.0	3.0	ns
TCIP	TxCLK IN Period (Figure 5)	8.928	T	30.3	ns
TCIH	TxCLK in High Time (Figure 5)	0.35T	0.5T	0.65T	ns
TCIL	TxCLK in Low Time (Figure 5)	0.35T	0.5T	0.65T	ns
TXIT	TxIN Transition Time	1.5		6.0	ns

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Transmitter Switching Characteristics

Over recommended operating supply and temperature ranges unless otherwise specified.

Symbol	Parameter		Min	Typ	Max	Units
LLHT	LVDS Low-to-High Transition Time (Figure 2), PRE = 0.75V (disabled)			0.14	0.7	ns
	LVDS Low-to-High Transition Time (Figure 2), PRE = Vcc (max)			0.11	0.6	ns
LHLT	LVDS High-to-Low Transition Time (Figure 2), PRE = 0.75V (disabled)			0.16	0.8	ns
	LVDS High-to-Low Transition Time (Figure 2), PRE = Vcc (max)			0.11	0.7	ns
TBIT	Transmitter Bit Width			1/7 TCIP		ns
TPPOS	Transmitter Pulse Positions - Normalized	f = 33 to 70 MHz	−250	0	+250	ps
		f = 70 to 112 MHz	−200	0	+200	ps
TJCC	Transmitter Jitter - Cycle-to-Cycle(1)			50	100	ps
TCCS	TxOUT Channel to Channel Skew			40		ps
TSTC	TxIN Setup to TxCLK IN, (Figure 5)		2.5			ns
THTC	TxIN Hold to TxCLK IN, (Figure 5)		0			ns
TPDL	Transmitter Propagation Delay - Latency, (Figure 7)		1.5(TCIP)+3.72	1.5(TCIP)+4.4	1.5(TCIP)+6.24	ns
TPLLS	Transmitter Phase Lock Loop Set, (Figure 9)				10	ms
TPDD	Transmitter Powerdown Delay, (Figure 11)				100	ns

(1) TJCC is a function of input clock quality and also PLLVCC noise. At 112MHz operation, with a +/−300ps input impulse at a 2us rate, TJCC has been measured to be in the 70-80ps range (<100ps). With a nominal input clock quality (no input impulse jitter, jitter < 500kHz), TJCC is typically 50ps or less. For RSKM/RSKMD calculations 100ps is typically used as the TJCC budget. See Clock Jitter discussion in the APPLICATIONS INFORMATION section of this datasheet for further information.

Receiver Switching Characteristics

Over recommended operating supply and temperature ranges unless otherwise specified.

Symbol	Parameter		Min	Typ	Max	Units
CLHT	CMOS/TTL Low-to-High Transition Time (Figure 3), Rx data out				2.0	ns
	CMOS/TTL Low-to-High Transition Time (Figure 3), Rx clock out				1.0	ns
CHLT	CMOS/TTL High-to-Low Transition Time (Figure 3), Rx data out				2.0	ns
	CMOS/TTL High-to-Low Transition Time (Figure 3), Rx clock out				1.0	ns
RCOP	RxCLK OUT Period, (Figure 6)		8.928	T	30.3	ns
RCOH	RxCLK OUT High Time, (Figure 6)(1)	f = 112 MHz	3.5			ns
		f = 66 MHz	6.0			ns
RCOL	RxCLK OUT Low Time, (Figure 6)(1)	f = 112 MHz	3.5			ns
		f = 66 MHz	6.0			ns
RSRC	RxOUT Setup to RxCLK OUT (Figure 6)(1)	f = 112 MHz	2.4			ns
		f = 66 MHz	3.6			ns
RHRC	RxOUT Hold to RxCLK OUT (Figure 6)(1)	f = 112 MHz	3.4			ns
		f = 66 MHz	7.0			ns
RPDL	Receiver Propagation Delay - Latency, (Figure 8)		3(TCIP)+4.0	3(TCIP)+4.8	3(TCIP)+6.5	ns
RPLLS	Receiver Phase Lock Loop Set, (Figure 10)				10	ms
RPDD	Receiver Powerdown Delay, (Figure 12)				1	µs

(1) The Minimum and Maximum Limits are based on statistical analysis of the device performance over voltage and temperature ranges. This parameter is functionally tested on Automatic Test Equipment (ATE). ATE is limited to 85MHz. A sample of characterization parts have been bench tested to verify functional performance.

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Chipset RSKM Characteristics

Over recommended operating supply and temperature ranges unless otherwise specified[1][2]. See APPLICATIONS INFORMATION section for more details on this parameter and how to apply it.

Symbol	Parameter		Min	Typ	Max	Units
RSKM	Receiver Skew Margin without Deskew in non-DC Balance Mode, (Figure 13)[3]	f = 112 MHz	170			ps
		f = 100 MHz	170	240		ps
		f = 85MHz	300	350		ps
		f = 66MHz	300	350		ps
RSKM	Receiver Skew Margin without Deskew in DC Balance Mode, (Figure 13)[3]	f = 112 MHz	170			ps
		f = 100 MHz	170	200		ps
		f = 85 MHz	250	300		ps
		f = 66 MHz	250	300		ps
		f = 50MHz	300	350		ps
RSKMD	Receiver Skew Margin with Deskew in DC Balance, (Figure 14)[4]	f = 33 to 80 MHz	0.25TBIT			ps
RDR	Receiver Deskew Range	f = 80 MHz	± 1			TBIT
RDSS	Receiver Deskew Step Size	f = 80 MHz		0.3 TBIT		ns

(1) The Minimum and Maximum Limits are based on statistical analysis of the device performance over voltage and temperature ranges. This parameter is functionally tested on Automatic Test Equipment (ATE). ATE is limited to 85MHz. A sample of characterization parts have been bench tested to verify functional performance.

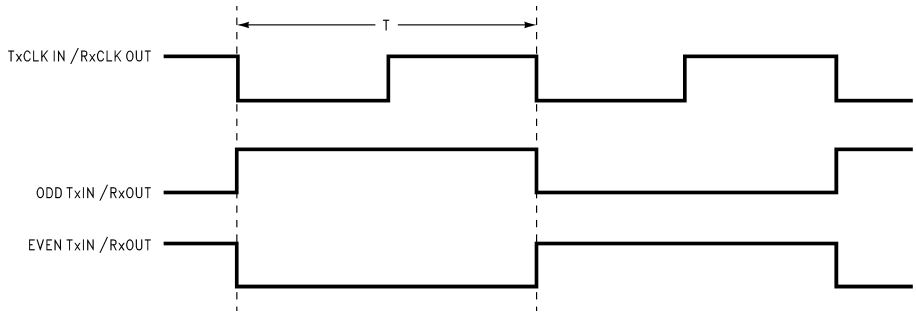
(2) Typical values for RSKM and RSKMD are applicable for fixed V_{CC} and T_A for the Transmitter and Receiver (both are assumed to be at the same V_{CC} and T_A points).

(3) Receiver Skew Margin (RSKM) is defined as the valid data sampling region at the receiver inputs. This margin takes into account transmitter output pulse positions (min and max) and the receiver input setup and hold time (internal data sampling window - RSPOS). This margin allows for LVDS interconnect skew, inter-symbol interference (both dependent on type/length of cable) and clock jitter.RSKM ≥ cable skew (type, length) + source clock jitter (cycle to cycle, TJCC) + ISI (if any). See APPLICATIONS INFORMATION section for more details.

(4) Receiver Skew Margin with Deskew (RSKMD) is defined as the valid data sampling region at the receiver inputs. The DESKEW function will constrain the receiver's sampling strobes to the middle half of the LVDS bit and removes (adjusts for) fixed interconnect skew. This margin (RSKMD) allows for inter-symbol interference (dependent on type/length of cable), Transmitter Pulse Position (TPPOS) variance, and LVDS clock jitter (TJCC).RSKMD ≥ ISI + TPPOS(variance) + source clock jitter (cycle to cycle). See APPLICATIONS INFORMATION section for more details.

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AC Timing Diagrams



The worst case test pattern produces a maximum toggling of digital circuits, LVDS I/O and CMOS/TTL I/O.

Figure 1. "Worst Case" Test Pattern

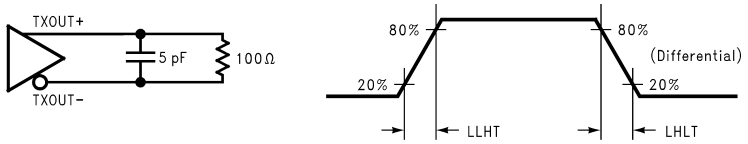


Figure 2. DS90CR483 (Transmitter) LVDS Output Load and Transition Times

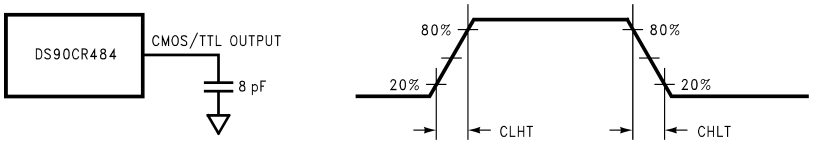


Figure 3. DS90CR484 (Receiver) CMOS/TTL Output Load and Transition Times

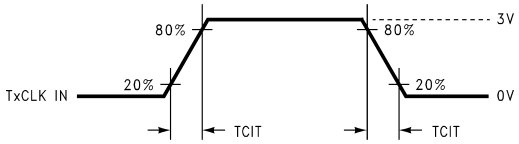


Figure 4. DS90CR483 (Transmitter) Input Clock Transition Time

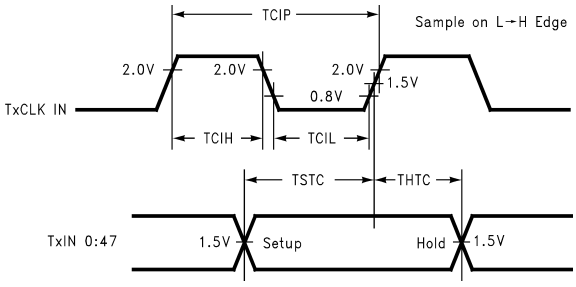


Figure 5. DS90CR483 (Transmitter) Setup/Hold and High/Low Times

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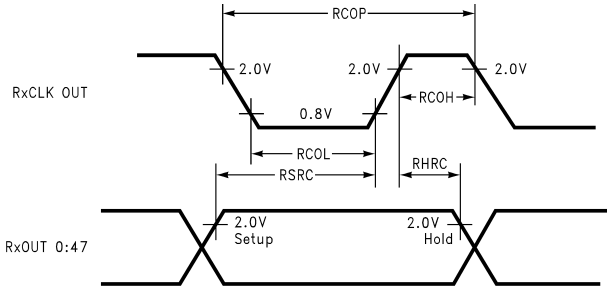


Figure 6. DS90CR484 (Receiver) Setup/Hold and High/Low Times

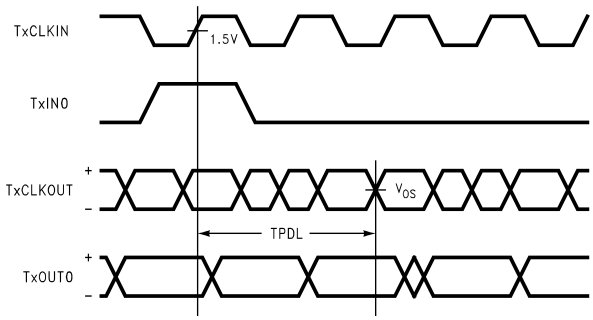


Figure 7. DS90CR483 (Transmitter) Propagation Delay - Latency

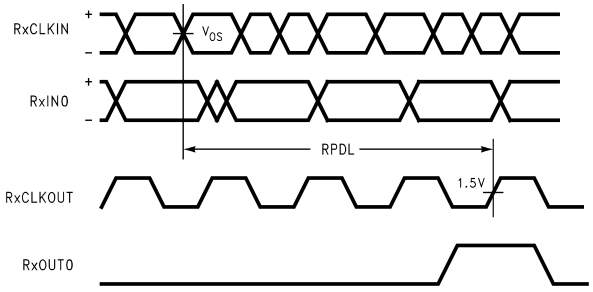


Figure 8. DS90CR484 (Receiver) Propagation Delay - Latency

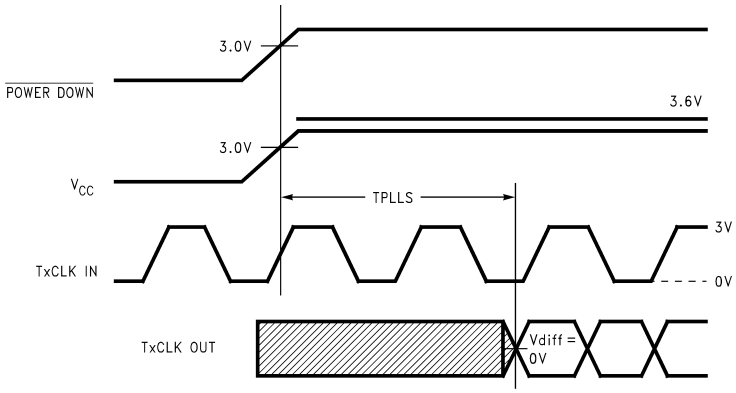


Figure 9. DS90CR483 (Transmitter) Phase Lock Loop Set Time

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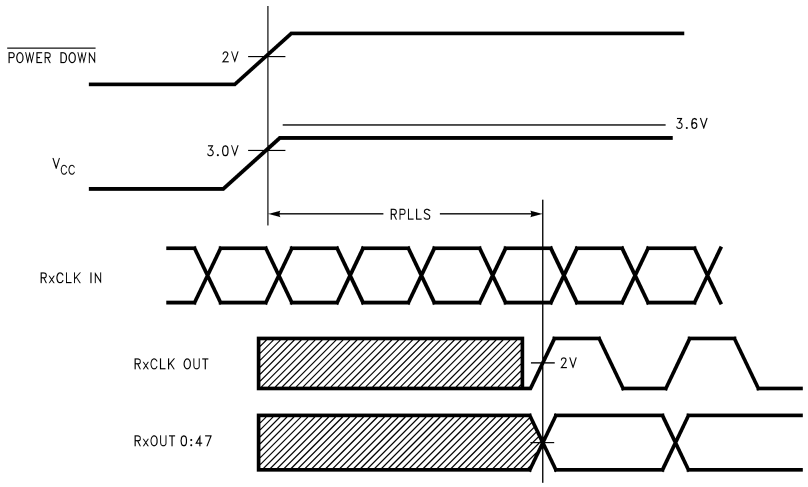


Figure 10. DS90CR484 (Receiver) Phase Lock Loop Set Time

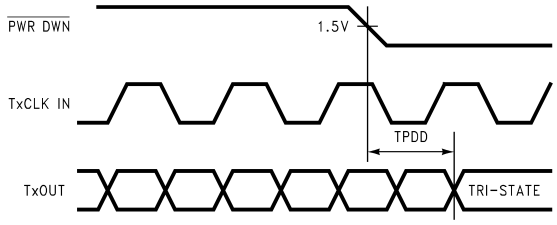


Figure 11. DS90CR483 (Transmitter) Power Down Delay

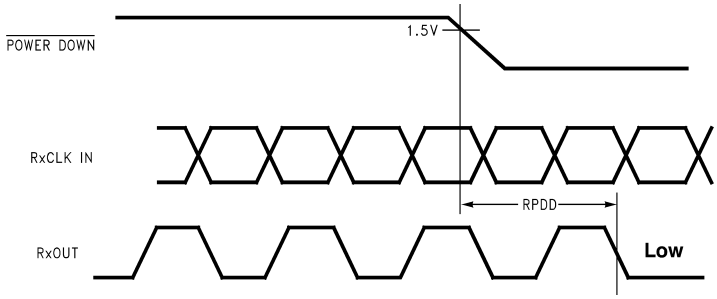
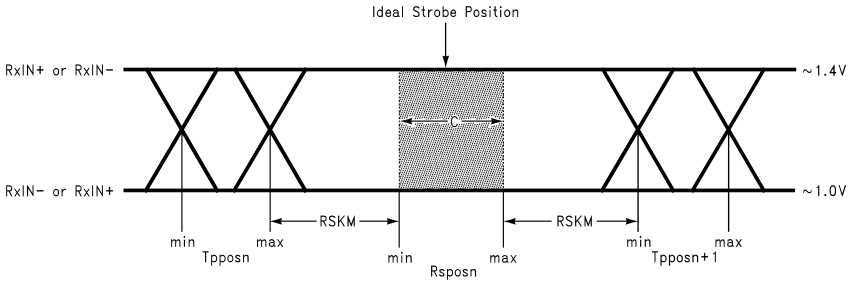


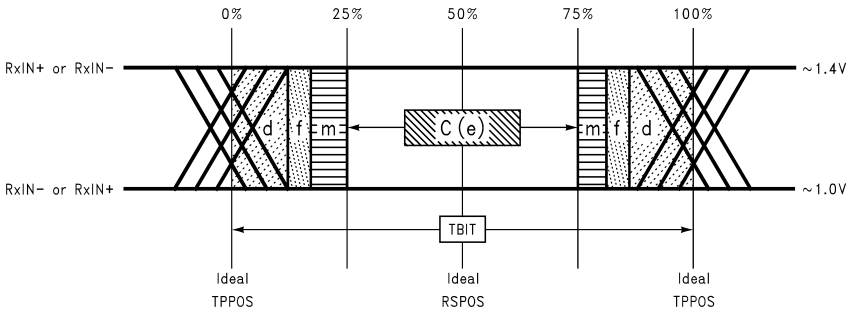
Figure 12. DS90CR484 (Receiver) Power Down Delay

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C — Setup and Hold Time (Internal data sampling window) defined by Rspos (receiver input strobe position) min and max
TPPOS — Transmitter output pulse position (min and max)
RSKM ≥ Cable Skew (type, length) + LVDS Source Clock Jitter (cycle to cycle) + ISI (Inter-symbol interference)
Cable Skew — typically 10 ps to 40 ps per foot, media dependent
TJCC — Cycle-to-cycle LVDS Output jitter (TJCC) is less than 100 ps (worse case estimate).
ISI is dependent on interconnect length; may be zero
See APPLICATIONS INFORMATION section for more details.

Figure 13. Receiver Skew Margin (RSKM) without DESKEW

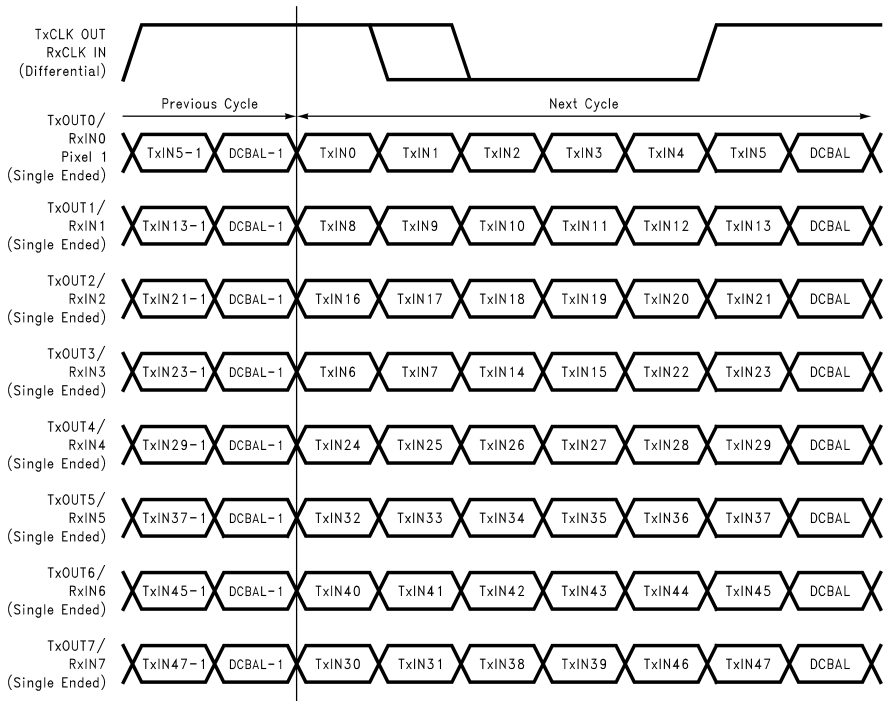


C — Setup and Hold Time (Internal data sampling window) defined by Rspos (receiver input strobe position) min and max
RSKMD ≥ TPPOSvariance (d) + TJCC (output jitter)(f) + ISI (m)
d = Tppos — Transmitter output pulse position (min and max)
f = TJCC — Cycle-to-cycle LVDS Output jitter (TJCC) is less than 100 ps (worse case estimate).
m = extra margin - assigned to ISI in long cable applications
See APPLICATIONS INFORMATION section for more details.

Figure 14. Receiver Skew Margin (RSKMD)with DESKEW

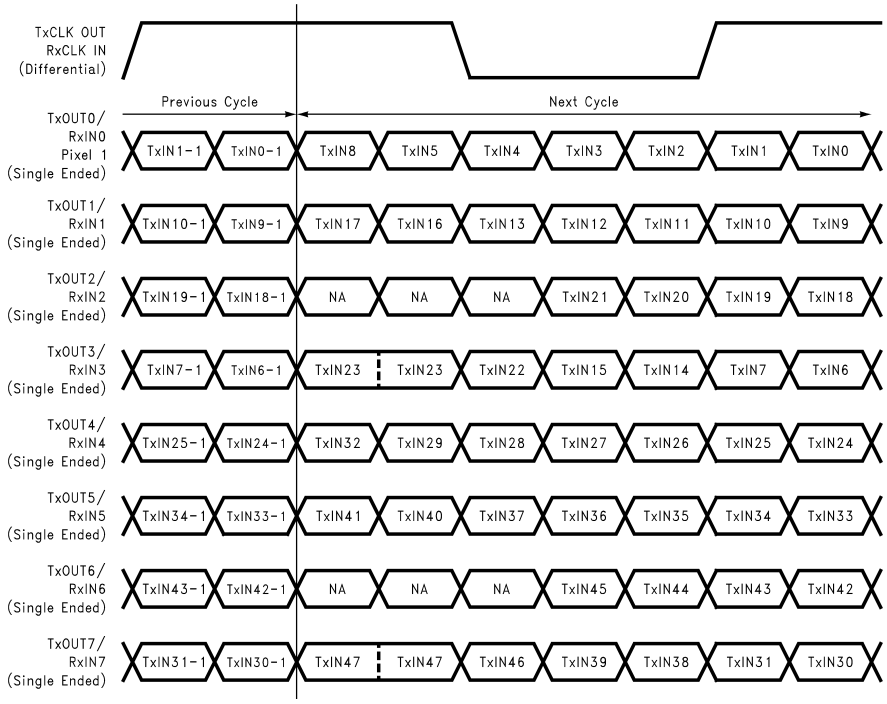
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LVDS Interface



Optional features supported: Pre-emphasis, and Deskew

Figure 15. 48 Parallel TTL Data Bits Mapped to LVDS Outputs with DC Balance Enabled



Optional feature supported: Pre-emphasis

Figure 16. 48 Parallel TTL Data Bits Mapped to LVDS Outputs with DC Balance Disabled

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APPLICATIONS INFORMATION

The DS90CR483/DS90CR484 chipset is improved over prior generations of Channel Link devices and offers higher bandwidth support and longer cable drive with three areas of enhancement. To increase bandwidth, the maximum clock rate is increased to 112 MHz and 8 serialized LVDS outputs are provided. Cable drive is enhanced with a user selectable pre-emphasis feature that provides additional output current during transitions to counteract cable loading effects. This requires the use of one pull up resistor to Vcc; please refer to Table 1 to set the level needed. Optional DC balancing on a cycle-to-cycle basis, is also provided to reduce ISI (Inter-Symbol Interference). With pre-emphasis and DC balancing, a low distortion eye-pattern is provided at the receiver end of the cable. A cable deskew capability has been added to deskew long cables of pair-to-pair skew of up to ±1 LVDS data bit time (up to 80 MHz clock rates). For details on deskew, refer to "Deskew" section below. These three enhancements allow cables 5+ meters in length to be driven depending upon media and clock rate.

The DS90CR483/484 chipset may also be used in a non-DC Balance mode. In this mode pre-emphasis is supported. In this mode, the chipset is also compatible with 21 and 28-bit Channel Link Receivers. See Figure 16 for the LVDS mapping.

New features Description:

1. Pre-emphasis: Adds extra current during LVDS logic transition to reduce the cable loading effects. Pre-emphasis strength is set via a DC voltage level applied from min to max (0.75V to Vcc) at the "PRE" pin. A higher input voltage on the "PRE" pin increases the magnitude of dynamic current during data transition. The "PRE" pin requires one pull-up resistor (Rpre) to Vcc in order to set the DC level. There is an internal resistor network, which cause a voltage drop. Please refer to the tables below to set the voltage level.

The waveshape at the Receiver input should not exhibit over or undershoot with the proper amount of pre-emphasis set. Too much pre-emphasis generates excess noise and increases power dissipation. Cables less than 2 meters in length typically do not require pre-emphasis.

Table 1. Pre-emphasis DC voltage level with (Rpre)

Rpre	Resulting PRE Voltage	Effect
1MΩ or NC	0.75V	Standard LVDS
50kΩ	1.0V	
9kΩ	1.5V	50% pre-emphasis
3kΩ	2.0V	
1kΩ	2.6V	
100Ω	Vcc	100% pre-emphasis

Table 2. Pre-emphasis needed per cable length

Frequency	PRE Voltage	Typical cable length
112MHz	1.0V	2 meters
112MHz	1.5V	5 meters
80MHz	1.0V	2 meters
80MHz	1.2V	5+ meters
66MHz	1.5V	7 meters

2. DC Balance: In addition to data information an additional bit is transmitted on every LVDS data signal line during each cycle as shown in Figure 15. This bit is the DC balance bit (DCBAL). The purpose of the DC Balance bit is to minimize the short- and long-term DC bias on the signal lines. This is achieved by selectively sending the data either unmodified or inverted.

The value of the DC balance bit is calculated from the running word disparity and the data disparity of the current word to be sent. The data disparity of the current word shall be calculated by subtracting the number of bits of value 0 from the number of bits value 1 in the current word. Initially, the running word disparity may be any value between +7 and −6. The running word disparity shall be calculated as a continuous sum of all the modified data disparity values, where the unmodified data disparity value is the calculated data disparity minus 1 if the data is sent unmodified and 1 plus the inverse of the calculated data disparity if the data is sent inverted. The value of the running word disparity shall saturate at +7 and −6.

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The value of the DC balance bit (DCBAL) shall be 0 when the data is sent unmodified and 1 when the data is sent inverted. To determine whether to send data unmodified or inverted, the running word disparity and the current data disparity are used. If the running word disparity is positive and the current data disparity is positive, the data shall be sent inverted. If the running word disparity is positive and the current data disparity is zero or negative, the data shall be sent unmodified. If the running word disparity is negative and the current data disparity is positive, the data shall be sent unmodified. If the running word disparity is negative and the current data disparity is zero or negative, the data shall be sent inverted. If the running word disparity is zero, the data shall be sent inverted.

DC Balance mode is set when the BAL pin on the transmitter is tied HIGH - see . DC Balancing is useful on long cable applications which are typically greater than 5 meters in length.

3. Deskew:

Deskew is supported in the DC Balance mode only (BAL = high on DS90CR483). The “DESKEW” pin on the receiver when set high will deskew a minimum of ±1 LVDS data bit time skew from the ideal strobe location between signals arriving on independent differential pairs (pair-to-pair skew). It is required that the “DS_OPT” pin on the Transmitter must be applied low for a minimum of four clock cycles to complete the deskew operation. It is also required that this must be performed at least once at any time after the PLLs have locked to the input clock frequency. If power is lost, or if the cable has been switched, this procedure must be repeated or else the receiver may not sample the incoming LVDS data correctly. When the receiver is in the deskew mode, all receiver data outputs are set to a LOW state, but the receiver clock output is still active and switching. Setting the “DESKEW” pin to low will disable the deskew operation and allow the receiver to operation on a fixed data sampling strobe. In this case, the ”DS_OPT” pin on the transmitter must then be set high.

The DS_OPT pin at the input of the transmitter (DS90CR483) is used to initiate the deskew calibration pattern. It must be applied low for a minimum of four clock cycles in order for the receiver to complete the deskew operation. For this reason, the LVDS clock signal with DS_OPT applied high (active data sampling) shall be 1111000 or 1110000 pattern. During the deskew operation with DS_OPT applied low, the LVDS clock signal shall be 1111100 or 1100000 pattern. The transmitter will also output a series of 1111000 or 1110000 onto the LVDS data lines (TxOUT 0-7) during deskew so that the receiver can automatically calibrated the data sampling strobes at the receiver inputs. Each data channel is deskewed independently and is tuned with a step size of 1/3 of a bit time over a range of +/−1 TBIT from the ideal strobe location. The Deskew feature operates up to clock rates of 80 MHz only. If the Receiver is enabled in the deskew mode, then it must be trained before data transfer.

Clock Jitter:

The transmitter is designed to reject cycle-to-cycle jitter which may be seen at the transmitter input clock. Very low cycle-to-cycle jitter is passed on to the transmitter outputs. Cycle-to-cycle jitter has been measured over frequency to be less than 100 ps with input step function jitter applied. This should be subtracted from the RSKM/RSKMD budget as shown and described in Figure 13 and Figure 14. This rejection capability significantly reduces the impact of jitter at the TXinput clock pin, and improves the accuracy of data sampling in the receiver. Transmitter output jitter is effected by PLLVCC noise and input clock jitter - minimize supply noise and use a low jitter clock source to limit output jitter. The falling edge of the input clock to the transmitter is the critical edge and is used by the PLL circuit.

RSKM - Receiver Skew Margin

RSKM is a chipset parameter and is explained in AN-1059 in detail. It is the difference between the transmitter’s pulse position and the receiver’s strobe window. RSKM must be greater than the summation of: Interconnect skew, LVDS Source Clock Jitter (TJCC), and ISI (if any). See Figure 13. Interconnect skew includes PCB traces differences, connector skew and cable skew for a cable application. PCB trace and connector skew can be compensated for in the design of the system. Cable skew is media type and length dependant.

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RSKMD - Receiver Skew Margin with DESKEW

RSKMD is a chipset parameter and is applicable when the DESKEW feature of the DS90CR484 is employed. It is the difference between the receiver's strobe window and the ideal pulse locations. The DESKEW feature adjusts for skew between each data channel and the clock channel. This feature is supported up to 80 MHz clock rate. RSKMD must be greater than the summation of: Transmitter's Pulse Position variance, LVDS Source Clock Jitter (TJCC), and ISI (if any). See Figure 14. With Deskew, RSKMD is ≥ 25% of TBIT. Deskew compensates for interconnect skew which includes PCB traces differences, connector skew and cable skew (for a cable application). PCB trace and connector skew can be compensated for in the design of the system. Note, cable skew is media type and length dependant. Cable length may be limited by the RSKMD parameter prior to the interconnect skew reaching 1 TBIT in length due to ISI effects.

Power Down:

Both transmitter and receiver provide a power down feature. When asserted current draw through the supply pins is minimized and the PLLs are shut down. The transmitter outputs are in TRI-STATE when in power down mode. The receiver outputs are forced to a active LOW state when in the power down mode. (See and tables). The $\overline{PD}$ pin should be driven HIGH to enable the device once V_{CC} is stable.

Configurations:

The transmitter is designed to be connected typically to a single receiver load. This is known as a point-to-point configuration. It is also possible to drive multiple receiver loads if certain restrictions are made. Only the final receiver at the end of the interconnect should provide termination across the pair. In this case, the driver still sees the intended DC load of 100 Ohms. Receivers connected to the cable between the transmitter and the final receiver must not load down the signal. To meet this system requirement, stub lengths from the line to the receiver inputs must be kept very short.

Cable Termination

A termination resistor is required for proper operation to be obtained. The termination resistor should be equal to the differential impedance of the media being driven. This should be in the range of 90 to 132 Ohms. 100 Ohms is a typical value common used with standard 100 Ohm twisted pair cables. This resistor is required for control of reflections and also to complete the current loop. It should be placed as close to the receiver inputs to minimize the stub length from the resistor to the receiver input pins.

How to configure for backplane applications:

In a backplane application with differential line impedance of 100Ω the differential line pair-to-pair skew can controlled by trace layout. The transmitter-DS90CR483 "DS_OPT" pin may be set high. In a backplane application with short PCB distance traces, pre-emphasis from the transmitter is typically not required. The "PRE" pin should be left open (do not tie to ground). A resistor pad provision for a pull up resistor to Vcc can be implemented in case pre-emphasis is needed to counteract heavy capacitive loading effects.

How to configure for cable interconnect applications:

In applications that require the long cable drive capability. The DS90CR483/DS90CR484 chipset is improved over prior generations of Channel Link devices and offers higher bandwidth support and longer cable drive with the use of DC balanced data transmission, pre-emphasis. Cable drive is enhanced with a user selectable pre-emphasis feature that provides additional output current during transitions to counteract cable loading effects. This requires the use of one pull up resistor to Vcc; please refer to Table 1 to set the level needed. Optional DC balancing on a cycle-to-cycle basis, is also provided to reduce ISI (Inter-Symbol Interference) for long cable applications. With pre-emphasis and DC balancing, a low distortion eye-pattern is provided at the receiver end of the cable. These enhancements allow cables 5+ meters in length to be driven. Depending upon clock rate and the media being driven, the cable Deskew feature may also be employed - see discussion on DESKEW, RSKM and RSKMD above.

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Supply Bypass Recommendations:

Bypass capacitors must be used on the power supply pins. Different pins supply different portions of the circuit, therefore capacitors should be nearby all power supply pins except as noted in the and tables. Use high frequency ceramic (surface mount recommended) 0.1µF capacitors close to each supply pin. If space allows, a 0.01µF capacitor should be used in parallel, with the smallest value closest to the device pin. Additional scattered capacitors over the printed circuit board will improve decoupling. Multiple (large) via should be used to connect the decoupling capacitors to the power plane. A 4.7 to 10 µF bulk cap is recommended near the PLLVCC pins and also the LVDSVCC (pin #40) on the Transmitter. Connections between the caps and the pin should use wide traces.

Input Signal Quality Requirements - Transmitter:

The input signal quality must comply to the datasheet requirements, please refer to the Recommended Transmitter Input Characteristics table for specifications. In addition undershoots in excess of the ABS MAX specifications are not recommended. If the line between the host device and the transmitter is long and acts as a transmission line, then termination should be employed. If the transmitter is being driven from a device with programmable drive strengths, data inputs are recommended to be set to a weak setting to prevent transmission line effects. The clock signal is typically set higher to provide a clean edge that is also low jitter.

Unused LVDS Outputs:

Unused LVDS output channels should be terminated with 100 Ohm at the transmitter's output pin.

Receiver output drive strength:

The DS90CR484 output specify a 8pF load, V_{OH} and V_{OL} are tested at ± 2mA, which is intended for only 1 or maybe 2 loads. If high fan-out is required or long transmission line driving capability, buffering the receiver output is recommended. Receiver outputs do not support / provide a TRI-STATE function.

LVDS Interconnect Guidelines:

See AN-1108 and AN-905 for full details.

- Use 100Ω coupled differential pairs
- Use the S/2S/3S rule in spacings
  - S = space between the pair
  - 2S = space between pairs
  - 3S = space to TTL signal
- Minimize the number of VIA
- Use differential connectors when operating above 500Mbps line speed
- Maintain balance of the traces
- Minimize skew within the pair
- Minimize skew between pairs
- Terminate as close to the RXinputs as possible

DS90CR481/482 and PLLSEL Function

The DS90CR481/2 chipset is electrically similar to the DS90CR483/4. The DS90CR481/2 differ only in the control circuit of the internal PLL and are specified for 65 to 112 MHz operation. The devices will directly inter-operate within the scope of the respective datasheets. The DS90CR483/4 supports a wide operating range from 33 to 112 MHz. The PLLSEL pin is used to select an auto-range feature. It shifts between the two ranges (High and Low) in the 55 to 68 MHz range. For operation in the 65 to 70 MHz range, the DS90CR481/2 is recommended as it will select High gear only and offer more margin to the system.

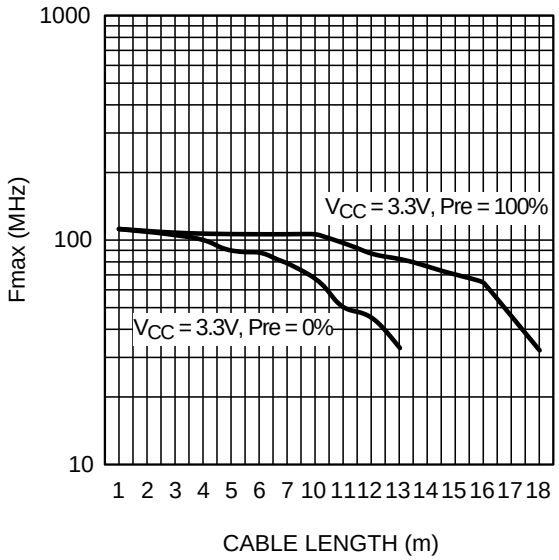
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For more information:

Channel Link Applications Notes currently available:

- AN-1041 Introduction to Channel Link
- AN-1059 RSKM Calculations
- AN-1108 PCB and Interconnect Guidelines
- AN-905 Differential Impedance
- LVDS Owner's Manual

Typical Data Rate vs Cable Length Curve



DATA RATE VS CABLE LENGTH TEST PROCEDURE

The Data Rate vs Cable Length graph was generated using CLINK3V48BT-112 Evaluation Kit and 3M's Mini D Ribbon (MDR) Cable under typical conditions (Vcc = 3.3V, Temp = +25°C). A Tektronix MB100 Bit-Error-Rate Tester (BERT) was used to send a PRBS (2^{15}) pattern to 32 of the 48 input channels on the transmitter (DS90CR483). The BERT was also used to monitor the corresponding 32 receiver (DS90CR484) output channels for bit errors. The frequency of the input signal were increased until bit errors were reported on the BERT. The frequency on the graph is the highest frequency without error.

Results:

The DS90CR483/4 link was error free at 100MHz over 10 meters of 3M cable using pre-emphasis and DC balance mode off.

DS90CR483 PIN DESCRIPTION—Channel Link Transmitter

Pin Name	I/O	Description
TxIN	I	TTL level input(1)
TxOUTP	O	Positive LVDS differential data output.
TxOUTM	O	Negative LVDS differential data output.
TxCLKIN	I	TTL level clock input. The rising edge acts as data strobe.
TxCLKP	O	Positive LVDS differential clock output.
TxCLKM	O	Negative LVDS differential clock output.
$\overline{PD}$	I	TTL level input. Assertion (low input) tri-states the outputs, ensuring low current at power down(1)
PLLSEL	I	PLL range select. This pin should be tied to V_{CC} for auto-range. Tied to ground or NC will force the PLL to low range only. Typical shift point is between 55 and 68 MHz for auto-range.(1)(2)

(1) Inputs default to "low" when left open due to internal pull-down resistor.
(2) The PLL range shift point is in the 55 - 68 MHz range, typically the shift will occur during the lock time. For 65-70 MHz applications, the DS90CR481/2 is recommended since its shift point is below its operation range. See Applications Information section.

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DS90CR483 PIN DESCRIPTION—Channel Link Transmitter (continued)

Pin Name	I/O	Description
PRE	I	Pre-emphasis “level” select. Pre-emphasis is active when input is tied to V_{CC} through external pull-up resistor. Resistor value determines Pre-emphasis level (See APPLICATIONS INFORMATION Section). For normal LVDS drive level (No Pre-emphasis) leave this pin open (do not tie to ground).
DS_OPT	I	Cable Deskew performed when TTL level input is low. No TxIN data is sampled during Deskew. To perform Deskew function, input must be held low for a minimum of 4 clock cycles. The Deskew operation is normally conducted after the TX and RX PLLs have locked. It should also be conducted after a system reset, or a reconfiguration event. It must be performed at least once when "DESKEW" is enabled.(1) Deskew is only supported in the DC Balance mode (BAL = High).
BAL	I	TTL level input. This pin was previously labeled as V_{CC}, which enabled the DC Balance function. But when tied low or left open, the DC Balance function is disabled. Please refer to Figure 15 and Figure 16 for LVDS data bit mapping respectively.(1)(3)
V_{CC}	I	Power supply pins for TTL inputs and digital circuitry. Bypass not required on Pins 20 and 21.
GND	I	Ground pins for TTL inputs and digital circuitry.
$PLLV_{CC}$	I	Power supply pin for PLL circuitry.
PLLGND	I	Ground pins for PLL circuitry.
$LVDSV_{CC}$	I	Power supply pin for LVDS outputs.
LVDSGND	I	Ground pins for LVDS outputs.
NC		No Connect. Make NO Connection to these pins - leave open.

(3) The DS90CR484 is design to automatically detect the DC Balance or non-DC Balance transmitted data from the DS90CR483 and deserialize the LVDS data according to the define bit mapping.

DS90CR484 PIN DESCRIPTION—Channel Link Receiver

Pin Name	I/O	Description
RxINP	I	Positive LVDS differential data inputs.
RxINM	I	Negative LVDS differential data inputs.
RxOUT	O	TTL level data outputs. In PowerDown ($\overline{PD}$ = Low) mode, receiver outputs are forced to a Low state.
RxCLKP	I	Positive LVDS differential clock input.
RxCLKM	I	Negative LVDS differential clock input.
RxCLKOUT	O	TTL level clock output. The rising edge acts as data strobe.
PLLSEL	I	PLL range select. This pin should be tied to V_{CC} for auto-range. Tied to ground or NC will force the PLL to low range only. Typical shift point is between 55 and 68 MHz for auto-range. (1) (2)
DESKEW	I	Deskew / Oversampling “on/off” select. When using the Deskew / Oversample feature this pin must be tied to V_{CC}. Tieing this pin to ground disables this feature. Deskew is only supported in the DC Balance mode.(1)
$\overline{PD}$	I	TTL level input. When asserted (low input) the receiver outputs are Low.(1)
V_{CC}	I	Power supply pins for TTL outputs and digital circuitry. Bypass not required on Pins 6 and 77.
GND	I	Ground pins for TTL outputs and digital circuitry.
$PLLV_{CC}$	I	Power supply for PLL circuitry.
PLLGND	I	Ground pin for PLL circuitry.
$LVDSV_{CC}$	I	Power supply pin for LVDS inputs.
LVDSGND	I	Ground pins for LVDS inputs.
NC		No Connect. Make NO Connection to these pins - leave open.

(1) Inputs default to “low” when left open due to internal pull-down resistor.
(2) The PLL range shift point is in the 55 - 68 MHz range, typically the shift will occur during the lock time. For 65-70 MHz applications, the DS90CR481/2 is recommended since its shift point is below its operation range. See Applications Information section.

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Pin Diagram

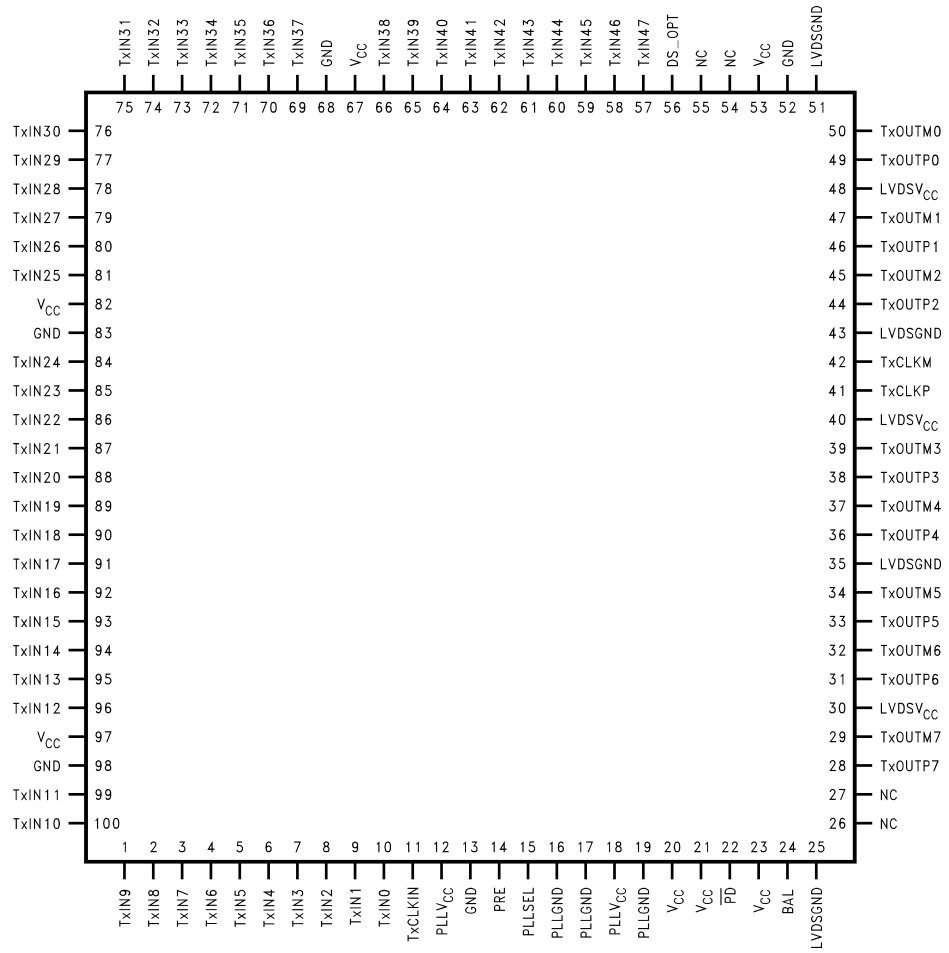


Figure 17. Transmitter - DS90CR483 - TQFP (TOP VIEW)

Pin Diagram

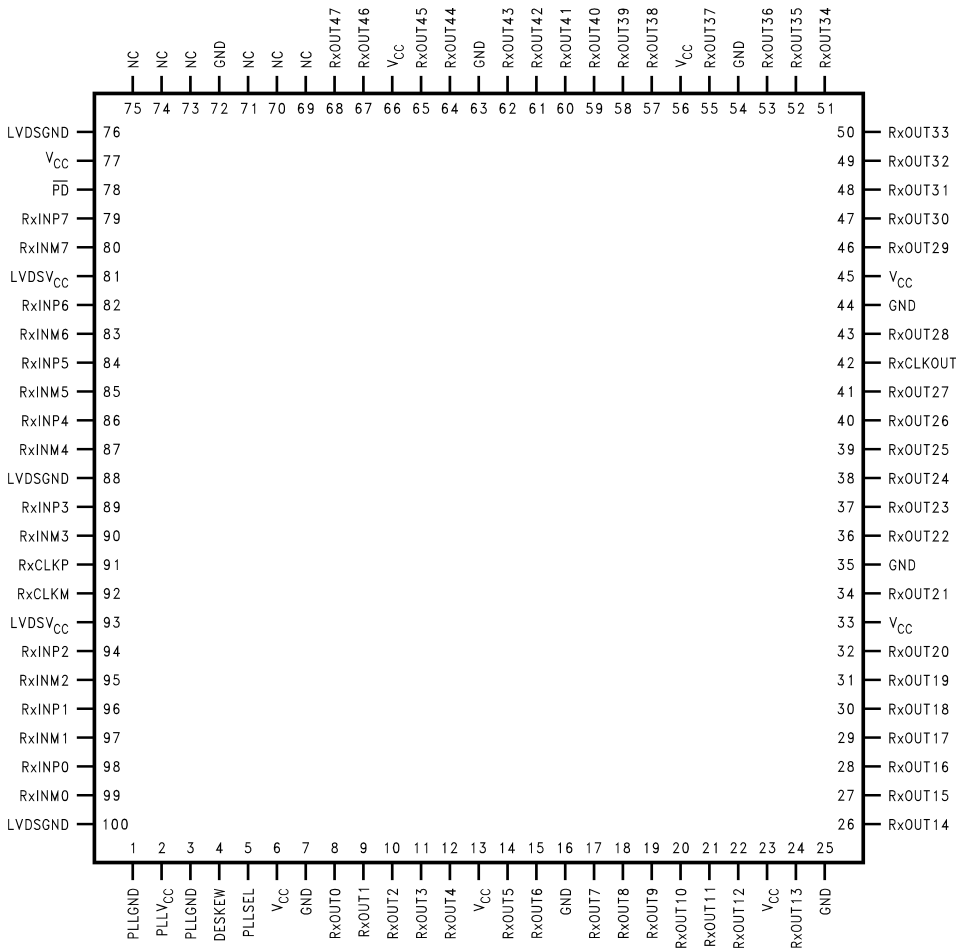


Figure 18. Receiver - DS90CR484 - TQFP (TOP VIEW)

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REVISION HISTORY

Changes from Revision G (April 2013) to Revision H	Page
• Changed layout of National Data Sheet to TI format	20

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
DS90CR483VJD/NOPB	NRND	TQFP	NEZ	100	90	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-10 to 70	DS90CR483VJD >B	
DS90CR483VJDX/NOPB	NRND	TQFP	NEZ	100	1000	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-10 to 70	DS90CR483VJD >B	
DS90CR484VJD/NOPB	NRND	TQFP	NEZ	100	90	RoHS & Green	NIPDAU	Level-3-260C-168 HR		DS90CR484VJD >B	

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

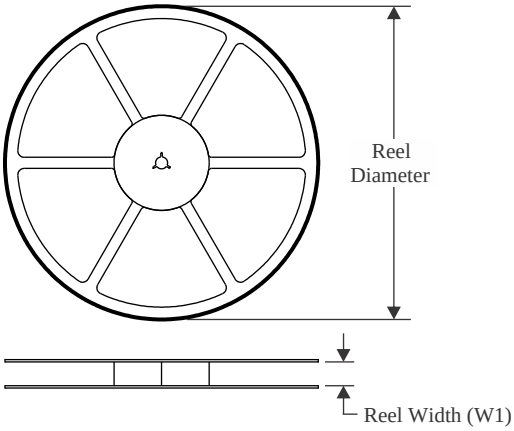
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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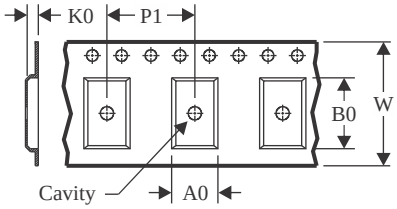
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TAPE AND REEL INFORMATION

REEL DIMENSIONS

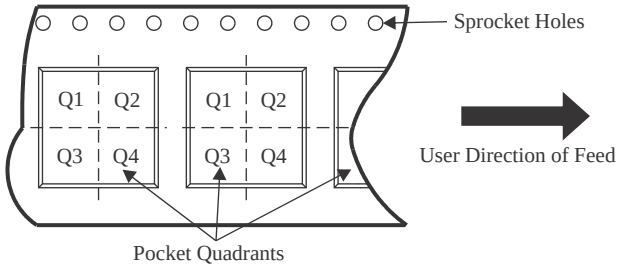


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

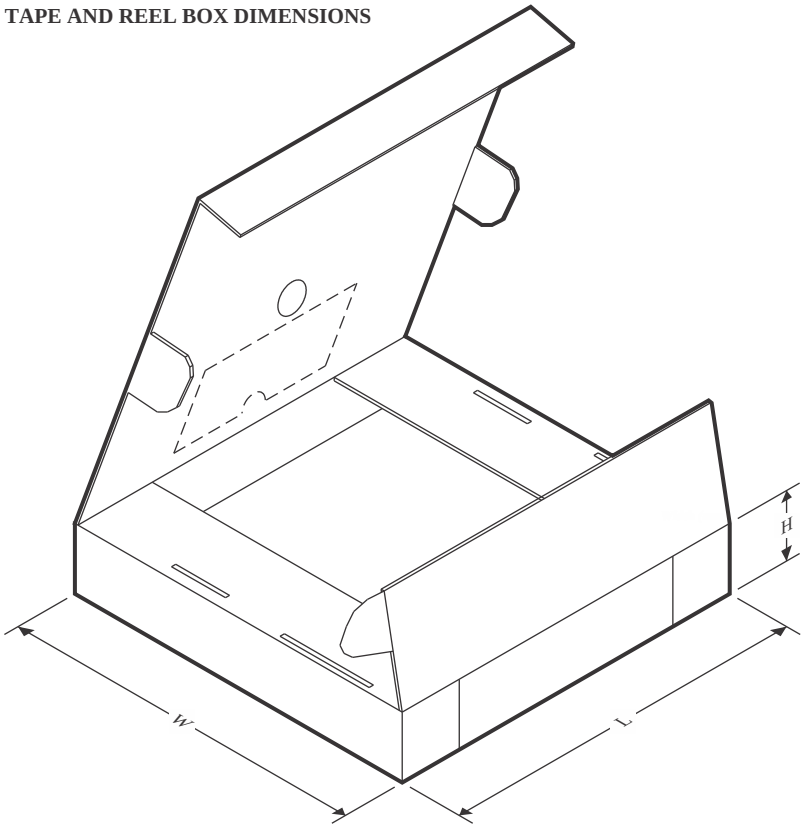
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
DS90CR483VJDX/NOPB	TQFP	NEZ	100	1000	330.0	32.4	18.0	18.0	1.6	24.0	32.0	Q2

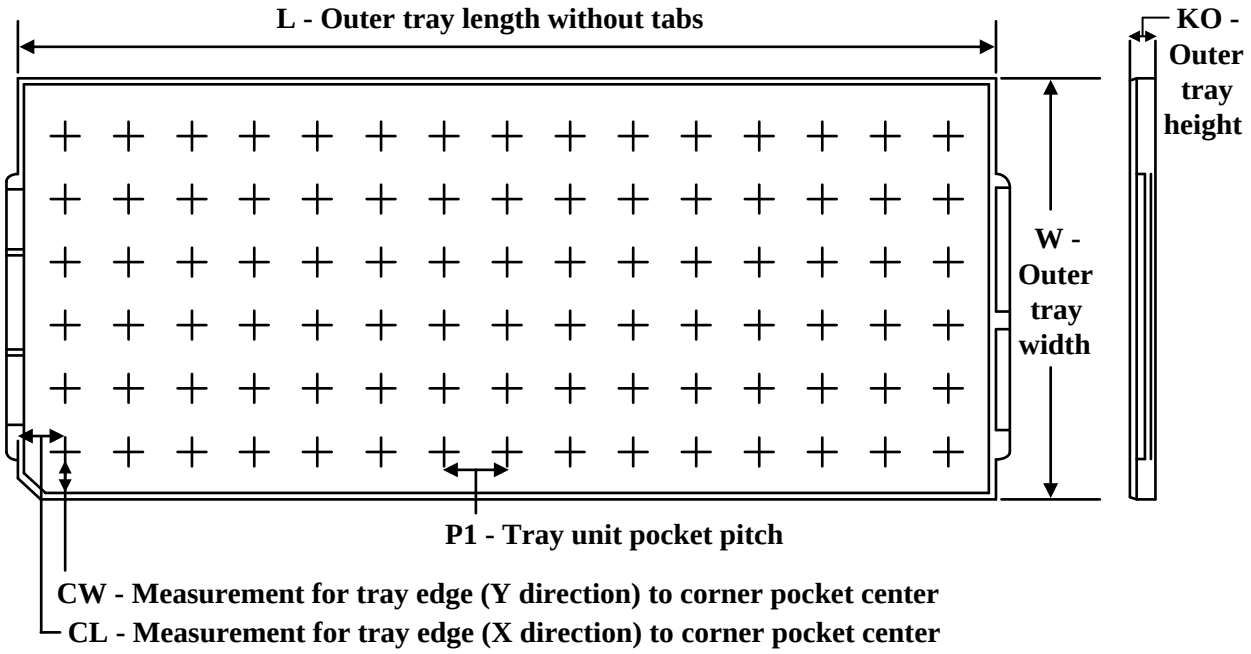
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
DS90CR483VJDX/NOPB	TQFP	NEZ	100	1000	367.0	367.0	55.0

TRAY

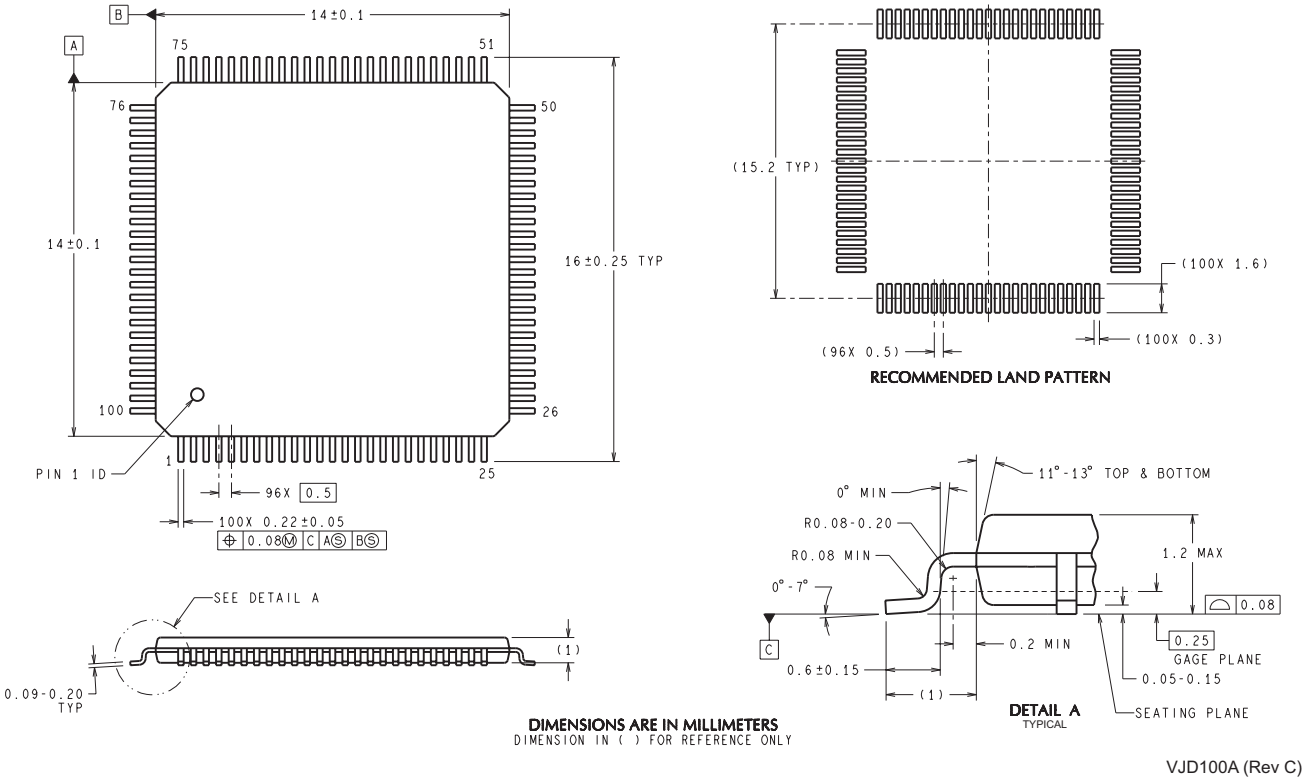


Chamfer on Tray corner indicates Pin 1 orientation of packed units.

*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	Unit array matrix	Max temperature (°C)	L (mm)	W (mm)	K0 (µm)	P1 (mm)	CL (mm)	CW (mm)
DS90CR483VJD/NOPB	NEZ	TQFP	100	90	6 x 15	150	322.6	135.9	7620	20.3	15.4	15.45
DS90CR484VJD/NOPB	NEZ	TQFP	100	90	6 x 15	150	322.6	135.9	7620	20.3	15.4	15.45

NEZ0100A



DIMENSIONS ARE IN MILLIMETERS
DIMENSION IN ( ) FOR REFERENCE ONLY

VJD100A (Rev C)

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