Silicon Radar GmbH
Im Technologiepark 1
15236 Frankfurt (Oder)
Germany

tel: +49 335 / 228 80 30
fax: +49 335 / 557 10 50
info@siliconradar.com
www.siliconradar.com

TRA_120_045
(T456)

120-GHz Wideband IQ Transceiver with Antennas on Chip

Data Sheet

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0.3	TRA_120_045 (T456)	QFN32, 5 × 5 mm²	TRA045 YYWW	1 of 12

Version Control

Version	Changed section	Description of change	Reason for change
0.1	Template, contents	Created with the latest template and simulated parameter and properties	New as information sheet
0.2	All sections	Review and update with latest test results	Update following first preseries fabrication
0.3	Section 4	TX output power revised	Power level specified at output of power amplifier.

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1 Features

- Wide-band radar frontend (RFE) with antennas on chip
- Frequency Bandwidth of ≥ 20 GHz
- Frequency Range from 114 GHz to 134GHz
- Single supply voltage of 3.3 V
- Fully ESD protected device
- Power consumption of 550 mW
- Integrated low phase noise VCO
- Receiver with homodyne quadrature mixer
- RX and TX dipole antennas
- QFN32 leadless plastic package 5 x 5 mm²
- Pb-free, RoHS compliant package
- IC is available as bare die as well

1.1 Overview

The radar frontend TRA_120_045 (T456) is an integrated wideband transceiver circuit with antennas on chip. It provides a frequency bandwidth of 20 GHz. The circuit includes a low-noise amplifier (LNA), quadrature mixers, a poly-phase filter, a voltage controlled oscillator, divide-by-32 outputs, and transmit and receive antennas (see Figure 1). The RF signal from the oscillator is directed to the RX path via buffer circuits. The RX signal is amplified by the LNA and converted to baseband by two mixers with quadrature local oscillator (LO). The integrated VCO has two analog tuning inputs. These two tuning inputs can be used to obtain the full tuning range of 20 GHz.
The on-chip VCO together with integrated frequency divider and external fractional-N PLL can be used for frequency modulated continuous wave (FMCW) radar operation. With a fixed oscillator frequency it can be used in continuous wave (CW) mode. Other modulation schemes such as FSK can be implemented by utilizing the analog tuning inputs.
The IC is fabricated in SG13S SiGe BiCMOS technology of IHP GmbH.

1.2 Applications

The main application field of the wideband transceiver radar frontend (RFE) without beam focusing element is in short range (in the order of about 5 meters) and high resolution radar systems. With the use of dielectric lenses, the range can be increased into the range of multiples of 10 meters up to 100 meters. High resolution measurement may require a compromise w.r.t. to the range evaluated.
The RFE can be used in FMCW mode as well as in CW mode. The transceivers are designed for maximum bandwidth by using two tuning inputs with different tuning ranges and tuning slopes. With these it is possible to extend the bandwidth to the full tuning range stated above.

2 Block Diagram

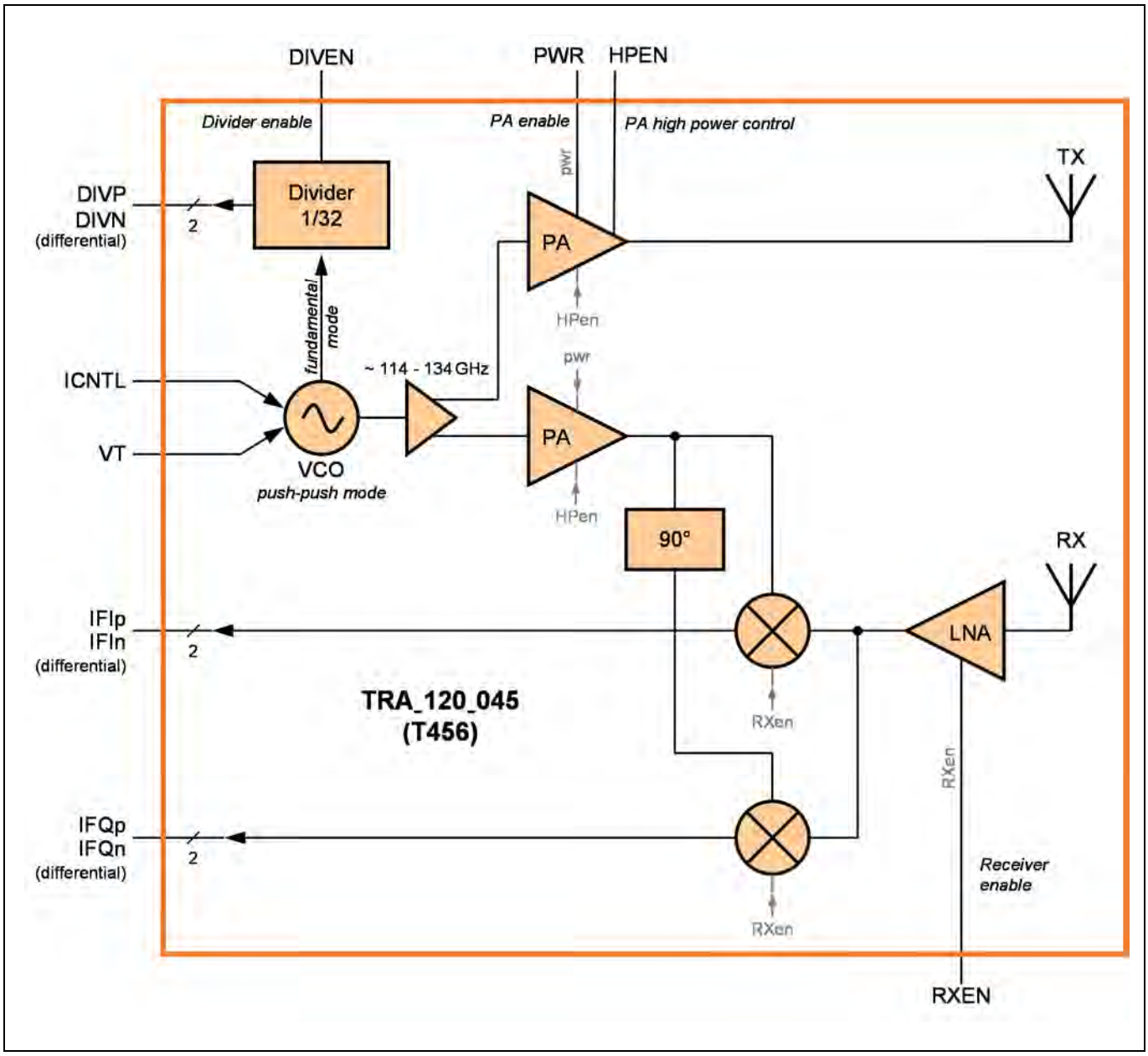


Figure 1 Block Diagram

3 Pin Configuration

3.1 Pin Assignment

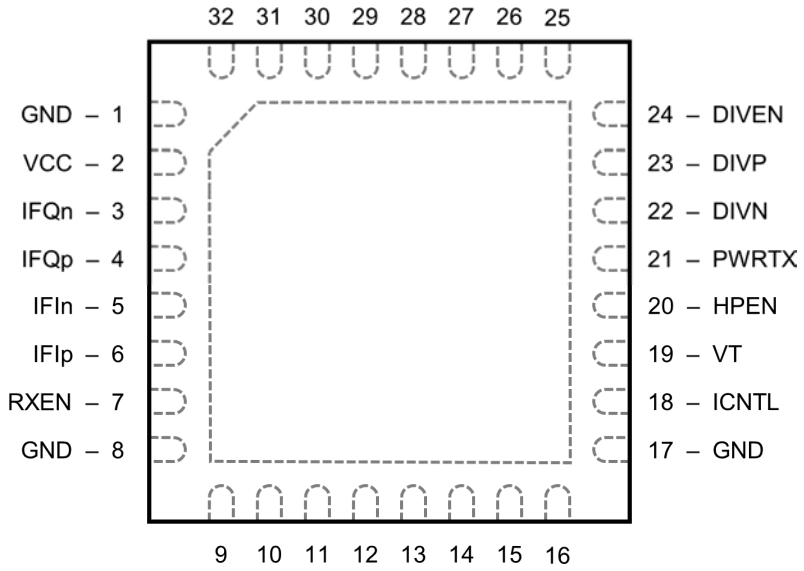


Figure 2 Pin assignment (QFN32, 5 mm x 5 mm, top view)

3.2 Pin Description

Table 1 Pin Description

Pin		Description
No.	Name	
1, 8, 17	GND	Ground
2	VCC	Supply voltage (3.3 V)
3	IFQn	Quadrature IF outputs, DC coupled
4	IFQp	
5	IFIn	
6	IFIp	
7	RXEN	Receiver enable input, 3.3-V level, high-active CMOS input, internal 100-kΩ pull-up resistor
18	ICNTL	VCO tuning input voltage (0 – 3.3 V), negative f(V_{ICNTL}) characteristic
19	VT	VCO frequency tuning input voltage (0 – 4.5 V), positive f(VT) characteristic
20	HPEN	TX high power control CMOS input: 3.3 V → high power; 0 (or open) → low power; internal 100-kΩ pull-down resistor
21	PWR	TX-PA and VCO-PA power enable CMOS input: 3.3 V → on; 0 (or open) → off; internal 100-kΩ pull-down resistor
22	DIVP	Divider output, 300 Ω differential, DC coupled, external decoupling capacitor is required
23	DIVN	
24	DIVEN	Divider enable input, 3.3-V level, high-active CMOS input, internal 100-kΩ pull-down resistor
9 - 16, 25 - 32	NC	Not connected. These pins may be connected to ground. Performance will not be affected
(33)	GND	Exposed die attach pad of the QFN package, must be soldered to ground

4 Specification

4.1 Absolute Maximum Ratings

Attempted operation outside the absolute maximum ratings of the part may cause permanent damage to the part. Actual performance of the IC is only guaranteed within the operational specifications, not at absolute maximum ratings.

Table 2 Absolute Maximum Ratings

Parameter	Symbol	Min	Typ.	Max	Unit	Condition / Remark
Supply voltage	V_{CC}		3.3	3.6	V	To GND
DC voltage at tuning input Vt	V_{vt}	-0.3	0…4.5	4.7	V	
DC voltage at tuning input Icont	V_{Icont}	-0.3	0...3.3	3.6	V	
DC voltage at enable inputs	V_{EN}	-0.3	3.3	V_{CC} + 0.3	V	Inputs RXEN, DIVEN, PWR, HPEN
Junction temperature	T_J		20…50	150	°C	
Storage temperature range	T_{STG}	-65	25	150	°C	
ESD robustness	V_{ESD}			1.2	kV	Human body model, HBM [1, 2)]

1) If the devices are stored outside of the packaging, beyond this time limit, the device should be baked before use. The devices should be ramped up to a temperature of 125°C and baked for up to 12 hours.
2) CLASS 1C according to ESDA/JEDEC Joint Standard for Electrostatic Discharge Sensitivity Testing, Human Body Model Component Level, ANSI/ESDA/JEDEC JS-001-2011

4.2 Operating Range

Table 3 Operating Range

Parameter	Symbol	Min	Max	Unit	Remarks / Condition
Ambient temperature	T_A	-40	85	°C	
Supply voltage	V_{CC}	3.13	3.47	V	(3.3 V ± 5%)
DC voltage at tuning input Icont	V_{Icont}	0	V_{CC}	V	
DC voltage at tuning input V_T	V_{vt}	0	4.5	V	
DC voltage at enable inputs	V_{EN}	0	V_{CC}	V	
DC voltage at other inputs	V_x	0	V_{CC}	V	

Note: Do not drive input signals without power supplied to the device.

Power-up sequence should be the following:
1. Connect to ground
2. Apply V_{CC}
3. Set all control voltages

Power-down sequence should be the reverse of the above.

4.3 Thermal Resistance

Table 4 Thermal Resistance

Parameter	Symbol	Min	Typ	Max	Unit	Remarks / Condition
Thermal resistance, junction-to-ambient	R_{thja}			30	K/W	JEDEC JESD51-5

4.4 Electrical Characteristics

T_A = -40°C to +85°C unless otherwise noted. Target Values specified for T_A = 25°C and V_{CC} = 3.3 V, deviations w.r.t. test results under series production conditions possible.

Table 5 Electrical Characteristics

Parameter	Symbol	Min	Typ	Max	Unit	Remarks / Condition
DC Parameters						
Supply current consumption	I_{CC}		166	190	mA	Maximum current with ICNTL = 3.4 V
Enable input voltage, low level	V_{EN_L}	0		0.85	V	
Enable input voltage, high level	V_{EN_H}	2.05	2.15	V_{CC}	V	
VCO tuning voltage	V_{Vt}	0		4.5	V	
	V_{ICTNL}	0		V_{CC}	V	
RF Parameters						
Tx output start frequency	$f_{TX, MIN}$	112.3	113.9	115.9	GHz	VT = 0.0 V, ICTNL = 3.3 V
Tx output stop frequency	$f_{TX, MAX}$	130.1	134.1	137.2	GHz	VT = 4.5 V, ICTNL = 0.0 V
Tx tuning full bandwidth	Δf_{TX}	14.2	20.2	24.9	GHz	VT and ICTNL
VCO slope f vs. V for VT	$\Delta f_{TX}/\Delta V_{VT}$		˜1.8		GHz/V	for f_{TX} = 119 GHz
VCO slope f vs. V for ICTNL	$\Delta f_{TX}/\Delta V_{ICTNL}$		˜3.6		GHz/V	for f_{TX} = 127 GHz
Transmitter output power	P_{TX_PA}	-7	-3	0	dBm	At f_{TX} = 123 GHz, measured at output of Power Amplifier
Adjustable range output power	P_{TX_adj}	-2		10.5		HPEN to be used to adjust
Ratio $f_{TX\ OUT}$ vs. f_{DIV}	$f_{TX:div}$		64			
Divider output power	P_{div}		-9		dBm	Note 1
Divider output frequency	f_{div}	1,75	1.9	2,15	GHz	(f_{TX}/64 = f_{VCO} /32)
Divider Phase Noise @ 1.9 GHz	P_N		-125		dBc/Hz	Simulated value
Adjustable RX conversion gain			10			HPEN to be used to adjust (Simulated value).
IF frequency range	f_{IF}	0		200	MHz	
IF output impedance	Z_{OUT}		600		Ω	Differential outputs (simulated value)
IQ amplitude imbalance			3		dB	
IQ phase imbalance		-10		10	deg	
Noise figure (DSB)			9		dB	Simulated at 120 GHz.
Input compression point	1dB ICP		-14		dBm	Simulated w/o insertion loss antenna-chip.

Note 1: Measured single-ended. Divider outputs are loaded with 50 Ω, external decoupling capacitors are required. No 50-Ω match is required in application.

5 Packaging

5.1 Outline Dimensions

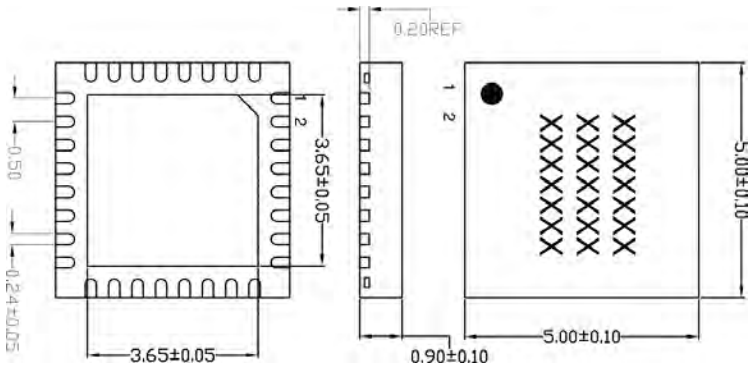


Figure 3 Outline Dimensions of QFN32 Package with Exposed Pad

5.2 Package Code

Top-Side Markings TRA045
YYWW

6 Application

6.1 Application Circuit Schematic

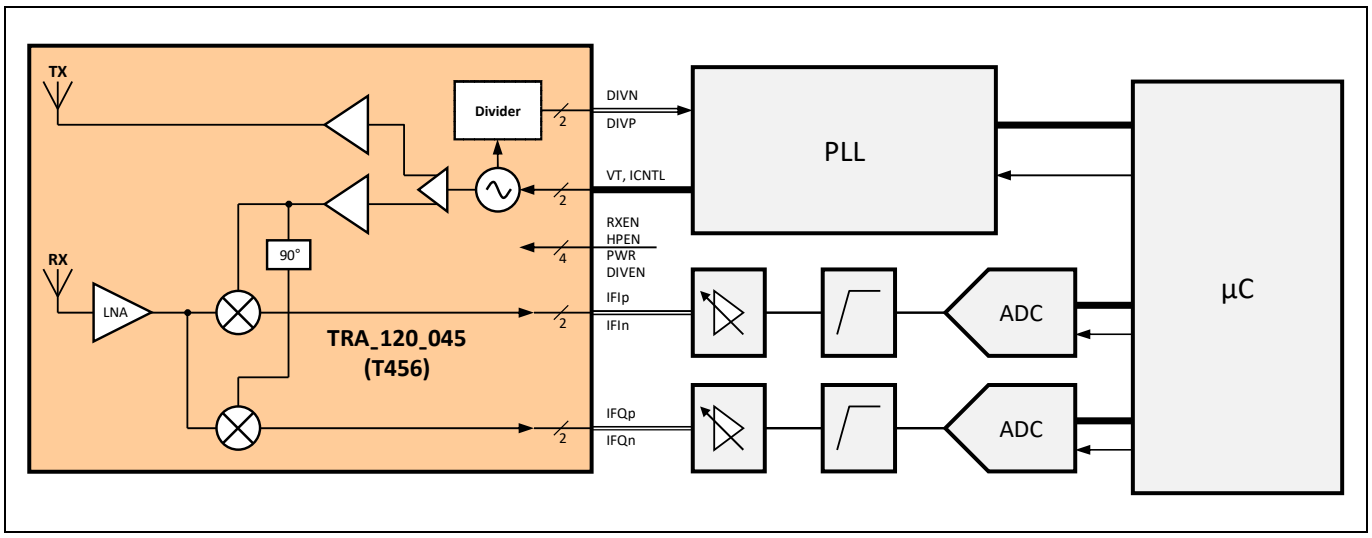


Figure 4 Application Circuit

6.2 Power Cycling

It is possible to reduce power consumption by power cycling the radar front end. Rapid power cycling can be implemented with voltage rise times between 10 and 100µs. At power-up, it must be ensured that no input signal is driven high before the supply voltage is stable. At power-down, all input signals must be pulled low before the supply voltage is switched off.

6.3 Evaluation Kit

For a quick and easy start into radar development Silicon Radar offers SiRad Easy® r4. It is a modular evaluation system for many of our integrated IQ transceivers with antennas in package or on PCB. It comes with a reference hardware and provides a complete design environment which can be configured via a browser-based graphical user interface. Its rich functionality and the open communication protocol make it a versatile tool – also for enhanced development projects.

It features:
- Distance measurement
- Velocity measurement
- Frequency modulated continuous wave mode (FMCW)
- Continuous wave mode (CW)

For more information about the features of SiRad Easy® r4 refer to the EvalKits-section in https://siliconradar.com/.

6.4 Input / Output Stages

The following figures show the simplified circuits of the input and output stages. It is important that the voltage applied to the input pins never exceeds V_{CC} by more than 0.3 V, which exception of V_{VT} cf. Section 4.1. Otherwise, the supply current may be conducted through the upper ESD protection diode connected at the pin.

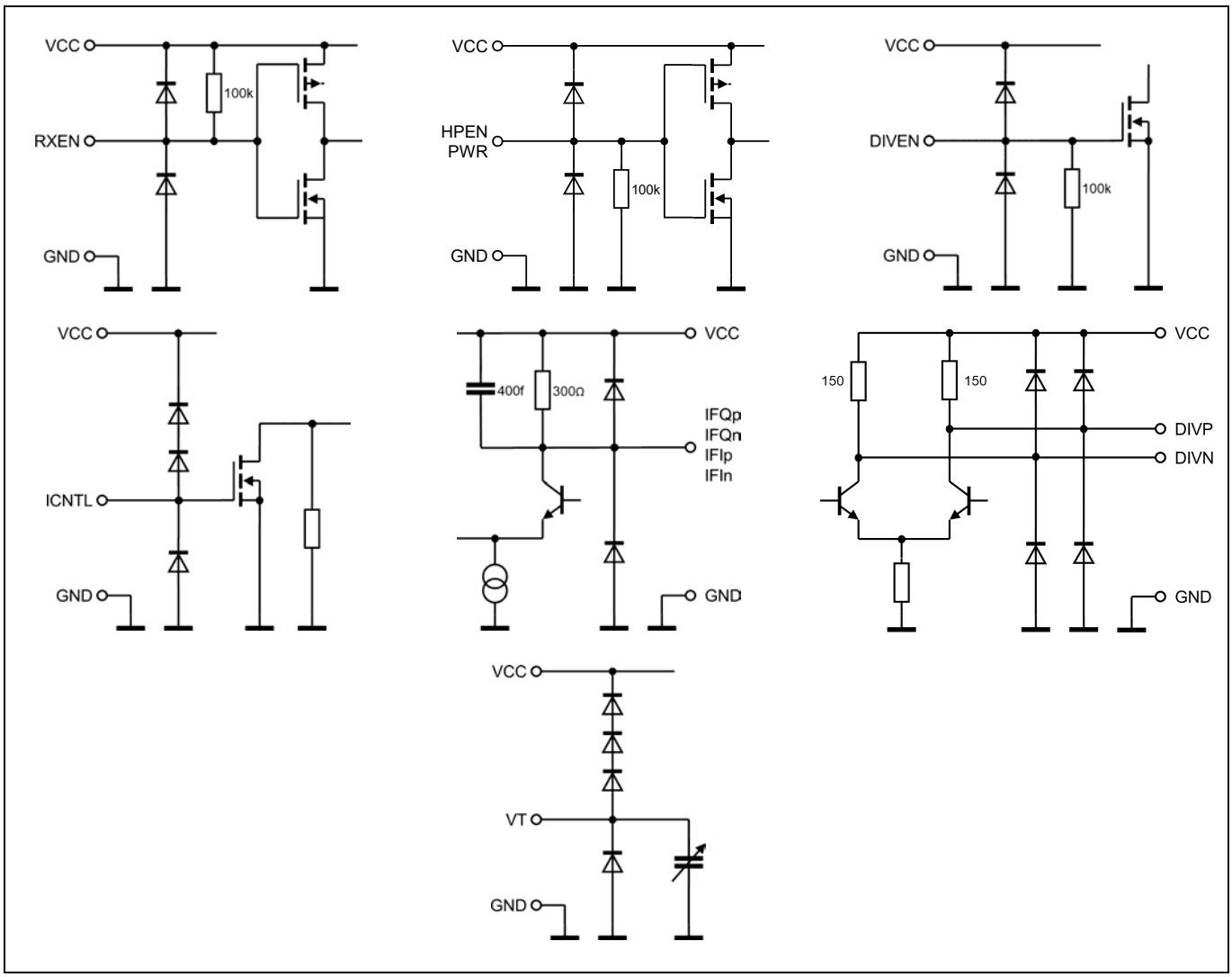


Figure 5 Equivalent I/O Circuits

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