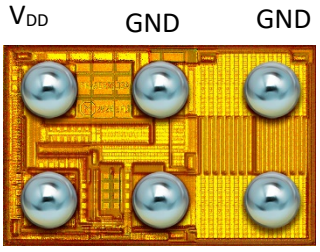
40 Volt, 10 Amp Peak, High-Frequency, Integrated Laser Driver

Description

The EPC21603 is a laser driver that is controlled using LVDS logic at high frequencies of up to 100 MHz to modulate laser driving currents of up to 10 Amps. Full driver integration is achieved using EPC's proprietary GaN IC technology.

Wafer level chip-scale packaging is used resulting in a BGA package that measures only 1.5 mm x 1 mm x 0.68 mm. The BGA package has low inductance and lays out very well with the laser system.

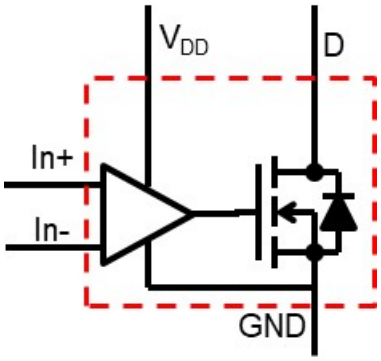


1.5 mm x 1 mm, 0.5 mm pitch
Bump side view

The EPC21603 uses a 5 V logic supply and is capable of interfacing to digital controllers. It can switch at frequencies exceeding 100 MHz.

Features

- V_{Laser} operating range up to 30 V
- 10 Amp peak current
- Switching frequency greater than 100 MHz
- Voltage switching time less than 500 ps
- 5 V nominal logic power supply
- LVDS logic compatible input control
- 2 ns minimum input pulse width
- 2.9 ns delay time from input to output

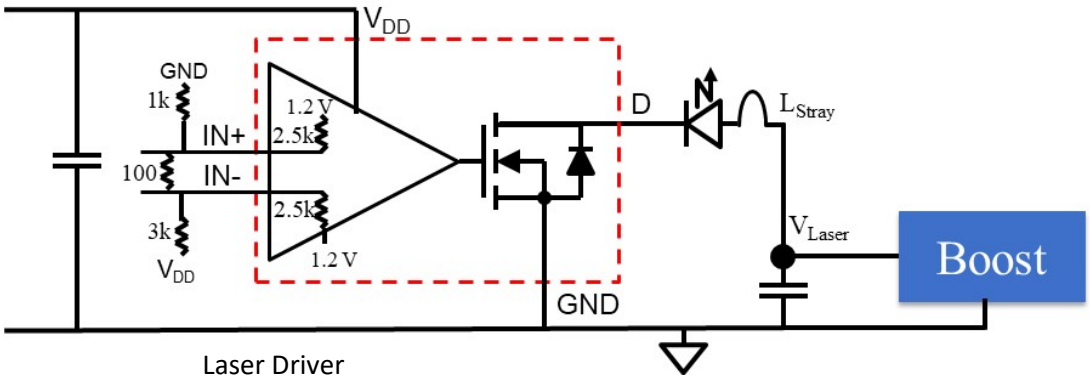


Functional Block Diagram

Applications

- Time of flight measurement
  - Gesture recognition
  - Gaming
  - Driver monitoring
  - Robotic vision
  - Vacuum cleaners
  - Industrial safety
  - Machine vision
- ToF module using VCEL laser for camera modules, laptops and smart phones

Typical Connection Diagram



Absolute Maximum Ratings

Absolute maximum ratings indicate sustained limits beyond which damage to the device may occur. All voltage parameters are absolute voltages referenced to GND unless indicated otherwise.

Symbol	Definition	Min	Max	Units
V_D	Drain Voltage		40	V
V_{DD}	Low Side Supply Voltage (V_{DD} to GND)	-0.3	5.5	V
IN	Logic Input	-0.3	5	V
I_D	Average Drain Current		1.7	A
T_J	Junction Temperature	-40	150	°C
T_{STG}	Storage Temperature	-40	150	°C

ESD Ratings

(Testing performed at EAG Lab. Need to get the relevant JEDEC specs for ESD ratings)

Symbol	Definition	Min	Units
HBM	Human-body model	+/-1000	V
CDM	Charged-device model	+/-500	V

Thermal Characteristics

$R_{\theta JA}$ is determined with the device mounted on one square inch of copper pad, single layer 2 oz copper on FR4 board.

Symbol	Definition	Typ	Units
$R_{\theta JC}$	Thermal Resistance, Junction to Case	TBD	°C/W
$R_{\theta JB}$	Thermal Resistance, Junction to Board	TBD	°C/W

$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	TBD	°C/W

Recommended Operating Conditions

For proper operation, the device should be used within the recommended conditions. All voltage parameters are absolute voltages referenced to GND unless indicated otherwise.

Symbol	Definition	Min	Typ	Max	Units
V_{Laser}	Input Voltage (V_{IN} to GND)	10		30	V
V_{DD}	Logic Supply Voltage		5		V

Truth Table

IN	Laser
IN+ ≤ IN-	Off
IN+ > IN-	On

Electrical Characteristics

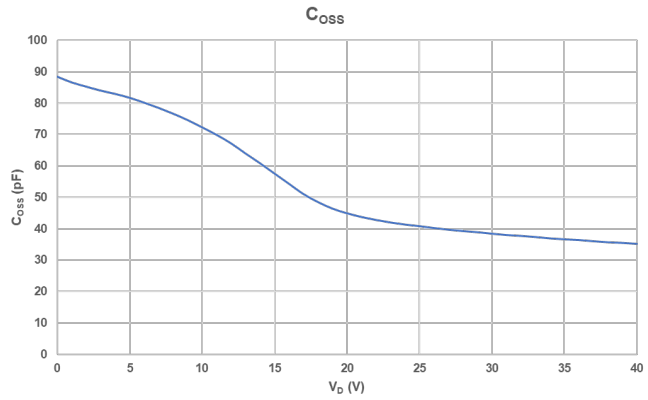
All ratings at T_J = 25 ˚C. V_{Laser} = 15 V, I_D = 5 A, V_{IL} = 0 V, V_{IH} = 3.3 V, V_{DD} = 5 V, R_D = 100 Ω unless indicated otherwise.

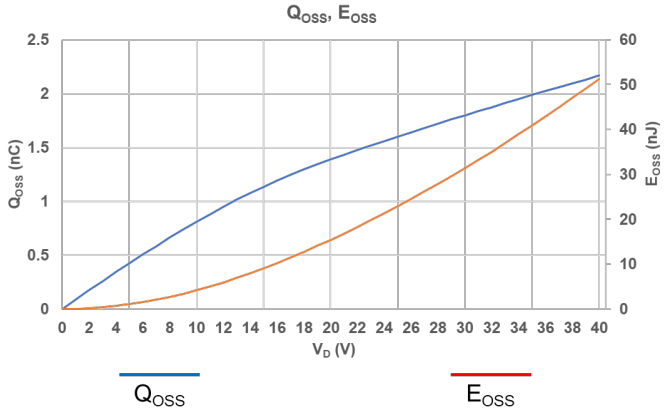
Symbol	Definition	Min	Typ	Max	Units
Operating Power Supply, V_{DD}					
$I_{DD\ (Off)}$	V_{DD} Quiescent current with laser driver off		10.5	12.5	mA
$I_{DD\ (30\ MHz)}$	Operating current off V_{DD}		47	58	mA
Input Pins					
V_{ITH+}	Positive-going differential input voltage, T_J = -40 ˚C to 150 ˚C			100	mV
V_{ITH-}	Negative-going differential input voltage, T_J = -40 ˚C to 150 ˚C	-100			mV
R_C	Common-mode input resistance to 1.2 V		2.5		kΩ
Power Stage					
$R_{DS(on)}$	Drain to Source Resistance		90		mΩ
$I_{D(peak)}$	Peak Laser Drive Current Capability	10			A
C_{OSS}	V_{DS} = 20 V		45		pF
Q_{OSS}	V_{DS} = 20 V		1.4		nC
E_{OSS}	V_{DS} = 20 V		15		nJ

Dynamic Characteristics					
$t_{D(on)}$	Turn on delay time		3.5	4.5	ns
t_F	Drain fall time		0.41	0.6	ns
$t_{D(off)}$	Turn off delay time		3.1	4.0	ns
t_R	Drain rise time *		0.32	0.5	ns
t_{dPW}	Pulse width distortion	-0.7	-0.4	-0.2	ns
$t_{in(min(on))}$	Minimum input pulse width		2.5		ns
$t_{On(Max)}$	Maximum on time		500		ns
$t_{Off(Max)}$	Maximum off time V_D < 10 V		100		ns

Pinout Description

Pin	Description
V_{DD}	Input Voltage Supply (Decouple to GND with small, low inductance capacitor)
In+	Differential (LVDS) non-inverting input
In-	Differential (LVDS) inverting input
D	Power Drain
GND	Power and Signal Ground

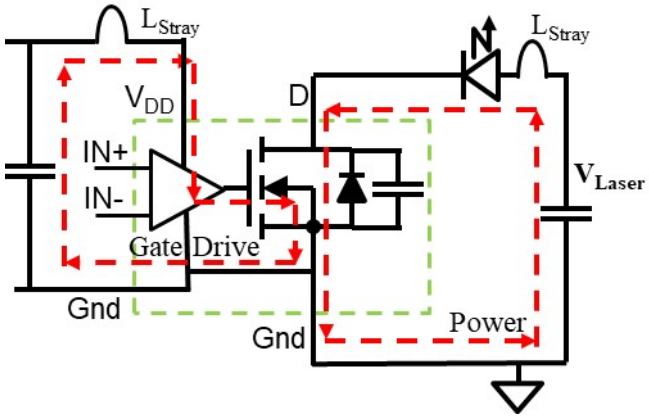


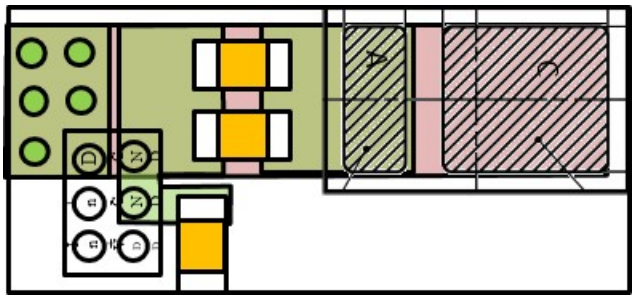


Application Information

Layout and decoupling: Minimizing inductance in both power and gate drive loops is critical. The power loop is primary, and gate drive loop secondary. Short, wide traces are required, and returning in the second layer, using a thin dielectric will cancel much of the inductance. Using multiple ceramic capacitors in parallel will reduce stray inductance and impedance in the power loop. Use high quality NPO or COG capacitors for both power and gate drive. This will increase effective capacitance as capacitors with lower quality materials will lose much more capacitance with voltage. Recommended layout is shown below. Component recommendations for power and gate drive decoupling capacitors are shown in the demonstration board quick start guide.

Turn off current is limited by the energy of the power loop stray inductance transferring to the C_{OSS} of the power FET of the laser driver. E_{OSS} versus V_{DS} curve is in the datasheet.

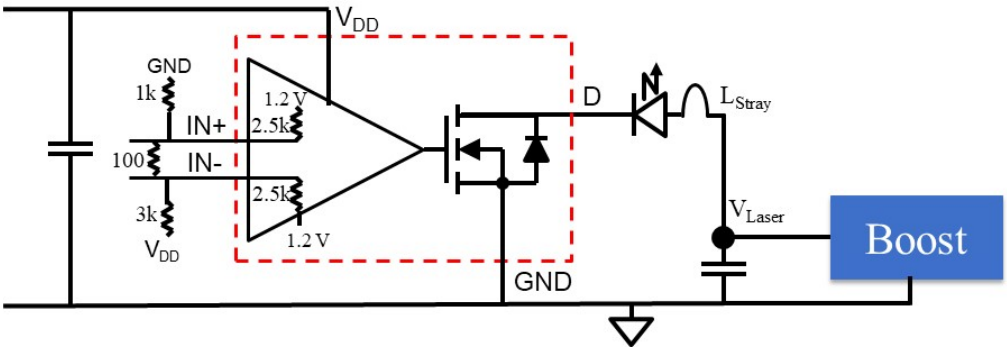




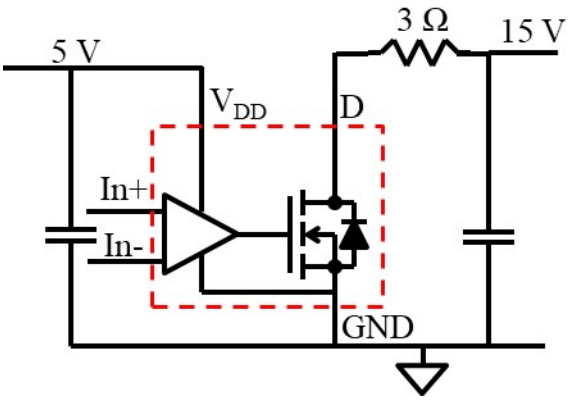
Cathode to drain connection on second conductor layer.

Start up: V_{DD} should be applied before the laser voltage. For applications where the laser voltage is below 10 V, it may take a few pulses before the pulse width stabilizes. For correct measurement, it may be necessary to ignore the first few pulses.

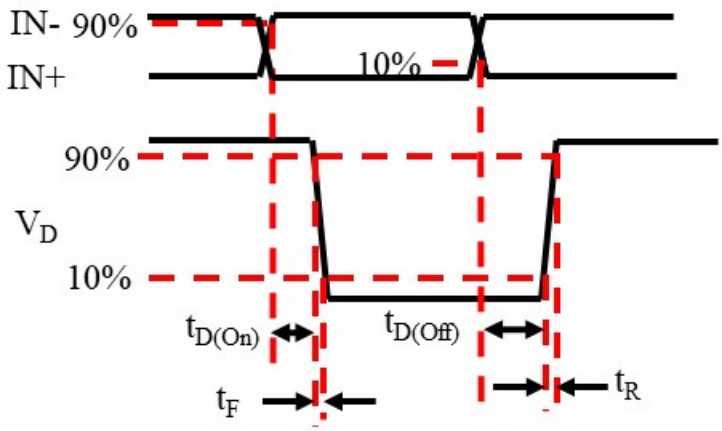
Input logic: LVDS inputs are used with each input internally pulled to 1.2 V with 2.5 kΩ . For safety IN+ should be pulled to ground with 1 kΩ and IN- should be pulled to V_{DD} with 3 kΩ.



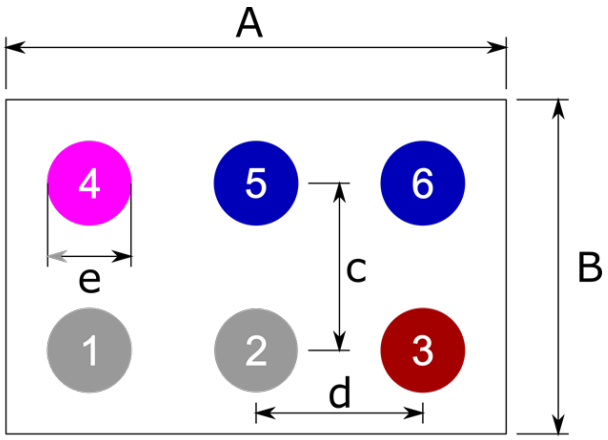
Parameter Measurement Test Circuits



Parameter Measurement Definitions



Die Outline (solder bump view)



DIM	MICROMETERS		
	MIN	Nominal	MAX
A	1420	1450	1480
B	920	950	980
c		500	
d		500	
e	238	264	290

Pad 1 is IN+

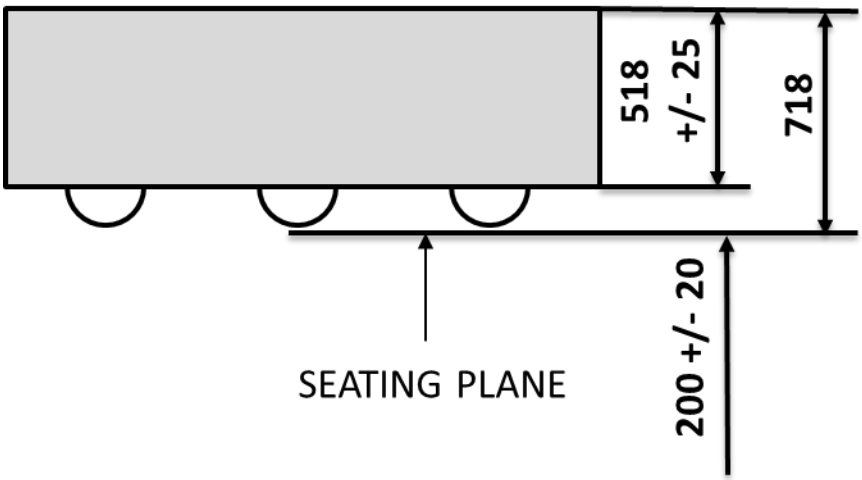
Pad 2 is IN-

Pad 3 is Drain

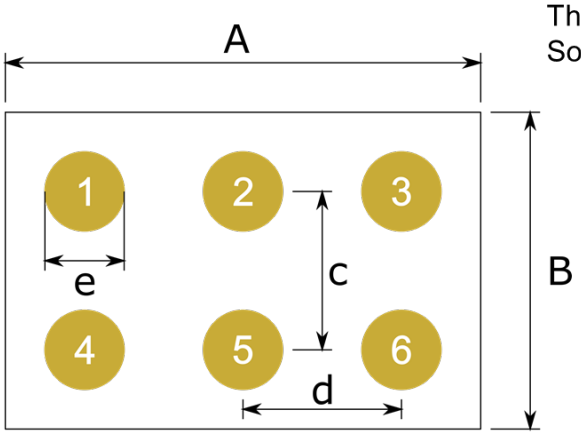
Pad 4 is VDD

Pads 5, 6 are Source

Side View



Recommended Land Pattern



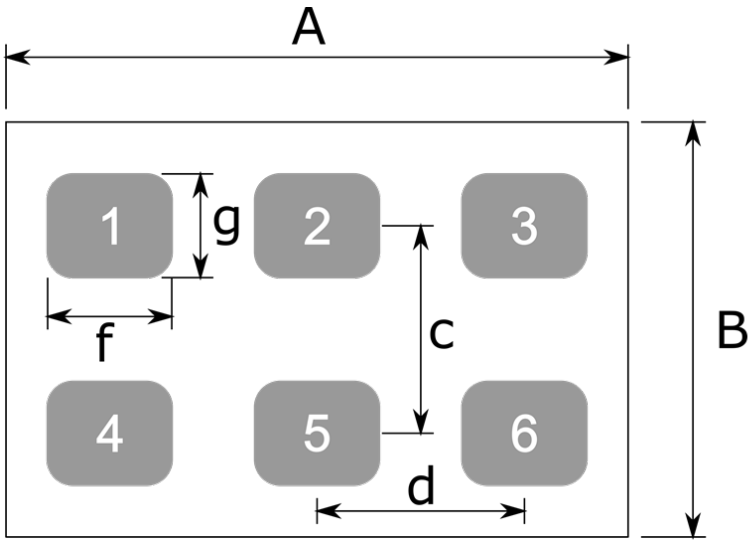
The land pattern is solder mask defined
Solder mask is 10µm smaller per side than bump

DIM	MICROMETERS
A	1450
B	950
c	500
d	500
e	230

Pad 1 is IN+
Pad 2 is IN-
Pad 3 is Drain
Pad 4 is VDD
Pads 5, 6 are Source

Recommended Stencil Drawing

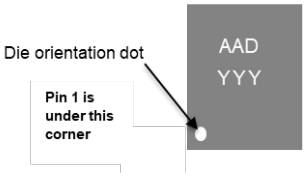
(measurements in µm)



DIM	MICROMETERS
A	1450
B	950
c	500
d	500
f	300
g	250

Recommended stencil should be 4mil (100 µm) thick, must be laser cut , opening per drawing.
The corner has a radius of R60
Intended for use with SAC305 Type 4 solder, reference 88.5% metals content.
Additional assembly resources are available at:
epc-co.com/epc/DesignSupport/AssemblyBasics.aspx

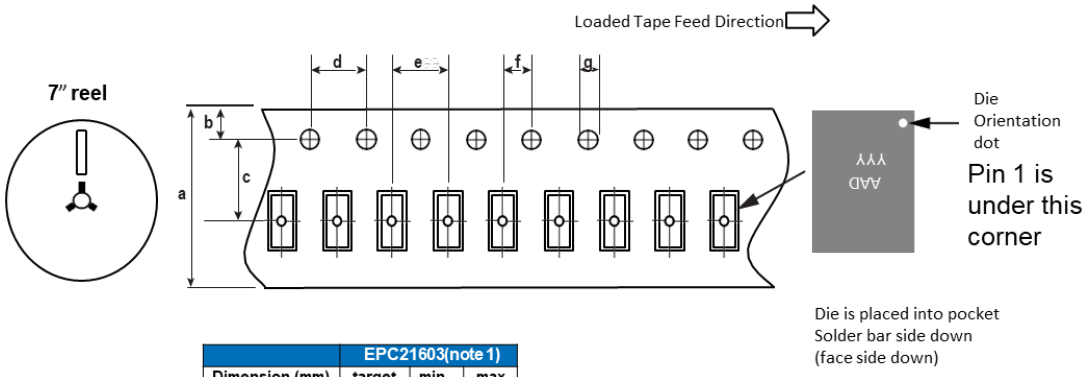
Die Marking



Part Number	Laser Markings	
	Part # Marking Line 1	Lot_Date Code Marking Line 2
EPC21603	AAD	YYY

Tape and Reel Configuration

4mm pitch, 8mm wide tape on 7" reel



	EPC21603(note 1)		
Dimension (mm)	target	min	max
A	8.00	7.90	8.30
B	1.75	1.65	1.85
c (see note)	3.50	3.45	3.55
d	4.00	3.90	4.10
e	4.00	3.90	4.10
f (see note)	2.00	1.95	2.05
g	1.50	1.50	1.60

Note 1: MSL 1 (moisture sensitivity level 1) classified according to IPC/JEDEC industry standard.
Note 2: Pocket position is relative to the sprocket hole measured as true position of the pocket, not the pocket hole.

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