Description

This document describes the specification for the F1385 Digital Pre-Distortion Demodulator for PA linearization. This series of devices is offered in two frequency variants to cover common UTRA bands.

Competitive Advantage

In typical Base Station transmitters digital pre-distortion is employed to improve the transmitter performance. The signal out of the PA is sampled and the incoming TX chain I & Q data is pre-distorted to counteract the distortion inherent in the PA. The PA signal is adjusted via a digital step attenuator to a lower level and then sub-sampled at an IF frequency of ~350 MHz which necessitates the need for a highly linear demodulator to downconvert to quadrature IF from the transmit frequency. By sampling IF_I and IF_Q independently and then digitally combining these signals, an effective doubling of the sample rate can be achieved. Any distortion in this path will degrade the performance of the DPD algorithm. By utilizing an ultra-linear demodulator with integrated DSA such as the F1385, the ACLR and/or power consumption of the full TX system can be improved significantly.

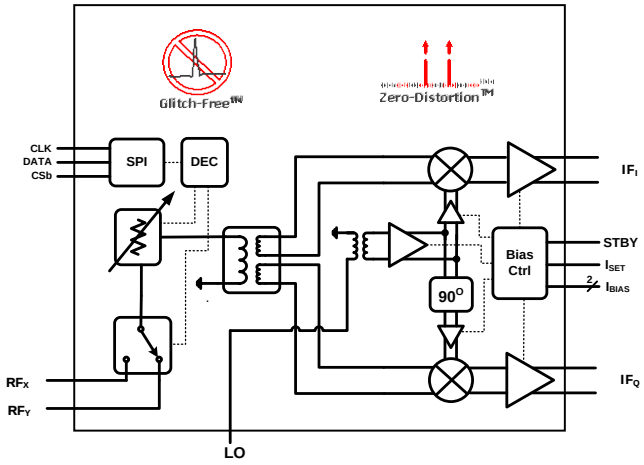
- DPD full path ACLR: Reduced by 1 dB
- I_{CC}: Typically 45% less current
- *Zero-Distortion™* eliminates 2 IF amps
- Integrates 2 Baluns, SP2T RF switch
- *Glitch-Free™* gain control

Features

- ✓ Wide flat performance IF BW
- ✓ Wide RF BW (~ 1.2 GHz)
- ✓ Ideal for Multi-Carrier Systems
- ✓ Drives ADC directly
- ✓ Ultra linear +39 dBm OIP3
- ✓ Excellent ACLR performance
- ✓ 100 Ω differential output impedance
- ✓ Fully integrated DPD demodulator
- ✓ 6 x 6 mm 36-pin package
- ✓ Standby Mode w/Fast Recovery
- ✓ I_{CC}: 210 mA

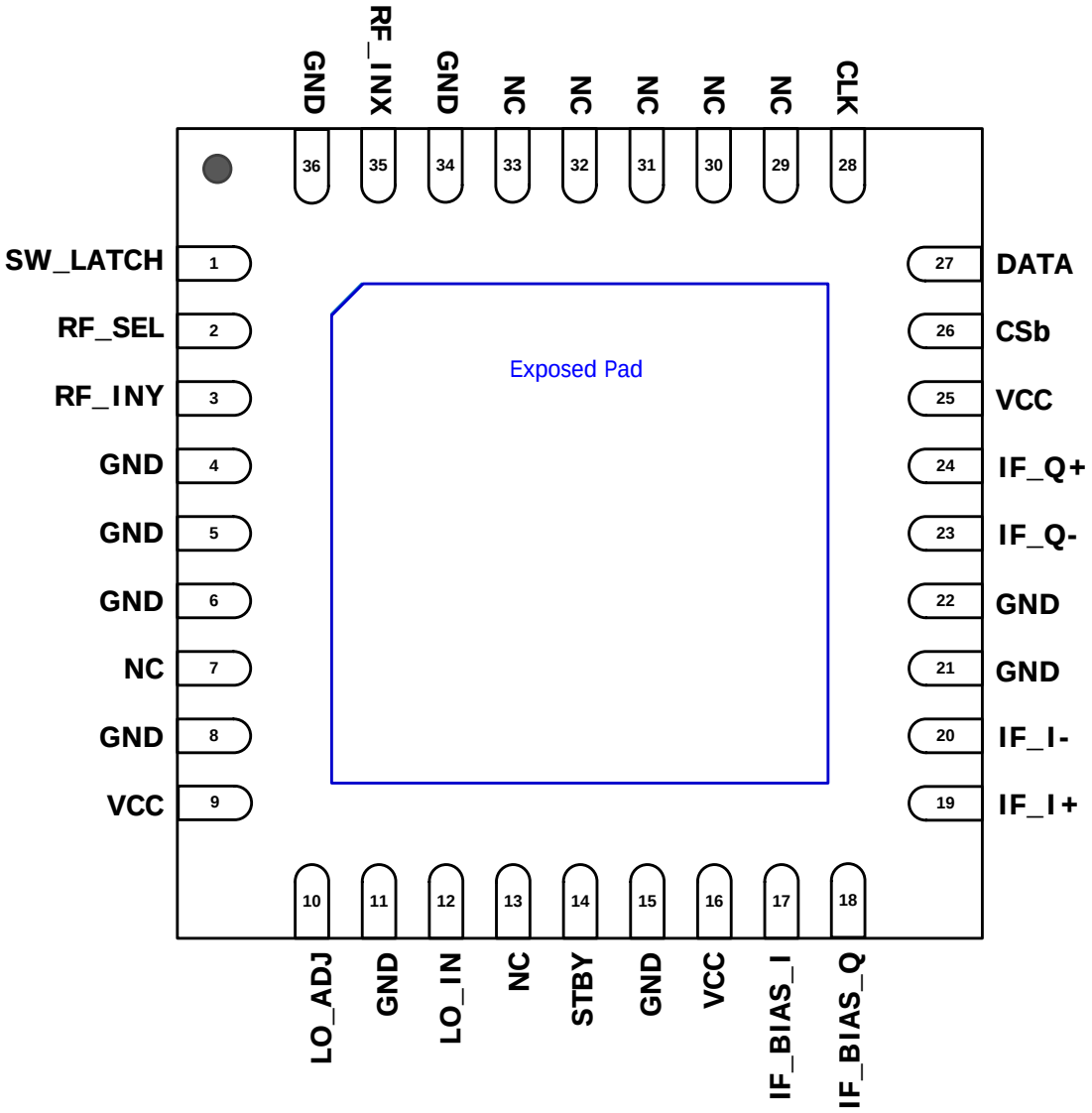
Block Diagram

Figure 1. Block Diagram



Pin Assignments

Figure 2. Pin Assignments for 6 x 6 x 0.75 mm-TQFN Package – Top View



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Pin Descriptions

Table 1. Pin Descriptions

Number	Name	Description
1	SW_LATCH	Stand-by latch. Pull Low or Ground for Normal Operation. If left floating, this input will be internally pulled high, disabling SPI writes to ENb (Standby) and RF SW bits (A0, A2).
2	RF_SEL	RF input selection. Pull high to select RF_INY. Pull low to select RF_INX.
3	RF_INY	Alternate RF Input. Separated from RF_INX by internal SP2T. AC couple to this pin. This is a reflective switch and is not internally matched to 50 ohms.
4, 5, 6, 8, 11,15, 21, 22, 34, 36	GND	Ground these Pins.
7, 13, 29, 30, 31, 32, 33	NC	No Connection. Not internally connected. OK to connect to Vcc. Recommended Connection is Ground.
9, 16, 25	VCC	Power Supply. Bypass to GND with capacitors shown in the Typical Application Circuit as close as possible to pin.
10	LO_ADJ	Connect the specified resistor from this pin to ground to set the LO path ICC. This is a current setting resistor.
12	LO_IN	LO Input. AC couple to this pin. Internally matched to 50 ohms.
14	STBY	STBY Mode. Pull this pin high for Standby mode (~20 mA). Pull low or Ground for normal operation.
17	IF_BIAS_I	Connect the specified resistor from this pin to ground to set the IF amplifier bias reference. This is NOT a current setting resistor.
18	IF_BIAS_Q	Connect the specified resistor from this pin to ground to set the IF amplifier bias reference. This is NOT a current setting resistor.
19	IF_I+	*In-Phase Positive* Port Mixer Differential IF Output. Connect pullup inductors from each of these pins to VCC (see the Typical Application Circuit).
20	IF_I-	*In-Phase Negative* Port Mixer Differential IF Output. Connect pullup inductors from each of these pins to VCC (see the Typical Application Circuit).
23	IF_Q-	*Quadrature Negative* Port Mixer Differential IF Output. Connect pullup inductors from each of these pins to VCC (see the Typical Application Circuit).
24	IF_Q+	*Quadrature Positive* Port Mixer Differential IF Output. Connect pullup inductors from each of these pins to VCC (see the Typical Application Circuit).
26	CSb	Chip Select Bar. The falling edge initiates a programming cycle and the rising edge latches the programmed shift register data into the active register.
27	DATA	Serial Data Input.
28	CLK	Serial Clock Input.
35	RF_INX	Main RF Input. Separated from RF_INY by internal SP2T. AC couple to this pin. This is a reflective switch and is not internally matched to 50 ohms.
	— EP	Exposed Pad. Internally connected to GND. Solder this exposed pad to a PCB pad that uses multiple ground vias to provide heat transfer out of the device into the PCB ground planes. These multiple grounds are also required to achieve the noted RF performance.

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Absolute Maximum Ratings

The absolute maximum ratings are stress ratings only. Stresses greater than those listed below can cause permanent damage to the device. Functional operation of the F1385 at absolute maximum ratings is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

Table 2. Absolute Maximum Ratings

Parameter	Symbol	Minimum	Maximum	Units
VCC to GND	V_{CC}	-0.3	+5.5	V
SW_Latch, DATA, CSb, CLK, RF_SEL	V_{CTRL}	-0.3	+3.6	V
STBY	V_{STBY}	-0.3	V_{CC}	V
IF_I+, IF_I-, IF_Q+, IF_Q-	V_{IF}	1	V_{CC} + 0.3	V
LO_IN	V_{LO}	-0.3	+0.3	V
RF_INX, RF_INY	V_{RX}	-0.3	+0.3	V
IF_Bias_I to GND IF_Bias_Q to GND	V_{IFBIAS}	-0.3	+1.2	V
LO_ADJ to GND	V_{LO_ADJ}	+2.1	+4.0	V
RF Input Power (Into RFIN_X or RFIN_Y) for 24 hours	P_{IN}		+27	dBm
Continuous Power Dissipation	P_{diss}		2.5	W
Junction Temperature	T_j		150	°C
Storage Temperature Range	T_{st}	-65	150	°C
Lead Temperature (soldering, 10s)			260	°C
ElectroStatic Discharge – HBM (JEDEC/ESDA JS-001-2012)			1000 (Class 1C)	V
ElectroStatic Discharge – CDM (JEDEC 22-C101F)			500 (Class C2)	V

Recommended Operating Conditions

Table 3. Recommended Operating Conditions

Parameter	Symbol	Condition	Minimum	Typical	Maximum	Units
Supply Voltage	V_{CC}	All V_{CC} pins	4.75		5.25	V
Operating Temperature Range	T_{CASE}	Exposed Paddle Temperature	-40		+105	°C
RF Frequency Range	F_{RF}		3200		4400	MHz
LO Frequency Range	F_{LO}		2850		4050	MHz
LO Power	P_{LO}		-6	-3	0	dBm
IF Frequency Range	F_{IF}		20		500	MHz
RF Input Impedance	Z_{RF}	Single Ended		50		Ω
IF Output Impedance	Z_{IF}	Differential		100		Ω
LO Input Impedance	Z_{LO}	Single Ended		50		Ω

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Electrical Characteristics

Table 4. Electrical Characteristics

See F1385 typical application circuit. Specifications apply at V_{CC} = +5.0 V, F_{RF} = 3600 MHz, F_{LO} = 3250 MHz, P_{LO} = 0 dBm, F_{IF} = 350 MHz, Gain = G_{MAX}, T_{CASE}= +25 °C, STBY = GND unless otherwise noted. Full Lineup measured through to I or Q path including 180 degree combiner. The IF transformers and RF input trace losses are de-embedded.

Parameter	Symbol	Condition	Minimum	Typical	Maximum	Units
Logic Input High	V_{IH}	For STBY, DATA, CSb, CLK, SW_Latch, RF_Sel	***1.1***			V
Logic Input Low	V_{IL}	For STBY, DATA, CSb, CLK, SW_Latch, RF_Sel			***0.5***	V
Logic Current	I_{IH}, I_{IL}	V_{IH} = 2.3 V, V_{IL} = 0 V	***-107***		***+10***	µA
Supply Current	I_{CC}	Total V_{CC}		210	***240*** [a]	mA
Supply Current	I_{STBY}	Standby Mode: STBY > V_{IH}		20	***30***	mA
Oversample RF Range	F_{RFD}	Measure Gain at I & Q Gain setting = G_{MAX} F_{IF}: 350 MHz F_{LO}: 2850 MHz to 4050 MHz Gain Delta < 3.5 dB	***3200***		***4400***	MHz
RF Linearity BW	RF_{LIN}	F_{IF}: 350 MHz Gain setting = G_{MAX} Input: RF_INX Pin = -18 dBm/Tone OIP3 > +35 dBm	3400 [b]		4200	MHz
Oversample IF Range	F_{IFD}	Measure Gain at I & Q Gain setting = G_{MAX} F_{RF}: 3400 MHz to 3880 MHz F_{LO}: 3380 MHz Gain Delta < 2.5 dB	***20***		***500***	MHz
IF Linearity BW	IF_{LIN}	F_{RF}: 3600 MHz F_{LO}: 3150 MHz to 3500 MHz Gain setting = G_{MAX} Input: RF_INX Pin = -18 dBm/Tone OIP3 > +35 dBm	100	350	450	MHz

[a] Items in min/max columns in ***bold italics*** are Guaranteed by Test.
[b] Items in min/max columns that are not bold/italics are Guaranteed by Design Characterization.

Table 5. Electrical Characteristics (continued)

See F1385 typical application circuit. Specifications apply at V_{CC} = +5.0 V, F_{RF} = 3600 MHz, F_{LO} = 3250 MHz, P_{LO} = 0 dBm, F_{IF} = 350 MHz, Gain = G_{MAX}, T_{CASE}= +25 °C, STBY = GND unless otherwise noted. Full Lineup measured through to I or Q path including 180 degree combiner. The IF transformers and RF input trace losses are de-embedded.

Parameter	Symbol	Condition	Minimum	Typical	Maximum	Units
Gain maximum	G_{MAX}	From RF_INX to I & Q Gain setting = G_{MAX} Pin = -20 dBm	***16***	18	***20***	dB
Gain minimum	G_{MIN}	From RF_INX to I & Q Gain setting = G_{MIN} Pin = +5 dBm		-7.5		dB
Gain Flatness	G_{FLAT1}	F_{RF}: 3400 MHz and 3600 MHz F_{LO}: 3150 MHz F_{IF}: 250 MHz and 450 MHz		0.5	***0.8***	dB
	G_{FLAT2}	F_{RF}: 3600 MHz and 3800 MHz F_{LO}: 3350 MHz F_{IF}: 250 MHz and 450 MHz		0.5	***0.8***	
	G_{FLAT3}	F_{RF}: 3350 MHz and 3650 MHz F_{LO}: 3150 MHz F_{IF}: 200 MHz and 500 MHz		1.0	***1.5***	
	G_{FLAT4}	F_{RF}: 3550 MHz and 3850 MHz F_{LO}: 3350 MHz F_{IF}: 200 MHz and 500 MHz		1.0	***1.5***	
RF Return Loss	RL_{RF}			14		dB
LO Return Loss	RL_{LO}			10		dB
IF Return Loss	RL_{IF}	Differential		15		dB
Noise Figure	NF	From RF_INX to I or Q Gain setting = G_{MAX}		20	23	dB
Output IP3 – G_{MAX}	$OIP3_{MAX}$	Measured at I & Q P_{IN} = -18 dBm per tone 5 MHz Tone Separation Gain setting = G_{MAX}	***35***	39		dBm
Output IP3 – G_{-20}	$OIP3_{-20}$	Measured at I & Q P_{IN} = +2 dBm per tone 5 MHz Tone Separation Gain setting = G_{-20}		38		dBm
Output IP2	OIP2	Measured at I & Q P_{IN} = -18 dBm per tone 5MHz Tone Separation Gain setting = G_{MAX} $F_1 + F_2$ (High Side)	50	59		dBm

[a] Items in min/max columns in ***bold italics*** are Guaranteed by Test.
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Table 6. Electrical Characteristics (continued)

See F1385 typical application circuit. Specifications apply at V_{CC} = +5.0 V, F_{RF} = 3600 MHz, F_{LO} = 3250 MHz, P_{LO} = 0 dBm, F_{IF} = 350 MHz, Gain = G_{MAX}, T_{CASE}= +25 °C, STBY = GND unless otherwise noted. Full Lineup measured through to I or Q path including 180 degree combiner. The IF transformers and RF input trace losses are de-embedded.

Parameter	Symbol	Condition	Minimum	Typical	Maximum	Units
2nd Harmonic	H2	Measured at I & Q P_{OUT} = -6 dBm Gain setting = G_{MAX}		-72	-65	dBc
Input Power 1dB Compression	IP1dB	Measured at I & Q Gain setting = G_{MAX}	***-2***	0		dBm
Quadrature Amplitude Balance	BAL_G	F_{LO}: 3150 MHz F_{RF}: 3500 MHz	***-0.25***		***+0.25***	dB
Quadrature Phase Balance	BAL_ϕ	F_{LO}: 3150 MHz F_{RF}: 3500 MHz		1.5		degrees
Equivalent Image Rejection over Environmental Conditions [c]	IR	T_a = -45 °C to T_c = 105 °C, LO drive = -6 dBm to 0 dBm, LO = 3.0 to 4.0 GHz, IF = 350 MHz Low Side LO	30	35		dB
LO to IF leakage	ISO_{LI}	Output Balun has not been de-embedded.		-30	-25	dBm
LO to RF leakage	ISO_{LR}			-42		dBm
RF to IF Isolation	ISO_{RI}	RF leakage at IF which is relative to IF output level Output balun has not been de-embedded.		-45	-40	dBc
RF Switch Isolation	ISO_{RFSW}			-35		dB

[a] Items in min/max columns in ***bold italics*** are Guaranteed by Test.
[b] Items in min/max columns that are not bold/italics are Guaranteed by Design Characterization.
[c] Calculated from the measured amplitude and phase balance.

Table 7. Electrical Characteristics (continued)

See F1385 typical application circuit. Specifications apply at V_{CC} = +5.0 V, F_{RF} = 3600 MHz, F_{LO} = 3250 MHz, P_{LO} = 0 dBm, F_{IF} = 350 MHz, Gain = G_{MAX}, T_{CASE}= +25 °C, STBY = GND unless otherwise noted. Full Lineup measured through to I or Q path including 180 degree combiner. The IF transformers and RF input trace losses are de-embedded.

Parameter	Symbol	Condition	Minimum	Typical	Maximum	Units
Attenuator Range	Range			25.5		dB
Attenuator Resolution	LSB			0.5		dB
Attenuator Glitching	$ATTN_G$	Step from 15.5 to 16.0 dB Step from 16.0 to 15.5 dB Measure maximum excursion		0.7		dB
Attenuator Step Accuracy	DNL			0.2		dB
Attenuator Absolute Accuracy	INL	0.5 dB to 25.5 dB range		0.2	***1***	dB
Serial Clock Speed	F_{CLOCK}	SPI 3 wire bus		20	***50***	MHz
Data to Clock Setup	τ_S	SPI 3 wire bus	3			ns
Data to Clock Hold	τ_H	SPI 3 wire bus	3			ns
Clock to CSb Setup	τ_{EN}	SPI 3 wire bus	3			ns
Clock Pulse Width	τ_W	SPI 3 wire bus	5			ns
RF Switch and attenuator settling times [c]						
EN bit on	EN_{ON}	LO_IN: 3250 MHz, 0 dBm RF_INX: 3600 MHz, -20 dBm		100		ns
EN bit off	EN_{OFF}			50		ns
RF switched X to Y (no RF Y signal)	$RFSW_{XY}$			150		ns
RF switched Y to X (no RF Y signal)	$RFSW_{YX}$			200		ns
Attenuator Switching Time 0.0 dB to 25.5 dB (max)	ATT_{SETL1}			300		ns
Attenuator Switching Time 25.5 dB (max) to 0.0 dB	ATT_{SETL2}			300		ns
Attenuator Switching Time 15.5 dB to 16.0 dB	ATT_{SETL3}			250		ns
Attenuator Switching Time 16.0 dB to 15.5 dB	ATT_{SETL4}			250		ns

[a] Items in min/max columns in ***bold italics*** are Guaranteed by Test.
[b] Items in min/max columns that are not bold/italics are Guaranteed by Design Characterization.
[c] SPI write time. Define Switching Time: The time from 50% CSb to within 0.1 dB of final value for switching states or 1 dB for isolation.

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Thermal Characteristics

Table 8. Package Thermal Characteristics

Parameter	Symbol	Value	Units
Junction to Ambient Thermal Resistance.	θ_{JA}	40	°C/W
Junction to Case Thermal Resistance. (Case is defined as the exposed paddle)	θ_{JC}	3	°C/W
Moisture Sensitivity Rating (Per J-STD-020)		MSL 1	

Typical Operating Conditions (TOC)

Unless otherwise noted, for the TOC graphs on the following pages, the following conditions apply:

- IF = 350 MHz
- Tone spacing = 5 MHz
- Pin = - 18dBm / Tone
- Pout ~ 0dBm / Tone
- RF_X, IF_Q selected
- Minimum Attenuation selected (0 dB ATTN)
- V_{CC} = 5.00 V
- LO level = 0 dBm
- Case (exposed paddle) Temperature = 25 °C
- All Temperatures are Case Temperature (T_{CASE} or T_C)
- Output Transformers losses are de-embedded
- Input RF trace losses are de-embedded
- Measurements are made to the individual IF combined ports (I and Q)

Typical Performance Characteristics

Figure 3. Gain vs. T_{case} [Low Side LO, RF_X]

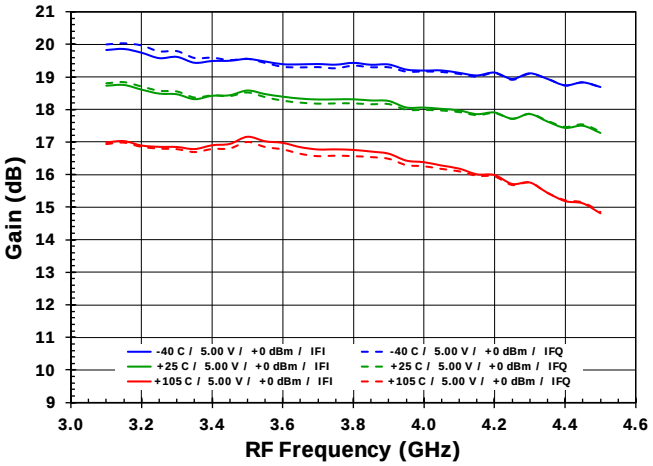


Figure 4. Gain vs. T_{case} [Low Side LO, RF_Y]

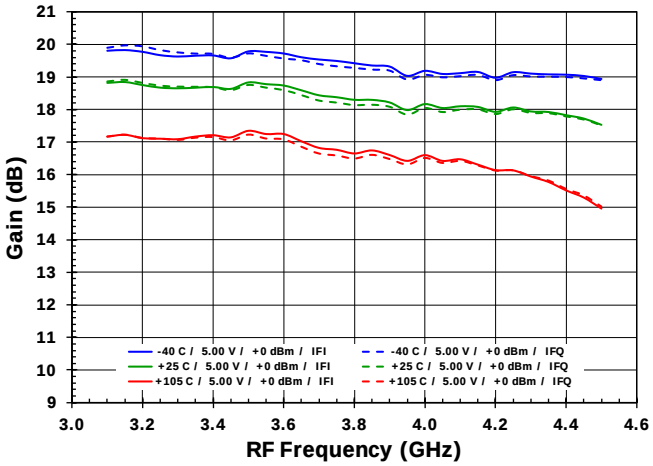


Figure 5. Gain vs. V_{cc} [Low Side LO, RF_X]

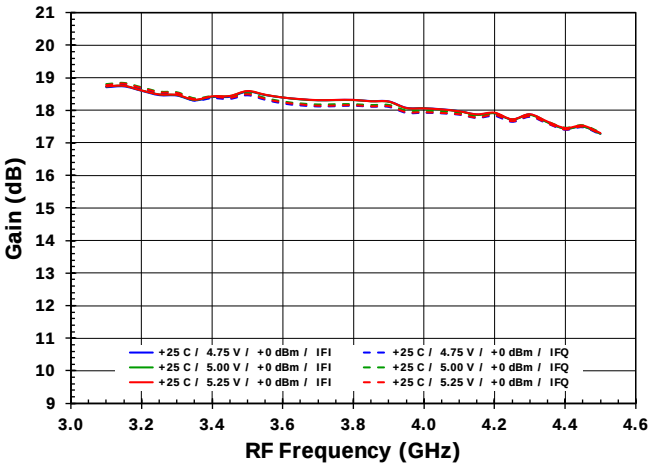


Figure 6. Gain vs. V_{cc} [Low Side LO, RF_Y]

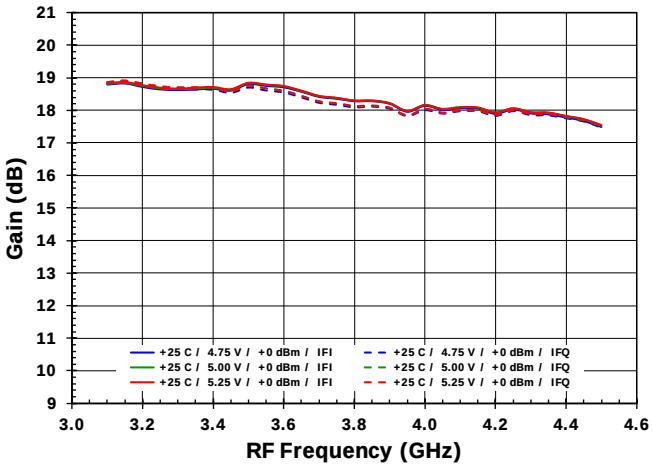


Figure 7. Gain vs. LO Power [Low Side LO, RF_X]

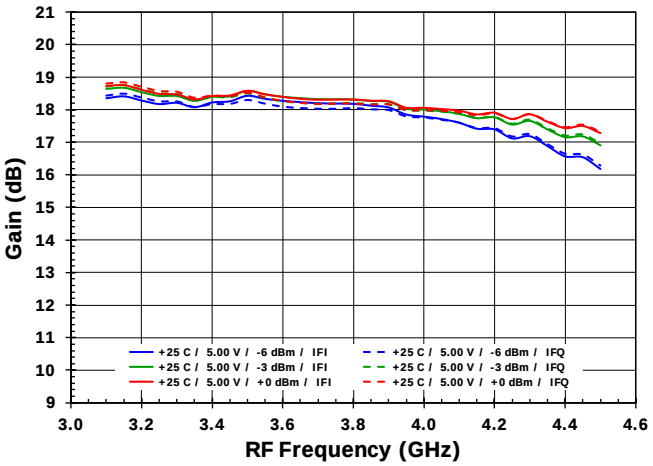


Figure 8. Gain vs. LO Power [Low Side LO, RF_Y]

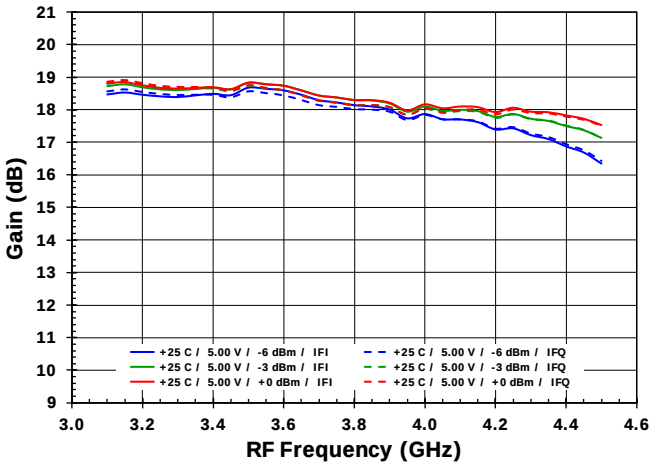


Figure 9. Gain vs. T_{case} [High Side LO, RF_X]

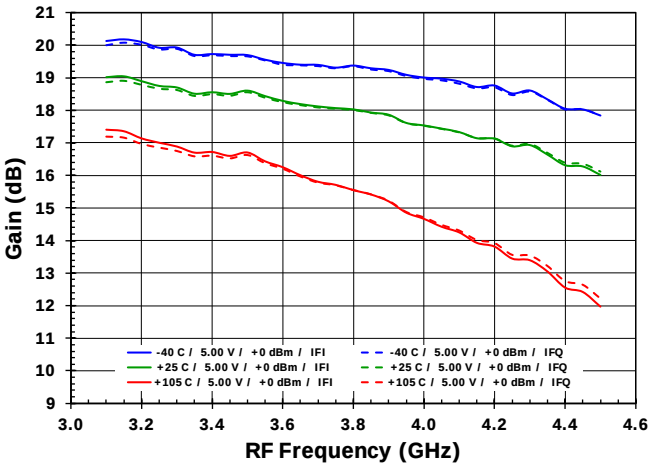
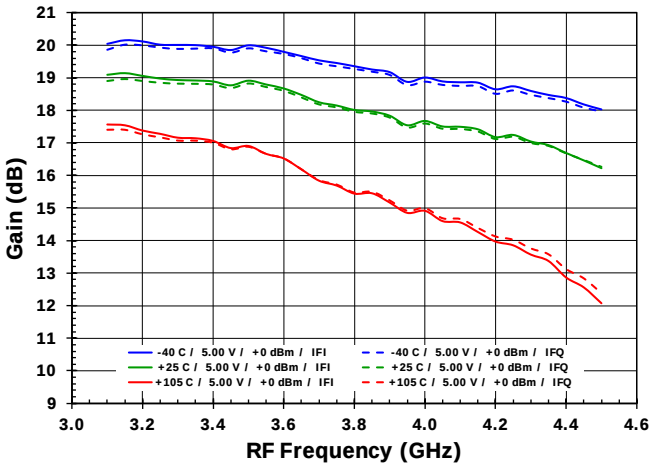


Figure 10. Gain vs. T_{case} [High Side LO, RF_Y]



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Figure 11. Gain vs. V_{cc} [High Side LO, RF_X]

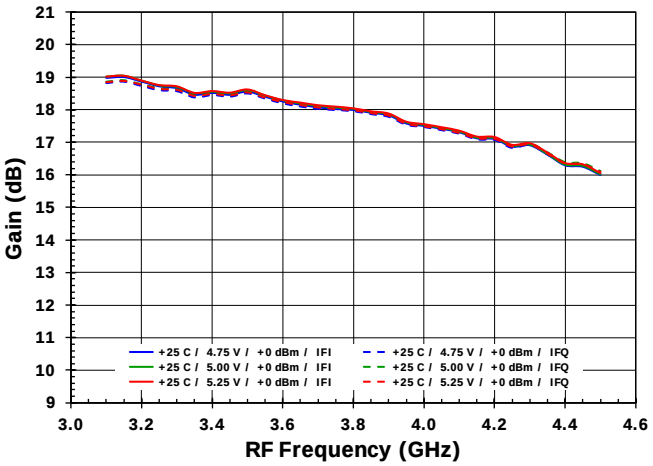


Figure 12. Gain vs. V_{cc} [High Side LO, RF_Y]

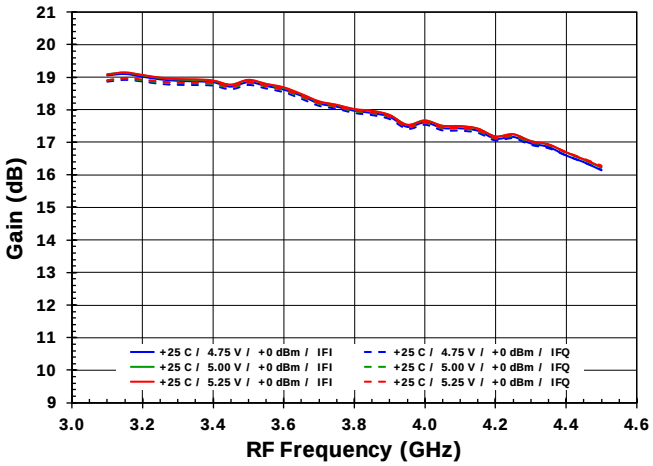


Figure 13. Gain vs. LO Power [High Side LO, RF_X]

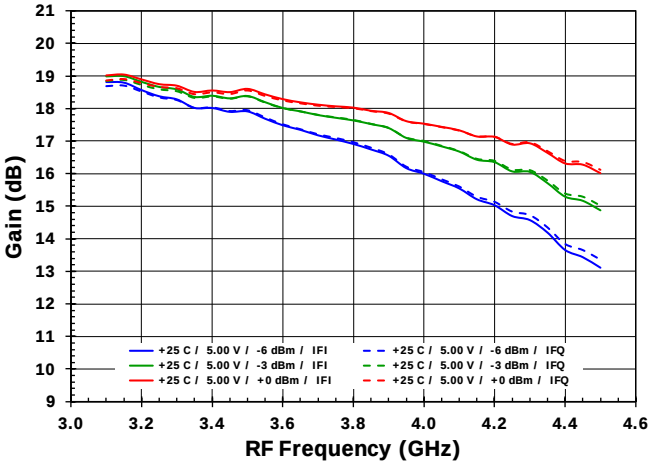


Figure 14. Gain vs. LO Power [High Side LO, RF_Y]

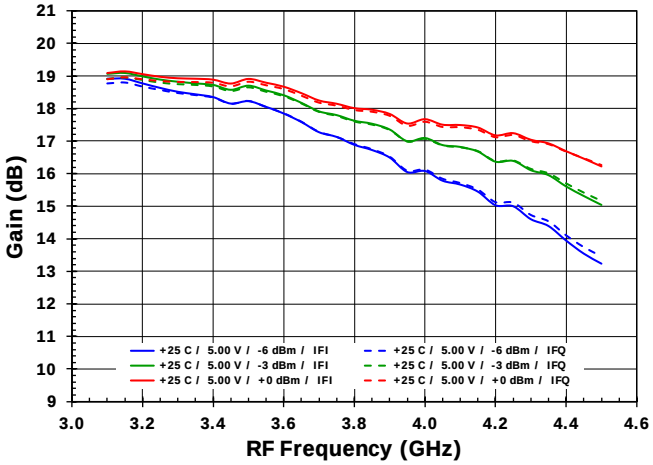


Figure 15. OIP3 vs. T_{case} [Low Side LO, RF_X]

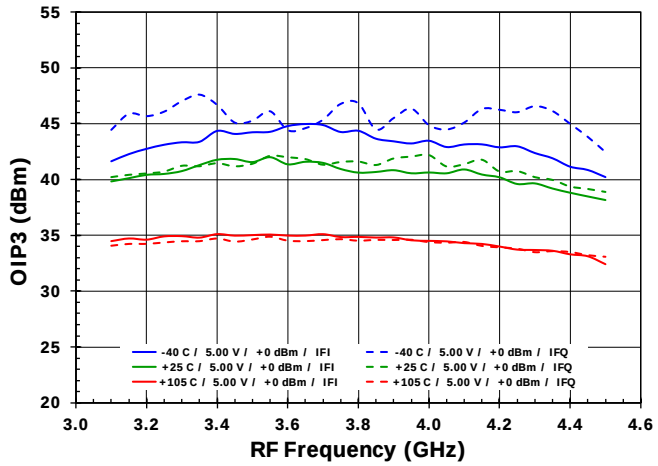


Figure 16. OIP3 vs. T_{case} [Low Side LO, RF_Y]

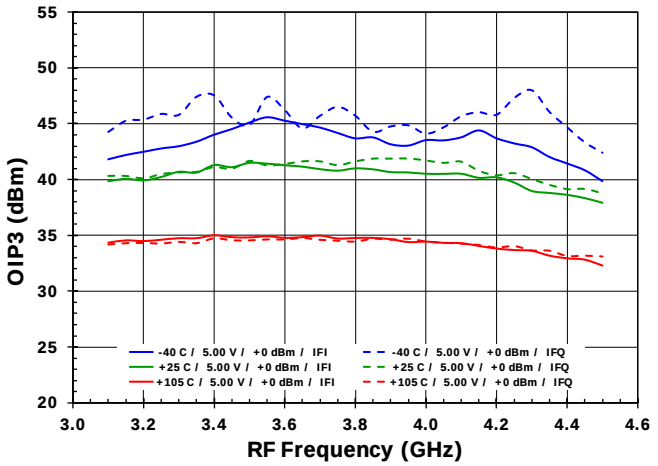


Figure 17. OIP3 vs. V_{cc} [Low Side LO, RF_X]

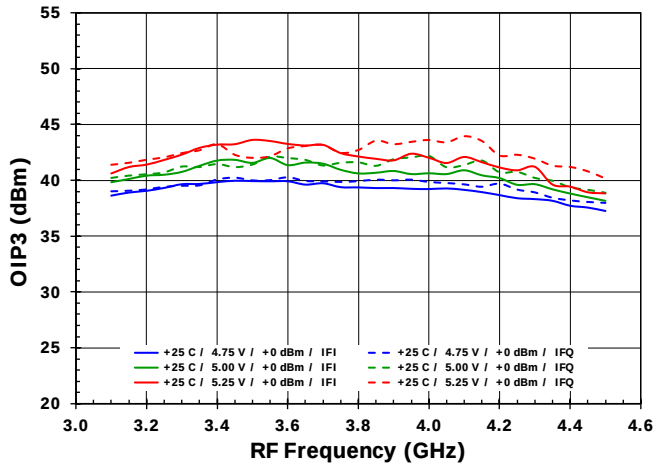


Figure 18. OIP3 vs. V_{cc} [Low Side LO, RF_Y]

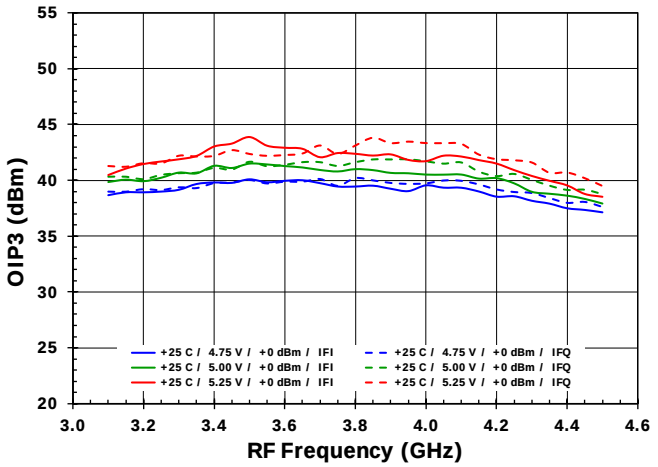


Figure 19. OIP3 vs. LO Power [Low Side LO, RF_X]

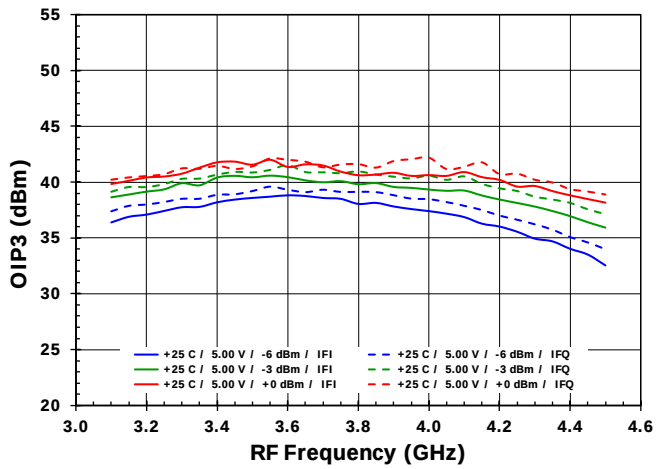
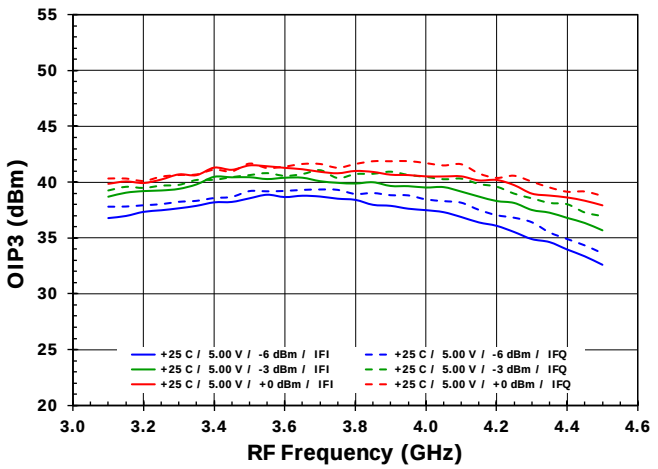


Figure 20. OIP3 vs. LO Power [Low Side LO, RF_Y]



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Figure 21. OIP3 vs. T_{case} [High Side LO, RF_X]

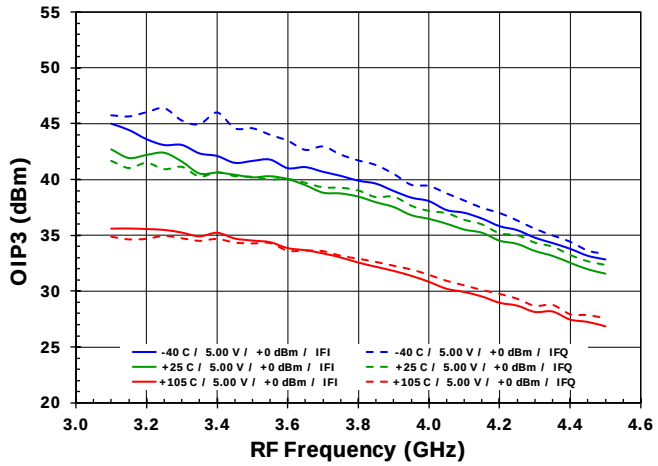


Figure 22. OIP3 vs. T_{case} [High Side LO, RF_Y]

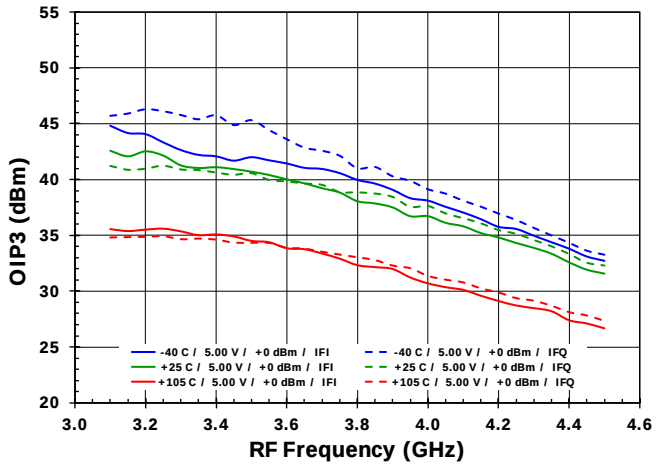


Figure 23. OIP3 vs. V_{cc} [High Side LO, RF_X]

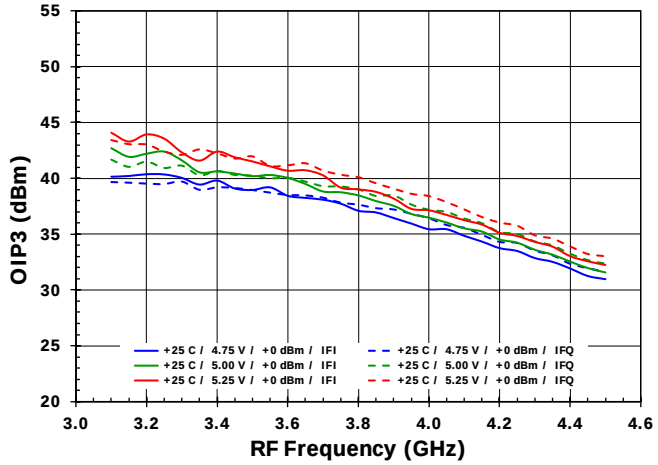


Figure 24. OIP3 vs. V_{cc} [High Side LO, RF_Y]

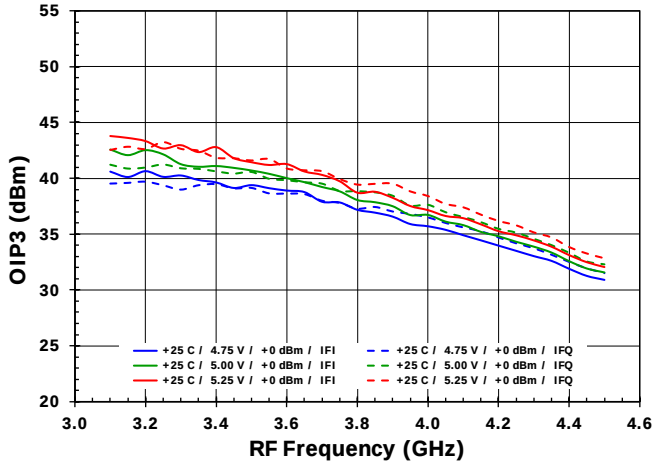


Figure 25. OIP3 vs. LO Power [High Side LO, RF_X]

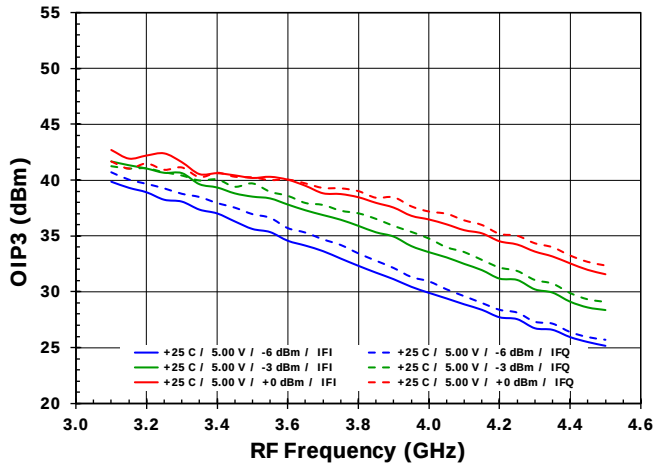
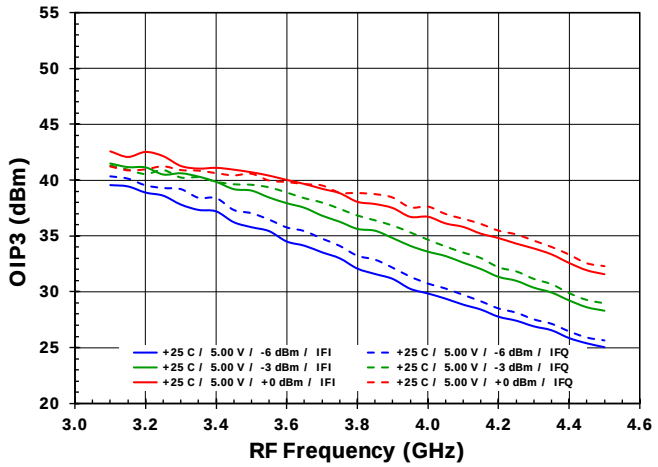


Figure 26. OIP3 vs. LO Power [High Side LO, RF_Y]



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Figure 27. OIP2 vs. T_{case} [Low Side LO, RF_X]

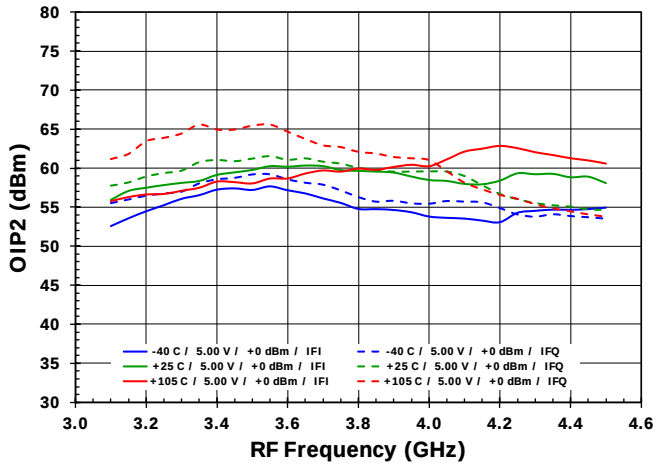


Figure 28. OIP2 vs. T_{case} [Low Side LO, RF_Y]

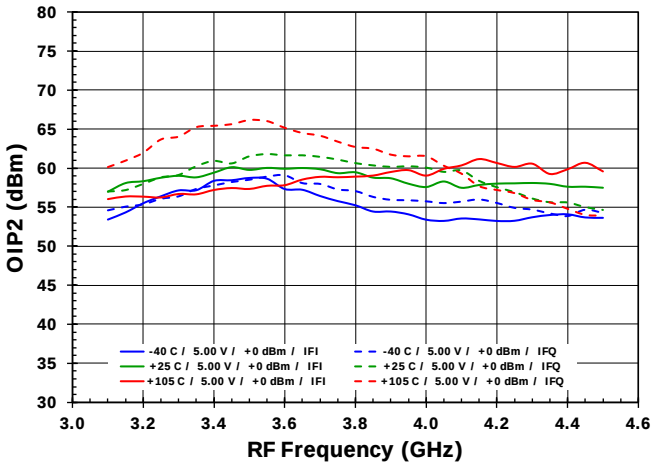


Figure 29. OIP2 vs. V_{cc} [Low Side LO, RF_X]

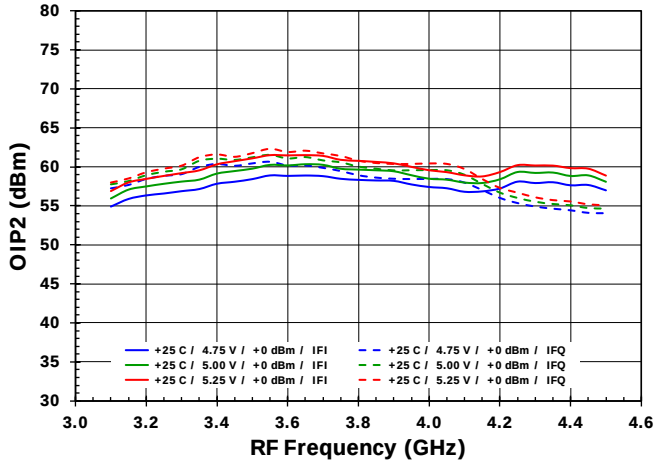


Figure 30. OIP2 vs. V_{cc} [Low Side LO, RF_Y]

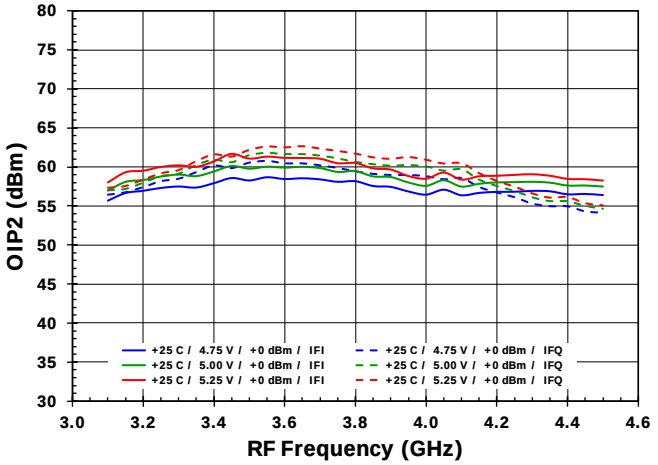


Figure 31. OIP2 vs. LO Power [Low Side LO, RF_X]

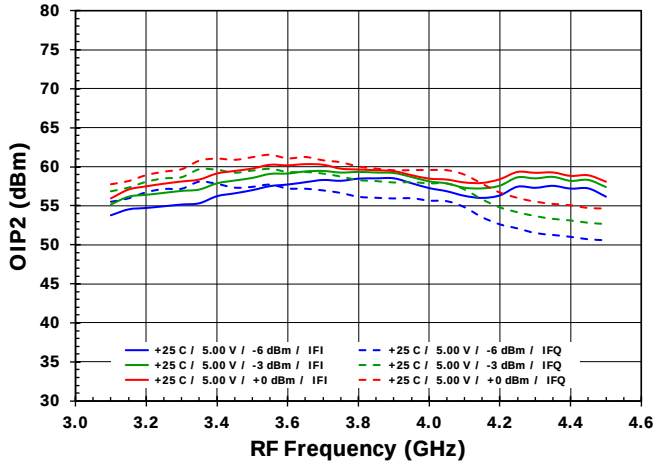


Figure 32. OIP2 vs. LO Power [Low Side LO, RF_Y]

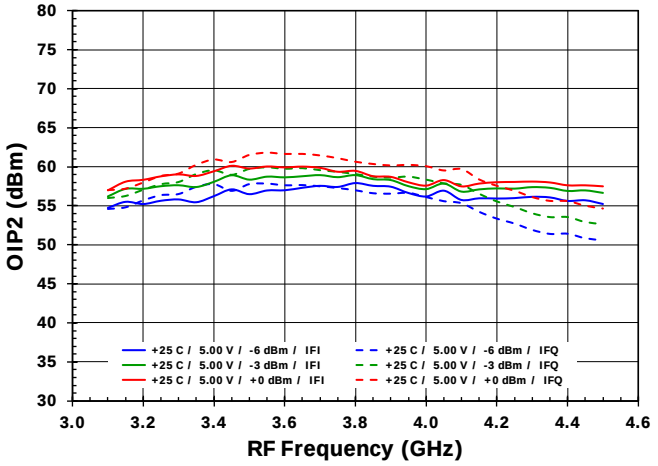


Figure 33. OIP2 vs. T_{case} [High Side LO, RF_X]

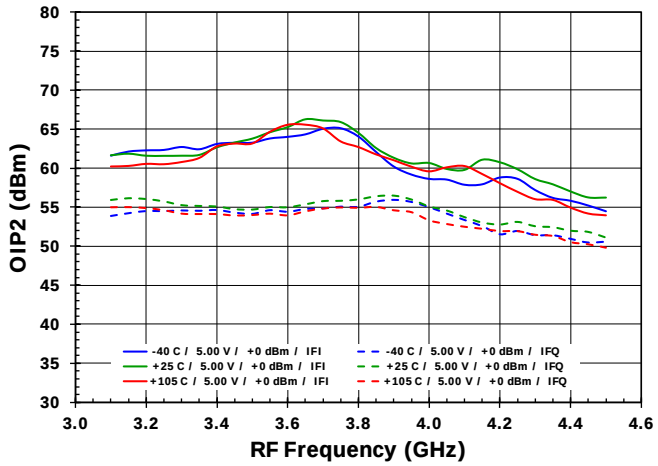


Figure 34. OIP2 vs. T_{case} [High Side LO, RF_Y]

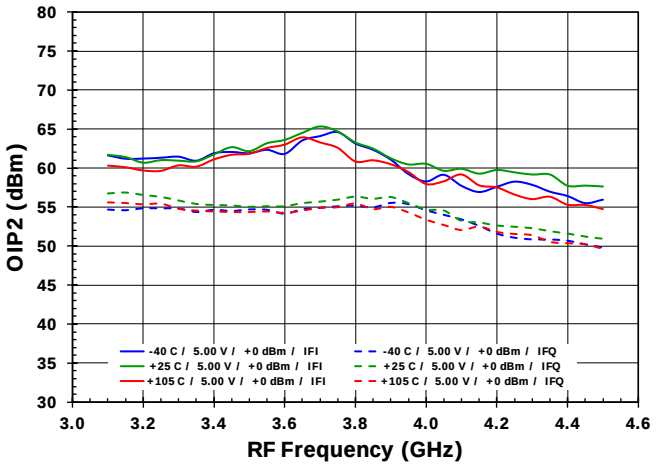


Figure 35. OIP2 vs. V_{cc} [High Side LO, RF_X]

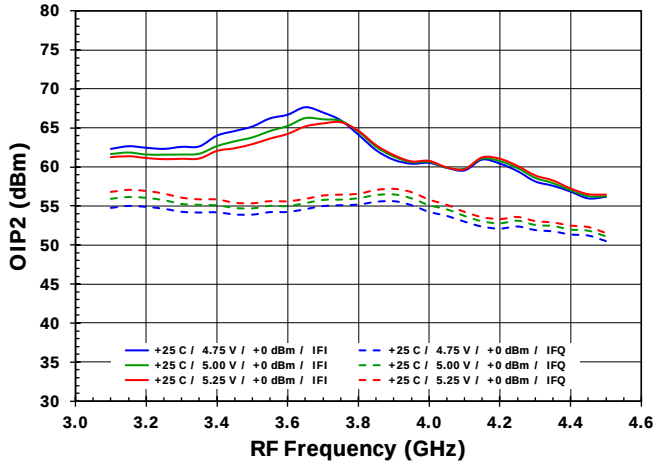


Figure 36. OIP2 vs. V_{cc} [High Side LO, RF_Y]

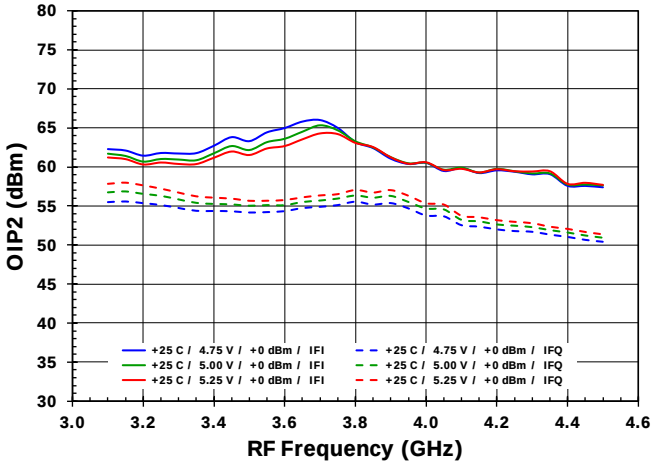


Figure 37. OIP2 vs. LO Power [High Side LO, RF_X]

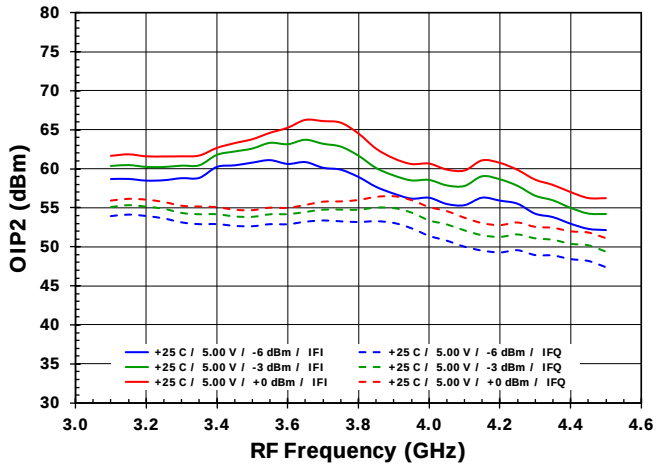
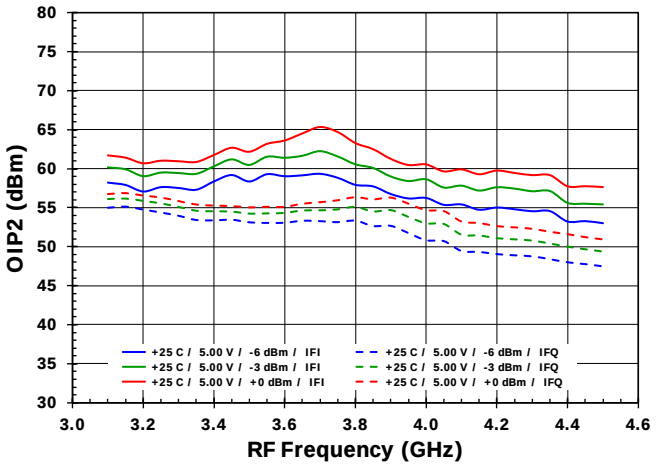


Figure 38. OIP2 vs. LO Power [High Side LO, RF_Y]



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Figure 39. OP1dB vs. T_{case} [Low Side LO, RF_X]

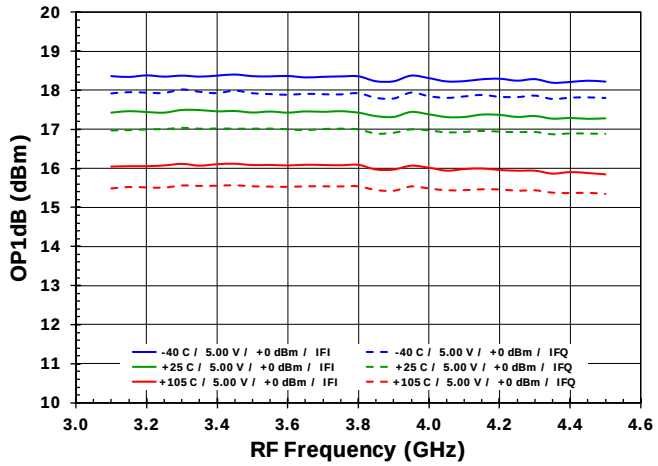


Figure 40. OP1dB vs. T_{case} [Low Side LO, RF_Y]

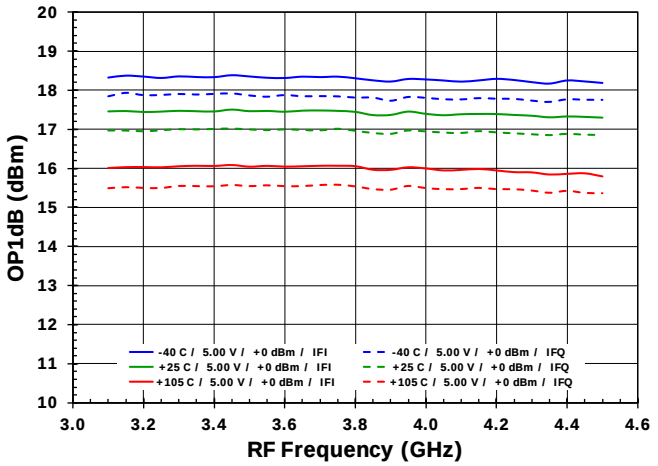


Figure 41. OP1dB vs. V_{cc} [Low Side LO, RF_X]

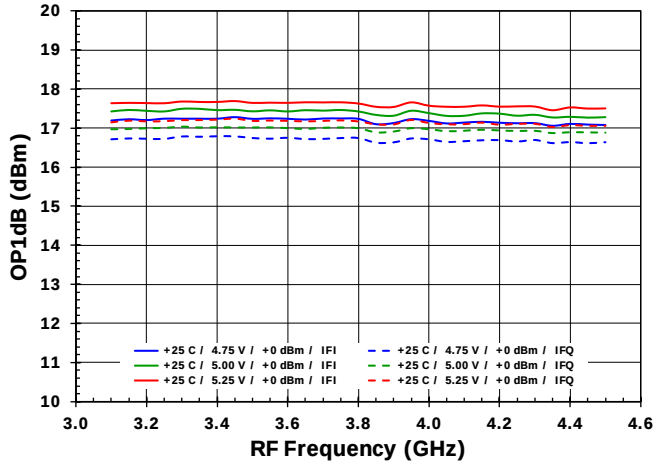


Figure 42. OP1dB vs. V_{cc} [Low Side LO, RF_Y]

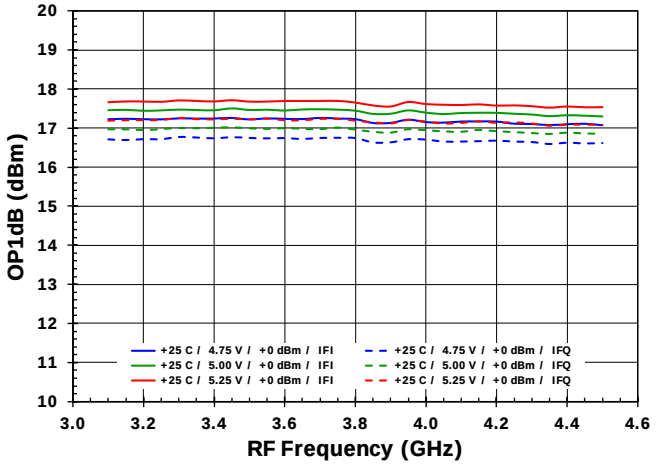


Figure 43. OP1dB vs. LO Power [Low Side LO, RF_X]

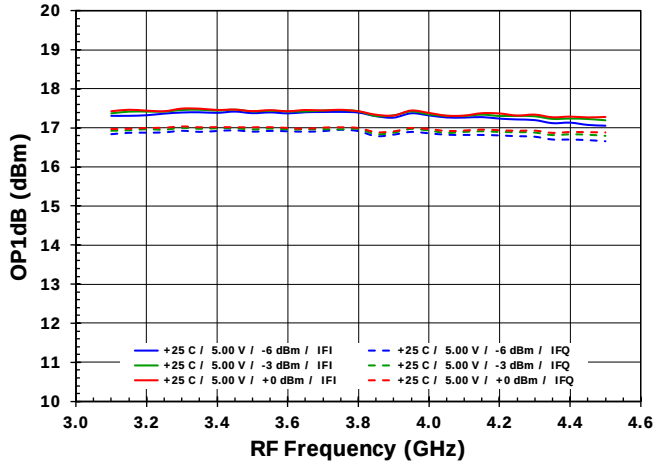
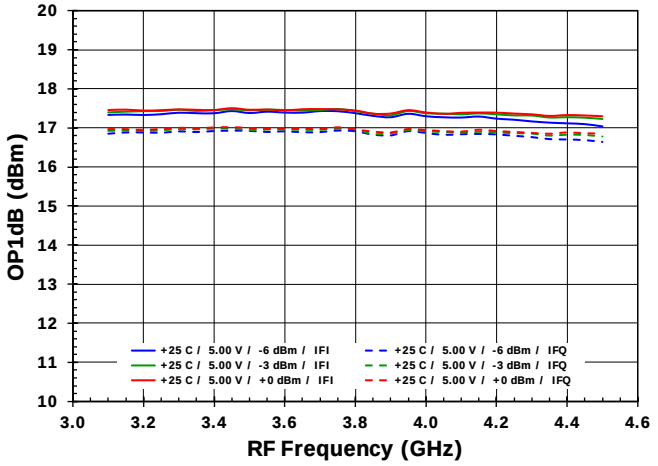


Figure 44. OP1dB vs. LO Power [Low Side LO, RF_Y]



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Figure 45. OP1dB vs. T_{case} [High Side LO, RF_X]

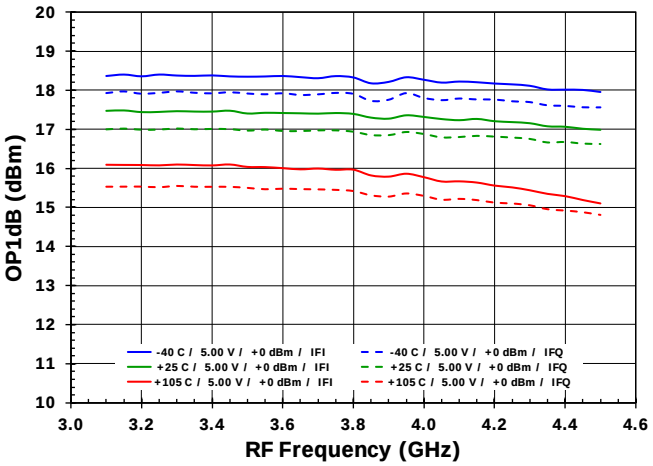


Figure 46. OP1dB vs. T_{case} [High Side LO, RF_Y]

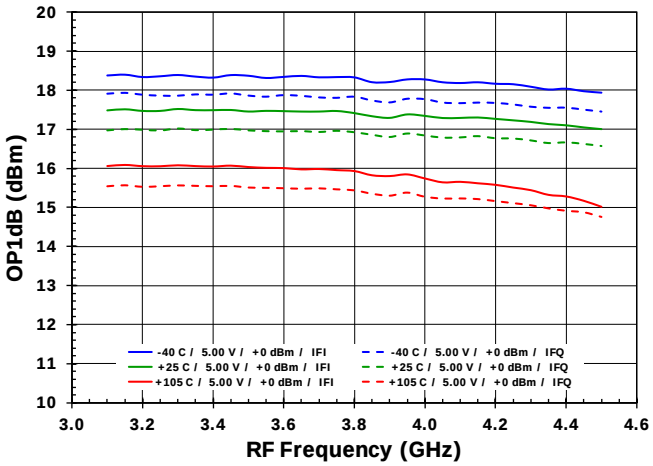


Figure 47. OP1dB vs. V_{cc} [High Side LO, RF_X]

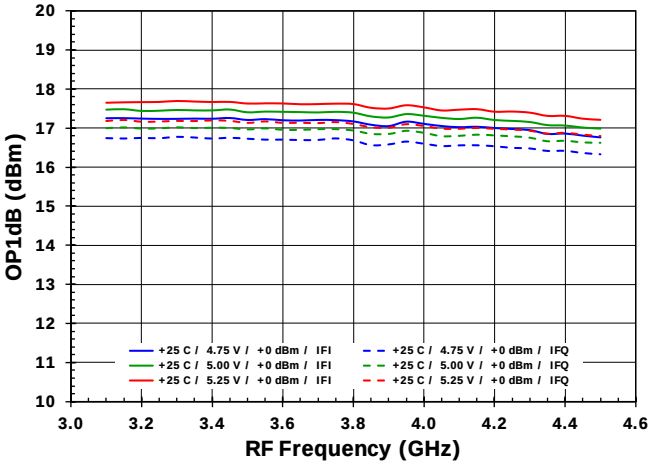


Figure 48. OP1dB vs. V_{cc} [High Side LO, RF_Y]

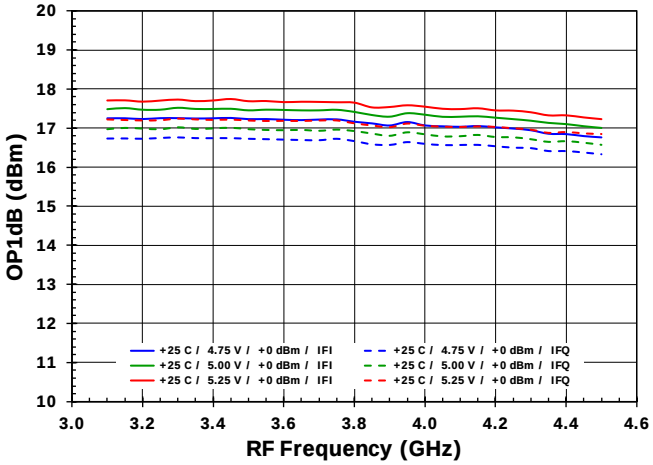


Figure 49. OP1dB vs. LO Power [High Side LO, RF_X]

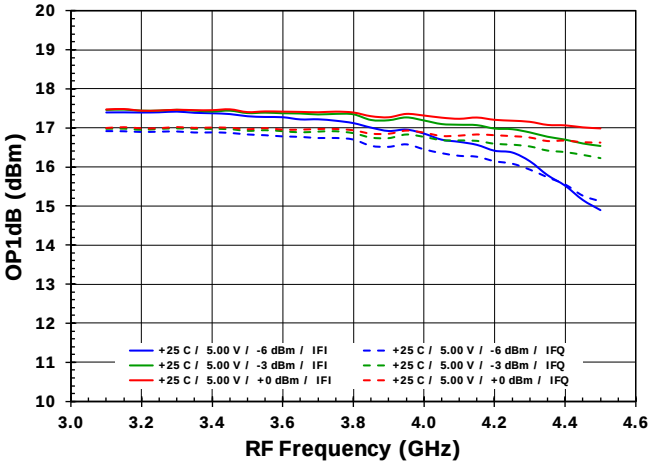
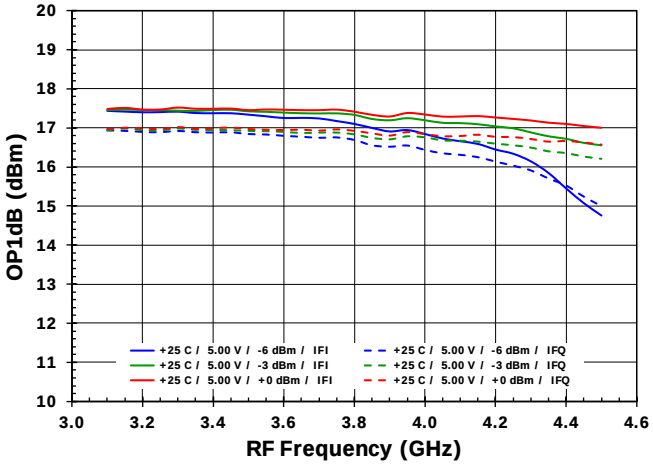


Figure 50. OP1dB vs. LO Power [High Side LO, RF_Y]



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Figure 51. 2nd Harmonic vs. T_{case} [Low Side LO, RF_X, P_{IF} = - 6 dBm]

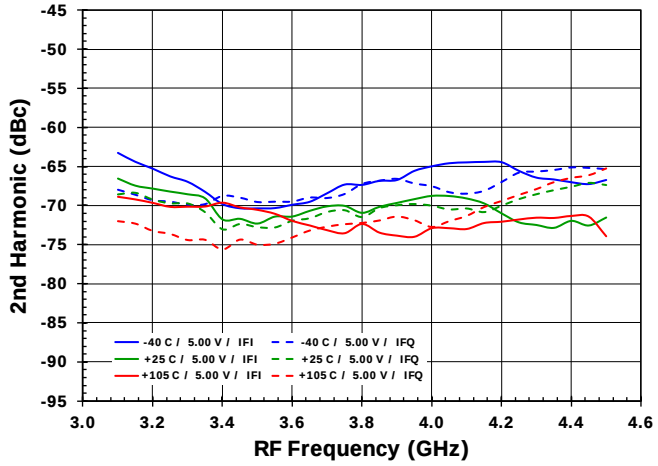


Figure 52. 2nd Harmonic vs. T_{case} [Low Side LO, RF_Y, P_{IF} = - 6 dBm]

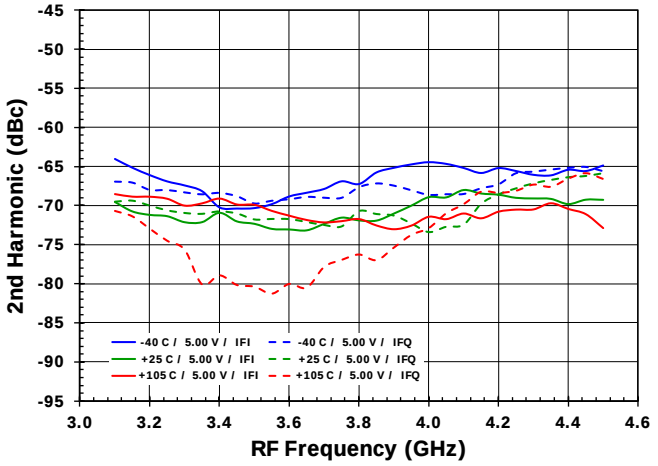


Figure 53. 2nd Harmonic vs. V_{cc} [Low Side LO, RF_X, P_{IF} = - 6 dBm]

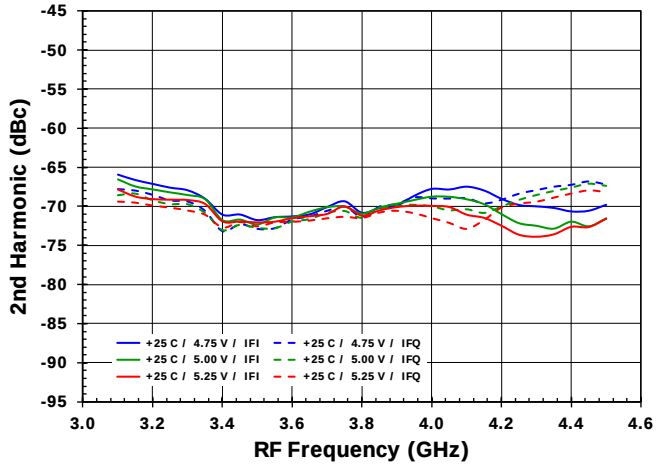


Figure 54. 2nd Harmonic vs. V_{cc} [Low Side LO, RF_Y, P_{IF} = - 6 dBm]

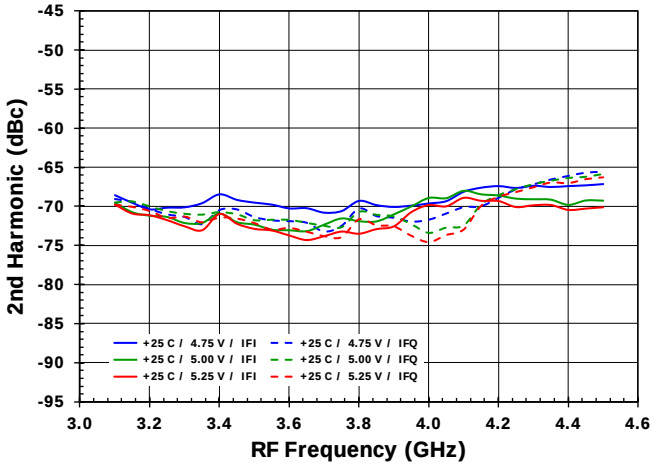


Figure 55. 2nd Harmonic vs. T_{case} [High Side LO, RF_X, P_{IF} = - 6 dBm]

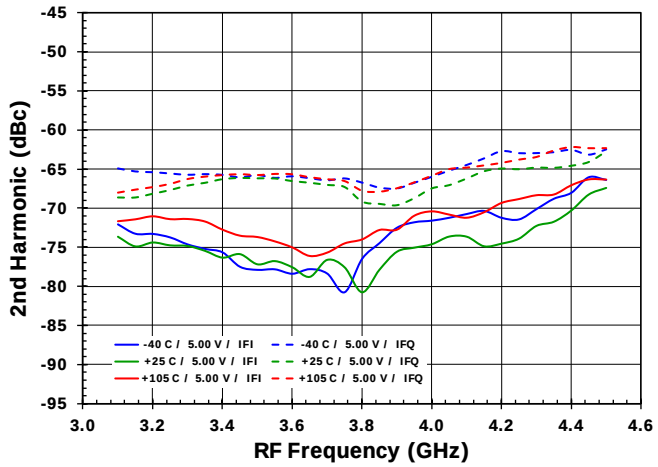


Figure 56. 2nd Harmonic vs. T_{case} [High Side LO, RF_Y, P_{IF} = - 6 dBm]

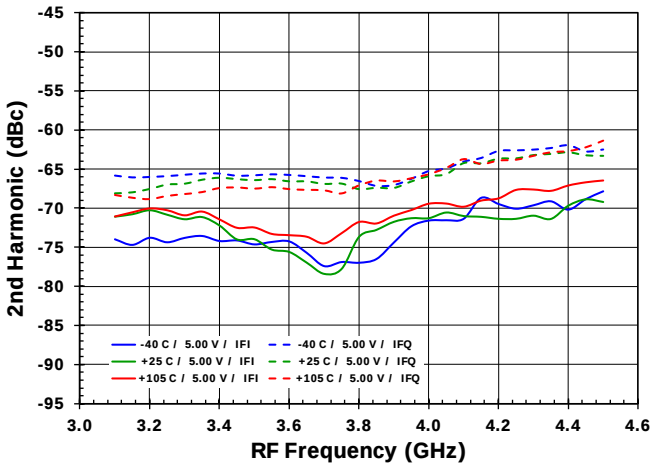


Figure 57. 2nd Harmonic vs. V_{cc} [High Side LO, RF_X, P_{IF} = - 6 dBm]

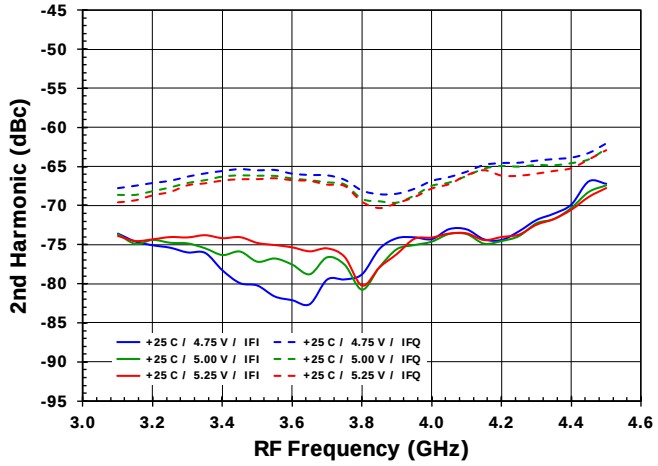


Figure 58. 2nd Harmonic vs. V_{cc} [High Side LO, RF_Y, P_{IF} = - 6 dBm]

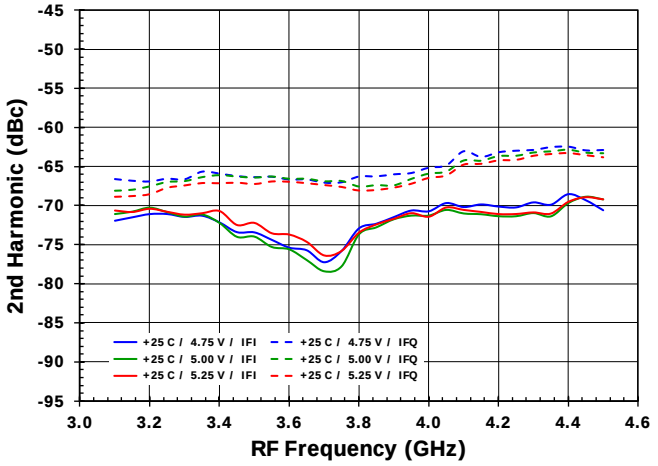


Figure 59. RF_X to IF Isolation vs. T_{case} [Low Side LO]

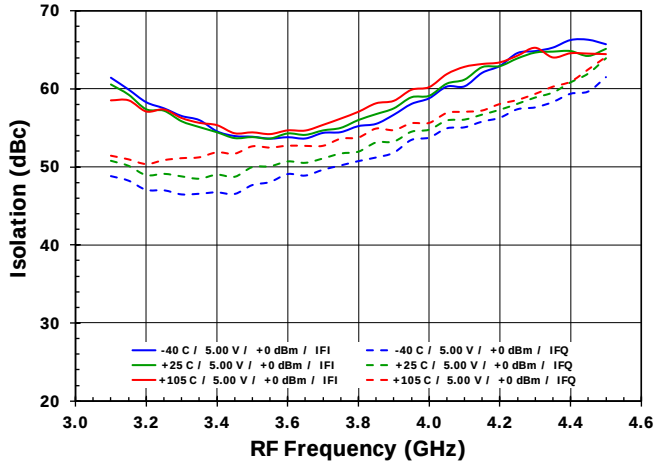


Figure 60. RF_Y to IF Isolation vs. T_{case} [Low Side LO]

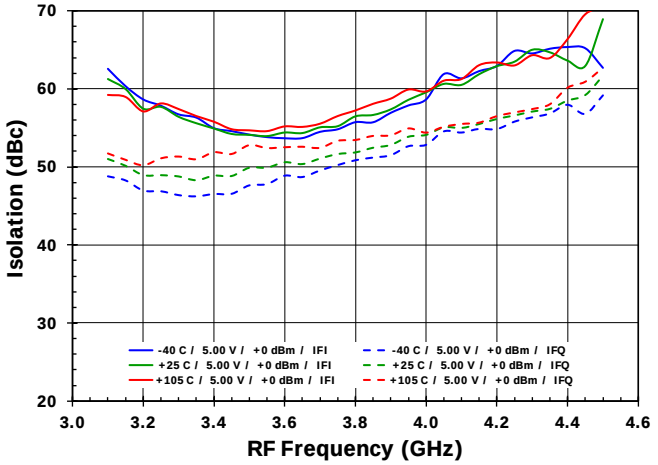


Figure 61. RF_X to IF Isolation vs. V_{cc} [Low Side LO]

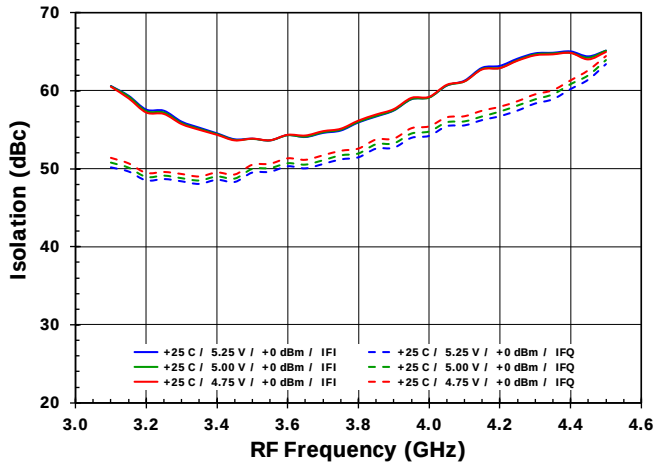
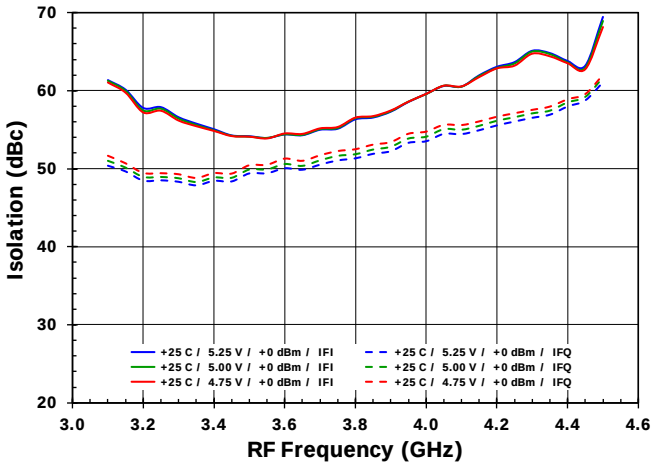


Figure 62. RF_Y to IF Isolation vs. V_{cc} [Low Side LO]



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Figure 63. RF_X to IF Isolation vs. LO Power [Low Side LO]

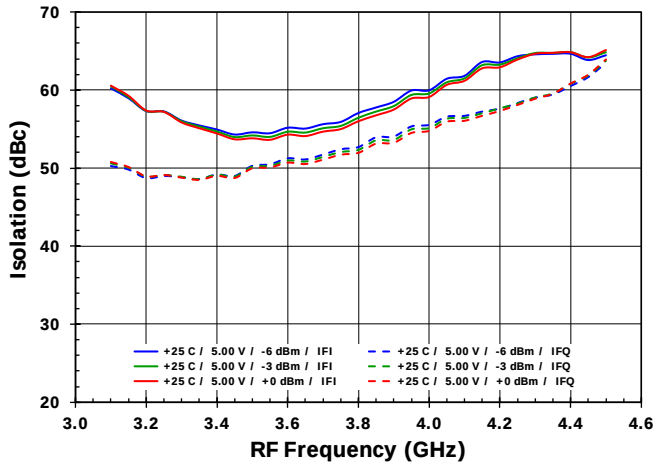


Figure 64. RF_Y to IF Isolation vs. LO Power [Low Side LO]

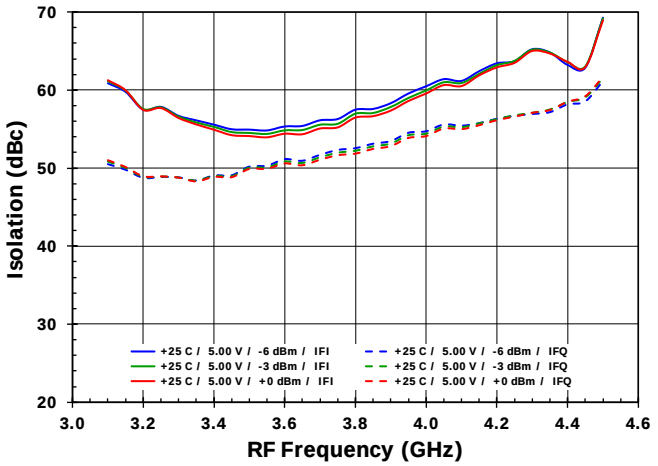


Figure 65. RF_X to IF Isolation vs. T_{case} [High Side LO]

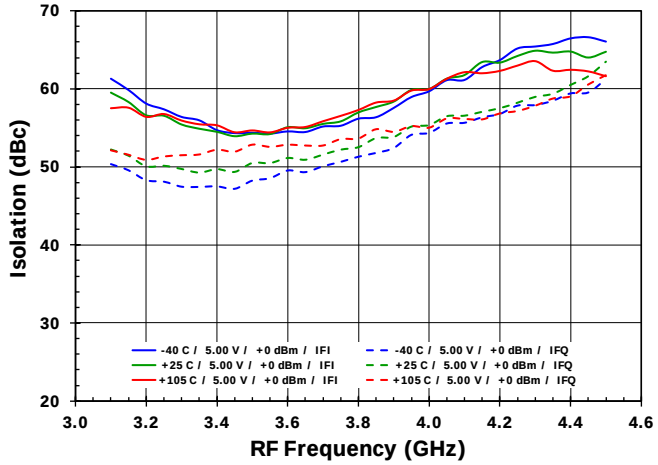


Figure 66. RF_Y to IF Isolation vs. T_{case} [High Side LO]

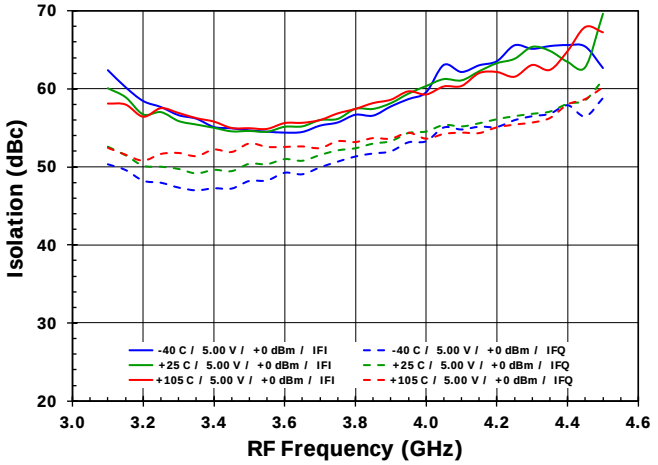


Figure 67. RF_X to IF Isolation vs. V_{cc} [High Side LO]

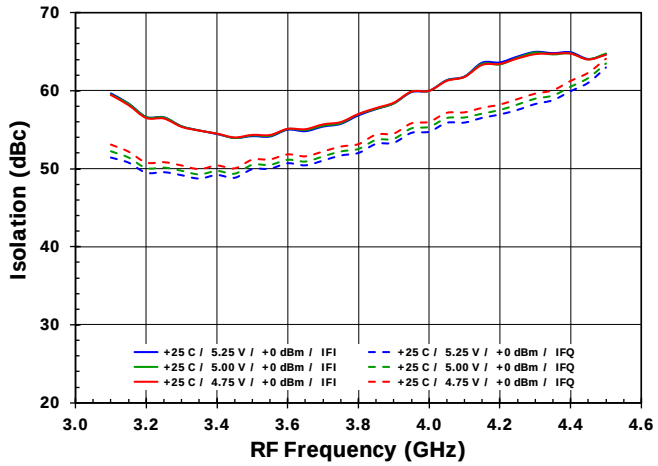
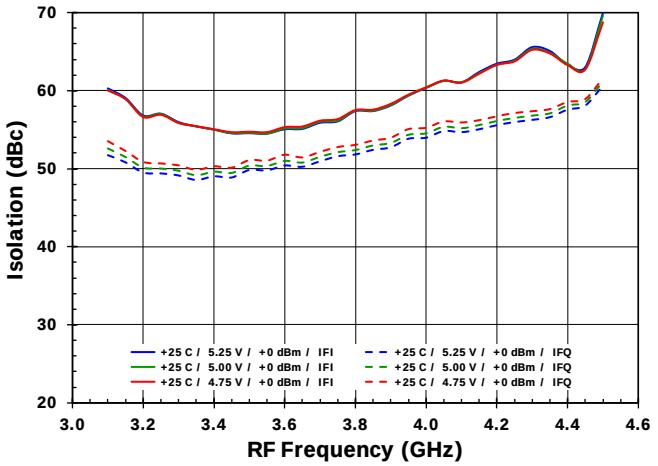


Figure 68. RF_Y to IF Isolation vs. V_{cc} [High Side LO]



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Figure 69. RF_X to IF Isolation vs. LO Power [High Side LO]

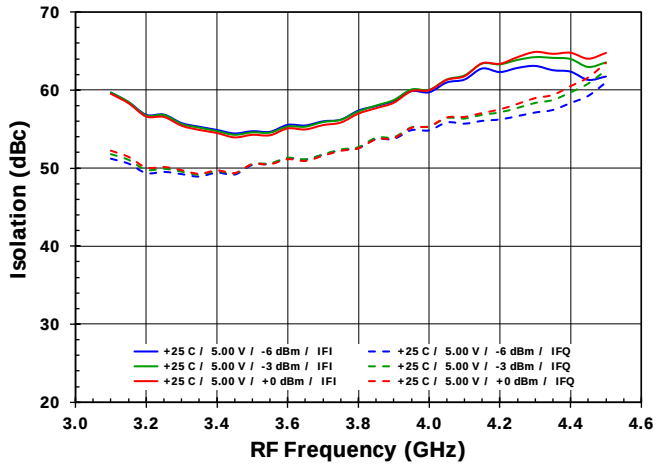


Figure 70. RF_Y to IF Isolation vs. LO Power [High Side LO]

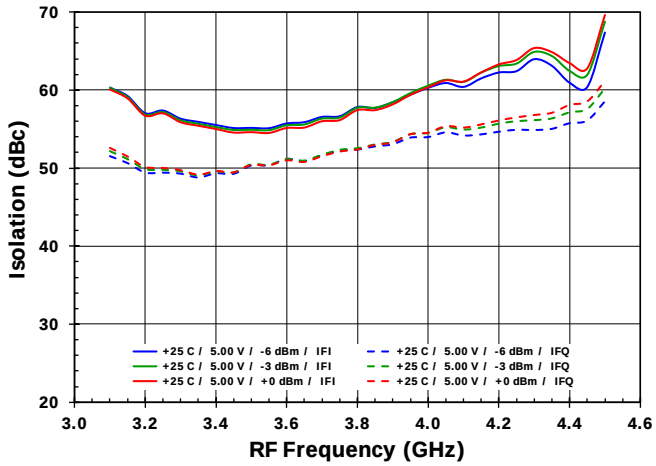


Figure 71. LO to IF Leakage vs. T_{case} [Low Side LO]

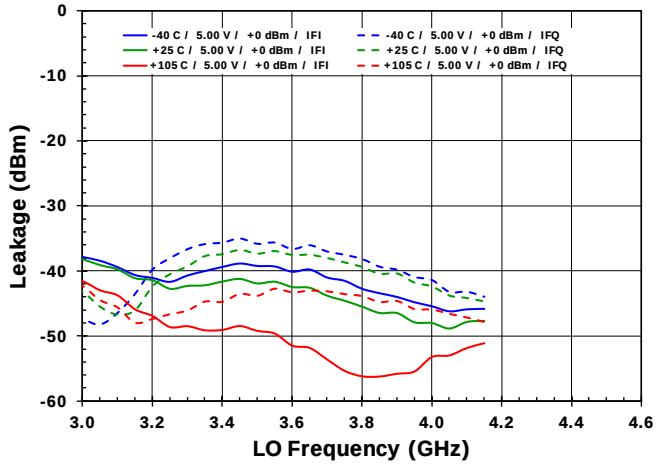


Figure 72. LO to IF Leakage vs. T_{case} [High Side LO]

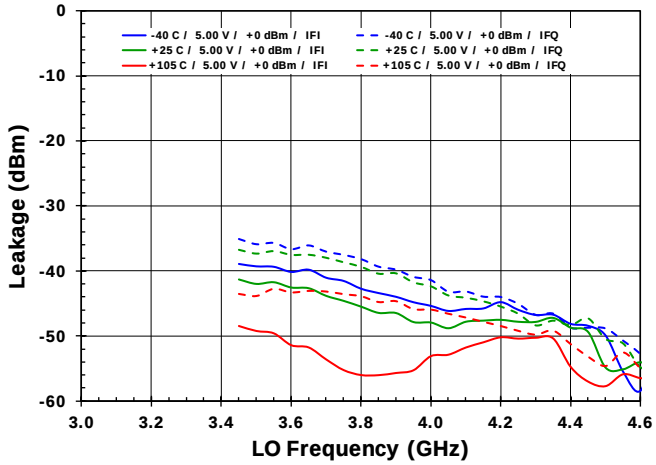


Figure 73. LO to IF Leakage vs. V_{cc} [Low Side LO]

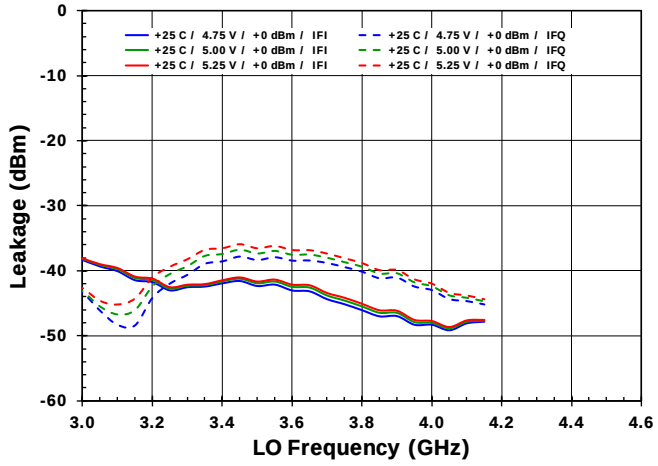
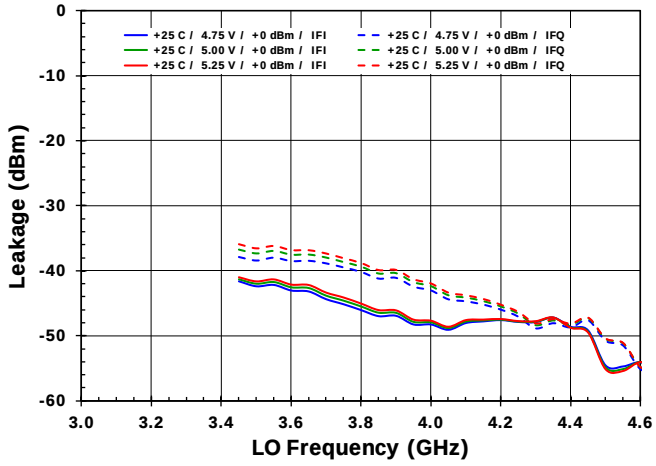


Figure 74. LO to IF Leakage vs. V_{cc} [High Side LO]



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Figure 75. LO to IF Leakage vs. LO Power [Low Side LO]

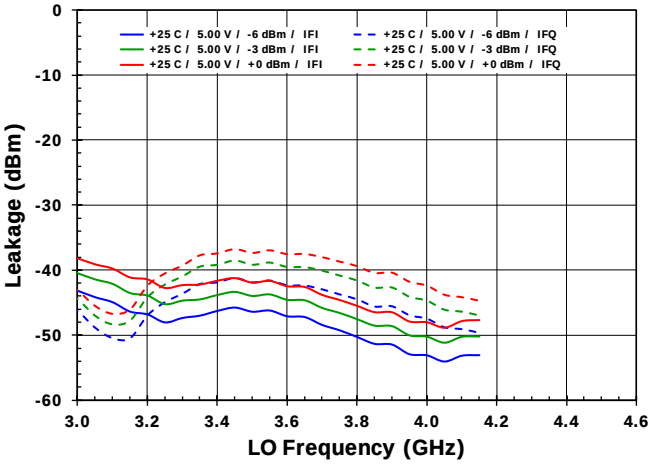


Figure 76. LO to IF Leakage vs. LO Power [High Side LO]

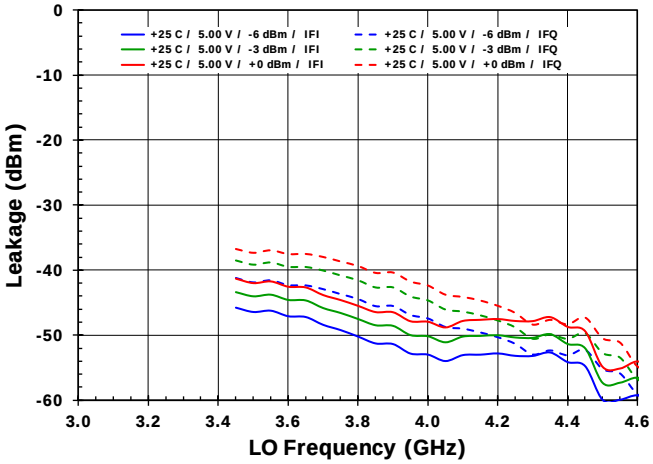


Figure 77. Current vs. T_{case} [Low Side LO, RF_X]

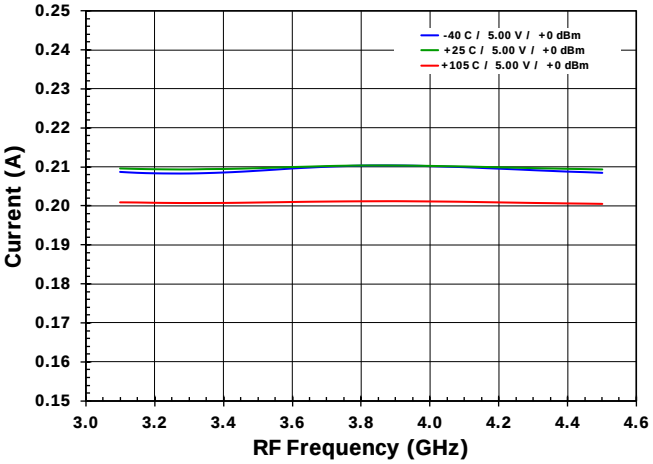


Figure 78. Current vs. T_{case} [Low Side LO, RF_Y]

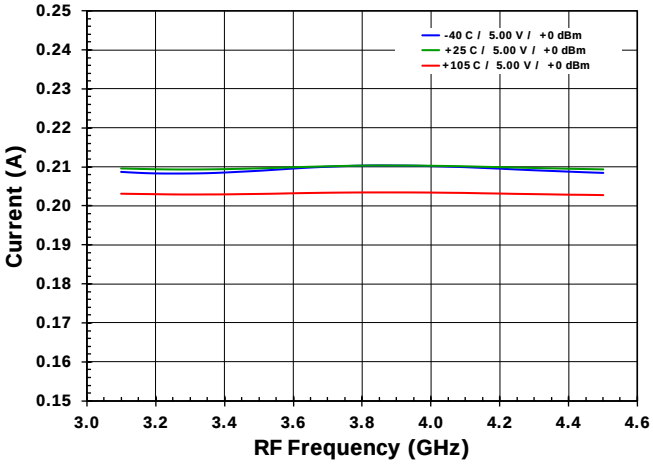


Figure 79. Current vs. V_{cc} [Low Side LO, RF_X]

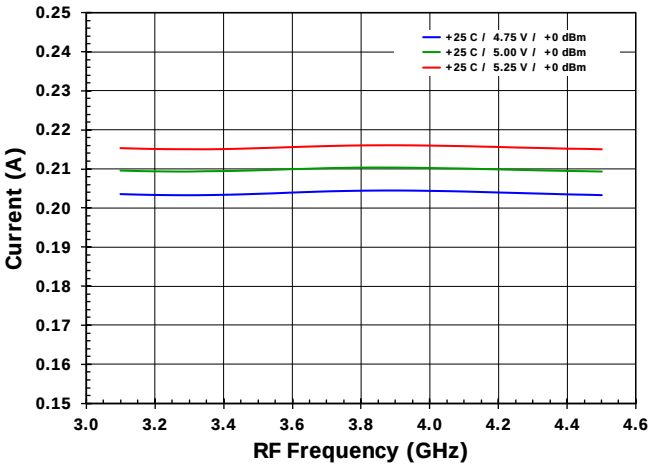
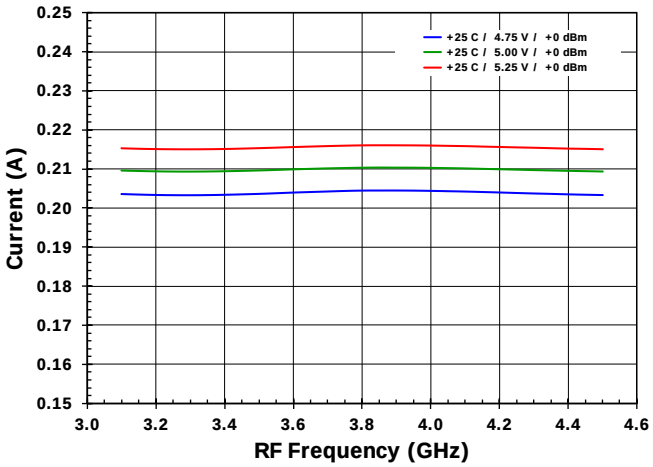


Figure 80. Current vs. V_{cc} [Low Side LO, RF_Y]



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Figure 81. Current vs. LO Power [Low Side LO, RF_X]

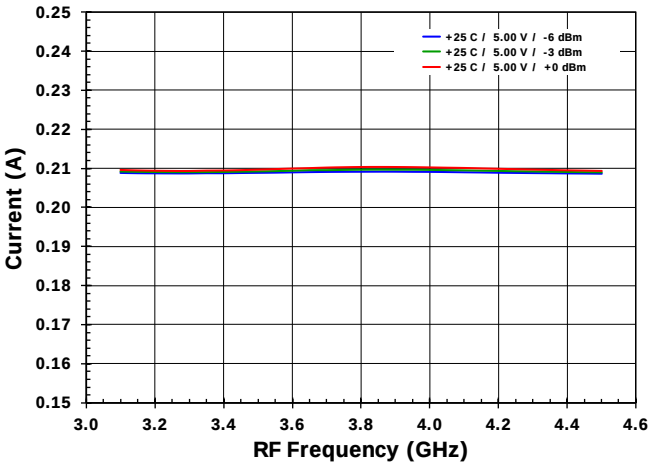


Figure 82. Current vs. LO Power [Low Side LO, RF_Y]

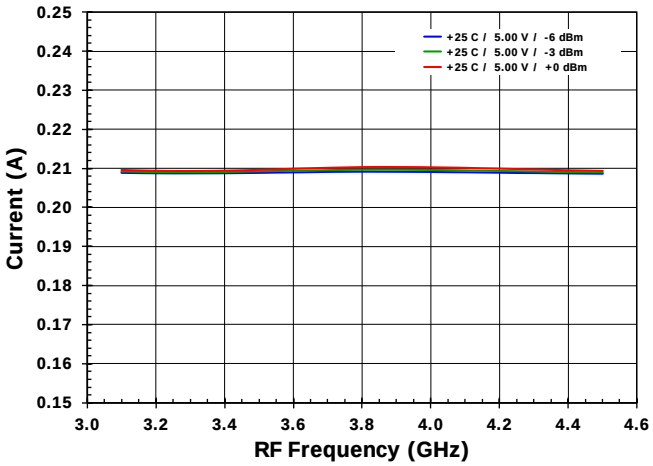


Figure 83. Current vs. T_{case} [High Side LO, RF_X]

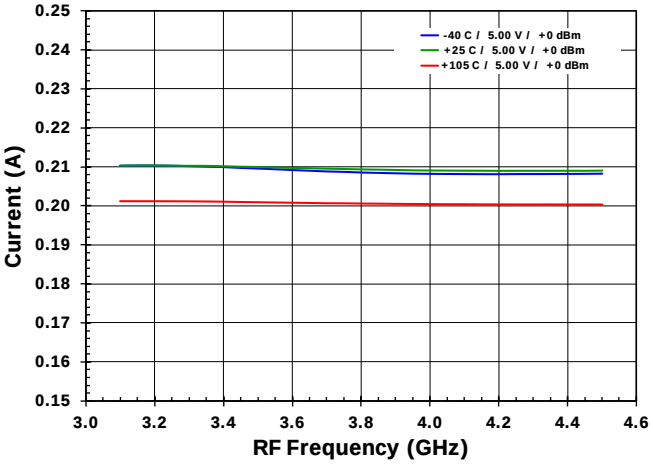


Figure 84. Current vs. T_{case} [High Side LO, RF_Y]

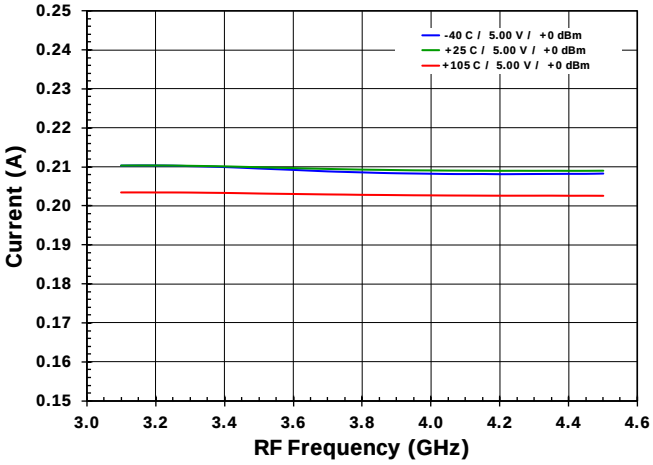


Figure 85. Current vs. V_{cc} [High Side LO, RF_X]

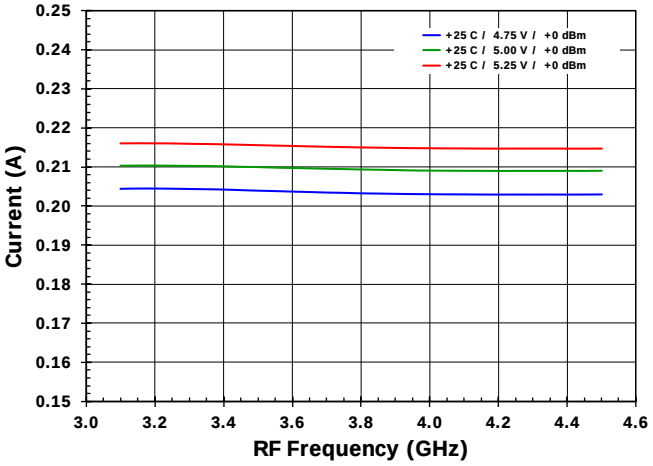


Figure 86. Current vs. V_{cc} [High Side LO, RF_Y]

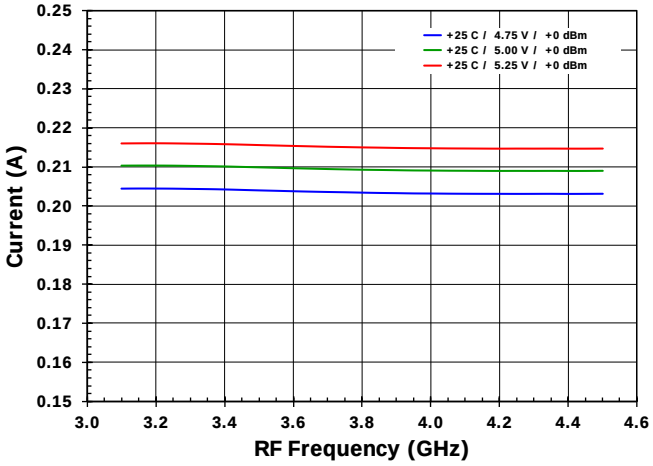


Figure 87. Current vs. LO Power [High Side LO, RF_X]

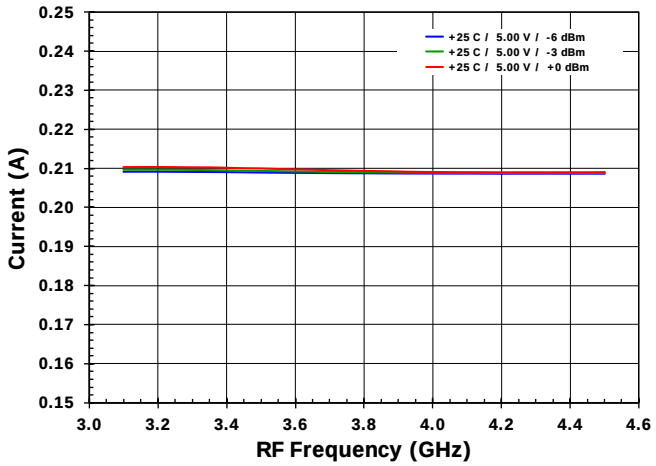


Figure 88. Current vs. LO Power [High Side LO, RF_Y]

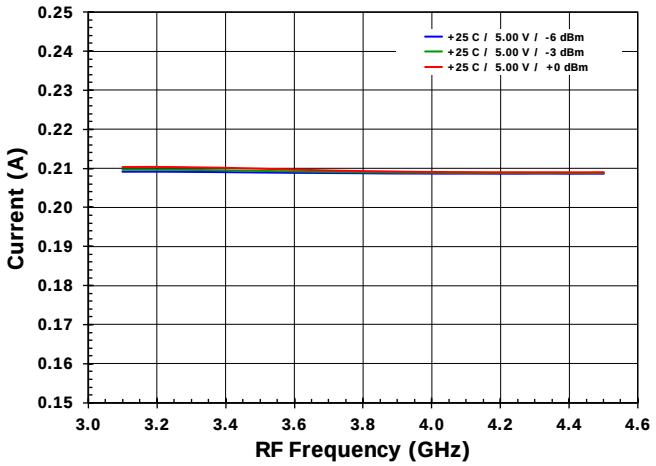


Figure 89. Gain vs. Attenuator Setting [Low Side LO, RF_X, at RF Frequency]

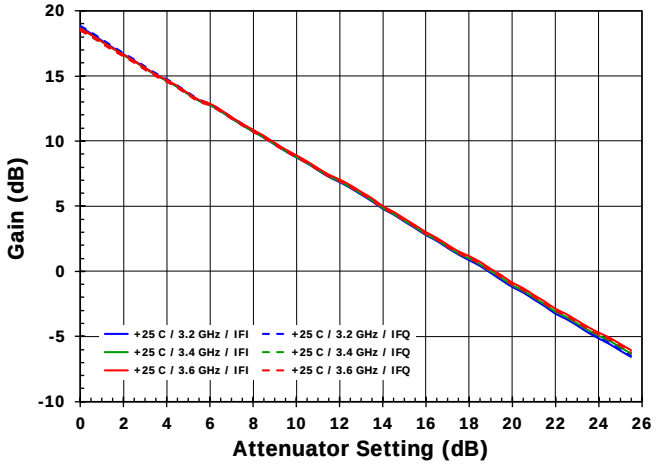


Figure 90. Gain vs. Attenuator Setting [Low Side LO, RF_Y, at RF Frequency]

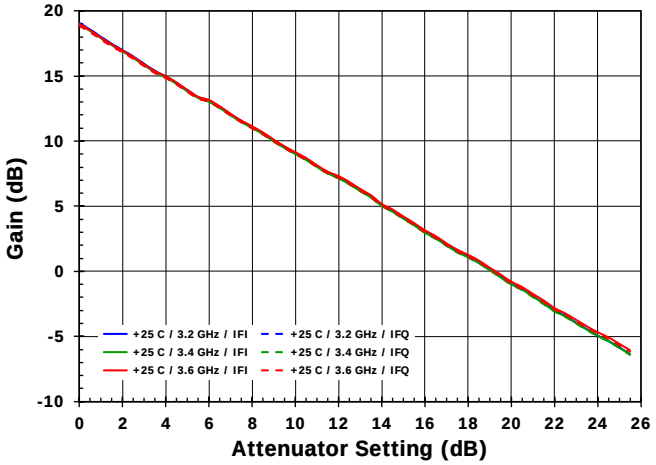


Figure 91. Gain vs. Attenuator Setting [High Side LO, RF_X, at RF Frequency]

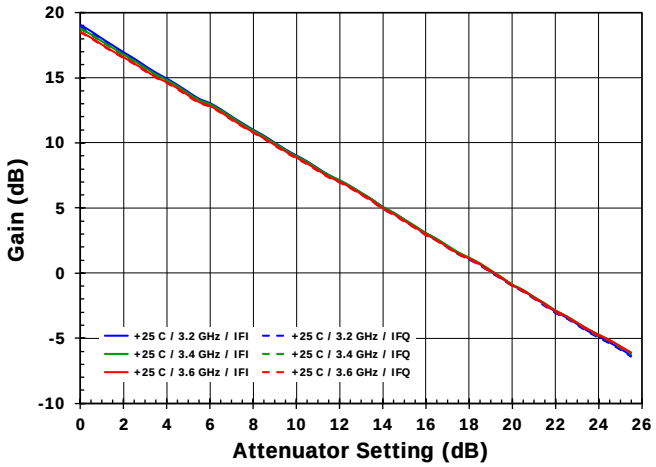
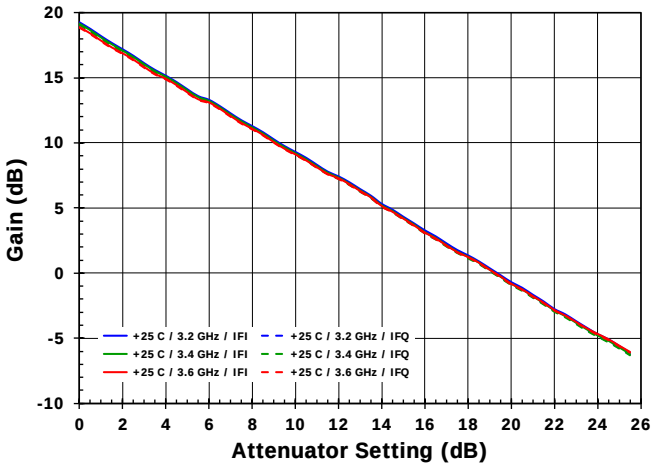


Figure 92. Gain vs. Attenuator Setting [High Side LO, RF_Y, at RF Frequency]



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Figure 93. OIP3 vs. Attenuator Setting [Low Side LO, RF_X, at RF Frequency]

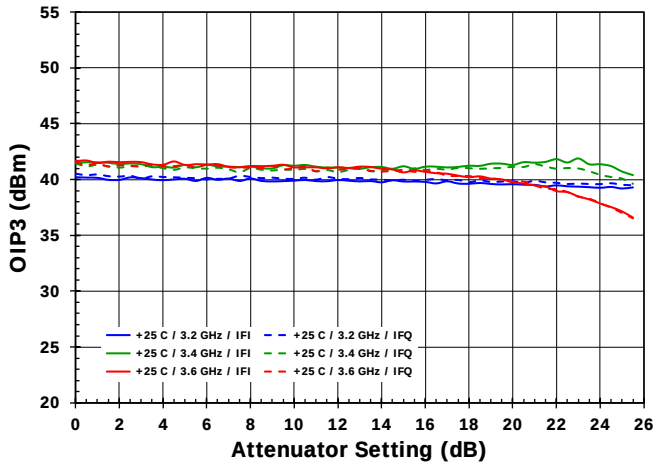


Figure 94. OIP3 vs. Attenuator Setting [Low Side LO, RF_Y, at RF Frequency]

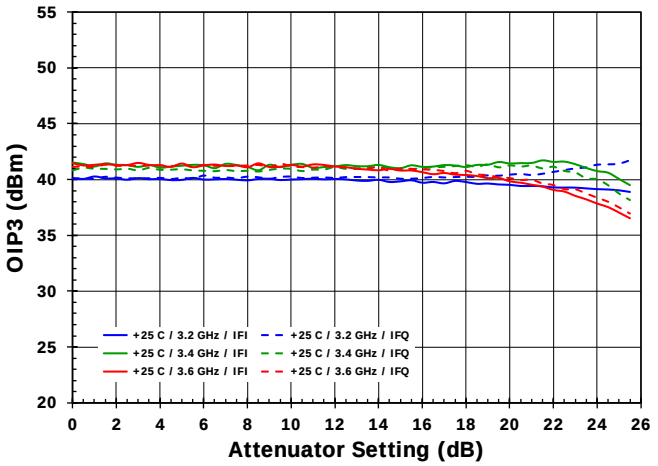


Figure 95. OIP3 vs. Attenuator Setting [High Side LO, RF_X, at RF Frequency]

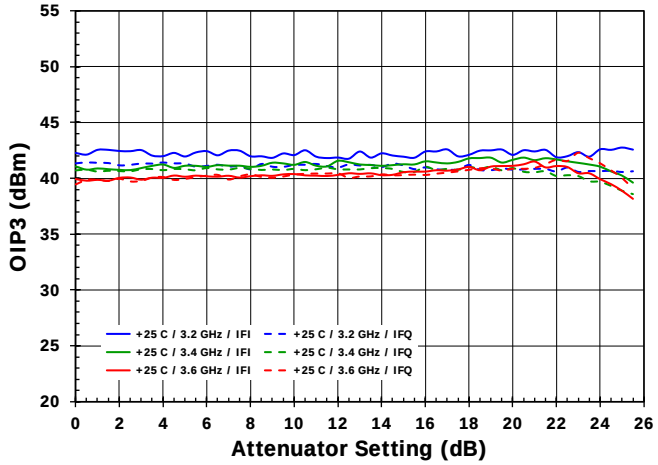


Figure 96. OIP3 vs. Attenuator Setting [High Side LO, RF_Y, at RF Frequency]

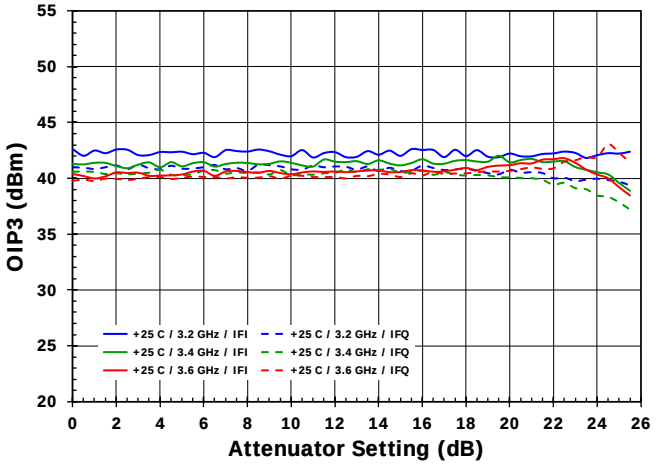


Figure 97. OIP2 vs. Attenuator Setting [Low Side LO, RF_X, at RF Frequency]

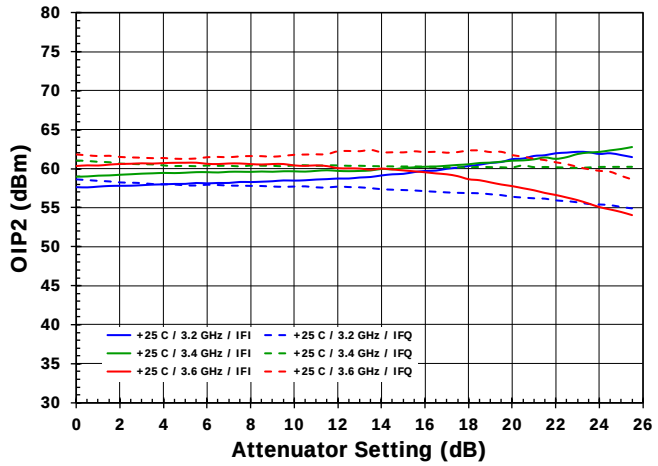


Figure 98. OIP2 vs. Attenuator Setting [Low Side LO, RF_Y, at RF Frequency]

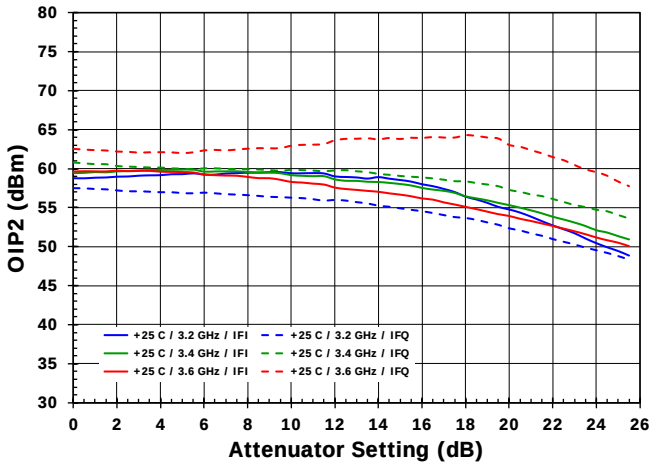


Figure 99. OIP2 vs. Attenuator Setting [High Side LO, RF_X, at RF Frequency]

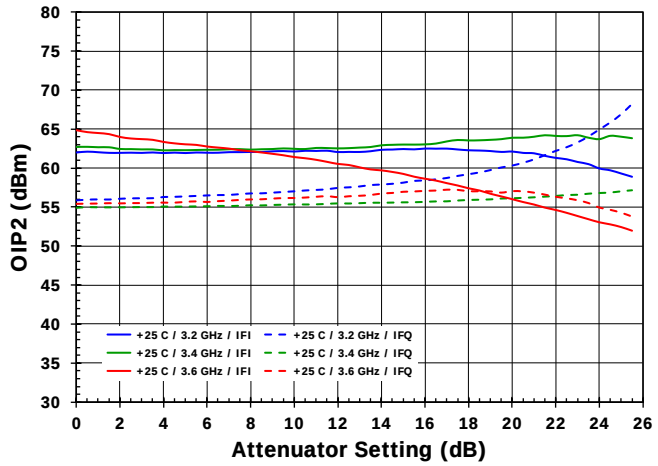


Figure 100. OIP2 vs. Attenuator Setting [High Side LO, RF_Y, at RF Frequency]

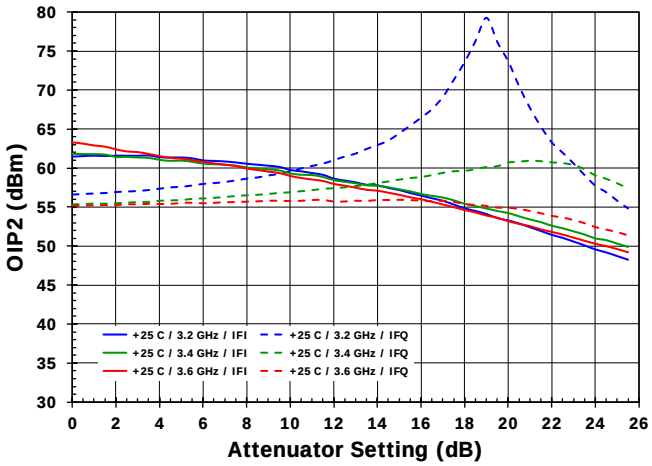


Figure 101. Amplitude Balance vs. Temp [RF_X]

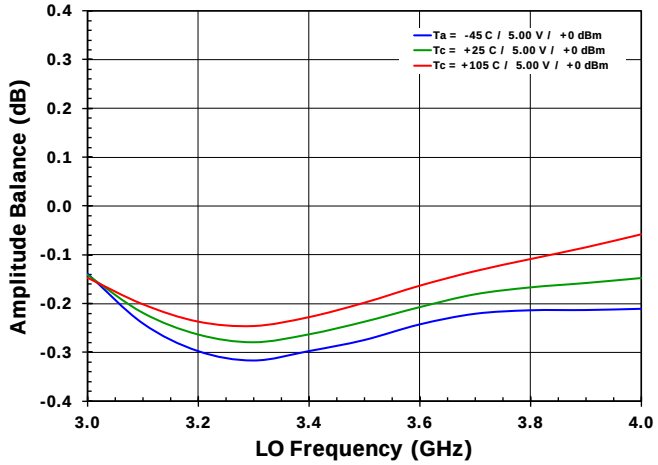


Figure 102. Phase Balance vs. Temp [RF_X]

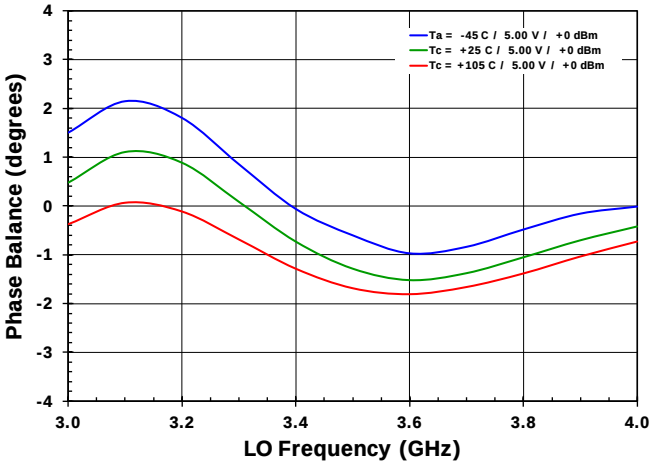


Figure 103. Amplitude Balance vs. V_{CC} [RF_X]

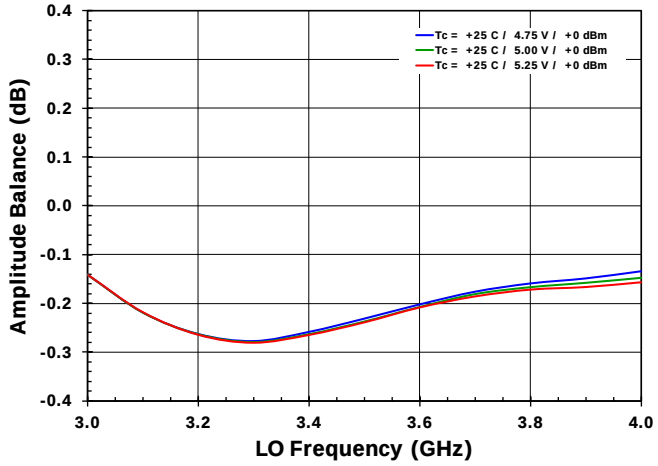


Figure 104. Phase Balance vs. V_{CC} [RF_X]

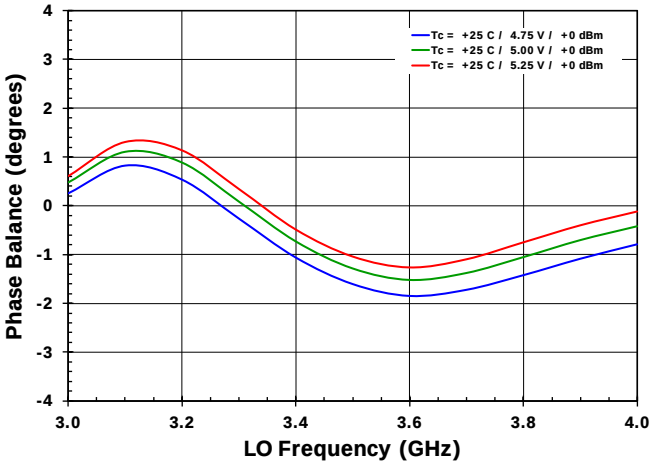


Figure 105. Amplitude Balance vs. LO Power [RFX]

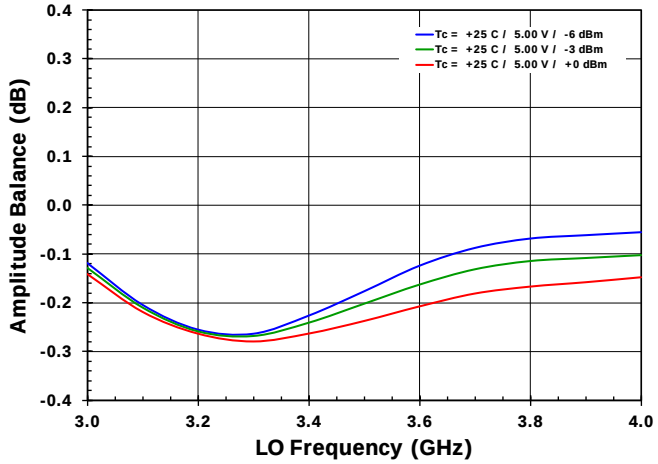


Figure 106. Phase Balance vs. LO Power [RFX]

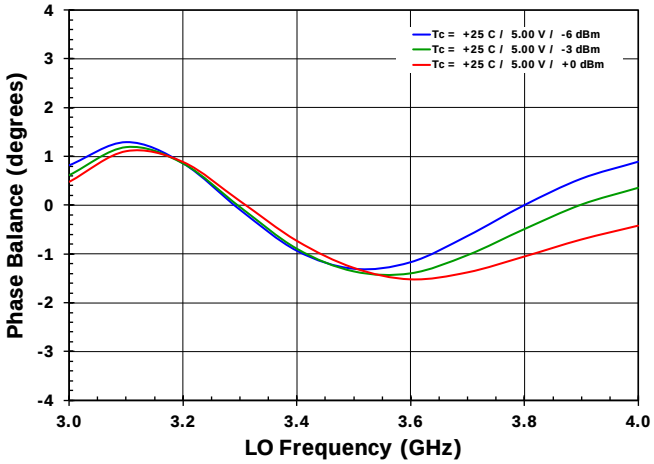


Figure 107 Image Rejection vs. Temp [RFX]

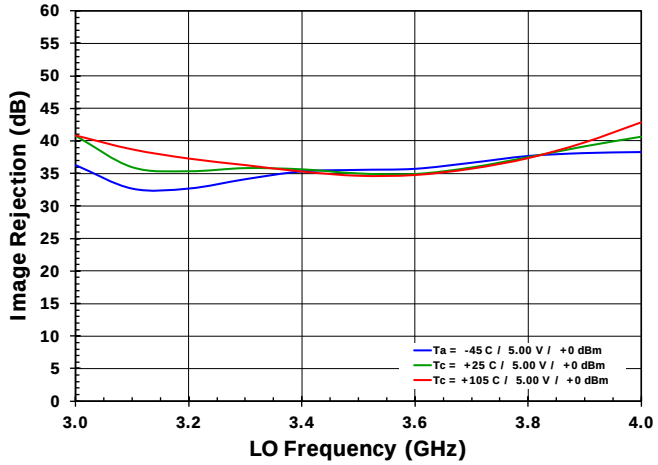


Figure 108. Noise Figure over Temperature

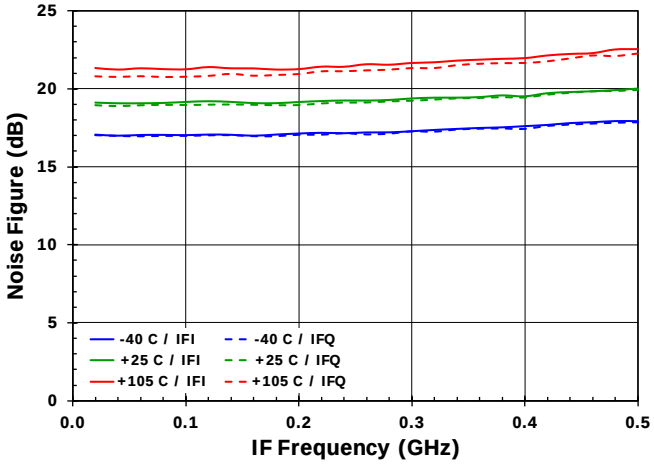


Figure 109. Image Rejection vs. Vcc [RFX]

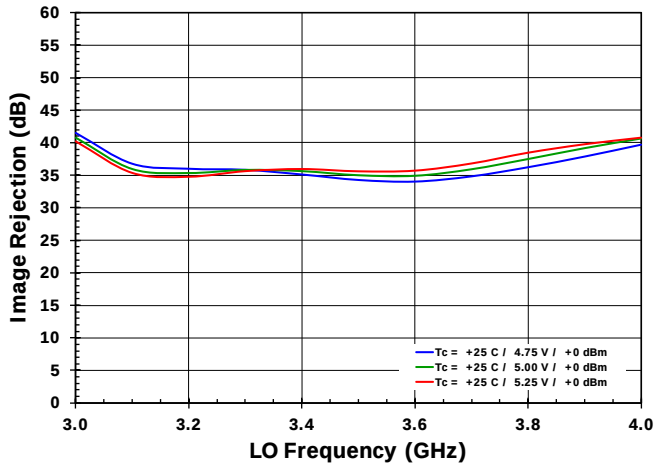


Figure 110. Image Rejection vs. LO Power [RFX]

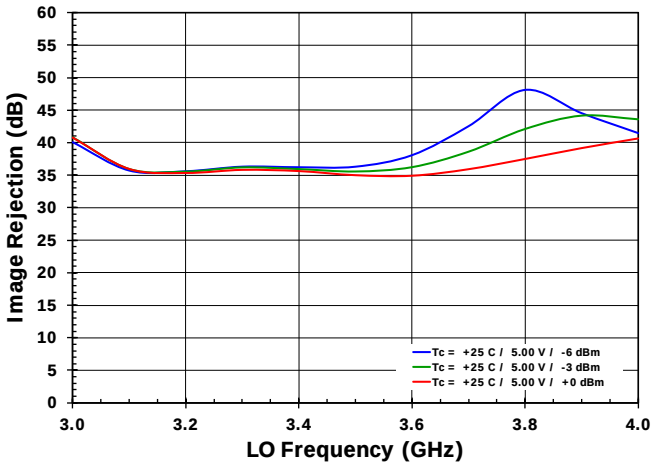


Figure 111. RF_X Match [Port Enabled]

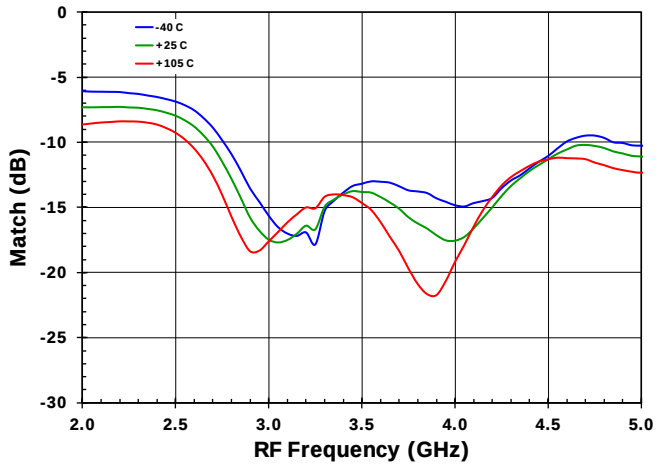


Figure 112. RF_Y Match [Port Enabled]

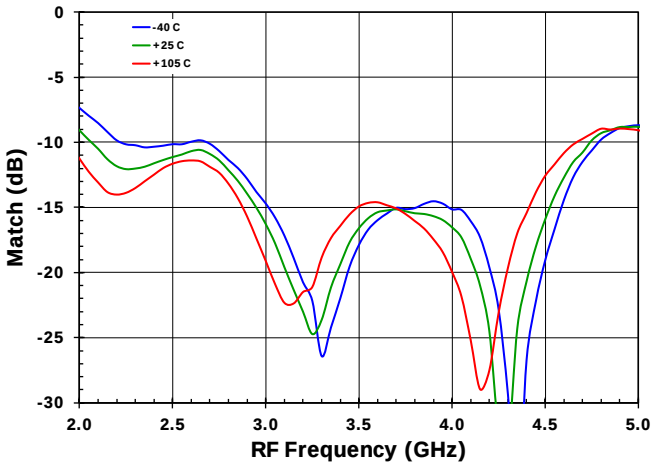


Figure 113. IFI Match

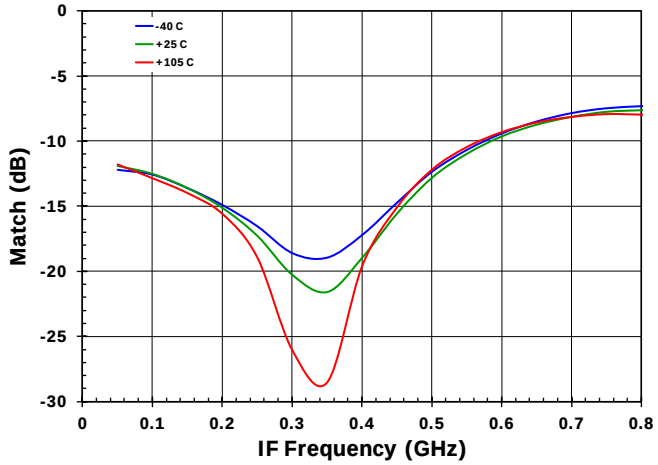


Figure 114. IFQ Match

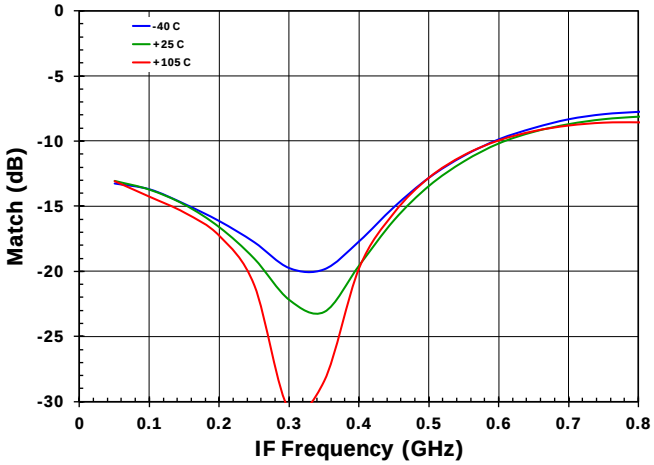


Figure 115. LO Match

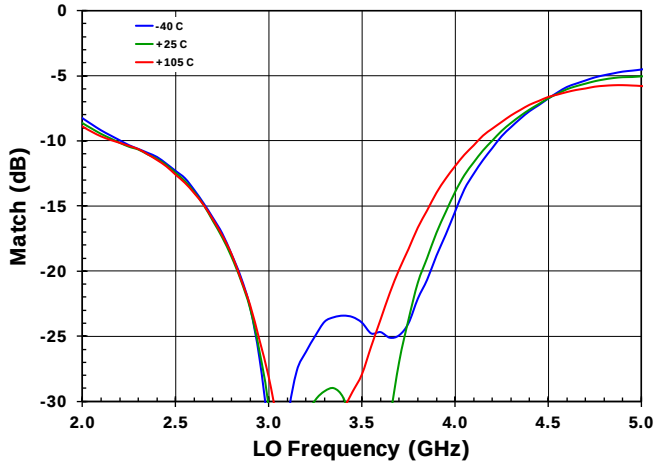
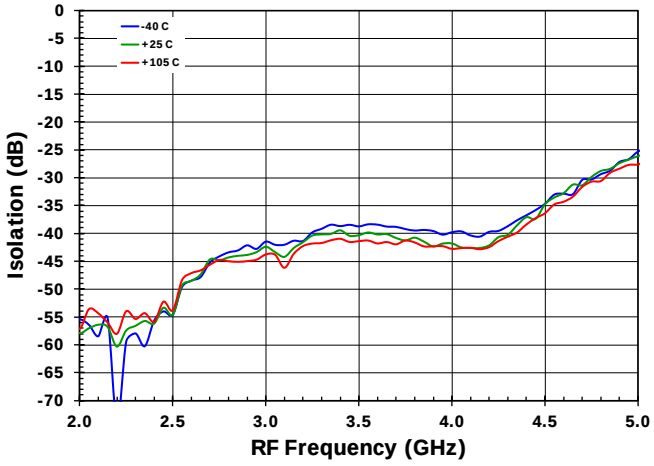


Figure 116. RF Switch Isolation



Power ON Sequence

The power-on sequence ensures F1385 works in default mode once powered on. If the F1385 is programmed after applying DC power, the following power-on sequence is not needed. Note: To use power on sequence, SW_LATCH cannot be grounded permanently.

The power-on sequence should be:

1. CSb & SW_LATCH must be set low at power-on.
2. Once powered on, first set SW_LATCH high, then set CSb high.
3. Proceed with normal programming.

The default state after using power-on sequence:

- Maximum attenuation
- Normal operation (not Standby Mode)

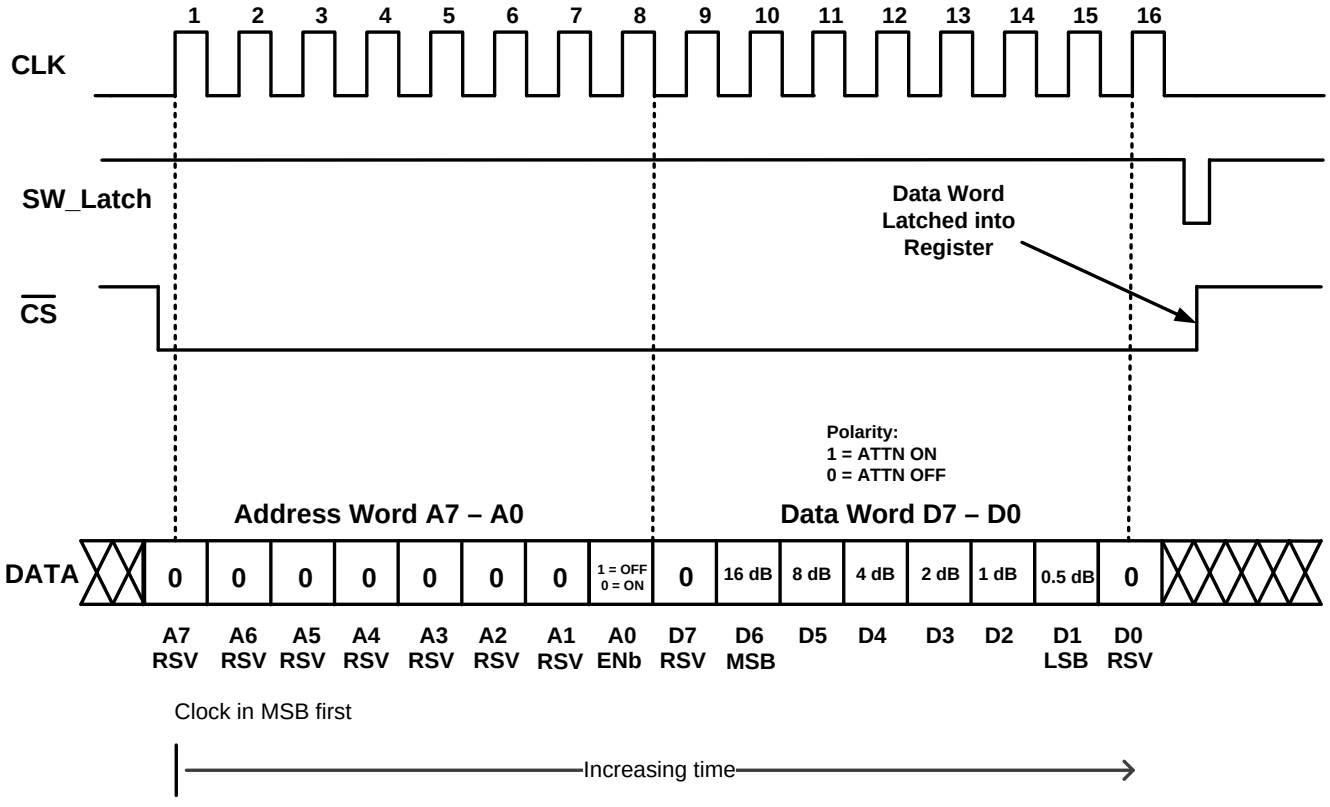
Regarding Phase of I & Q:

- When LO is high-side injected, IF_I leads IF_Q by 90 degrees
- When LO is low-side injected, IF_Q leads IF_I by 90 degrees

Serial Programming

The device is programmed via the serial port by asserting Chip Select (CSb). Note: Most-Significant-Bit (MSB) first, where the Address Word is the most significant.

Figure 117. Serial mode timing diagram high level



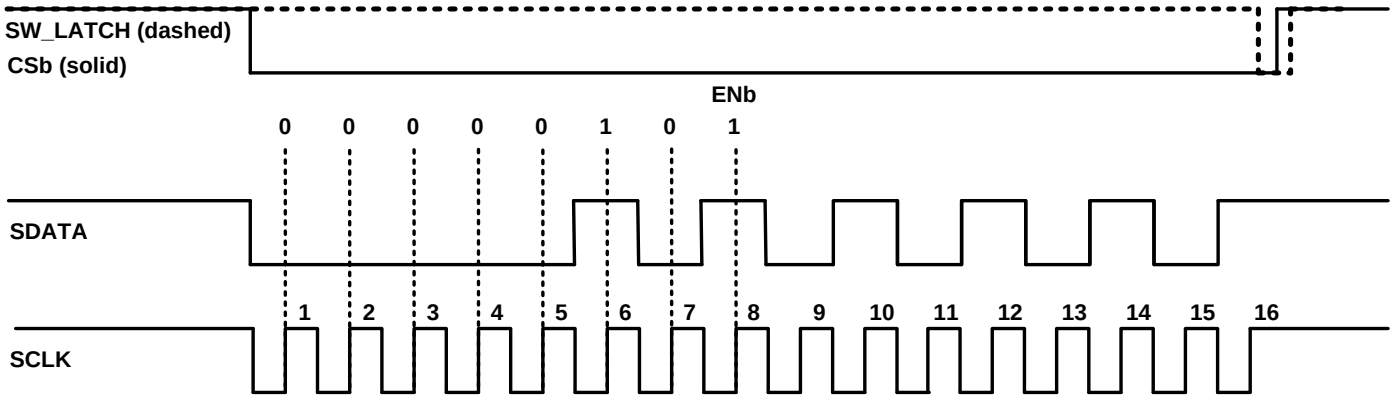
To program the serial interface:

If CSb is de-asserted (set to high), the serial interface will ignore the CLK line. Once CSb is asserted (set to low), the serial interface will recognize the CLK and any data present on DATA will be clocked into the registers with each rising CLK edge. After the 16th CLK cycle, and before the 17th CLK cycle, CSb must be de-asserted to successfully program the part with the desired bytes. If CSb is de-asserted before the 16th CLK cycle, or after the 17th CLK cycle, there is no guarantee that the correct bytes will be programmed and the user will have to re-program the interface in accordance with the aforementioned procedure.

SW_LATCH programming sequence

- When SW_LATCH is pinned high during the programming sequence, the "ENb" register cannot be programmed and therefore will not toggle.
- If SW_LATCH is pinned low during the programming sequence, the "ENb" register will toggle. This can be prevented with the "Programming Sequence" below.

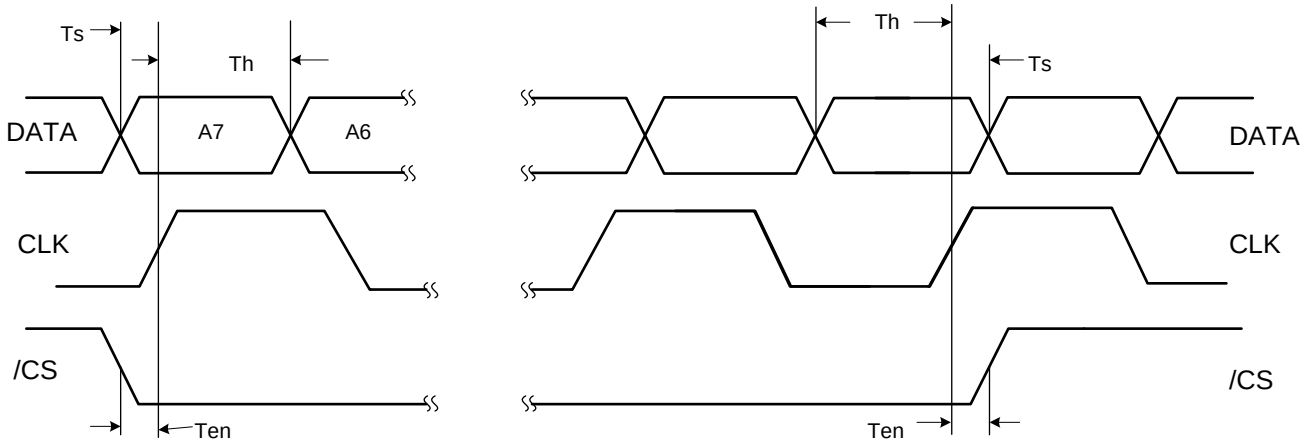
Figure 118. Serial mode timing diagram



Sequence for programming registers A<2>:A<0>

1. SW_Latch = 1; CSb = 0
2. CLK in 8- or 16-bit word, *do not de-assert (pull high) CSb*
3. Set SW_LATCH = 0 while CSb = 0 remains
4. With SW_Latch = 0, set CSb = 1
5. Set SW_Latch = 1
6. Program complete

Figure 119. Serial mode timing diagram zoom:



- Data is shifted with the rising edge of CLK when /CS is low
- The rising edge of /CS latches data into the device

Table 9. Logic Truth Table

STBY	SW_LATCH	Mode	Write Access
0	0	Operating Mode	A2:A0 Enabled, D7:D0 Enabled
0	1	Operating Mode	A2:A0 Disabled, D7:D0 Enabled
1	0	Off	A2:A0 Enabled, D7:D0 Enabled
1	1	Off	A2:A0 Disabled, D7:D0 Enabled

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Attenuation Table

The F1385 attenuation setting is controlled by 6 bits in the data word. The device provides for a attenuation range from 0 dB to 25.5 dB in 0.5 dB steps. A “high” or “1” bit corresponds to attenuation stepped IN, while a “low” or “0” bit corresponds to attenuation stepped OUT.

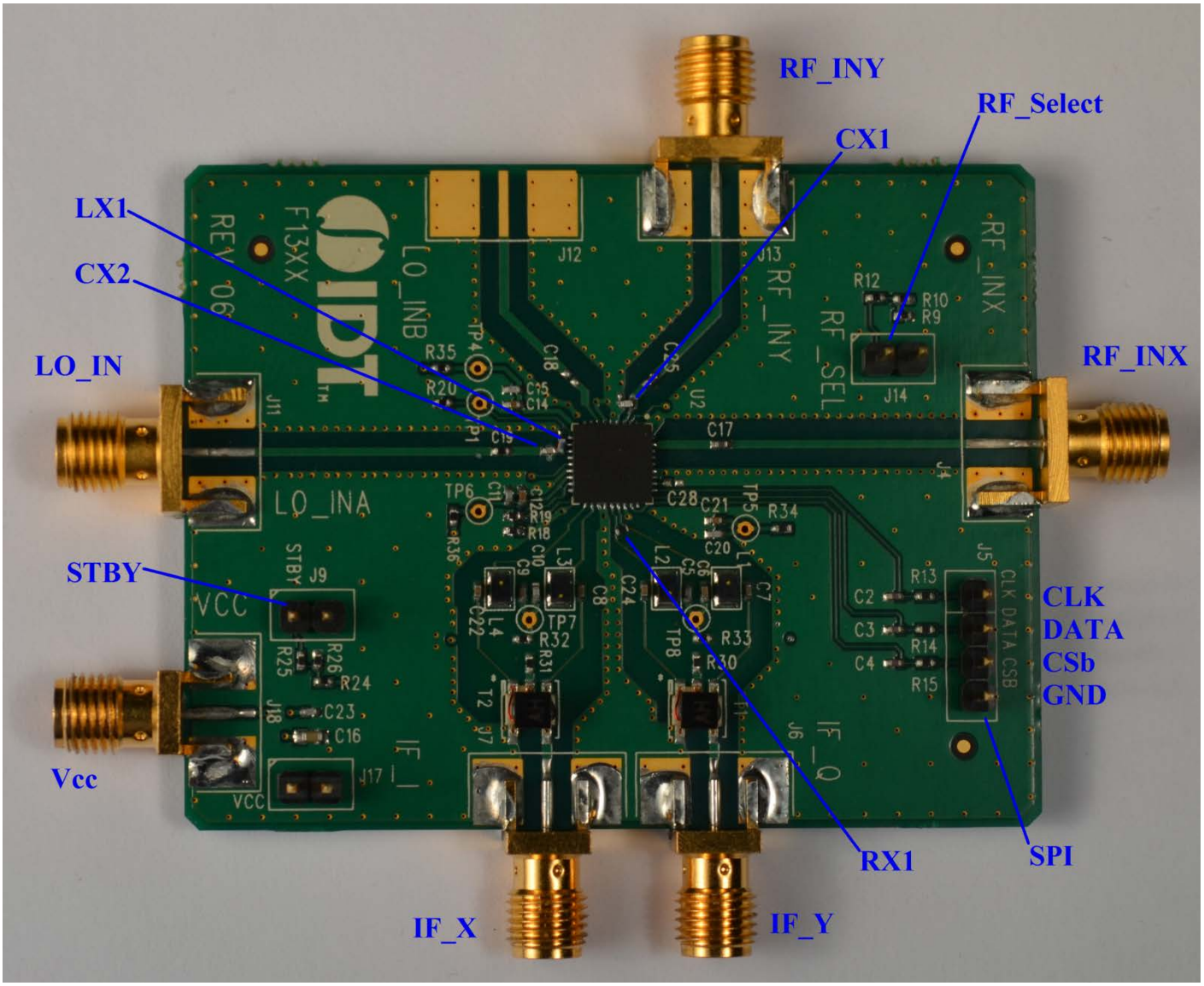
Because the first and last bits of the Data Word are not presently used by the F1385, two additional hex character pairs exist for each of those in this table. For example, data words of either H00, H80, or H01 (binary “00000000,” “10000000,” or 00000001) will place the F1385 in its minimum attenuation state. Likewise, data words of either H66, HE6, or H67 (binary “01100110” or “11100110” or “01100111”) will place the F1385 in its maximum attenuation state of 25.5 added attenuation.

Table 10. Attenuation Table

State	Attenuation (dB)	Hex	Binary D7 – D0	State	Attenuation (dB)	Hex	Binary D7 – D0
0	0.0	00	00000000	26	13.0	34	00110100
1	0.5	02	00000010	27	13.5	36	00110110
2	1.0	04	00000100	28	14.0	38	00111000
3	1.5	06	00000110	29	14.5	3A	00111010
4	2.0	08	00001000	30	15.0	3C	00111100
5	2.5	0A	00001010	31	15.5	3E	00111110
6	3.0	0C	00001100	32	16.0	40	01000000
7	3.5	0E	00001110	33	16.5	42	01000010
8	4.0	10	00010000	34	17.0	44	01000100
9	4.5	12	00010010	35	17.5	46	01000110
10	5.0	14	00010100	36	18.0	48	01001000
11	5.5	16	00010110	37	18.5	4A	01001010
12	6.0	18	00011000	38	19.0	4C	01001100
13	6.5	1A	00011010	39	19.5	4E	01001110
14	7.0	1C	00011100	40	20.0	50	01010000
15	7.5	1E	00011110	41	20.5	52	01010010
16	8.0	20	00100000	42	21.0	54	01010100
17	8.5	22	00100010	43	21.5	56	01010110
18	9.0	24	00100100	44	22.0	58	01011000
19	9.5	26	00100110	45	22.5	5A	01011010
20	10.0	28	00101000	46	23.0	5C	01011100
21	10.5	2A	00101010	47	23.5	5E	01011110
22	11.0	2C	00101100	48	24.0	60	01100000
23	11.5	2E	00101110	49	24.5	62	01100010
24	12.0	30	00110000	50	25.0	64	01100100
25	12.5	32	00110010	51	25.5	66	01100110

Evaluation Kit Picture

Figure 120. Top View



Evaluation Kit / Applications Circuit

Figure 121. Electrical Schematic

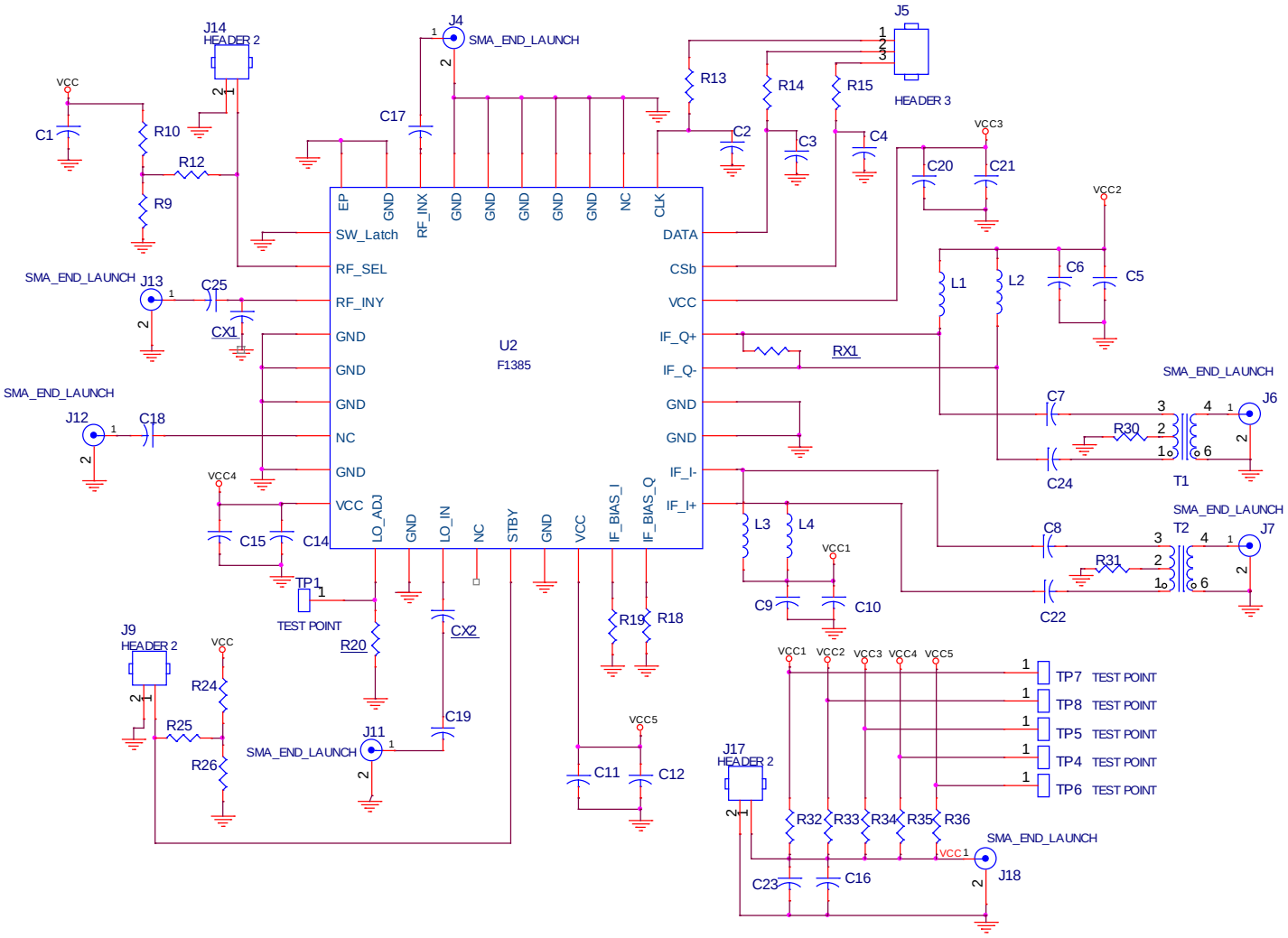


Table 11. Bill of Material (BOM Rev 3)

Part Reference	QTY	Description	Manufacturer Part #	Manufacturer
C2, C3, C4	3	100 pF ±5%, 50 V, C0G Ceramic Capacitor (0402)	GRM1555C1H101J	MURATA
C6, C7, C8, C9, C12, C14, C21, C22, C24	9	10 nF ±5%, 50 V, X7R Ceramic Capacitor (0402)	GRM155R71H103J	MURATA
C5, C10, C11, C15, C20, C23	6	1000 pF ±5%, 50 V, C0G Ceramic Capacitor (0402)	GRM1555C1H102J	MURATA
C17, C25	2	39 pF ±5%, 50 V, C0G Ceramic Capacitor (0402)	GRM1555C1H390J	MURATA
C16	1	10 uF ±20%, 16 V, X5R Ceramic Capacitor (0603)	GRM188R81C106M	MURATA
CX1	1	0.4 pF ±0.05 pF, 50 V, C0G Ceramic Capacitor (0402)	GRM1555C1HR40W	MURATA
CX2	1	0.8 pF ±0.05 pF, 50 V, C0G Ceramic Capacitor (0402)	GJM1555C1HR80W	MURATA
R30, R31, R32, R33, R34, R35, C19	7	0 Ω Resistor (0402)	ERJ-2GE0R00X	Panasonic
R36	1	20 Ω ±1%, 1/10W, Resistor (0402)	ERJ-2RKF20R0X	Panasonic
R13, R14, R15	3	100 Ω ±1%, 1/10W, Resistor (0402)	ERJ-2RKF1000X	Panasonic
R18, R19	2	127 Ω ±1%, 1/10W, Resistor (0402)	ERJ-2RKF1270X	Panasonic
R20	1	4.3 kΩ ±1%, 1/10W, Resistor (0402)	ERJ-2RKF4301X	Panasonic
R10, R24	2	43 kΩ ±1%, 1/10W, Resistor (0402)	ERJ-2RKF4302X	Panasonic
R12, R25	2	47 kΩ ±1%, 1/10W, Resistor (0402)	ERJ-2RKF4702X	Panasonic
R9, R26	2	75 kΩ ±1%, 1/10W, Resistor (0402)	ERJ-2RKF7502X	Panasonic
RX1	1	1.74 kΩ ±1%, 1/10W, Resistor (0402)	ERJ-2RKF1741X	Panasonic
J9, J14, J17	3	CONN HEADER VERT SGL 2 X 1 POS GOLD	961102-6404-AR	3M
J5	1	CONN HEADER VERT SGL 4 X 1 POS GOLD	961104-6404-AR	3M
J6, J7, J18	3	Edge Launch SMA (0.250 inch pitch ground, round)	142-0711-821	Emerson Johnson
J4, J11, J13	3	Edge Launch SMA (0.375 inch pitch ground, tab)	142-0701-851	Emerson Johnson
L1, L2, L3, L4	4	1 uH ±5%, .500 A, Ferrite Chip Inductor (0805)	0805LS-102XJLB	COILCRAFT
T1, T2	2	10-700 MHz 50 Ω, RF Transformer (2:1)	TC2-72T+	Mini Circuits
U1	1	DPD Demodulator	F1385	IDT
	1	Printed Circuit Board	F13XX	IDT

Application Information

F1385 has been optimized for use in high performance RF applications from 3200 MHz to 4400 MHz.

Power Supplies

All supply pins should be bypassed with external capacitors to minimize noise and fast transients. Supply noise can degrade noise figure and fast transients can trigger ESD clamps and cause them to fail. Supply voltage change or transients should have a slew rate smaller than 1 V / 20 µS. In addition, all control pins should remain at 0 V (+/-0.3 V) while the supply voltage ramps or while it returns to zero.

Control Pin Voltage & Resistance Values (pins not connected)

The following table provides open-circuit DC voltage and resistance values referenced to ground for each of the control pins listed.

Table 12. Control Pin Voltage and resistances

Pin	Name	DC voltage (volts)	Resistance (ohms)
1	SW_LATCH	1.75	1.6M
2	RF_SEL	1.75	800K
14	STBY	5.00	50K
26	CSb	1.75	1.6M
27	DATA	1.75	1.6M
28	CLK	1.75	1.6M

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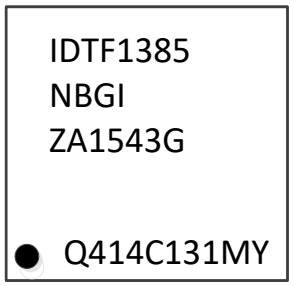
Package Outline Drawings

The package outline drawings are located at the end of this document and are accessible from the Renesas website (see Ordering Information for POD links). The package information is the most current data available and is subject to change without revision of this document.

Ordering Information

Orderable Part Number	Package	MSL Rating	Shipping Packaging	Temperature
F1385NBGI	6 x 6 x 0.75 mm 36-VFQFPN	MSL1	Tray	-40 °C to +105 °C
F1385NBGI8	6 x 6 x 0.75 mm 36-VFQFPN	MSL1	Tape and Reel	-40 °C to +105 °C
F1385EVBI	Evaluation Board			-40 °C to +105 °C
F1385EVS	Evaluation Board with Controller			-40 °C to +105 °C

Marking Diagram



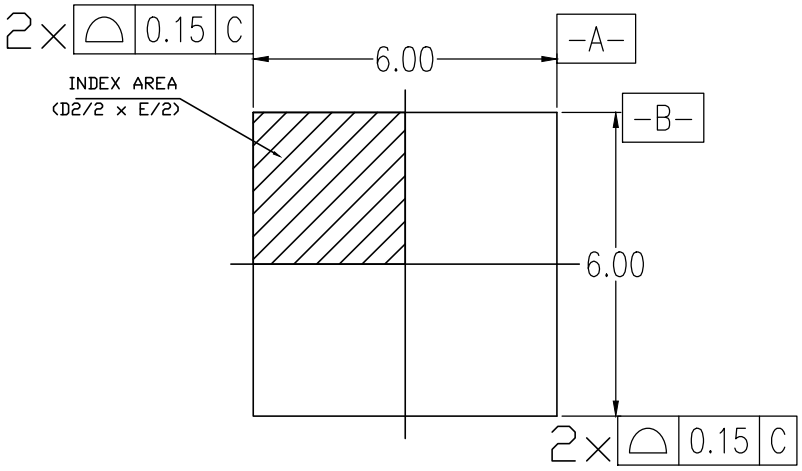
1. Line 1 and 2 are the part number.
2. Line 3 - “ZA” are ASM Test Step.
3. Line 3 - “1537” is the Date Code YYWW.
4. Line 3 - “G” Assembler Code.
5. Line 4 – “Q414C131MY” Assembly Lot Code.

Revision History

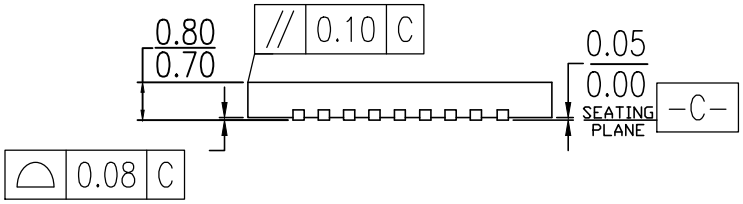
Revision Date	Description of Change
February 7, 2022	Rebranded to Renesas.
August 16, 2016	Updated spec table, Typ-Ops plots per new device stepping ZA with improved image rejection
October 23, 2015	Production Release

36-VFQFPN, Package Outline Drawing

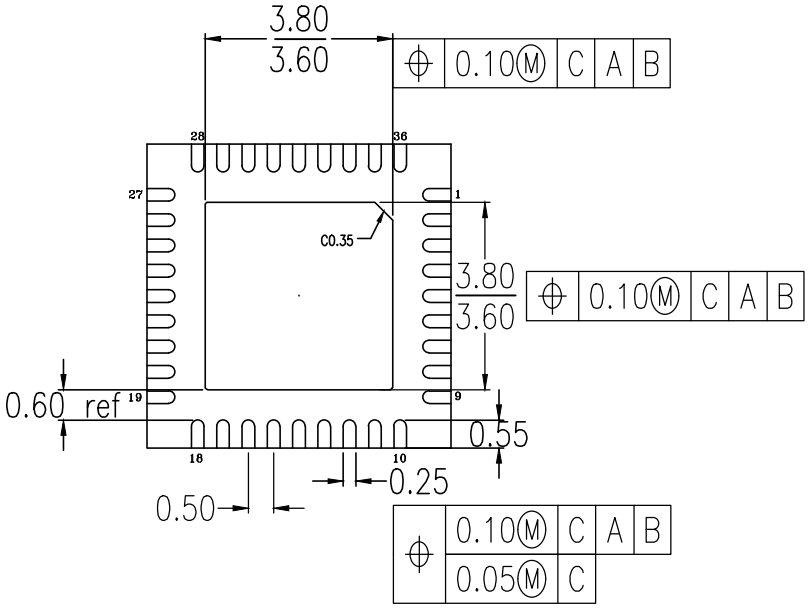
6.00 x 6.00 x 0.75 mm Body, 3.70 x 3.70 mm Epad, 0.5mm Pitch



TOP VIEW



SIDE VIEW

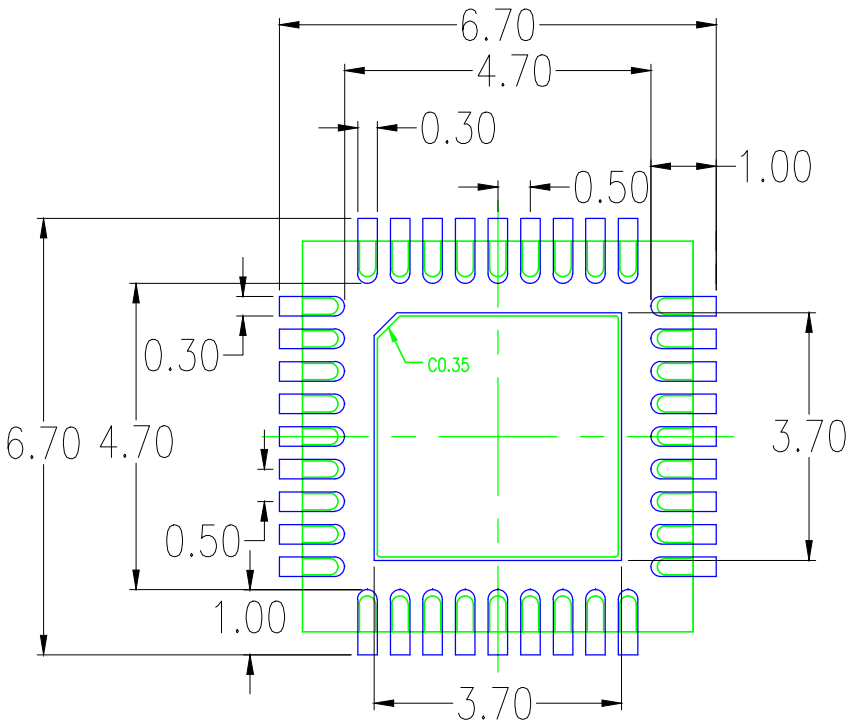


BOTTOM VIEW

NOTES:

1. ALL DIMENSIONING AND TOLERANCING CONFORM TO ANSI Y14.5M–1982
2. ALL DIMENSIONS ARE IN MILLIMETERS.

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RECOMMENDED LAND PATTERN DIMENSION

NOTES:

1. ALL DIMENSION ARE IN mm. ANGLES IN DEGREES.
2. TOP DOWN VIEW. AS VIEWED ON PCB.
3. COMPONENT OUTLINE SHOW FOR REFERENCE IN GREEN.
4. LAND PATTERN IN BLUE. NSMD PATTERN ASSUMED.
5. LAND PATTERN RECOMMENDATION PER IPC-7351B GENERIC REQUIREMENT FOR SURFACE MOUNT DESIGN AND LAND PATTERN.

Package Revision History		
Date Created	Rev No.	Description
Nov 8, 2021	01	Update IDT format to Renesas format
Apr 6, 2016	00	Initial Release

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