Description

The F2913 is a high isolation, low insertion loss, 50Ω SP2T absorptive RF switch designed for a multitude of wireless and RF applications. This device covers a broad frequency range of 50MHz to 6000MHz. In addition to providing low insertion loss, the F2913 also delivers high linearity and high isolation performance while providing a 50Ω termination at all RF ports.

The F2913 uses a single positive supply voltage of +2.7V to +5.5V and supports three states using either +1.8V or +3.3V control logic.

Competitive Advantage

- Low insertion loss
- High isolation
- Excellent linearity
- Fast switching time
- High termination power handling
- Extended temperature range

Typical Applications

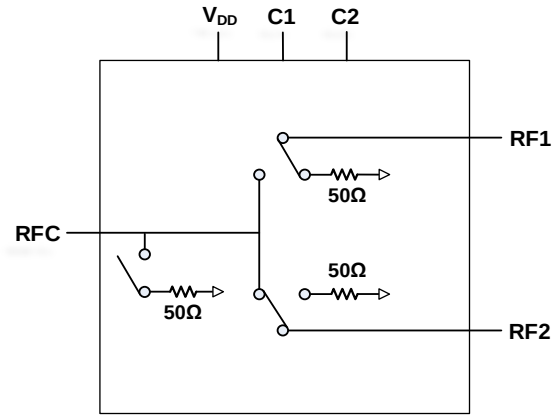
- Base Station 2G, 3G, 4G, 5G
- Portable Wireless
- Repeaters and E911 Systems
- Digital Pre-Distortion
- Point-to-Point Infrastructure
- Public Safety Infrastructure
- WIMAX Receivers and Transmitters
- Military Systems, JTRS Radios
- RFID Handheld and Portable Readers
- Test / ATE Equipment

Features

- Low insertion loss: 0.79dB at 2GHz
- High isolation:
  - 71dB at 1GHz
  - 65dB at 2GHz
  - 58dB at 4GHz
- High IIP3: +65dBm at 2.6GHz
- Supply voltage: +2.7V to +5.5V
- 1.8V and 3.3V compatible control logic
- Operating temperature: -40°C to +110°C
- 4 × 4 mm 20-VFQFPN package

Block Diagram

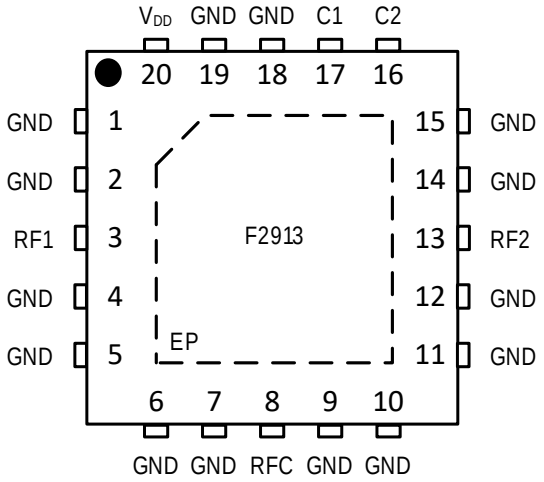
Figure 1. Block Diagram



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Pin Assignments

Figure 2. Pin Assignments for 4mm x 4mm x 0.95mm 20-QFN – Top View



Pin Descriptions

Table 1. Pin Descriptions

Pin	Name	Function
1, 15, 18	GND	This pin is internally connected to the exposed paddle. Connect this pin to ground as close as possible to the pin.
2, 4, 5, 6, 7, 9, 10, 11, 12, 14, 19	GND	Connect this pin directly to ground as close as possible to the pin with thru vias.
3	RF1	RF1 Port. If this pin is not 0V DC, then an external coupling capacitor must be used.
8	RFC	RF Common Port. If this pin is not 0V DC, then an external coupling capacitor must be used.
13	RF2	RF2 Port. If this pin is not 0V DC, then an external coupling capacitor must be used.
16	C2	Logic control pin. See Table 7 for proper logic setting.
17	C1	Logic control pin. See Table 7 for proper logic setting.
20	V_{DD}	Power supply. Bypass to GND with capacitors shown in the Figure 30 as close as possible to the pin.
	EP	Exposed Pad. This is internally connected to GND. Solder this exposed pad to a PCB pad that uses multiple ground vias to provide heat transfer out of the device into the PCB ground planes. These multiple ground vias are also required to achieve the specified RF performance.

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Absolute Maximum Ratings

Stresses beyond those listed below may cause permanent damage to the device. Functional operation of the device at these or any other conditions beyond those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 2. Absolute Maximum Ratings

Parameter		Symbol	Minimum	Maximum	Units
V_{DD} to GND		V_{DD}	-0.5	+6.0	V
C1, C2 to GND		V_{LOGIC}	-0.3	Lower of (V_{DD} + 0.3, 3.9)	V
RF1, RF2, RFC to GND		V_{RF}	-0.3	0.3	V
Maximum Input CW Power, $Z_S = Z_L = 50\Omega$, $T_{EP} = 25°C$, $V_{DD} = 5.5V$ (any port) [a]	Insertion loss states	P_{ABSCW}		33	dBm
	Terminated states	P_{ABSCW_TERM}		27	
Maximum Input Peak Power, $Z_S = Z_L = 50\Omega$, $T_{EP} = 25°C$, $V_{DD} = 5.5V$ (any port) [a, b]	Insertion loss states	P_{ABSPK}		36	dBm
	Terminated states	P_{ABSPK_TERM}		30	
Junction Temperature		T_{JMAX}		140	°C
Storage Temperature Range		T_{ST}	-65	150	°C
Lead Temperature (soldering, 10s)		T_{LEAD}		260	°C
Electrostatic Discharge – HBM (JEDEC/ESDA JS-001-2012)		V_{ESDHBM}		2500 (Class 2)	V
Electrostatic Discharge – CDM (JEDEC 22-C101F)		V_{ESDCDM}		1000 (Class C2)	V

a. T_{EP} = Temperature of the exposed paddle.
b. 5% duty cycle of a 4.6ms period.

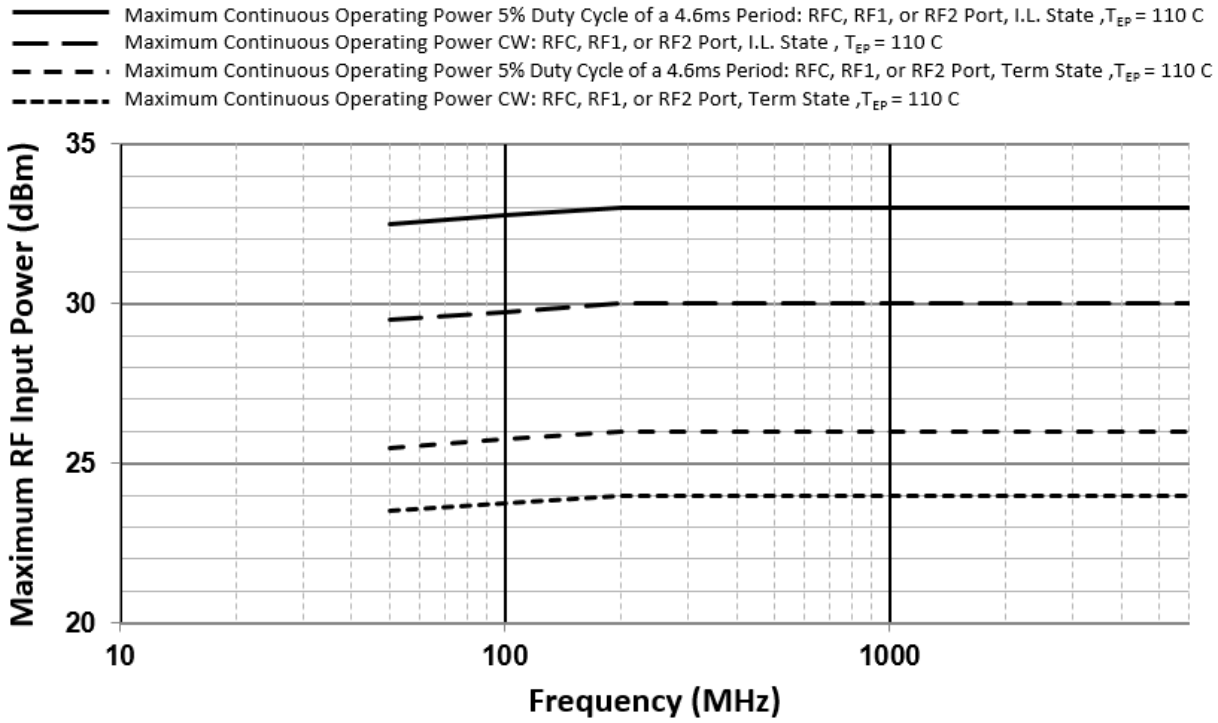
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Recommended Operating Conditions

Table 3. Recommended Operating Conditions

Parameter	Symbol	Condition	Minimum	Typical	Maximum	Units
Supply Voltage	V_{DD}		2.7	3.3	5.5	V
Operating Temperature Range	T_{EP}	Exposed Paddle	-40		+110	°C
RF Frequency Range	f_{RF}		50		6000	MHz
Maximum Operating Input Power	P_{MAX}	$Z_S = Z_L = 50\Omega$			See Figure 3	dBm
Port Impedance (RFC, RF1, RF2)	Z_{RF}			50		Ω

Figure 3. Maximum RF Input Operating Power vs. RF Frequency ($Z_S = Z_L = 50\Omega$)



Electrical Characteristics

Table 4. Electrical Characteristics

See the F2913 Typical Application Circuit. Specifications apply when operated with V_{DD} = +3.3V, T_{EP} = +25°C, Z_S = Z_L = 50Ω, RF signals applied at RF1 or RF2 and measured at RFC, and Evaluation Board trace and connector losses are de-embedded, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Logic Input High	V_{IH}	C1, C2 pins	1.17 [b]		Lower of (V_{DD}, 3.6)	V
Logic Input Low	V_{IL}	C1, C2 pins	-0.3		0.6	V
Logic Current	I_{IH}, I_{IL}		*-1 [a]*		*+1*	µA
DC Current (V_{DD})	I_{DD}			90	*170*	µA
Insertion Loss RF1 to RFC or RF2 to RFC	IL	50MHz ≤ f_{RF} ≤ 400MHz		0.77	0.97	dB
		400MHz < f_{RF} ≤ 1GHz [c]		0.79	*1.00*	
		1GHz < f_{RF} ≤ 2GHz		0.79	1.00	
		2GHz < f_{RF} ≤ 3GHz		0.88	1.10	
		3GHz < f_{RF} ≤ 4GHz		1.03	1.40	
		4GHz < f_{RF} ≤ 5GHz		1.15	1.50	
		5GHz < f_{RF} ≤ 6GHz		1.25	1.65	
Isolation (RFC to RF1, RF2) (one path on)	ISO1	50MHz ≤ f_{RF} ≤ 400MHz	74	79		dB
		400MHz < f_{RF} ≤ 1GHz	66	71		
		1GHz < f_{RF} ≤ 2GHz	60	65		
		2GHz < f_{RF} ≤ 3GHz	57	62		
		3GHz < f_{RF} ≤ 4GHz	53	58		
		4GHz < f_{RF} ≤ 5GHz	50	54		
		5GHz < f_{RF} ≤ 6GHz	46	51		
Isolation (RF1 to RF2, RF2 to RF1) (one path on)	ISO2	50MHz ≤ f_{RF} ≤ 400MHz	80	85		dB
		400MHz < f_{RF} ≤ 1GHz	75	80		
		1GHz < f_{RF} ≤ 2GHz	67	72		
		2GHz < f_{RF} ≤ 3GHz	62	67		
		3GHz < f_{RF} ≤ 4GHz	57	62		
		4GHz < f_{RF} ≤ 5GHz	53	58		
		5GHz < f_{RF} ≤ 6GHz	51	56		
Return Loss RF1, RF2 [d] Insertion Loss State	RL1	50MHz ≤ f_{RF} ≤ 4GHz		20		dB
		4GHz < f_{RF} ≤ 6GHz		18.7		
Return Loss RFC [d] Insertion Loss State	RL2	50MHz ≤ f_{RF} ≤ 4GHz		18.0		dB
		4GHz < f_{RF} ≤ 6GHz		15.2		

a. Items in min/max columns in ***bold italics*** are guaranteed by test.
b. Items in min/max columns that are not bold italics are guaranteed by design characterization.
c. Maximum spec guaranteed by test at 1GHz and by design characterization over the whole frequency range.
d. Return loss includes mismatch effects of Evaluation Kit PCB and RF connectors.

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Electrical Characteristics

Table 5. Electrical Characteristics

See F2913 Typical Application Circuit. Specifications apply when operated with V_{DD} = +3.3V, T_{EP} = +25°C, Z_S = Z_L = 50Ω, RF signals applied at RF1 or RF2 and measured at RFC, Evaluation Board trace and connector losses are de-embedded, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Return Loss RF1, RF2 [c] Terminated State, All Off State	RL3	50MHz ≤ f_{RF} ≤ 4GHz		20.3		dB
		4GHz < f_{RF} ≤ 6GHz		19.3		
Return Loss RFC [c] All Off State	RL4	50MHz ≤ f_{RF} ≤ 4GHz		17.5		dB
		4GHz < f_{RF} ≤ 6GHz		15.3		
Input IP2 (RF1, RF2 to RFC)	IIP2	f_1 = 2.55GHz f_2 = 2.65GHz P_{IN} = +20dBm/tone Measure 5.2GHz product		115		dBm
Input IP3 (RF1, RF2 to RFC)	IIP3	f_1 = 2.55GHz f_2 = 2.65GHz P_{IN} = +13dBm/tone Measure 2.75GHz product	60 [b]	65		dBm
Input 1dB Compression [d]	IP1dB	f_{RF} = 50MHz	35	37		dBm
		f_{RF} = 100MHz	35	37		
		f_{RF} = 2400MHz	34	36		
		f_{RF} = 6000MHz	34	36		
Spurious Output (No RF Applied) [e]	P_{SPUR}	All unused ports terminated RBW = 100Hz		-127	-120	dBm
Insertion Loss Flatness	IL_{FLAT}	Any 400MHz range		0.1	0.2	dB
Group Delay	GD			0.05		ns
Switching Time [f]	SW_{TIME}	50% control to 90% RF		155	230	ns
		50% control to 10% RF		142	200	
		50% control to 99% RF		234	300	
		50% control to 1% RF		205	265	
Switching Rate	SW_{RATE}				25	kHz

a. Items in min/max columns in ***bold italics*** are guaranteed by test.
b. Items in min/max columns that are not bold italics are guaranteed by design characterization.
c. Return loss includes mismatch effects of Evaluation Kit PCB and RF connectors.
d. The input 1 dB compression point is a linearity figure of merit. Refer to Figure 3 for the maximum RF operating input power levels.
e. Spurious due to on-chip negative voltage generator. Typical generator fundamental frequency is 2.2MHz.
f. Measured at f_{RF} = 1GHz.

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Thermal Characteristics

Table 6. Package Thermal Characteristics

Parameter	Symbol	Value	Units
Junction to Ambient Thermal Resistance	θ_{JA}	60.2	°C/W
Junction to Case Thermal Resistance (Case is defined as the exposed paddle)	θ_{JC_BOT}	9.5	°C/W
Moisture Sensitivity Rating (Per J-STD-020)		MSL1	

Typical Operating Conditions (TOCs)

Unless otherwise noted:

- V_{DD} = +3.3V
- T_{EP} = 25°C. All temperatures are referenced to the exposed paddle.
- $Z_S = Z_L = 50\Omega$
- f_{RF} = 1GHz
- Small signal tests done at 0dBm input power.
- +13dBm per tone for IIP3 measurements.
- RF1 or RF2 are the driven ports.
- Evaluation Kit traces and connector losses are de-embedded for the insertion loss and isolation plots. All other plots include the loss and effects of the PCB.

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Typical Performance Characteristics (1)

Figure 4. RFC to RF1 Insertion Loss vs. Freq. over Temperature and Voltage

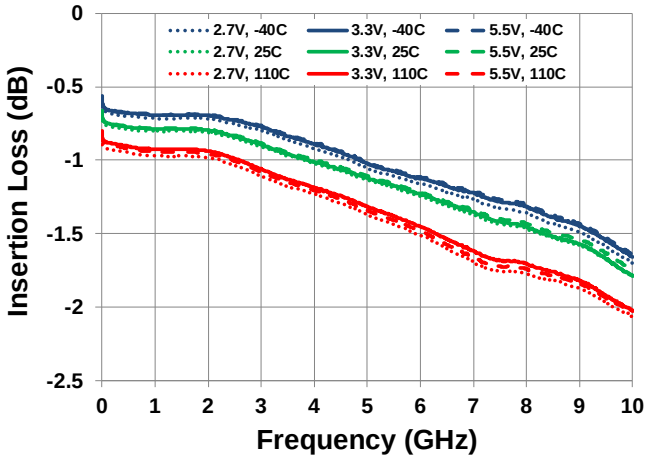


Figure 5. RFC to RF2 Insertion Loss vs. Freq. over Temperature and Voltage

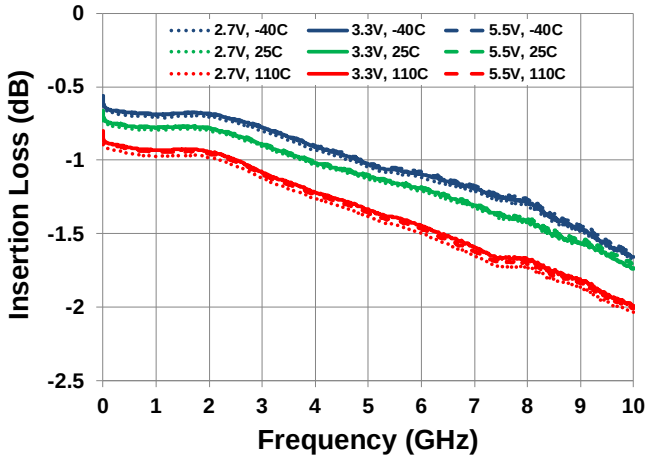


Figure 6. RFC to RF1 Isolation vs. Freq. over Temp. and Voltage (RF2 On State]

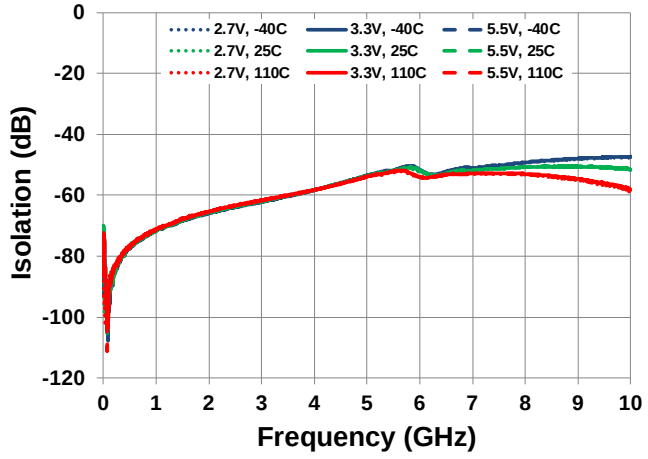


Figure 7. RFC to RF2 Isolation vs. Freq. over Temp. and Voltage (RF1 On State]

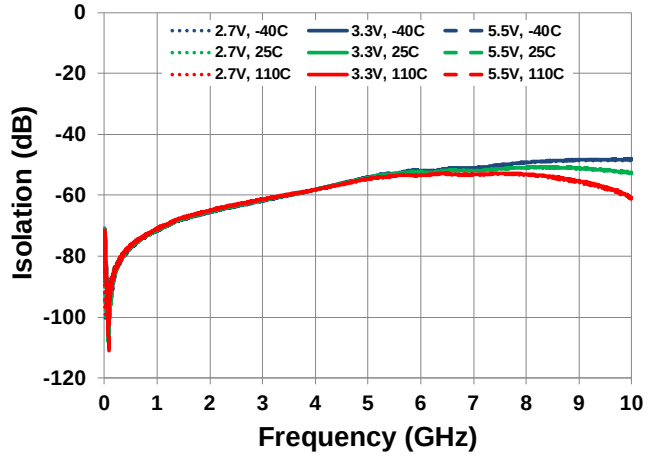


Figure 8. RF1 to RF2 Isolation vs. Freq. over Temp. and Voltage (RF1 On State)

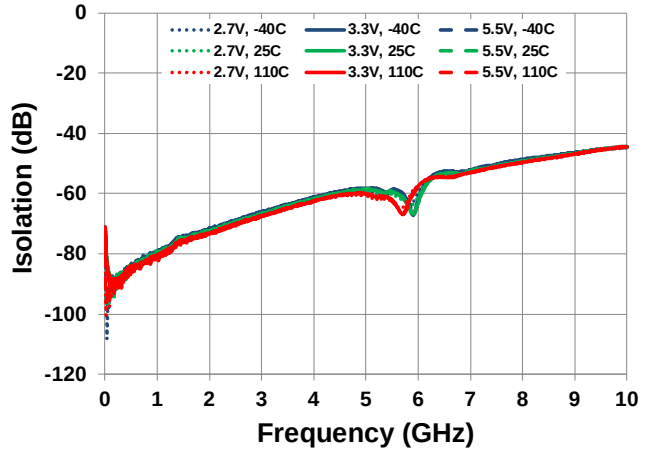
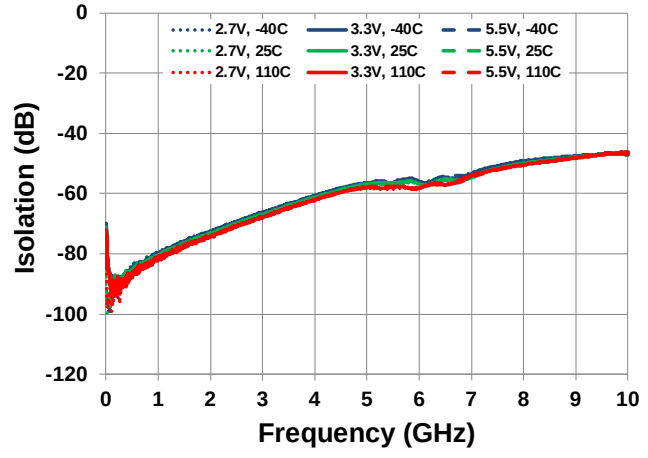


Figure 9. RF2 to RF1 Isolation vs. Freq. over Temp. and Voltage (RF2 On State)



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Typical Performance Characteristics (2)

Figure 10. RFC to RF1 Isolation vs. Freq. over Temp. and Voltage (All Off State)

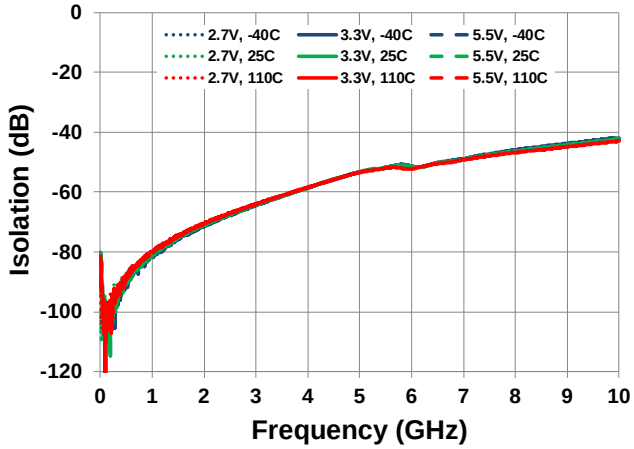


Figure 11. RFC to RF2 Isolation vs. Freq. over Temp. and Voltage (All Off State)

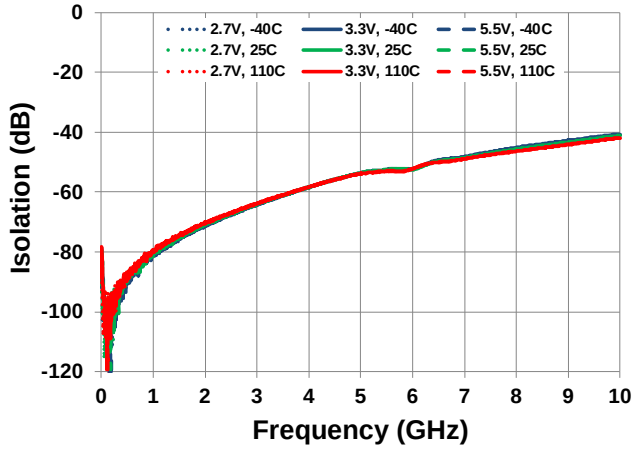


Figure 12. RF1 to RF2 Isolation vs. Freq. over Temp. and Voltage (All Off State)

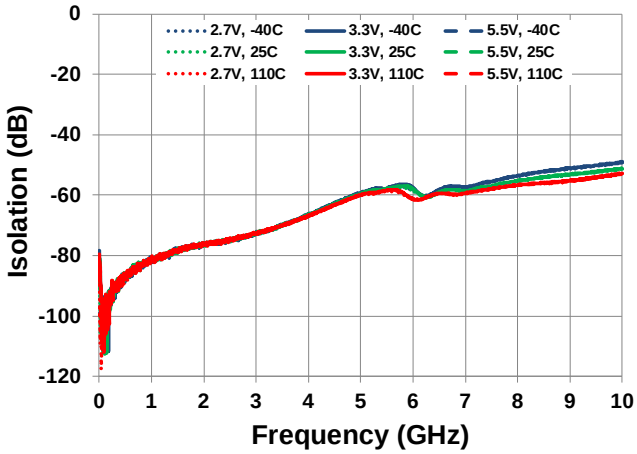


Figure 13. Evaluation Board Thru Line Loss over Temperature

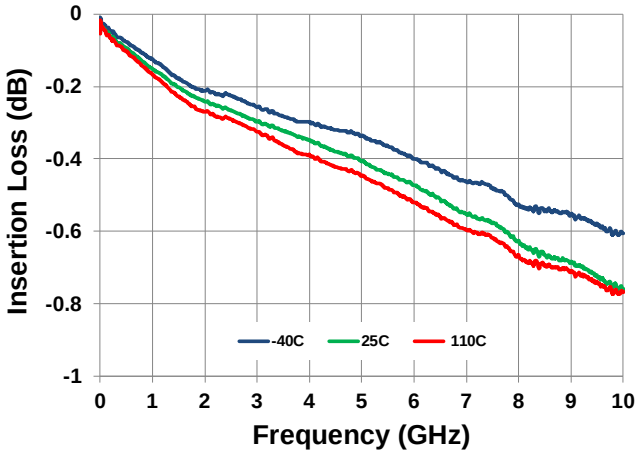
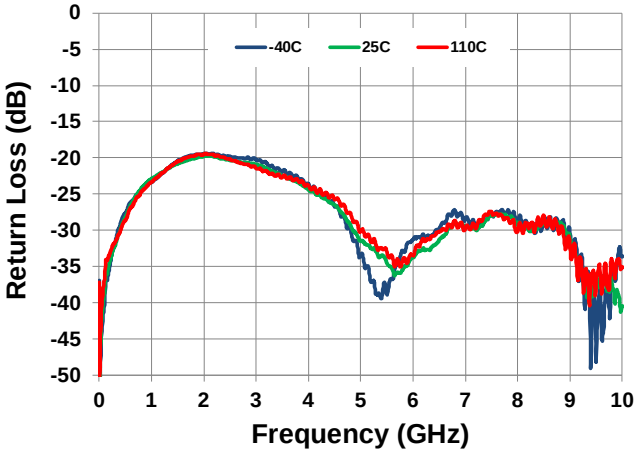


Figure 14. Evaluation Board Thru Line Match over Temperature



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Typical Performance Characteristics (3)

Figure 15. RF1 Return Loss vs. Frequency over Temp. and Voltage (RF1 On State)

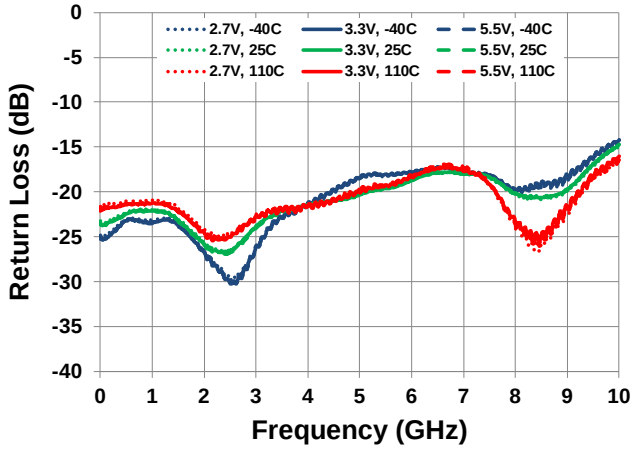


Figure 16. RF1 Return Loss vs. Frequency over Temp. and Voltage (RF2 On State)

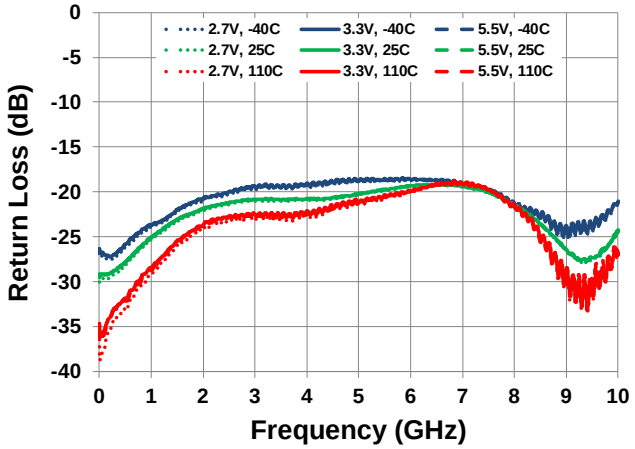


Figure 17. RF2 Return Loss vs. Frequency over Temp. and Voltage (RF2 On State)

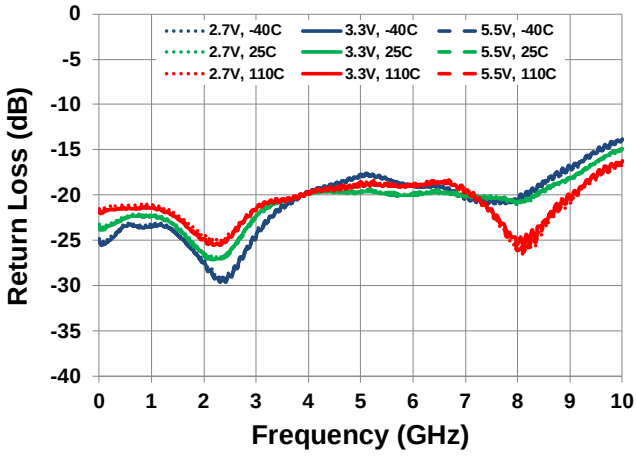


Figure 18. RF2 Return Loss vs. Frequency over Temp. and Voltage (RF1 On State)

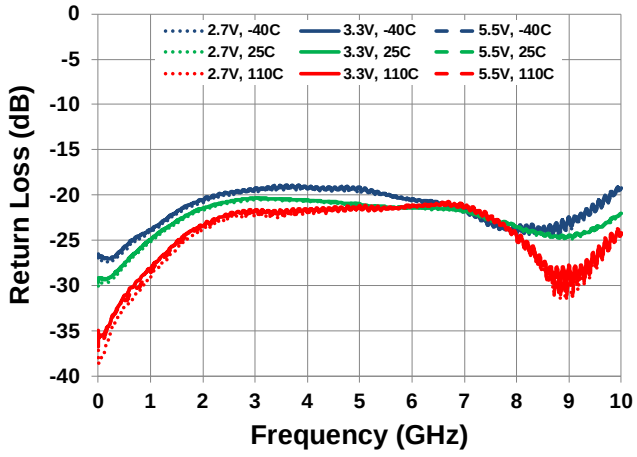


Figure 19. RFC Return Loss vs. Frequency over Temp. and Voltage (RF1 On State)

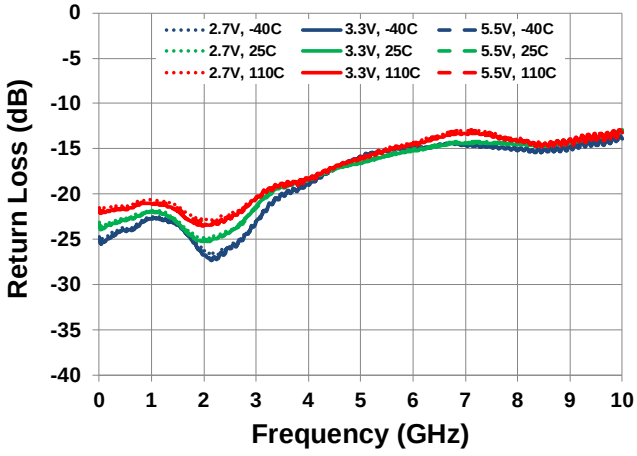
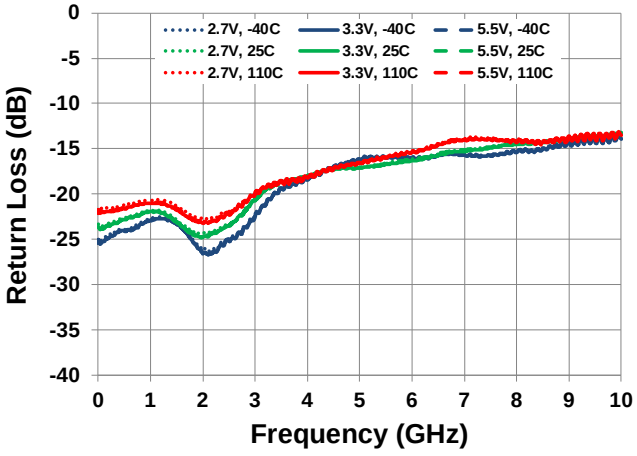


Figure 20. RFC Return Loss vs. Frequency over Temp. and Voltage (RF2 On State)



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Typical Performance Characteristics (4)

Figure 21. RF1 Return Loss vs. Frequency over Temp. and Voltage (All Off State)

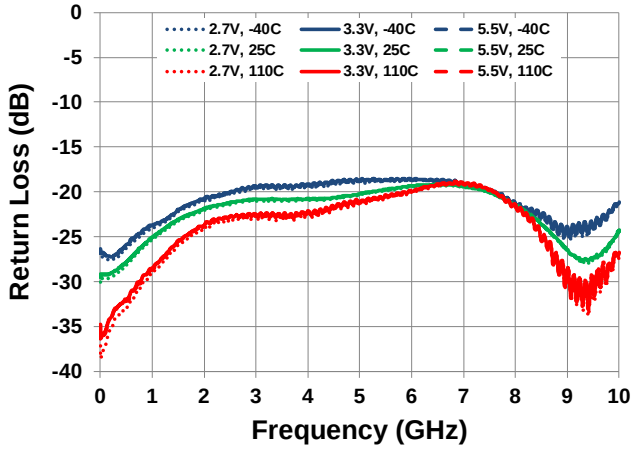


Figure 22. RF2 Return Loss vs. Frequency over Temp. and Voltage (All Off State)

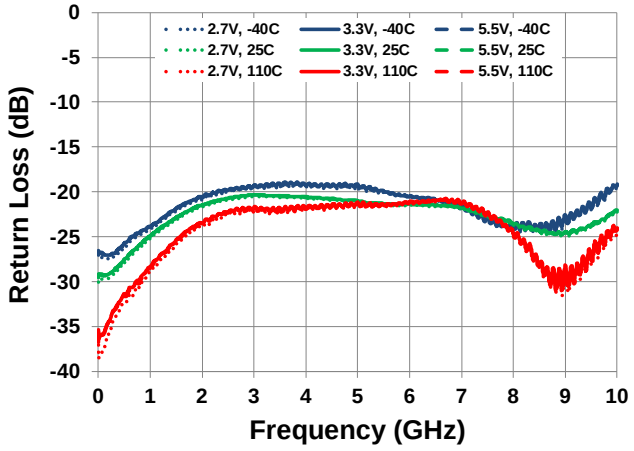


Figure 23. RFC Return Loss vs. Frequency over Temp. and Voltage (All Off State)

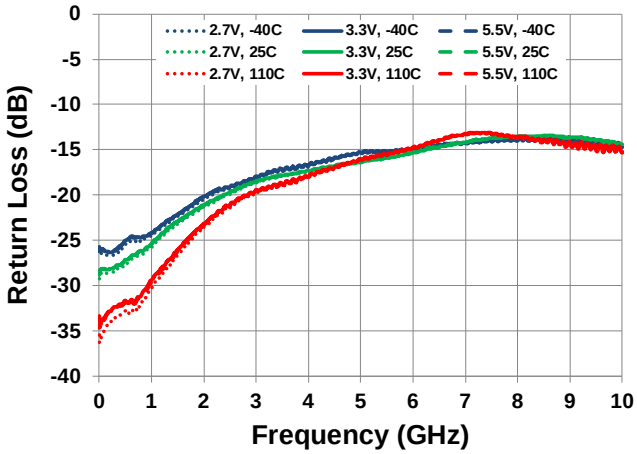


Figure 24. RF1 Input IP3 vs. Frequency over Temp. and Voltage (RF1 On State)

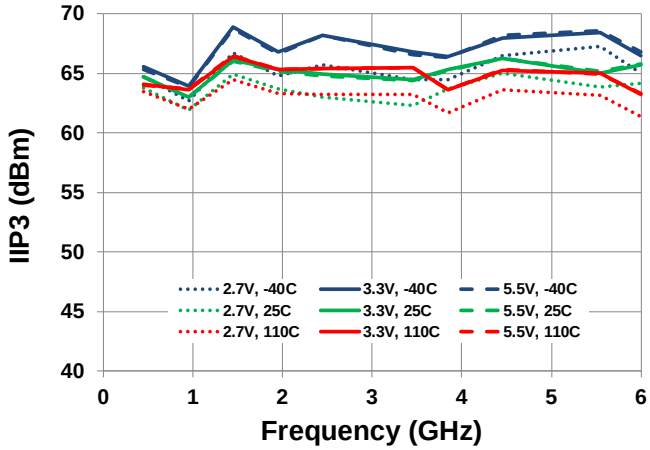


Figure 25. RF2 Input IP3 vs. Frequency over Temp. and Voltage (RF2 On State)

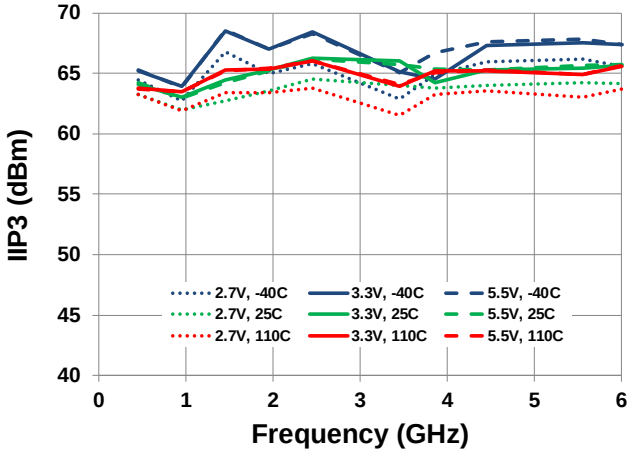
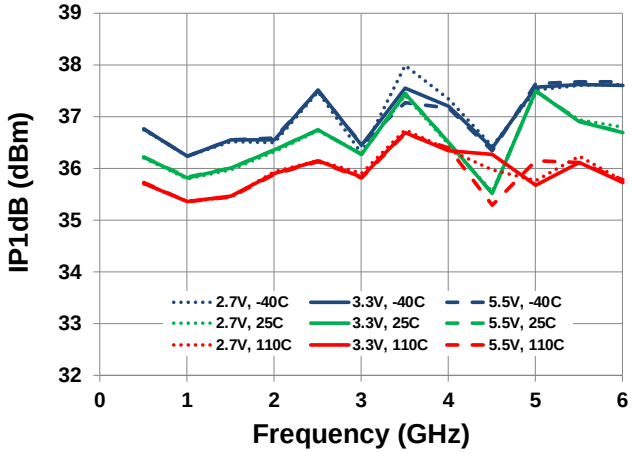


Figure 26. Input P1dB vs. Frequency over Temp. and Voltage (On States)



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Control Mode

Table 7. Switch Control Truth Table

C1	C2	RFC – RF1	RFC – RF2
LOW	LOW	OFF	OFF
LOW	HIGH	OFF	ON
HIGH	LOW	ON	OFF
HIGH	HIGH	N/A	N/A

Application Information

Default Start-up

The C1 and C2 control pins include no internal pull-down resistors to logic LOW or pull-up resistors to logic HIGH.

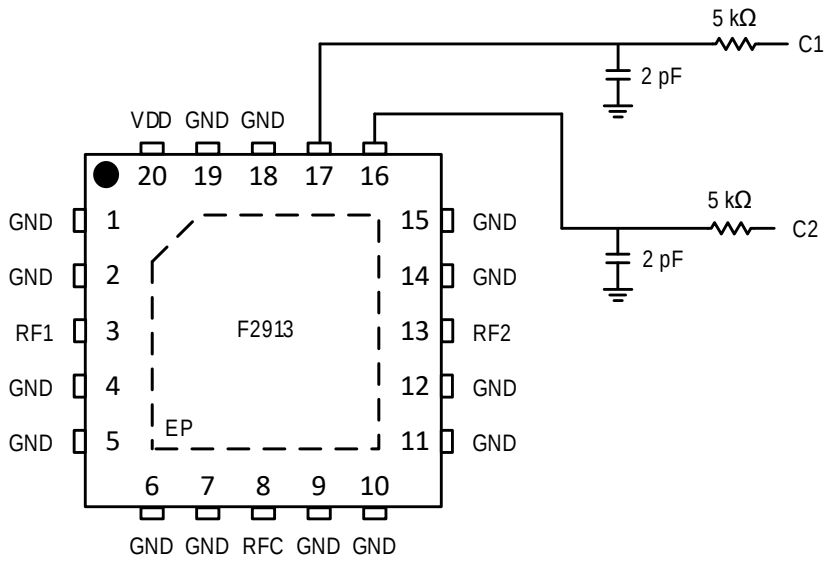
Power Supplies

A common V_{DD} power supply should be used for all pins requiring DC power. All supply pins should be bypassed with external capacitors to minimize noise and fast transients. Supply noise can degrade the noise figure, and fast transients can trigger ESD clamps and cause them to fail. Supply voltage change or transients should have a slew rate slower than 1V / 20µs. In addition, all control pins should remain at 0V (± 0.3V) while the supply voltage ramps up or while it returns to zero.

Control Pin Interface

If a clean control signal for pins 16 and 17 cannot be guaranteed due to overshoot, undershoot, or ringing, etc., the following circuit at the input of the control pins is recommended.

Figure 27. Control Pin Signal Integrity Improvement Circuit



Evaluation Kit Picture

Figure 28. Top View

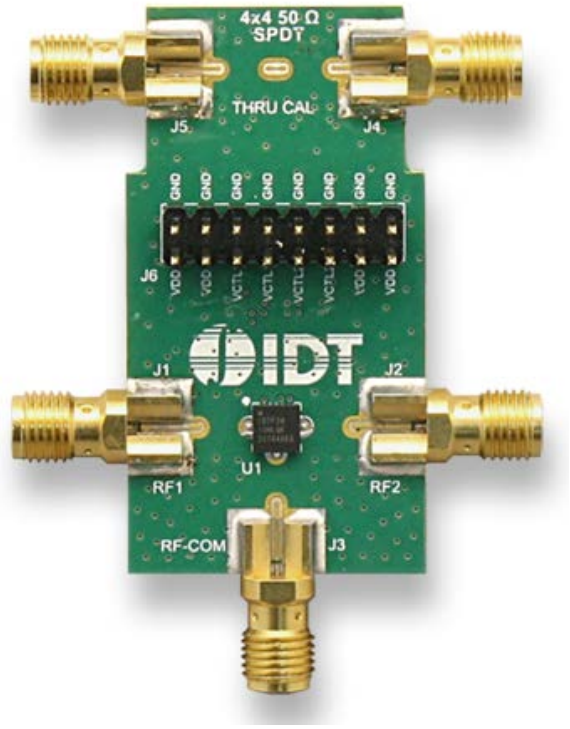
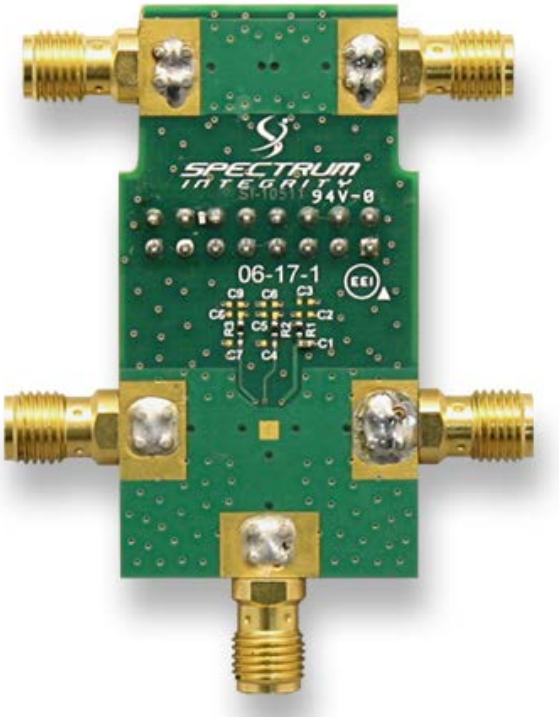


Figure 29. Bottom View



Evaluation Kit / Applications Circuit

Figure 30. Electrical Schematic

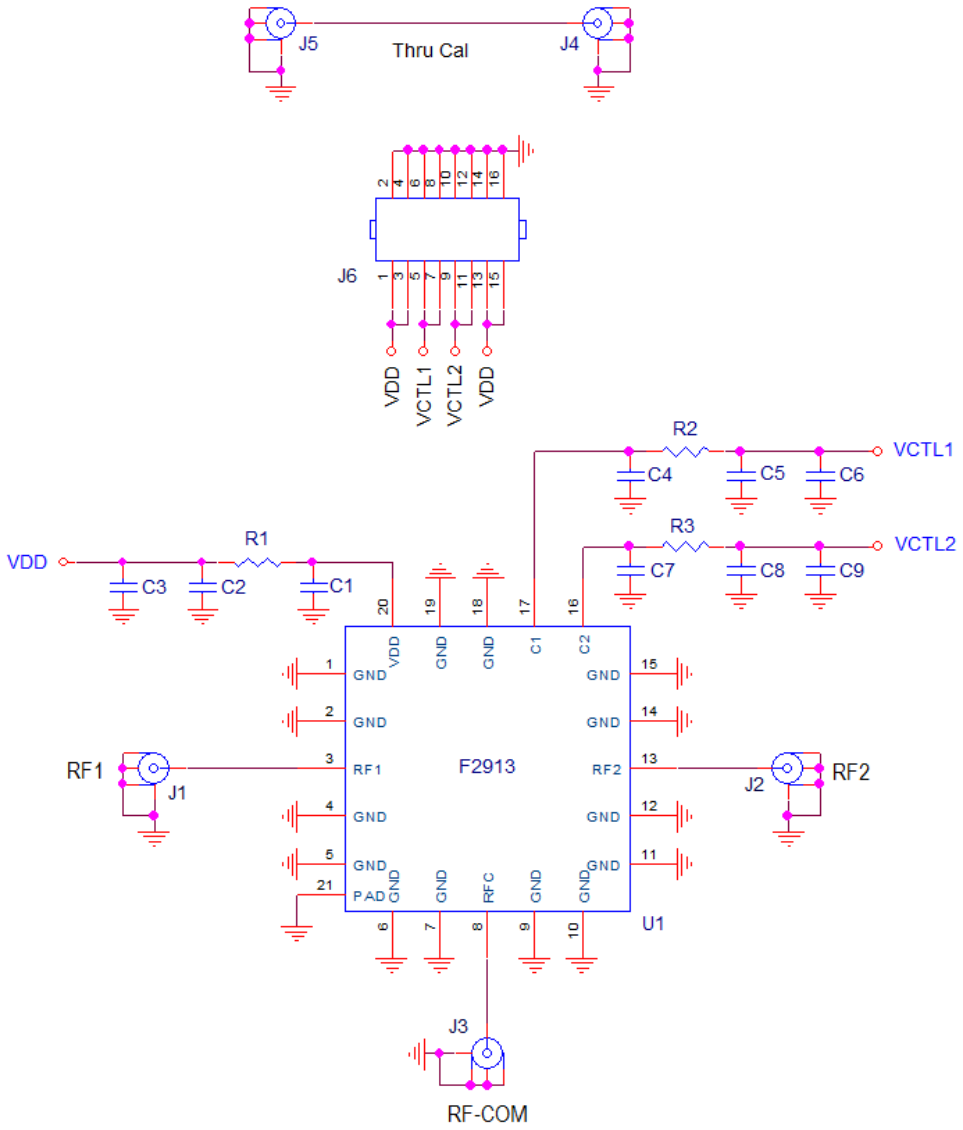


Table 8. Bill of Material (BOM)

Part Reference	QTY	Description	Manufacturer Part #	Manufacturer
C1	1	0.1µF ±10%, 16V X7R Ceramic Capacitor (0402)	GRM155R71C104KA88D	Murata
C2 – C9	0	Not Installed (0402)		
R1 – R3	3	0Ω ±1%, 1/10W, Resistor (0402)	ERJ-2RKF1000X	Panasonic
J1 – J5	5	SMA Edge Mount	142-0761-881	Cinch Connectivity
J6	1	8x2 Vertical Pin Strip Header	961216-6404-AR	Amphenol FCI
U1	1	SP2T Switch 4mm x 4mm QFN	F2913NLGK	IDT
	1	Printed Circuit Board	F2913 PCB	IDT

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Evaluation Kit (EVKit) Operation

External Supply Setup

1. Set up a V_{DD} power supply in the range of +2.7V to +5.5V with the power supply output disabled.
2. Connect the disabled V_{DD} supply connection to J6 pins 1, 3, 13, or 15 and GND to J6 pins 2, 4, 6, 8, 10, 12, 14, or 16.

Logic Control Setup

1. With the logic control lines disabled, set the HIGH and LOW logic levels to satisfy the levels stated in the electrical specifications table.
2. Connect the disabled logic control to J6 VCTRL1 (pins 5 or 7) and VCTRL2 (pins 9 or 11).
3. See Table 7 for the logic truth table. Note that C1 in the table corresponds to VCTRL1 on the EVKIT and C2 corresponds to VCTRL2.

Turn On Procedure

1. Set up the supplies and EVKIT as noted in the External Supply Setup and Logic Control Setup sections above.
2. Enable the V_{DD} supply.
3. Enable the logic control signals.
4. Set the logic settings to achieve the desired Table 7 configuration. Note that external control logic should not be applied without V_{DD} being present.

Turn Off Procedure

1. Set the logic control pins to 0V.
2. Disable the V_{DD} supply.

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Package Drawings

The package outline drawings are appended at the end of this document and are accessible from the link below. The package information is the most current data available.

www.idt.com/document/psc/20-vfqfpn-package-outline-drawing-40-x-40-x-095-mm-body-05mm-pitch-epad-20-x-20-mm-nlg20t1

Marking Diagram



Lines 1 and 2 – Part number
Line 3 “ZE” – Die version
Line 3 “705” – Production period, last digit of year plus workweek
Line 3 “AHG” – Production process

Ordering Information

Orderable Part Number	Package	MSL Rating	Shipping Packaging	Temperature
F2913NLGK	4 × 4 × 0.95 mm 20-VFQFPN	MSL1	Cut Tape	-40°C to +110°C
F2913NLGK8	4 × 4 × 0.95 mm 20-VFQFPN	MSL1	Reel	-40°C to +110°C
F2913EVBI	Evaluation Board			

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Revision History

Revision Date	Description of Change
January 31, 2019	Updated package for correct drawing number
September 29, 2017	Initial release