Description

The F4482 is a 1300MHz to 2800MHz Quad Path TX DVGA outfitted with 100Ω differential inputs and 50Ω single-ended outputs. The device is part of a complete family of VGAs targeting FDD and TDD applications within the 400MHz to 4200MHz frequency range.

Using a single 3.3V power supply and only 500mA of I_{CC}, the F4482 provides four independent transmit paths, each with 28dB typical maximum gain, +34dBm OIP3, +17dBm output P1dB, and 5.7dB NF. Each channel includes a glitch-free digital step attenuator that reduces gain by up to 31.5dB in precise 0.5dB steps.

The F4482 is packaged in an 8 × 8 mm 56-LGA, with matched 100Ω differential input and 50Ω single-ended output impedances for ease of integration into the signal path.

Competitive Advantage

- Combines four independent TX channels consisting of an LPF, LNA, DSA, and Driver in a compact 8 × 8 LGA package
- Low DC power
- High linearity
- High reliability
- Uses Renesas' patented *Zero-Distortion™* and *Glitch-Free™* technologies, providing superior performance and PA damage protection over the entire RF gain range

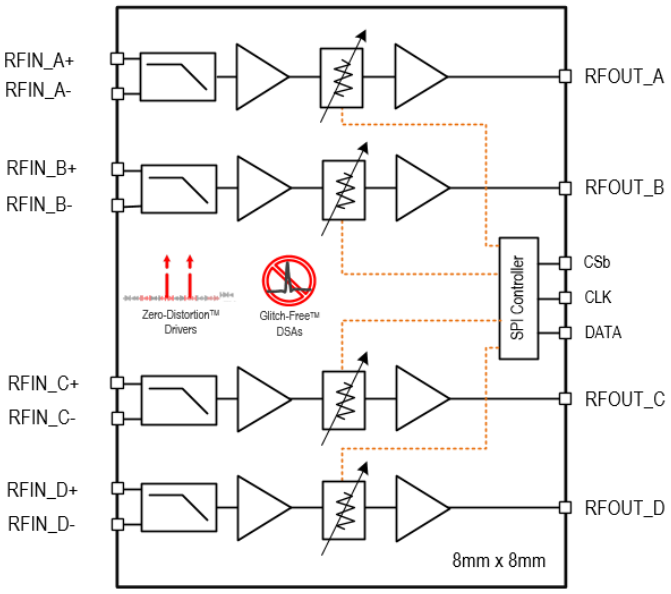
Typical Applications

- 4G and 5G Multi-mode, Multi-carrier Transmitters
- LTE and UMTS/WCDMA Base Stations
- Active Antenna Systems
- Digital Radio

Features

- Independent Quad Channels for FDD TX applications
- RF Range: 1300MHz to 2800MHz
  - F4481: 400MHz to 1100MHz
- 28dB Typical Maximum Gain at 2100MHz
- Precise SPI-Controlled *Glitch-Free™* Gain Adjustment
  - 31.5dB Gain Range with 0.5dB Step Size
- 5.7dB NF at 2100MHz
- +34dBm OIP3 at 2100MHz
- +17dBm Output P1dB at 2100MHz
- 3.3V Supply Voltage
- I_{CC} = 500mA
- 100Ω Differential Input Impedances
- 50Ω Single-ended Output Impedances
- 1.8V and 3.3V Logic Support
- Independent Channel Standby Modes for Power Savings
- Operating Temperature (T_{EP}) Range: -40°C to +105°C
- 8 × 8 mm, 56-LGA package

Block Diagram



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Contents

Pin Assignments....6
Pin Descriptions....7
Absolute Maximum Ratings....9
Recommended Operating Conditions....10
Electrical Characteristics – General....11
Electrical Characteristics – Band 1 (1300MHz to 1700MHz)....14
Electrical Characteristics – Band 2 (1700MHz to 2800MHz)....18
Thermal Characteristics....22
Typical Operating Conditions (TOC)....22
Typical Performance Characteristics....23
Programming....36
Serial Programming....36
Device Register Maps....36
Serial Mode Default Condition....38
Timing Associated with Programming the Serial Registers....38
SPI Timing Intervals....39
Standby Mode Programming....40
Control Pin Interface....41
Evaluation Kit Picture....42
Evaluation Kit / Applications Circuit....43
Evaluation Kit Operation....45
Power Supplies....45
Power Supply Setup....45
Power-On Procedure....45
Power-Off Procedure....45
Startup Condition....45
Default Channel Power On....45
Chip Select (CSb)....45
Standby Mode (STBY)....45
Package Outline Drawings....46
Ordering Information....46
Marking Diagram....46
Revision History....46

List of Figures

Figure 1. Pin Assignments for 8 × 8 × 0.65 mm LGA Package – Top View....6
Figure 2. Gain vs DSA Setting....23
Figure 3. Gain vs Attenuation....23

Figure 4. Gain at DSA = 0dB 23
Figure 5. Gain at DSA = 14dB 23
Figure 6. Gain at DSA = 31.5dB 23
Figure 7. Gain vs Channel (DSA = 0dB) 23
Figure 8. Reverse Isolation vs DSA Setting 24
Figure 9. Reverse Isolation vs Attenuation 24
Figure 10. Reverse Isolation at DSA = 0dB 24
Figure 11. Reverse Isolation at DSA = 14dB 24
Figure 12. Reverse Isolation at DSA = 31.5dB 24
Figure 13. Reverse Isolation vs Channel (DSA = 0dB) 24
Figure 14. Input Return Loss vs DSA Setting 25
Figure 15. Input Return Loss vs Attenuation 25
Figure 16. Input Return Loss at DSA = 0dB 25
Figure 17. Input Return Loss at DSA = 14dB 25
Figure 18. Input Return Loss at DSA = 31.5dB 25
Figure 19. Input Return Loss vs Channel (DSA = 0dB) 25
Figure 20. Output Return Loss vs DSA Setting 26
Figure 21. Output Return Loss vs Attenuation 26
Figure 22. Output Return Loss at DSA = 0dB 26
Figure 23. Output Return Loss at DSA = 14dB 26
Figure 24. Output Return Loss at DSA = 31.5dB 26
Figure 25. Output Return Loss vs Channel (DSA = 0dB) 26
Figure 26. Out of Band Rejection (w.r.t. 1.45GHz) 27
Figure 27. Out of Band Rejection vs Channel (w.r.t. 1.45GHz) 27
Figure 28. Out of Band Rejection (w.r.t. 2.1GHz) 27
Figure 29. Out of Band Rejection vs Channel (w.r.t. 2.1GHz) 27
Figure 30. Out of Band Rejection (w.r.t. 2.1GHz) 27
Figure 31. Out of Band Rejection vs Channel (w.r.t. 2.1GHz) 27
Figure 32. Absolute Error (INL) 28
Figure 33. Absolute Error (INL) vs Channel 28
Figure 34. Step Error (DNL) 28
Figure 35. Step Error (DNL) vs Channel 28
Figure 36. Common Mode Rejection 28
Figure 37. Common Mode Rejection vs Channel 28
Figure 38. Amplitude Imbalance 29
Figure 39. Amplitude Imbalance vs Channel 29
Figure 40. Phase Imbalance 29
Figure 41. Phase Imbalance vs Channel 29
Figure 42. Phase Shift Relative to DSA = 0dB 29
Figure 43. Phase Shift Relative to DSA = 0dB vs Channel 29

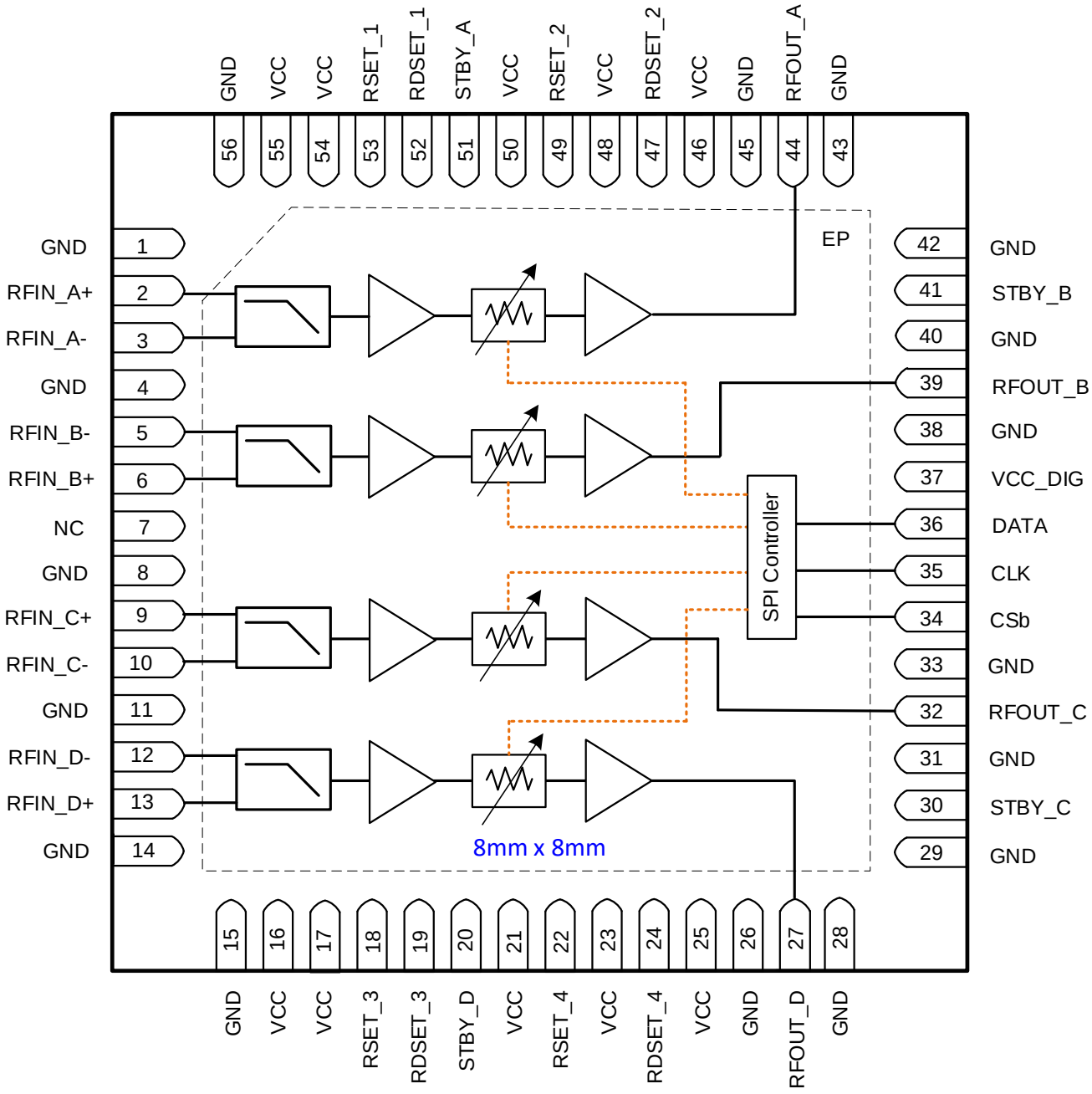
Figure 44. Group Delay at DSA = 0dB 30
Figure 45. Group Delay vs Channel (DSA = 0dB) 30
Figure 46. K Factor 30
Figure 47. Cross Channel vs Channel Group Delay at DSA = 0dB 30
Figure 48. Cross Channel vs Channel Group Delay at DSA = 14dB 30
Figure 49. Cross Channel vs Channel Group Delay at DSA = 28dB 30
Figure 50. Inter/Intra Channel Isolation at DSA = 0dB 31
Figure 51. Supply Current 31
Figure 52. Noise Figure at DSA = 0dB 31
Figure 53. Noise Figure at DSA = 14dB 31
Figure 54. Noise Figure at DSA = 28dB 31
Figure 55. Noise Figure vs Channel (DSA = 0dB) 31
Figure 56. Band 1 OIP3 at DSA = 0dB 32
Figure 57. Band 1 OIP3 at DSA = 4dB 32
Figure 58. Band 1 OIP3 at DSA = 14dB 32
Figure 59. Band 1 OIP3 at DSA = 28dB 32
Figure 60. Band 2 OIP3 at DSA = 0dB 32
Figure 61. Band 2 OIP3 at DSA = 4dB 32
Figure 62. Band 2 OIP3 at DSA = 14dB 33
Figure 63. Band 2 OIP3 at DSA = 28dB 33
Figure 64. Band 1 OIP3 vs Channel (DSA = 0dB) 33
Figure 65. Band 2 OIP3 vs Channel (DSA = 0dB) 33
Figure 66. Band 1 OP1dB at DSA = 0dB 33
Figure 67. Band 1 OP1dB at DSA = 4dB 33
Figure 68. Band 1 OP1dB at DSA = 14dB 34
Figure 69. Band 1 OP1dB at DSA = 28dB 34
Figure 70. Band 2 OP1dB at DSA = 0dB 34
Figure 71. Band 2 OP1dB at DSA = 4dB 34
Figure 72. Band 2 OP1dB at DSA = 14dB 34
Figure 73. Band 2 OP1dB at DSA = 28dB 34
Figure 74. Band 1 OP1dB vs Channel (DSA = 0dB) 35
Figure 75. Band 2 OP1dB vs Channel (DSA = 0dB) 35
Figure 76. Register Bit Map for Each Channel 36
Figure 77. Serial Mode Default Condition Upon Initial Power-Up 38
Figure 78. Timing Diagram Associated with Programming the Serial Register 38
Figure 79. Serial Register Timing Diagram (Timing Spec Intervals are denoted in Blue) 39
Figure 80. Control Pin Interface for Signal Integrity 41
Figure 81. Top View 42
Figure 82. Bottom View 42
Figure 83. Electrical Schematic 43

List of Tables

Table 1. Pin Descriptions....7
Table 2. Absolute Maximum Ratings....9
Table 3. Recommended Operating Conditions....10
Table 4. Electrical Characteristics – General....11
Table 5. Electrical Characteristics – Band 1 (1300MHz to 1700MHz)....14
Table 6. Electrical Characteristics – Band 2 (1700MHz to 2800MHz)....18
Table 7. Package Thermal Characteristics....22
Table 8. Channel Select Truth Table....36
Table 9. DVGA Attenuation Word Truth Table....37
Table 10. SPI Timing Diagram Values for the Serial Mode....39
Table 11. STBY Logic Truth Table....40
Table 12. Bill of Material (BOM)....44

Pin Assignments

Figure 1. Pin Assignments for 8 × 8 × 0.65 mm LGA Package – Top View



Pin Descriptions

Table 1. Pin Descriptions

Number	Name	Description
1, 4, 8, 11, 14, 15, 26, 28, 29, 31, 33, 38, 40, 42, 43, 45, 56	GND	Internally grounded. These pins must be grounded as close to the device as possible.
2	RFIN_A+	Channel A RF differential input. Internally matched to 100Ω. Must use external DC blocks.
3	RFIN_A-	
5	RFIN_B-	Channel B RF differential input. Internally matched to 100Ω. Must use external DC blocks.
6	RFIN_B+	
7	NC	No internal connection. It is highly recommended that these pins be connected to a ground via that is located as close to the pin as possible.
9	RFIN_C+	Channel C RF differential input. Internally matched to 100Ω. Must use external DC blocks.
10	RFIN_C-	
12	RFIN_D-	Channel D RF differential input. Internally matched to 100Ω. Must use external DC blocks.
13	RFIN_D+	
16, 17, 21, 23, 25, 46, 48, 50, 54, 55	V_{CC}	Power Supply. Must place the bypass capacitor as close to the pin as possible.
18	RSET_3	Connect external resistor to GND to optimize amplifier performance. Refer to Table 12, Bill of Materials (BOM).
19	RDSET_3	Connect external resistor to GND to optimize amplifier performance. Refer to Table 12, Bill of Materials (BOM).
20	STBY_D	Standby channel D. With Logic LOW applied to this pin (or if the pin is left unconnected), channel D enters STBY mode and is powered off. With Logic HIGH applied to this pin, channel D is powered on and is fully operational.
22	RSET_4	Connect external resistor to GND to optimize amplifier performance. Refer to Table 12, Bill of Materials (BOM).
24	RDSET_4	Connect external resistor to GND to optimize amplifier performance. Refer to Table 12, Bill of Materials (BOM).
27	RFOUT_D	RF output D internally matched to 50Ω. Must use external DC block.
30	STBY_C	Standby channel C. With Logic LOW applied to this pin (or if the pin is left unconnected), channel C enters STBY mode and is powered off. With Logic HIGH applied to this pin, channel C is powered on and is fully operational.
32	RFOUT_C	RF output C internally matched to 50Ω. Must use external DC block.
34	CSb	Serial Chip Select. CSb pin can be pulled up to V_{CC} and down to GND. 1.8 V and 3.3 V logic compatible.

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Number	Name	Description
35	CLK	Serial Clock Input. 1.8 V and 3.3 V logic compatible.
36	DATA	Data write for the 3-wire serial interface. 1.8V and 3.3V logic compatible.
37	V_{CC_DIG}	Digital Power Supply. Must place the bypass capacitor as close to the pin as possible.
39	RFOUT_B	RF output B internally matched to 50Ω. Must use external DC block.
41	STBY_B	Standby channel B. With Logic LOW applied to this pin (or if the pin is left unconnected), channel B enters STBY mode and is powered off. With Logic HIGH applied to this pin, channel B is powered on and is fully operational.
44	RFOUT_A	RF output A internally matched to 50Ω. Must use external DC block.
47	RDSET_2	Connect external resistor to GND to optimize amplifier performance. Refer to Table 12, Bill of Materials (BOM).
49	RSET_2	Connect external resistor to GND to optimize amplifier performance. Refer to Table 12, Bill of Materials (BOM).
51	STBY_A	Standby channel A. With Logic LOW applied to this pin (or if the pin is left unconnected), channel A enters STBY mode and is powered off. With Logic HIGH applied to this pin, channel A is powered on and is fully operational.
52	RDSET_1	Connect external resistor to GND to optimize amplifier performance. Refer to Table 12, Bill of Materials (BOM).
53	RSET_1	Connect external resistor to GND to optimize amplifier performance. Refer to Table 12, Bill of Materials (BOM).
	– EPAD	Exposed paddle. Internally connected to ground. Solder this exposed paddle to a printed circuit board (PCB) pad that uses multiple ground vias to provide heat transfer out of the device into the PCB ground planes. These multiple ground vias are also required to achieve the specified RF performance.

Absolute Maximum Ratings

The absolute maximum ratings are stress ratings only. Stresses greater than those listed below can cause permanent damage to the device. Functional operation of the F4482 at absolute maximum ratings is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

Table 2. Absolute Maximum Ratings

Parameter	Symbol	Minimum	Maximum	Units
V_{CC} to GND	V_{CC}	-0.3	+3.6	V
DATA, CSb, CLK	V_{CTL}	-0.3	V_{CC} + 0.25	V
STBY	V_{CTL}	-0.3	V_{CC} + 0.25	V
STBY minus V_{CC} voltage (voltage difference)	$V_{STBY-VCC}$		0.3	V
RSET_1, RSET_2, RSET_3, RSET_4 pin maximum output DC current [a]	I_{RSET}		+1	mA
RDSET_1, RDSET_2, RDSET_3, RDSET_4 pin maximum output DC current [a]	I_{RDSET}		+1	mA
RFIN_A, RFIN_B, RFIN_C, RFIN_D to GND externally applied DC voltage	V_{RFIN}	-0.3	+0.3	V
RFOUT_A, RFOUT_B, RFOUT_C, RFOUT_D to GND externally applied DC voltage	V_{RFOUT}	V_{CC} - 0.15	V_{CC} + 0.15	V
RF Input Power (RFIN_A, RFIN_B, RFIN_C, RFIN_D) Applied for 24 Hours Maximum [b]	P_{IN_MAX24}		+17	dBm
Storage Temperature Range	T_{STOR}	-65	+150	°C
Lead Temperature (soldering, 10s)	T_{LEAD}		+260	°C
Electrostatic Discharge – HBM (JEDEC/ESDA JS-001-2012)	V_{ESDHBM}		2000 (Class 2)	V
Electrostatic Discharge – CDM (JEDEC 22-C101F)	V_{ESDCDM}		250 (Class C1)	V

[a] RSET_1, RSET_2, RSET_3, RSET_4, RDSET_1, RDSET_2, RDSET_3, and RDSET_4 pins MUST be connected to ground with resistors; otherwise, damage to the part may result. For suggested resistor values, see Table 12.

[b] Exposure to these maximum RF levels can result in significant VCC current draw due to overdriving the amplifier stages.

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Recommended Operating Conditions

Table 3. Recommended Operating Conditions

Parameter	Symbol	Condition	Minimum	Typical	Maximum	Units
Power Supply Voltage [a]	V_{CC}	All V_{CC} pins	3.15	3.3	3.45	V
Operating Temperature Range	T_{EP}	Exposed Paddle Temperature	-40		+105	°C
Junction Temperature	T_{JMAX}				+125	°C
RF Frequency Range [b]	f_{RF}	Band 1 Tuning	1300		1700	MHz
		Band 2 Tuning	1700		2800	
Maximum CW Input Power	P_{IN_MAX}	Z_S = 100 Ω, Z_L = 50Ω			Note [c]	dBm
RF Input Port Impedance	Z_{RFI}	Differential Impedance		100		Ω
RF Output Port Impedance	Z_{RFO}	Single-ended Impedance		50		Ω

[a] Power-on resets will only occur for VCC < 3V. The device is designed to function with any supply voltage ≥ 3V, although performance may be degraded when operated outside the recommended voltage range.

[b] To optimize RF performance, different matching components might be used as described in the BOM. Using external matching, gain flatness is optimized from either 1300MHz to 1700MHz (band 1) or 1700MHz to 2800MHz (band 2).

[c] Level = Lower of (-7.5dBm + attenuation setting) or 5dBm.

Electrical Characteristics – General

See the F4482 Typical Application Circuit. Unless stated otherwise, specifications apply when operated with V_{CC} = +3.3V, T_{EP} = +25°C, f_{RF} = 2100MHz, STBY_A = STBY_B = STBY_C = STBY_D = HIGH, Z_S = 100Ω differential, Z_L = 50Ω single-ended, maximum gain setting, and output power = 0dBm/tone. EVKit trace and connector losses are de-embedded.

Table 4. Electrical Characteristics – General

Parameter	Symbol	Condition	Minimum	Typical	Maximum	Units
Logic Input HIGH	V_{IH}	Supports both 1.8V and 3.3V logic	*1.07* [a]			V
Logic Input LOW	V_{IL}				*0.63*	V
SPI Logic Current (CSb, CLK, DATA)	I_{CTL}	3.3V Logic	*-5*		*5*	µA
		1.8V Logic	*-5*		*5*	
Standby Logic Current (STBY_A, STBY_B, STBY_C, STBY_D)	I_{IH}, I_{IL}	3.3V Logic	*5*		*50*	µA
		1.8V Logic	*5*		*30*	
Supply Current [b]	I_{CC_4}	Four channels on		490	*600*	mA
	I_{CC_3}	Three channels on		374		
	I_{CC_2}	Two channels on		252		
	I_{CC_1}	One channel on		135		
Standby Current	I_{CC_STBY}	All channels off		13	*18*	mA
Power ON Switching Time	t_{ON}	50% STBY to RF output settled to within ±0.5dB			1	µs
Power OFF Switching Time	t_{OFF}	50% STBY to 35 dBc reduction of output power			1	µs
Lineup Out-of-Band Rejection at Max Gain	$f_{REJECTION}$	Total gain variation over f_{RF} = 1300MHz to 1700MHz. Referred to f_{RF} = 1450MHz. DSA 0dB attenuation.			3	dBc
		Total gain variation over f_{RF} = 1700MHz to 2800MHz. Referred to f_{RF} = 2100MHz. DSA 0dB attenuation.			3	
		6GHz < f_{RF} < 11.75GHz. Referred to f_{RF} = 2100MHz. DSA 0dB attenuation.	50			
Gain Settling Time [c]	G_{ST}	Any 2dB step in the 0dB to 31.5dB range. 50% of CSb to 1% / 99% RF.		0.4	1	µs

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Parameter	Symbol	Condition		Minimum	Typical	Maximum	Units
DSA Adjustment Range	G_{RANGE}				31.5		dB
DSA Step Resolution	G_{STEP}	LSB			0.5		dB
Adjacent State Attenuator Glitching	$ATTN_G$	DSA step: 5.5dB to 6dB.			0.7		dB
		DSA step: 6dB to 5.5dB.			0.7		
		DSA step: 11.5dB to 12dB.			0.7		
		DSA step: 12dB to 11.5dB.			0.7		
		DSA step: 17.5dB to 18dB.			0.7		
		DSA step: 18dB to 17.5dB.			0.7		
		DSA step: 23.5dB to 24dB.			0.7		
		DSA step: 24dB to 23.5dB.			0.7		
		DSA step: 29.5dB to 30dB.			1		
		DSA step: 30dB to 29.5dB.			1		
		All Other 0.5dB DSA steps.			0.6		
		All Other 2dB DSA steps.			1		
Common Mode Rejection	CMR	f_{RF} = 1300MHz to 1800MHz		30			dB
		f_{RF} = 1800MHz to 2800MHz		20			
Amplitude Imbalance	$IMBAL_{AMP}$	Measures RFIN- to RFOUT and compares RFOUT to RFIN+ amplitude.	Worst Case Over f_{RF} = 1300MHz to 1800MHz		0.25		dB
			Worst Case Over f_{RF} = 1800MHz to 2800MHz		0.5		
Phase Imbalance	$IMBAL_{PH}$	Measures RFIN- to RFOUT and compares RFOUT to RFIN+ phase. Deviation is from ideal 180 degrees	Worst Case Over f_{RF} = 1300MHz to 1800MHz		0.75		deg
			Worst Case Over f_{RF} = 1800MHz to 2800MHz		4		

Parameter	Symbol	Condition	Minimum	Typical	Maximum	Units
Serial Clock Speed	f_{CLK}				*50*	MHz
CSb to First Serial Clock Rising Edge	t_{LS}	SPI 3 wire bus. 50% of CSb falling edge to 50% of CLK rising edge	*10*			ns
Serial Data Hold Time	t_H	SPI 3 wire bus. 50% of CLK rising edge to 50% of DATA falling edge	*10*			ns
Final Serial Clock Rising Edge to CSb	t_{LCS}	SPI 3 wire bus. 50% of CLK rising edge to 50% of CSb rising edge	*10*			ns
Stability K Factor	K_{FACTOR}	T_{EP} = -40˚C to +105˚C 10MHz to 9GHz	1			

[a] Specifications in the minimum/maximum columns that are shown in bold italics are guaranteed by test. Specifications in these columns that are not shown in bold italics are confirmed by design characterization.

[b] For input signal power level equal to P1dB, expect DC current to increase above typical value.

[c] Timing is measured after SPI programming is completed (data latched with CSb = HIGH).

Electrical Characteristics – Band 1 (1300MHz to 1700MHz)

See the F4482 Typical Application Circuit. Unless stated otherwise, specifications apply when operated with V_{CC} = +3.3V, T_{EP} = +25°C, f_{RF} = 1450MHz, STBY_A = STBY_B = STBY_C = STBY_D = HIGH, Z_S = 100Ω differential, Z_L = 50Ω single-ended, maximum gain setting, and output power = 0dBm/tone. EVKit trace and connector losses are de-embedded.

Table 5. Electrical Characteristics – Band 1 (1300MHz to 1700MHz)

Parameter	Symbol	Condition	Minimum	Typical	Maximum	Units
RF Input Return Loss	RL_{IN}		13[a]	19		dB
RF Output Return Loss	RL_{OUT}		12	18		dB
Maximum Gain	G_{MAX}	DSA = 0dB	*26*	28	*30*	dB
Mid-Range Gain	G_{MID}	DSA = 14dB	*11.5*	14	*16*	dB
Minimum Gain	G_{MIN}	DSA = 31.5dB	*-6*	-3.5	*-1.5*	dB
Gain Variation Over Temperature	G_{TEMP}	DSA = 0dB Over T_{EP} = -40°C to +105°C, and relative to 25°C		+0.8 / -1.5		dB
		DSA = 14dB Over T_{EP} = -40°C to +105°C, and relative to 25°C		+0.8 / -1.1		
Gain Flatness	G_{FLAT}	Any 400MHz BW		0.4		dB
Gain Ripple	G_{RIPPLE}	In any 20MHz range		0.2		dB
Intra-die Channel-to-Channel Differences in Gain	G_A - G_B	Worst case difference in Gain for any 2dB step over the 0dB to 30dB attenuation range (with channels A and B both set to identical DSA attenuation levels).		0.2		dB
Reverse Isolation	G_{REV}	DSA = 0dB		-47		dB
		DSA = 31.5dB		-73		
Intra-die Channel Isolation [b]	$ISOL_{A-B}$	Any RF input/output combination involving channel A paired with channel B DSA 0dB Attenuation	50	60		dB
Inter-die Channel Isolation [b]	$ISOL_{B-C}$	Any RF input/output combination involving channel B (die 1) paired with channel C (die 2). DSA 0dB Attenuation	50	60		dB

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Parameter	Symbol	Condition		Minimum	Typical	Maximum	Units
Group Delay in Passband	τ	f_{RF} = 1300MHz to 1700MHz			1	2	ns
Group Delay Ripple	τ_{RIPPLE}	Any 280MHz band within f_{RF} = 1300MHz to 1700MHz			0.1	1	ns
Intra-die Channel-to-Channel Differences in Group Delay	$\tau_A - \tau_B$	Worst case difference in Group Delay for any 2dB step over the 0dB to 30dB attenuation range (with channels A and B both set to identical DSA attenuation levels).			0.1		ns
Cross Channel Group Delay in Passband vs. Channel Group Delay in Passband	$\tau_{XCHANNEL} - \tau$	f_{RF} = 1300MHz to 1700MHz Worst case cross-channel leakage combinations (A to B) - B; (B to A) - A; (B to C) - C; (C to B) - B; (C to D) - D; (D to C) - C	DSA = 0dB		0.6		ns
			DSA = 14dB		0.4		
			DSA = 28dB		0.4		
Step Error (DNL)	$ERROR_{STEP}$	Maximum error between adjacent steps			±0.1		dB
Absolute Error (INL)	$ERROR_{ABS}$	Over attenuation range referenced to maximum gain state			Note [c]		dB
Phase Shift Over Any 5ºC Temperature Change Over the -40ºC to 105ºC Range	$\Phi_{\Delta Temp\ at\ 0dB}$	DSA 0dB Attenuation			0.5		deg
	$\Phi_{\Delta Temp\ at\ 14dB}$	DSA 14dB Attenuation			0.5		
	$\Phi_{\Delta Temp\ at\ 28dB}$	DSA 28dB Attenuation			0.5		
Phase Shift Between Startups	$\Phi_{ON\text{-}OFF\text{-}ON}$	Channel A or Channel B Phase Shifts. Measuring “On State” phase shifts occurring over time as the device is powered on/off via STBY mode or via PORs (power-on resets).				2	
	$[\Phi_A - \Phi_B]_{ON\text{-}OFF\text{-}ON}$	Channel A - Channel B Phase Shifts. Measuring “On State” phase shifts occurring over time as the device is powered on/off via STBY mode or via PORs (power-on resets).				10	
Phase Shift Between Any 2dB Step	$\Phi_{2dB\ Step}$	Worst case, any 2dB step			1.2		deg

Parameter	Symbol	Condition		Minimum	Typical	Maximum	Units
Phase Shift Between Any 8dB Step	$\Phi_{8dB\ Step}$	Worst case, any 8dB step			5		deg
Phase Shift Relative to 0dB Attenuation State	$\Phi_{\Delta MAX}$	DSA 31.5dB Attenuation			4.5		deg
	$\Phi_{\Delta MID}$	DSA 14dB Attenuation			1.7		
Intra-die Channel-to-Channel Differences in Phase	$\Phi_A - \Phi_B$	$\Phi_{A\ @\ 16dB} - \Phi_{B\ @\ 16dB}$ Worst case difference in phase with channels A and B both set to DSA = 16dB attenuation levels.			2.5		deg
		$[\Phi_{A\ @\ XdB} - \Phi_{B\ @\ XdB}] - [\Phi_{A\ @\ 16dB} - \Phi_{B\ @\ 16dB}]$ Worst case difference in phase between the 16dB DSA attenuation case and any other state when the DSAs are set to XdB. X = 16 ± 2N, where N is an integer ranging from 1 to 8.			0.2		
Noise Figure at Room (25˚C) [d]	NF_{ROOM}	T_{EP} = 25˚C	DSA = 0dB		5.2	6.6	dB
			DSA = 14dB		8.4		
			DSA = 28dB		20		
Noise Figure at Hot (105˚C) [d]	NF_{HOT}	T_{EP} = 105˚C	DSA = 0dB		6.7		dB
			DSA = 14dB		10.5		
			DSA = 28dB		22		
Noise Figure at Cold (-40˚C) [d]	NF_{COLD}	T_{EP} = -40˚C	DSA = 0dB		4		dB
			DSA = 14dB		7		
			DSA = 28dB		18.5		

Parameter	Symbol	Condition	Minimum	Typical	Maximum	Units
Output Third Order Intercept Point [d]	OIP3	DSA = 0dB T_{EP} = 105˚C P_{OUT} = 0dBm / tone 5MHz tone separation		36		dBm
		DSA = 4dB T_{EP} = 105˚C P_{OUT} = 0dBm / tone 5MHz tone separation		36		
		DSA = 14dB T_{EP} = 25˚C P_{OUT} = -3dBm / tone 5MHz tone separation	28.5	34		
		DSA = 28dB T_{EP} = -40˚C P_{OUT} = -13dBm / tone 5MHz tone separation		20.5		
Output 1dB Compression Point [d]	OP1dB	DSA = 0dB, T_{EP} = 105˚C		17		dBm
		DSA = 4dB, T_{EP} = 105˚C		16.5		
		DSA = 14dB, T_{EP} = 25˚C	12.5	14.5		
		DSA = 28dB, T_{EP} = -40˚C		0.6		

[a] Specifications in the minimum/maximum columns that are shown in ***bold italics*** are guaranteed by test. Specifications in these columns that are not shown in bold italics are confirmed by design characterization.

[b] Signal applied to RFIN_X. Measure desired signal at RFOUT_X and compare to undesired leakage signal level at RFOUT_Y.

[c] Absolute Error = +[0.1 + 0.05*(DSA Attenuator Setting)].

[d] Measured by terminating one differential RFIN port to 50Ω load and applying RF signal to second RFIN port.

Electrical Characteristics – Band 2 (1700MHz to 2800MHz)

See the F4482 Typical Application Circuit. Unless stated otherwise, specifications apply when operated with V_{CC} = +3.3V, T_{EP} = +25°C, f_{RF} = 2100MHz, STBY_A = STBY_B = STBY_C = STBY_D = HIGH, Z_S = 100Ω differential, Z_L = 50Ω single-ended, maximum gain setting, and output power = 0dBm/tone. EVKit trace and connector losses are de-embedded.

Table 6. Electrical Characteristics – Band 2 (1700MHz to 2800MHz)

Parameter	Symbol	Condition	Minimum	Typical	Maximum	Units
RF Input Return Loss	RL_{IN}		8[a]	10		dB
RF Output Return Loss	RL_{OUT}		11.5	19		dB
Maximum Gain	G_{MAX}	DSA 0dB Attenuation	*25.5*	28	*29*	dB
Mid-Range Gain	G_{MID}	DSA 14dB Attenuation	*11*	13.5	*16*	dB
Minimum Gain	G_{MIN}	DSA 31.5dB Attenuation	*-6.5*	-4	*-2*	dB
Gain Variation Over Temperature	G_{TEMP}	DSA 0dB Attenuation Over T_{EP} = -40°C to +105°C, and relative to 25°C		+1 / -1.25		dB
		DSA 14dB Attenuation Over T_{EP} = -40°C to +105°C, and relative to 25°C		+0.8/ -1.1		
Gain Flatness	G_{FLAT}	Any 400MHz BW		0.4		dB
		Any 800MHz BW		0.8		
Gain Ripple	G_{RIPPLE}	In any 20MHz range		0.2		dB
Intra-die Channel-to-Channel Differences in Gain	G_A - G_B	Worst case difference in Gain for any 2dB step over the 0dB to 30dB attenuation range (with channels A and B both set to identical DSA attenuation levels).		0.2		dB
Reverse Isolation	G_{REV}	DSA 0dB Attenuation		-47		dB
		DSA 31.5dB Attenuation		-78		
Intra-die Channel Isolation [b]	$ISOL_{A-B}$	Any RF input/output combination involving channel A paired with channel B DSA 0dB Attenuation	45	50		dB
Inter-die Channel Isolation [b]	$ISOL_{B-C}$	Any RF input/output combination involving channel B (die 1) paired with channel C (die 2). DSA 0dB Attenuation	50	55		dB

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Parameter	Symbol	Condition		Minimum	Typical	Maximum	Units
Group Delay in Passband	τ	f_{RF} = 1700MHz to 2800MHz			1	2	ns
Group Delay Ripple	τ_{RIPPLE}	Any 280MHz band within f_{RF} = 1700MHz to 2800MHz			0.1	1	ns
Cross Channel Group Delay in Passband vs. Channel Group Delay in Passband	$\tau_{XCHANNEL} - \tau$	f_{RF} = 170MHz to 2800MHz Worst case cross-channel leakage combinations (A to B) - B; (B to A) - A; (B to C) - C; (C to B) - B; (C to D) - D; (D to C) - C	DSA = 0dB		0.6		ns
			DSA = 14dB		0.4		
			DSA = 28dB		0.4		
Intra-die Channel-to-Channel Differences in Group Delay	$\tau_A - \tau_B$	Worst case difference in Group Delay for any 2dB step over the 0dB to 30dB attenuation range (with channels A and B both set to identical DSA attenuation levels).			0.1		ns
Step Error (DNL)	$ERROR_{STEP}$	Maximum error between adjacent steps			± 0.1		dB
Absolute Error (INL)	$ERROR_{ABS}$	Over attenuation range referenced to maximum gain state			Note [c]		dB
Phase Shift Over Any 5ºC Temperature Change Over the -40ºC to 105ºC Range	$\Phi_{\Delta Temp\ at\ 0dB}$	DSA 0dB Attenuation			0.5		deg
	$\Phi_{\Delta Temp\ at\ 14dB}$	DSA 14dB Attenuation			0.5		
	$\Phi_{\Delta Temp\ at\ 31.5dB}$	DSA 31.5dB Attenuation			0.5		
Phase Shift Between Startups	$\Phi_{ON-OFF-ON}$	Channel A or Channel B Phase Shifts. Measuring “On State” phase shifts occurring over time as the device is powered on/off via STBY mode or via PORs (power on resets).				2	deg
	$[\Phi_A - \Phi_B]_{ON-OFF-ON}$	Channel A - Channel B Phase Shifts. Measuring “On State” phase shifts occurring over time as the device is powered on/off via STBY mode or via PORs (power on resets).				10	
Phase Shift Between Any 2dB Step	$\Phi_{2dB\ Step}$	Worst case, any 2dB step.			1.2		deg

Parameter	Symbol	Condition		Minimum	Typical	Maximum	Units
Phase Shift Between Any 8dB Step	$\Phi_{8dB\ Step}$	Worst case 8dB step			5		deg
Phase Shift Relative to 0dB Attenuation State	$\Phi_{\Delta MAX}$	DSA 31.5dB Attenuation			8.5		deg
	$\Phi_{\Delta MID}$	DSA 14dB Attenuation			2.7		
Intra-die Channel-to-Channel Differences in Phase	$\Phi_A - \Phi_B$	$\Phi_{A\ @\ 16dB} - \Phi_{B\ @\ 16dB}$ Worst case difference in phase with channels A and B both set to DSA = 16dB attenuation levels.			2.5		deg
		$[\Phi_{A\ @\ XdB} - \Phi_{B\ @\ XdB}] - [\Phi_{A\ @\ 16dB} - \Phi_{B\ @\ 16dB}]$ Worst case difference in phase between the 16dB DSA attenuation case and any other state when the DSAs are set to XdB. X = 16 ± 2N, where N is an integer ranging from 1 to 8.			0.2		deg
Noise Figure at Room (25˚C) [d]	NF_{ROOM}	T_{EP} = 25˚C	DSA = 0dB		5.7	7.1 [a]	dB
			DSA = 14dB		9		
			DSA = 28dB		20.4		
Noise Figure at Hot (105˚C) [d]	NF_{HOT}	T_{EP} = 105˚C	DSA = 0dB		6.6		dB
			DSA = 14dB		10.6		
			DSA = 28dB		22		
Noise Figure at Cold (-40˚C) [d]	NF_{COLD}	T_{EP} = -40˚C	DSA = 0dB		4.4		dB
			DSA = 14dB		7.6		
			DSA = 28dB		19		
Output Third Order Intercept Point with DSA Set to 0dB Attenuation [d]	$OIP3_{0dB\ Attn}$	DSA = 0dB T_{EP} = 105˚C P_{OUT} = 0dBm / tone 5MHz tone separation	f = 1.8GHz		34		dBm
			f = 2.1GHz		35		
			f = 2.6GHz		31		
Output Third Order Intercept Point with DSA Set to 4dB Attenuation [d]	$OIP3_{4dB\ Attn}$	DSA = 4dB T_{EP} = 105˚C P_{OUT} = 0dBm / tone 5MHz tone separation	f = 1.8GHz		34		dBm
			f = 2.1GHz		33.5		
			f = 2.6GHz		30.5		

Parameter	Symbol	Condition		Minimum	Typical	Maximum	Units
Output Third Order Intercept Point with DSA Set to 14dB Attenuation [d]	$OIP3_{14dB\ Attn}$	DSA = 14dB T_{EP} = 25˚C P_{OUT} = -3dBm / tone 5MHz tone separation	f = 1.8GHz		31		dBm
			f = 2.1GHz		31.5		
			f = 2.6GHz		32		
Output Third Order Intercept Point with DSA Set to 28dB Attenuation [d]	$OIP3_{28dB\ Attn}$	DSA = 28dB T_{EP} = -40˚C P_{OUT} = -13dBm / tone 5MHz tone separation	f = 1.8GHz		20		dBm
			f = 2.1GHz		18.5		
			f = 2.6GHz		16.5		
Output 1dB Compression Point with DSA Set to 0dB Attenuation [d]	$OP1dB_{0dB\ Attn}$	DSA = 0dB T_{EP} = 105˚C	f = 1.8GHz		16.5		dBm
			f = 2.1GHz		16		
			f = 2.6GHz		15		
Output 1dB Compression Point with DSA Set to 4dB Attenuation [d]	$OP1dB_{4dB\ Attn}$	DSA = 4dB T_{EP} = 105˚C	f = 1.8GHz		16.5		dBm
			f = 2.1GHz		16		
			f = 2.6GHz		15		
Output 1dB Compression Point with DSA Set to 14dB Attenuation [d]	$OP1dB_{14dB\ Attn}$	DSA = 14dB T_{EP} = 25˚C	f = 1.8GHz	12.5	14.6		dBm
			f = 2.1GHz	12	14		
			f = 2.6GHz	12	14		
Output 1dB Compression Point with DSA Set to 28dB Attenuation [d]	$OP1dB_{28dB\ Attn}$	DSA = 28dB T_{EP} = -40˚C	f = 1.8GHz		0.9		dBm
			f = 2.1GHz		-0.4		
			f = 2.6GHz		-0.7		

[a] Specifications in the minimum/maximum columns that are shown in ***bold italics*** are guaranteed by test. Specifications in these columns that are not shown in bold italics are confirmed by design characterization.

[b] Signal applied to RFIN_X. Measure desired signal at RFOUT_X and compare to undesired leakage signal level at RFOUT_Y.

[c] Absolute Error = +[0.1 + 0.05*(DSA Attenuator Setting)].

[d] Measured by terminating one differential RFIN port to 50Ω load and applying RF signal to second RFIN port.

Thermal Characteristics

Table 7. Package Thermal Characteristics

Parameter	Symbol	Value	Units
Junction to Ambient Thermal Resistance	θ_{JA}	26.89	°C/W
Junction to Case Thermal Resistance (Case is defined as the exposed paddle)	$\theta_{JC\text{-}BOT}$	3.33	°C/W
Moisture Sensitivity Rating (Per J-STD-020)		MSL 3	

Typical Operating Conditions (TOC)

Unless otherwise noted, for the TOC graphs on the following pages, the following conditions apply:

- Vcc = 3.3V
- Z_S = 100Ω Differential
- Z_L = 50Ω Single Ended
- f_{RF} = 1.45GHz (set 1)
- f_{RF} = 2.1GHz (set 2)
- T_{EP} = +25°C
- STBY_A = STBY_B = STBY_C = STBY_D = HIGH (All channels enabled)
- P_{OUT} = 0dBm / Tone unless otherwise specified for multi-tone tests
- 5MHz Tone Spacing
- Gain setting = Maximum Gain
- All temperatures are referenced to the exposed paddle
- Evaluation Kit traces and connector losses are de-embedded

Typical Performance Characteristics

Figure 2. Gain vs DSA Setting

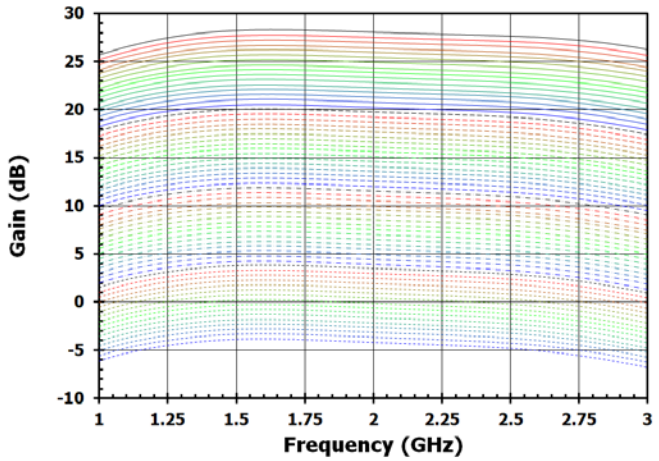


Figure 3. Gain vs Attenuation

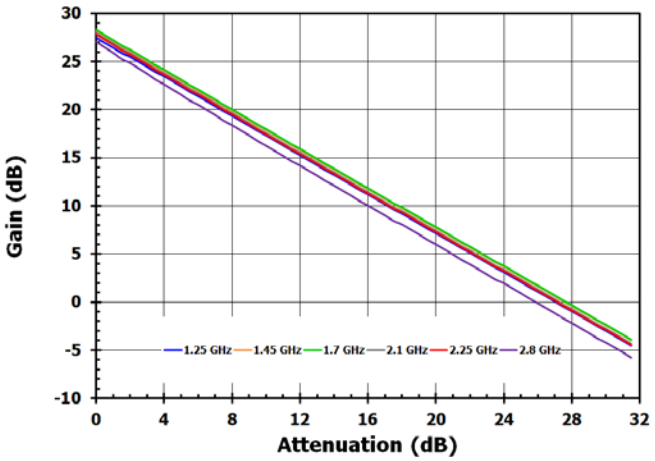


Figure 4. Gain at DSA = 0dB

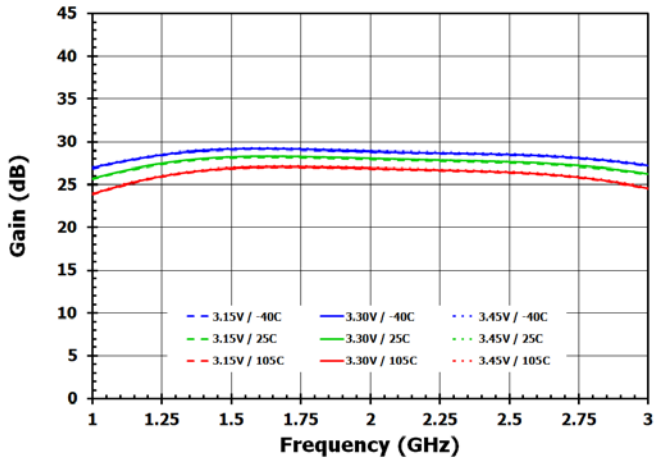


Figure 5. Gain at DSA = 14dB

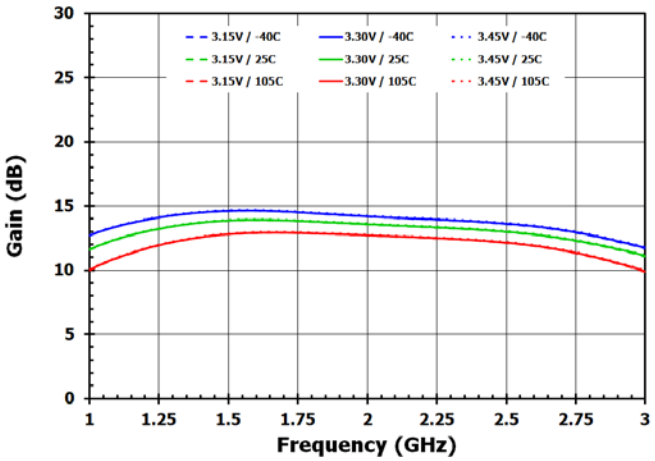


Figure 6. Gain at DSA = 31.5dB

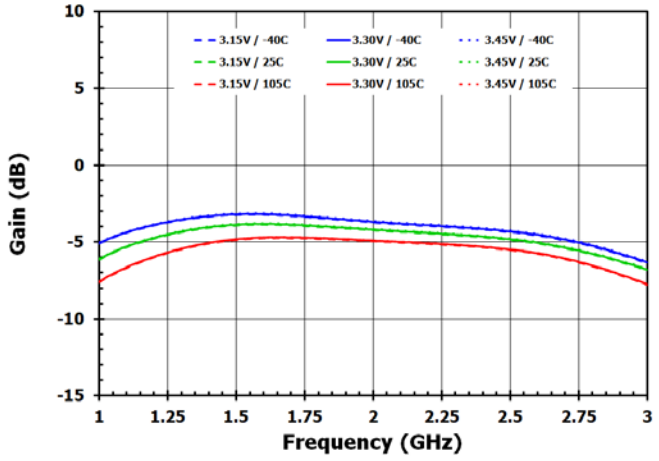
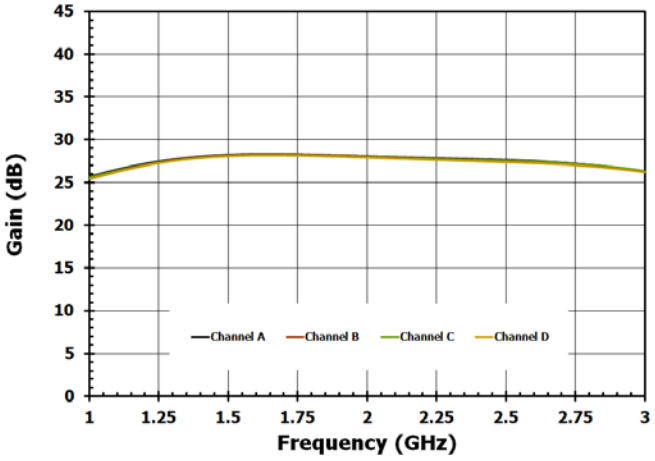


Figure 7. Gain vs Channel (DSA = 0dB)



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Figure 8. Reverse Isolation vs DSA Setting

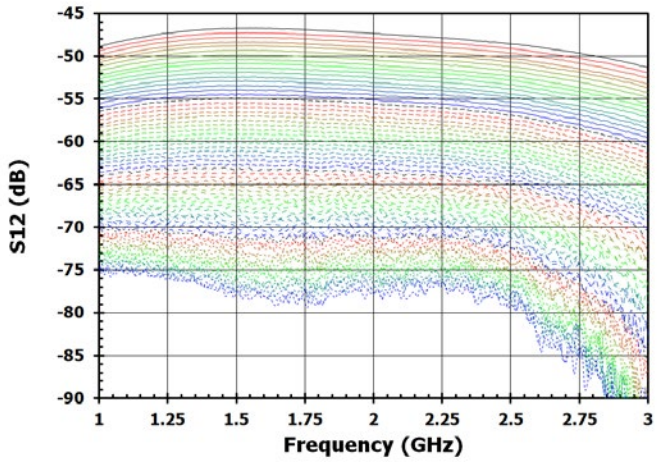


Figure 9. Reverse Isolation vs Attenuation

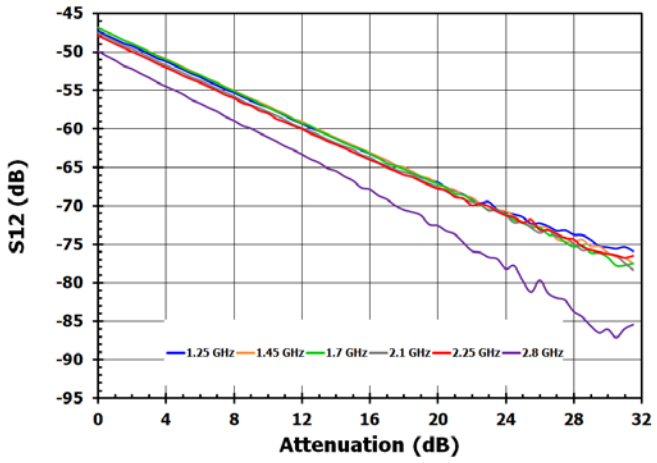


Figure 10. Reverse Isolation at DSA = 0dB

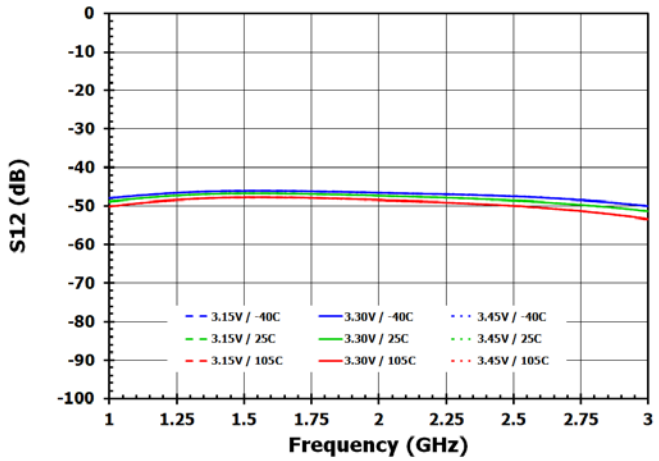


Figure 11. Reverse Isolation at DSA = 14dB

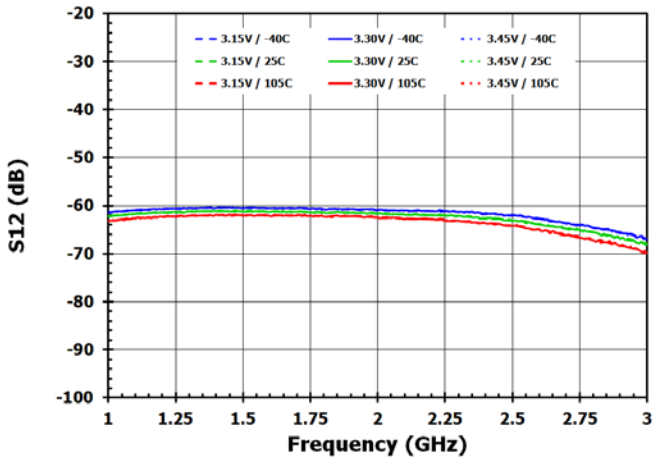


Figure 12. Reverse Isolation at DSA = 31.5dB

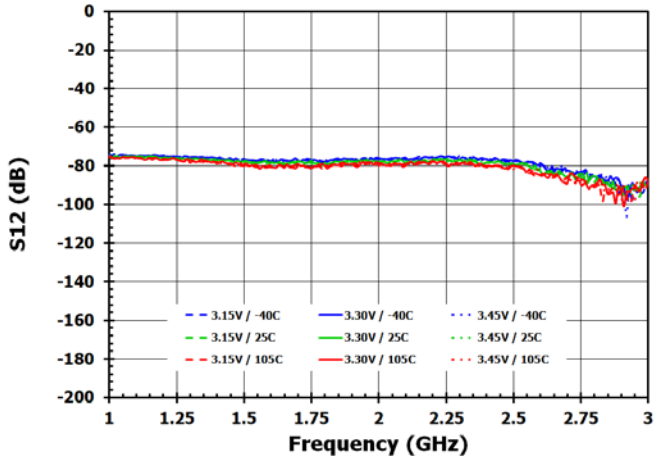


Figure 13. Reverse Isolation vs Channel (DSA = 0dB)

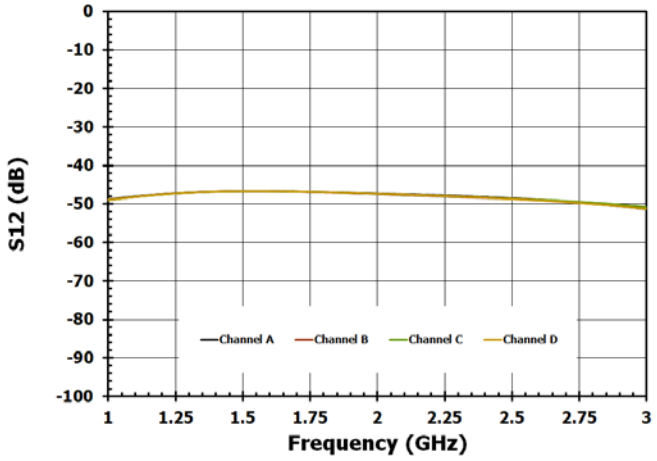


Figure 14. Input Return Loss vs DSA Setting

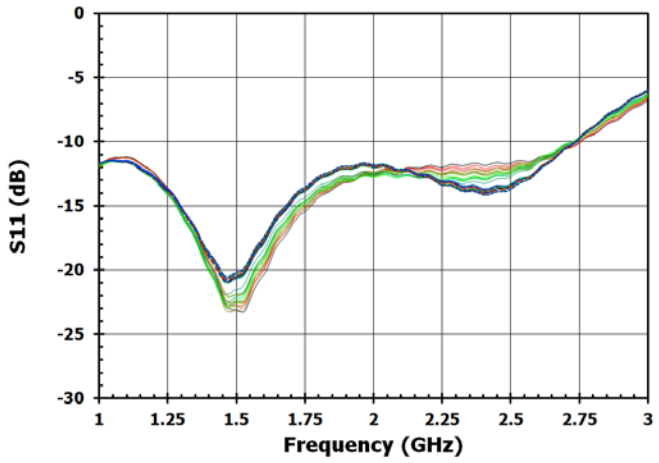


Figure 15. Input Return Loss vs Attenuation

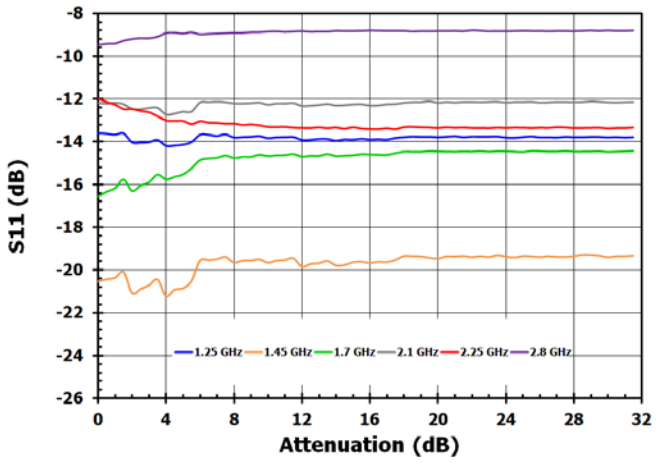


Figure 16. Input Return Loss at DSA = 0dB

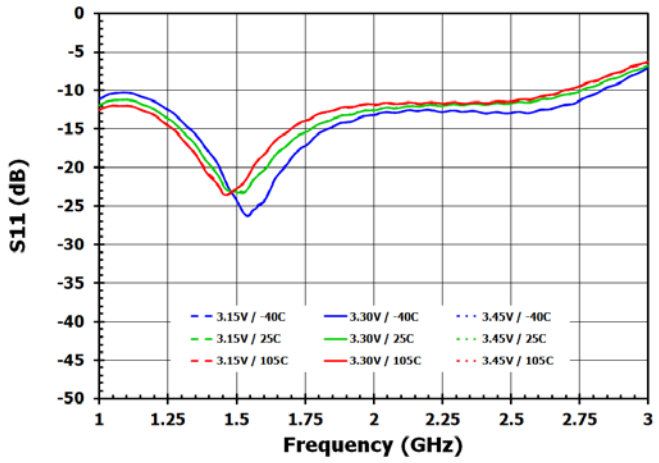


Figure 17. Input Return Loss at DSA = 14dB

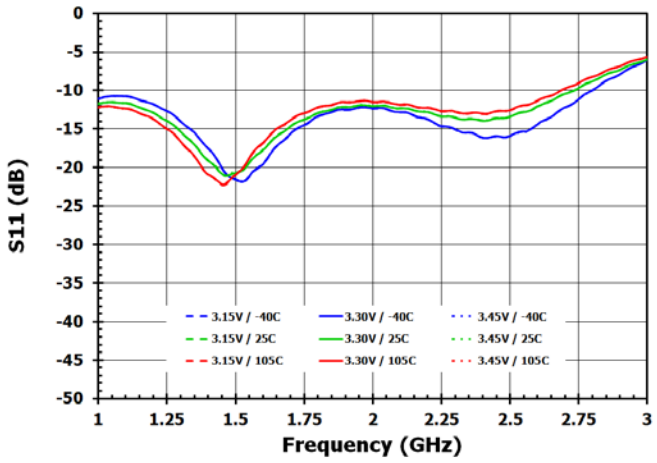


Figure 18. Input Return Loss at DSA = 31.5dB

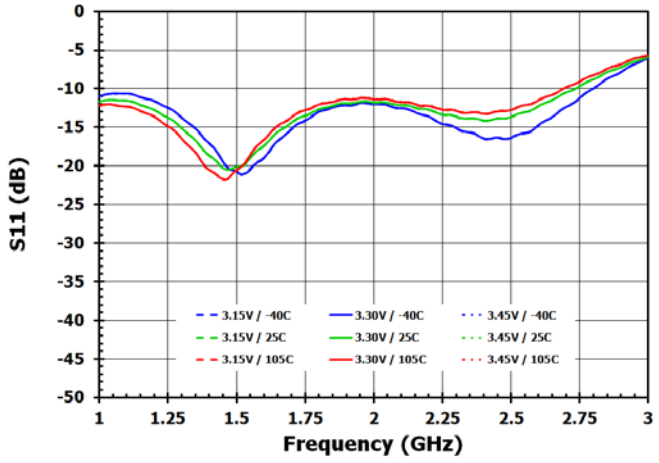


Figure 19. Input Return Loss vs Channel (DSA = 0dB)

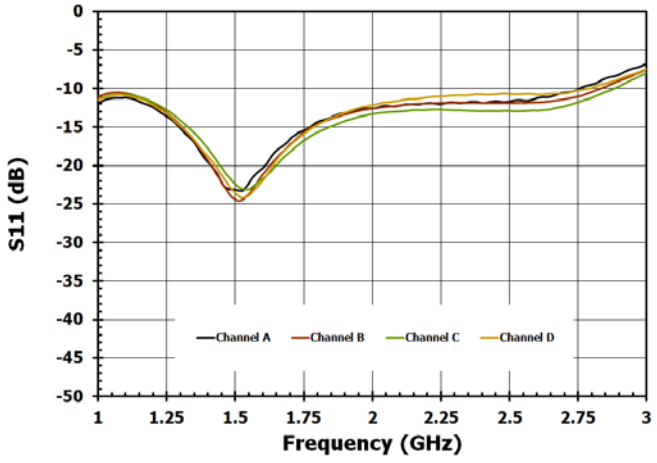


Figure 20. Output Return Loss vs DSA Setting

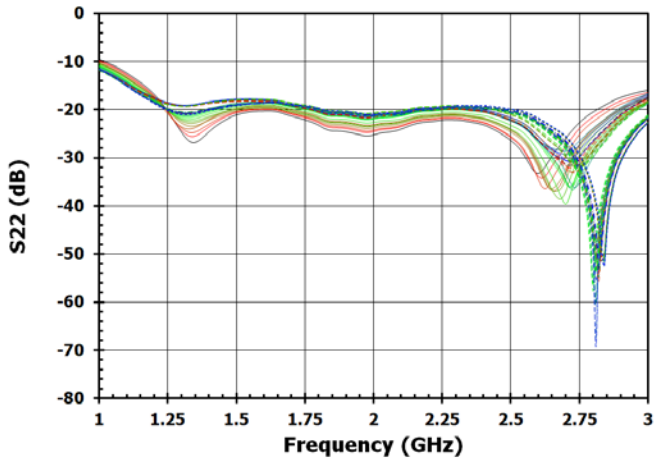


Figure 21. Output Return Loss vs Attenuation

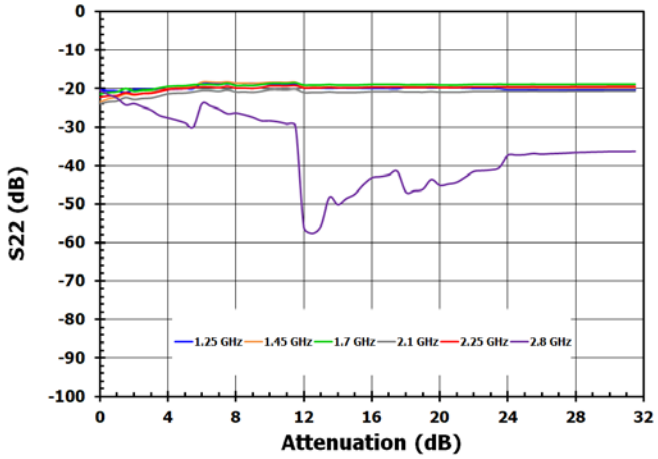


Figure 22. Output Return Loss at DSA = 0dB

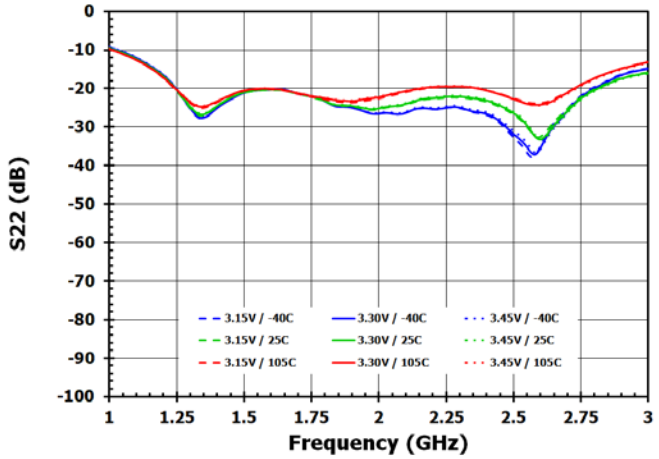


Figure 23. Output Return Loss at DSA = 14dB

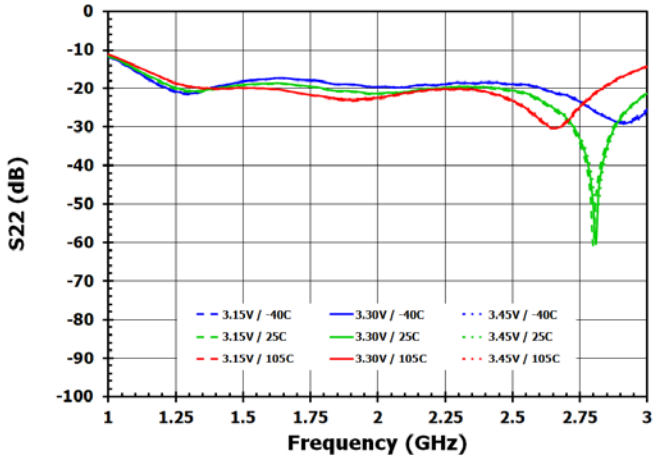


Figure 24. Output Return Loss at DSA = 31.5dB

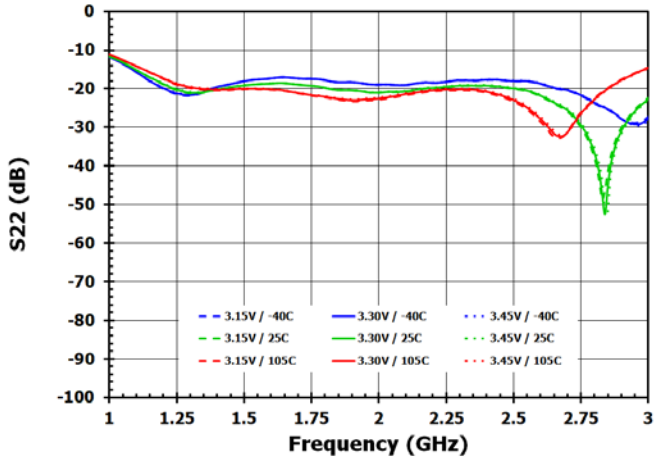


Figure 25. Output Return Loss vs Channel (DSA = 0dB)

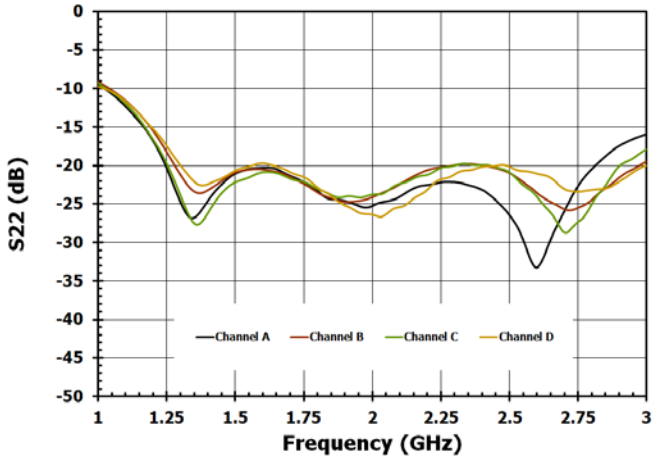


Figure 26. Out of Band Rejection (w.r.t. 1.45GHz)

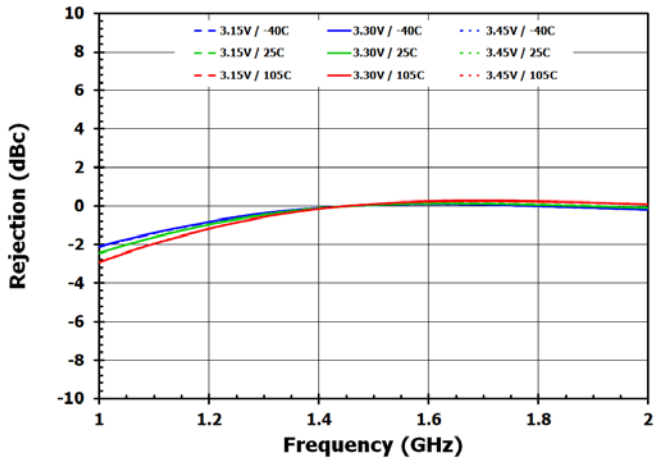


Figure 27. Out of Band Rejection vs Channel (w.r.t. 1.45GHz)

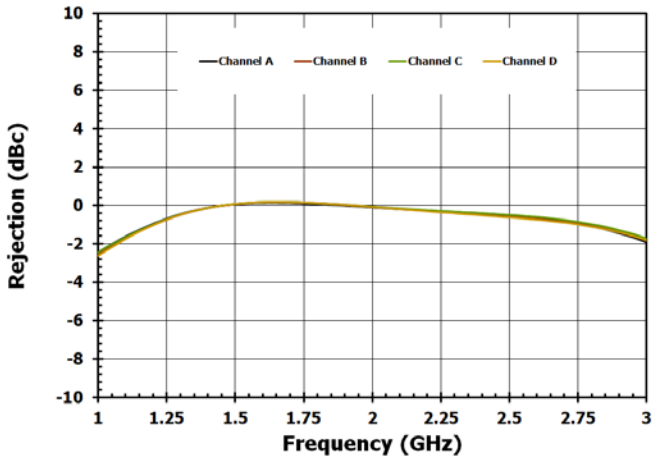


Figure 28. Out of Band Rejection (w.r.t. 2.1GHz)

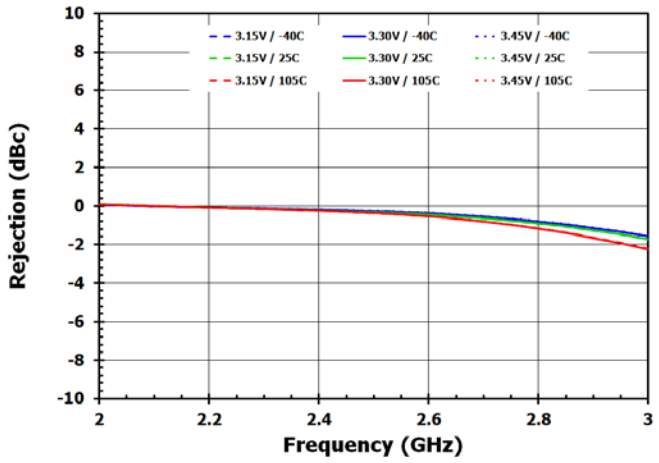


Figure 29. Out of Band Rejection vs Channel (w.r.t. 2.1GHz)

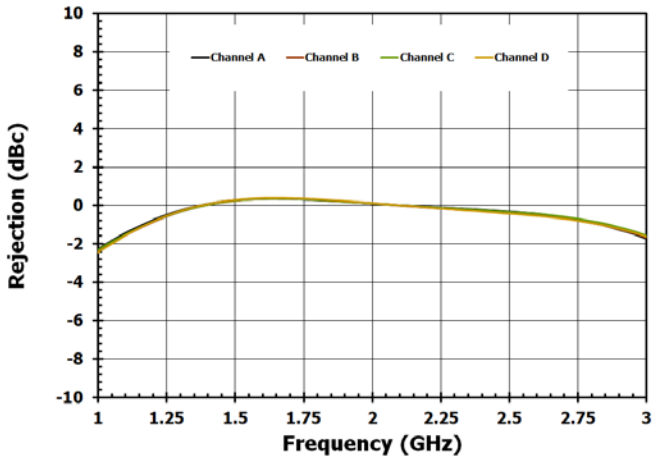


Figure 30. Out of Band Rejection (w.r.t. 2.1GHz)

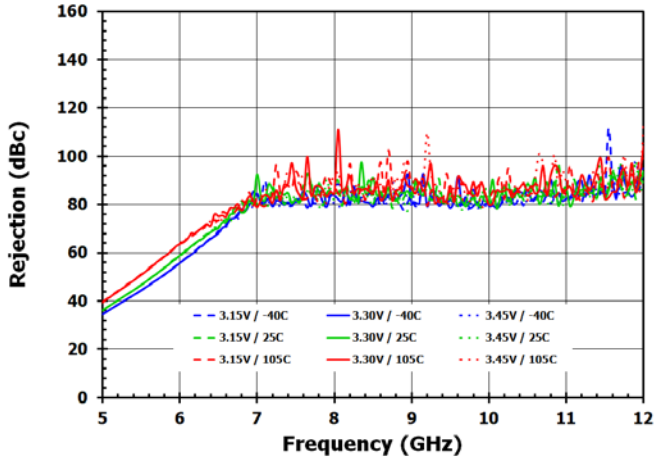


Figure 31. Out of Band Rejection vs Channel (w.r.t. 2.1GHz)

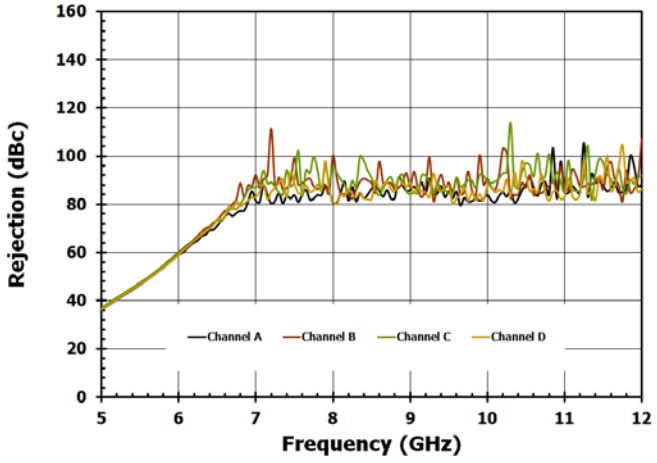


Figure 32. Absolute Error (INL)

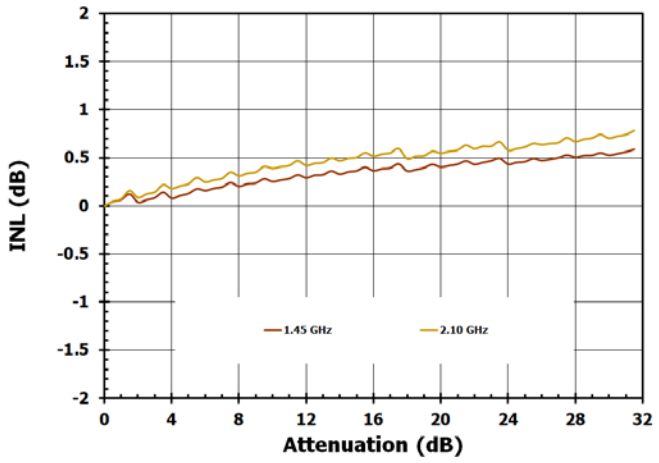


Figure 33. Absolute Error (INL) vs Channel

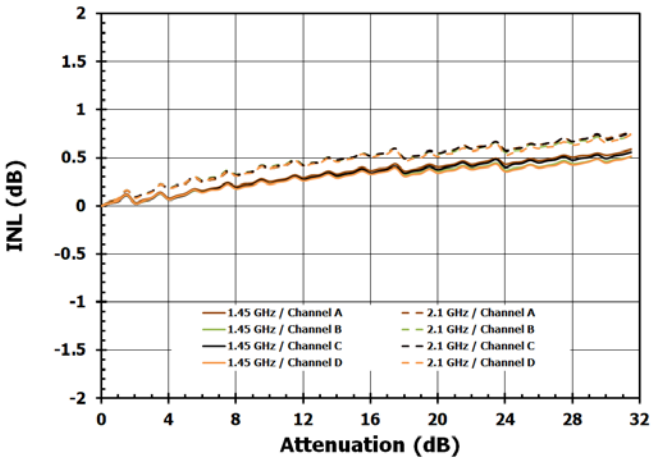


Figure 34. Step Error (DNL)

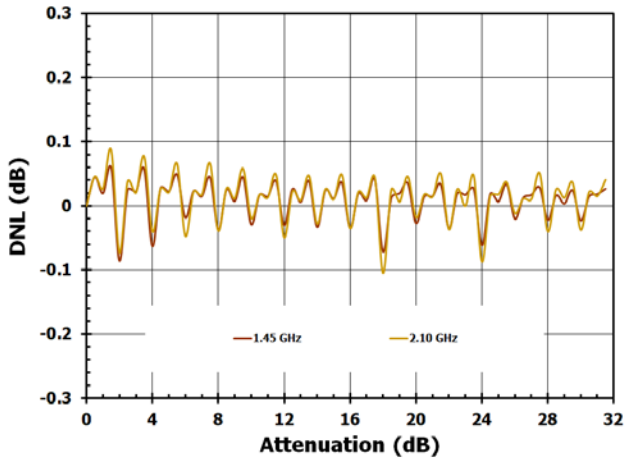


Figure 35. Step Error (DNL) vs Channel

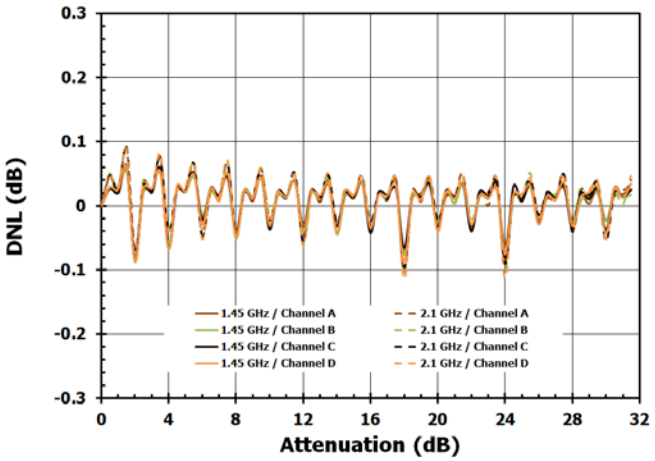


Figure 36. Common Mode Rejection

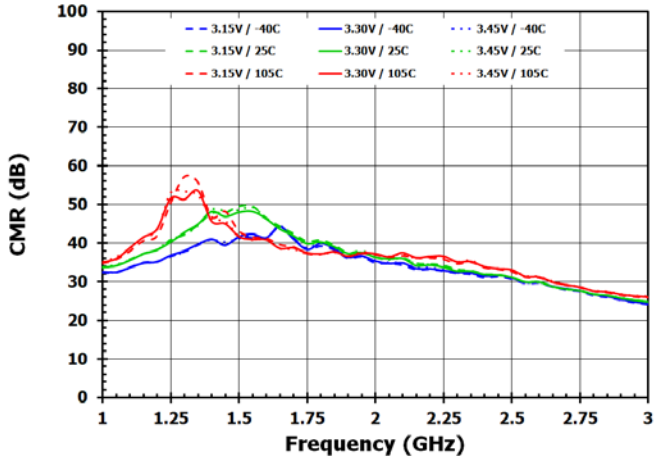


Figure 37. Common Mode Rejection vs Channel

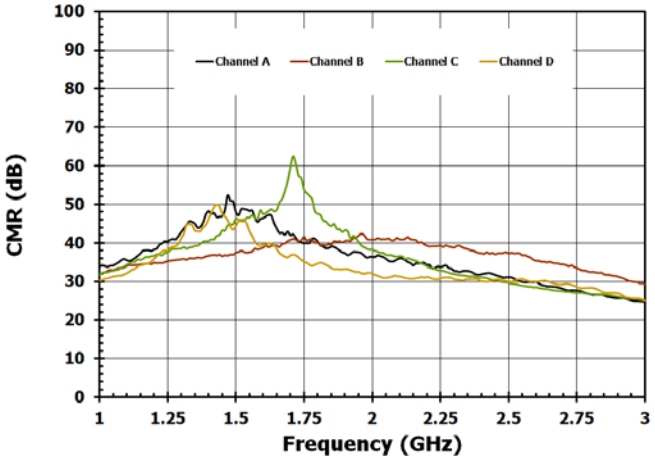


Figure 38. Amplitude Imbalance

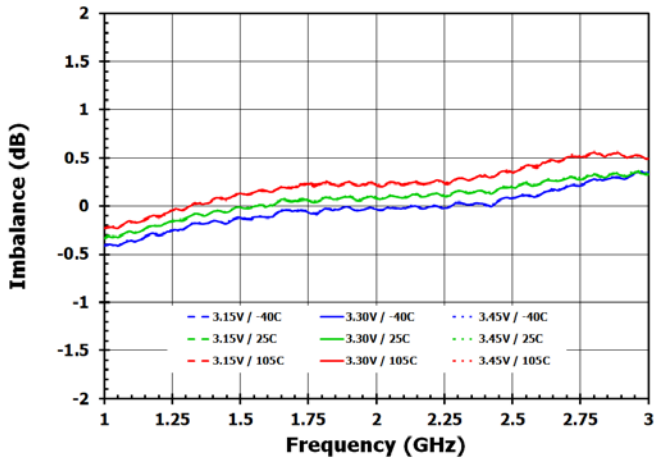


Figure 39. Amplitude Imbalance vs Channel

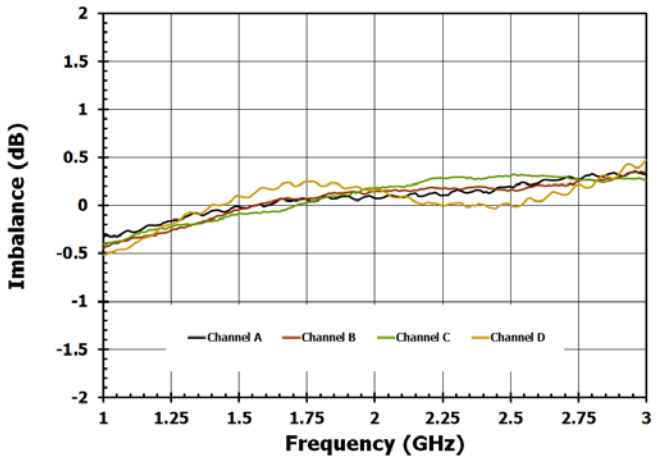


Figure 40. Phase Imbalance

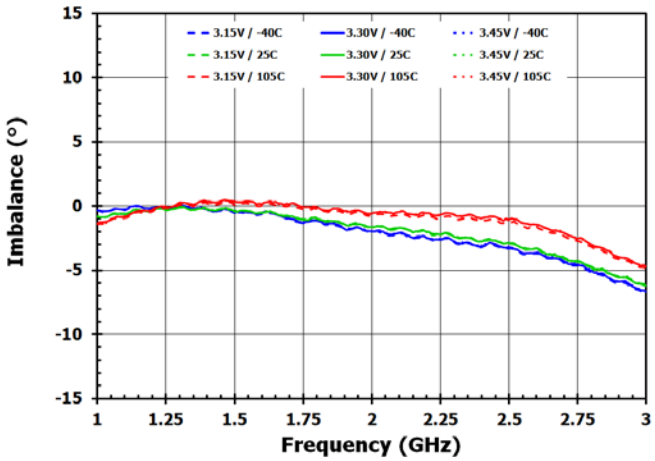


Figure 41. Phase Imbalance vs Channel

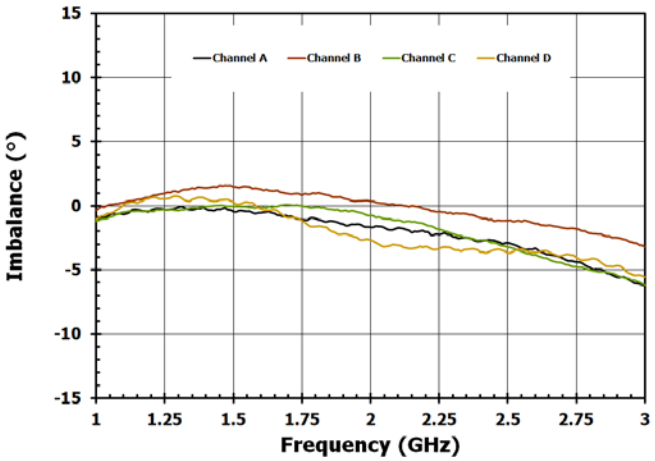


Figure 42. Phase Shift Relative to DSA = 0dB

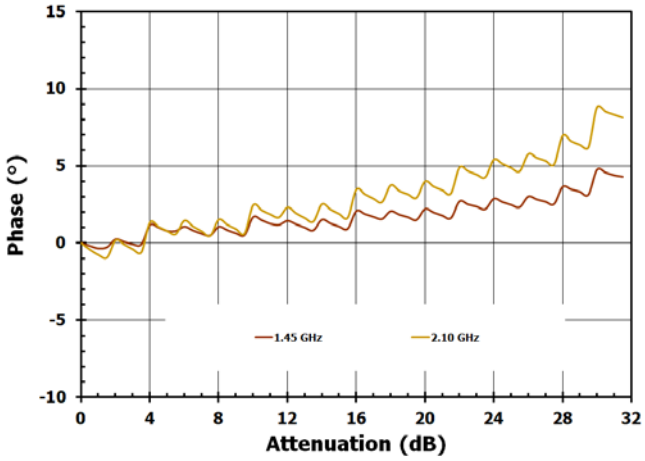
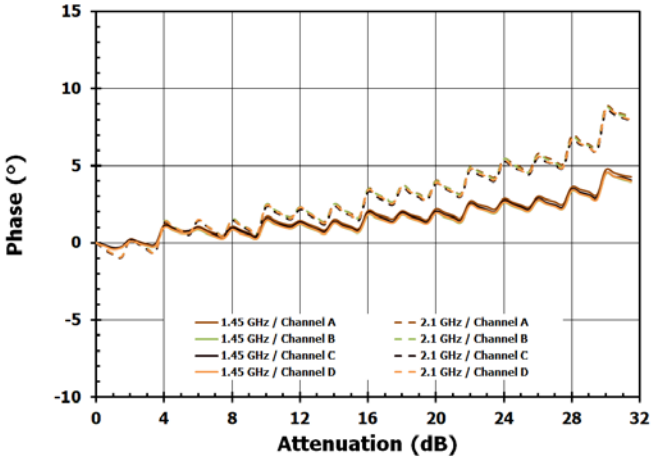


Figure 43. Phase Shift Relative to DSA = 0dB vs Channel



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Figure 44. Group Delay at DSA = 0dB

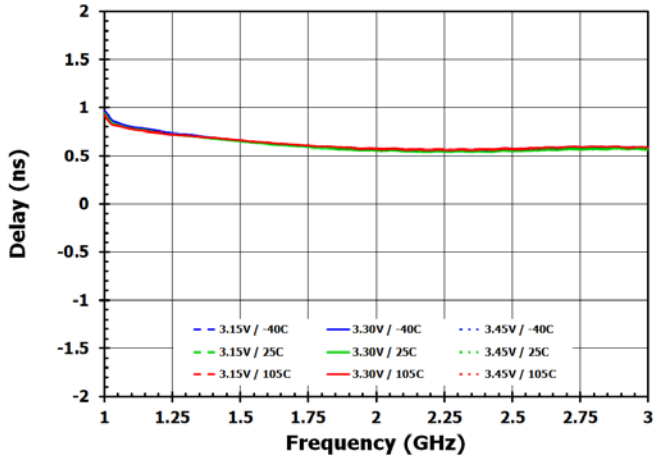


Figure 45. Group Delay vs Channel (DSA = 0dB)

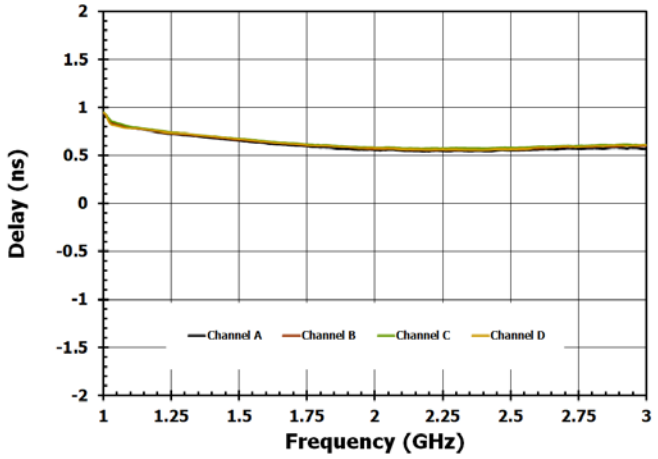


Figure 46. K Factor

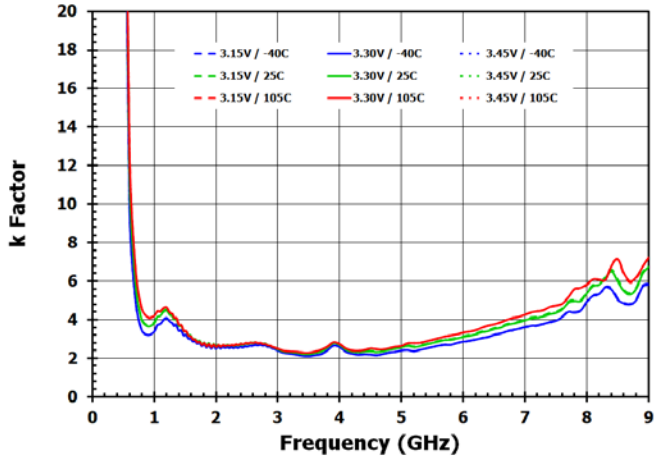


Figure 47. Cross Channel vs Channel Group Delay at DSA = 0dB

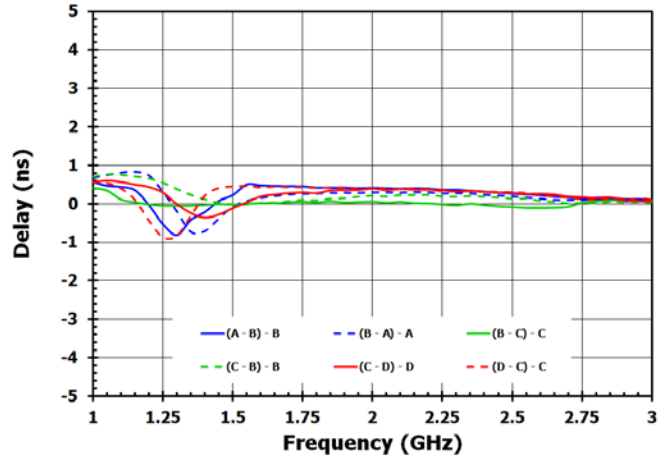


Figure 48. Cross Channel vs Channel Group Delay at DSA = 14dB

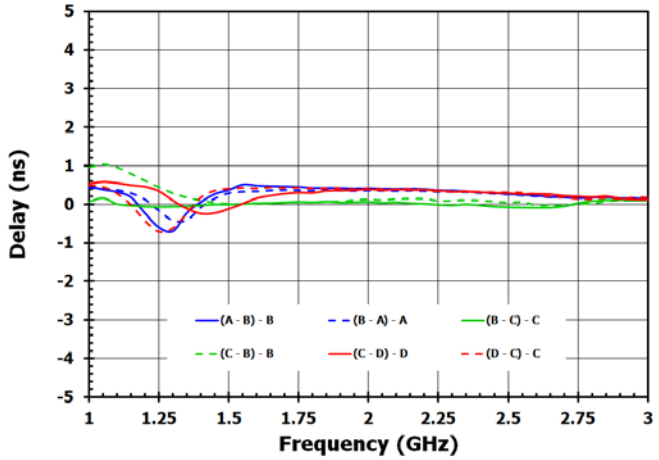


Figure 49. Cross Channel vs Channel Group Delay at DSA = 28dB

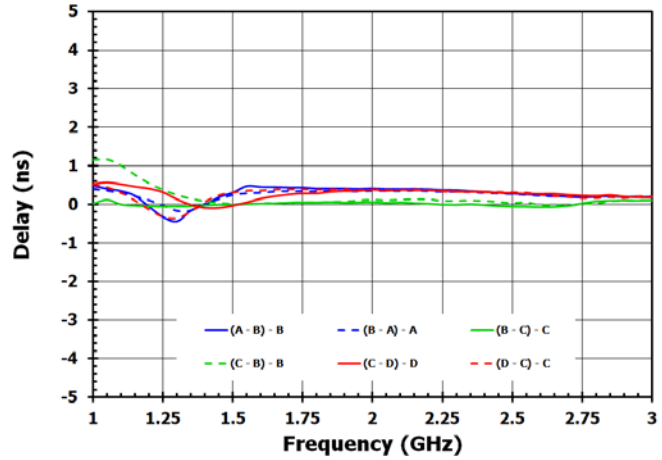


Figure 50. Inter/Intra Channel Isolation at DSA = 0dB

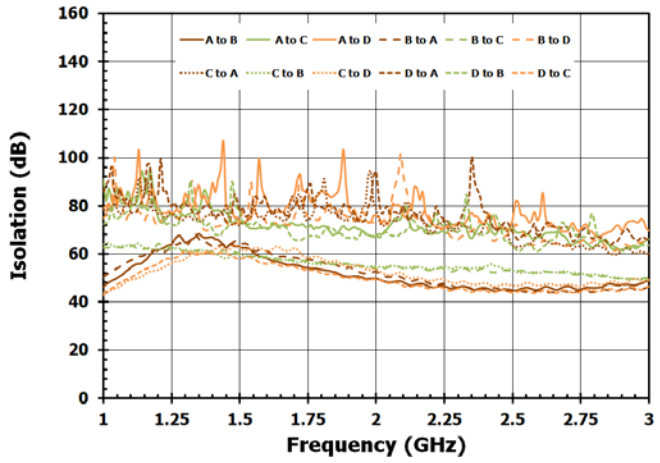


Figure 51. Supply Current

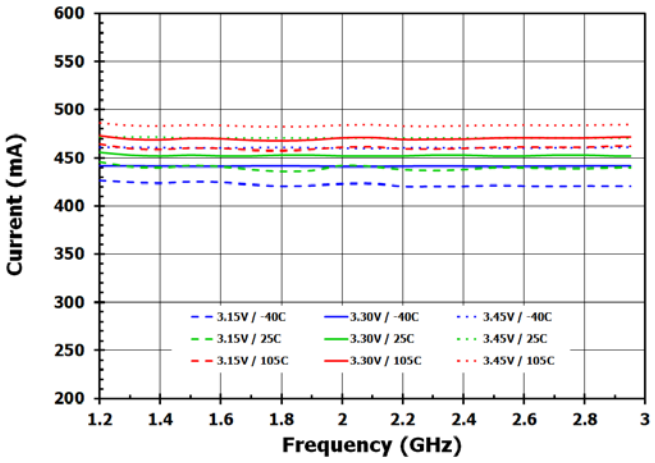


Figure 52. Noise Figure at DSA = 0dB

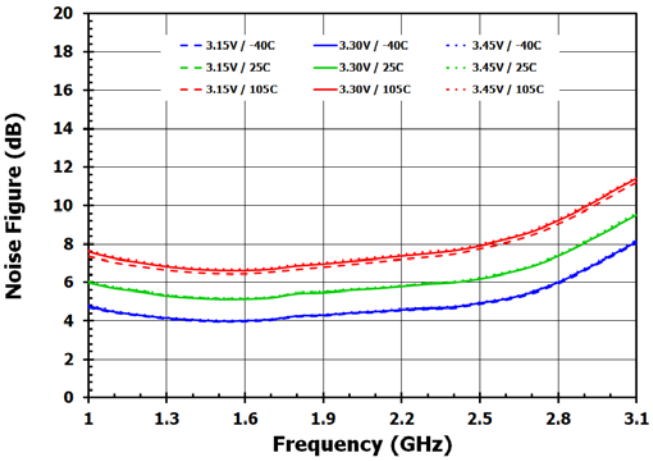


Figure 53. Noise Figure at DSA = 14dB

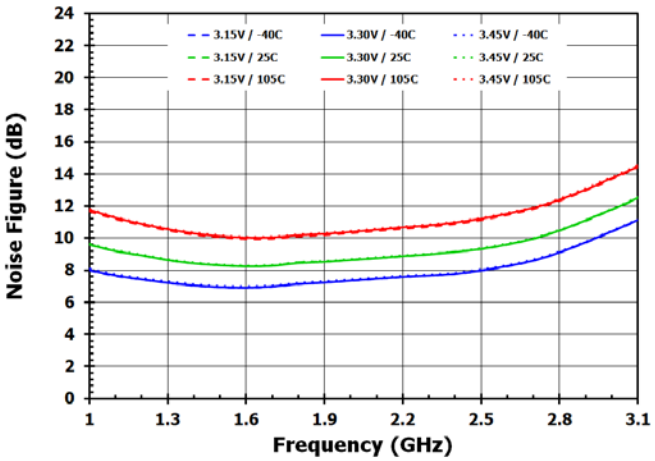


Figure 54. Noise Figure at DSA = 28dB

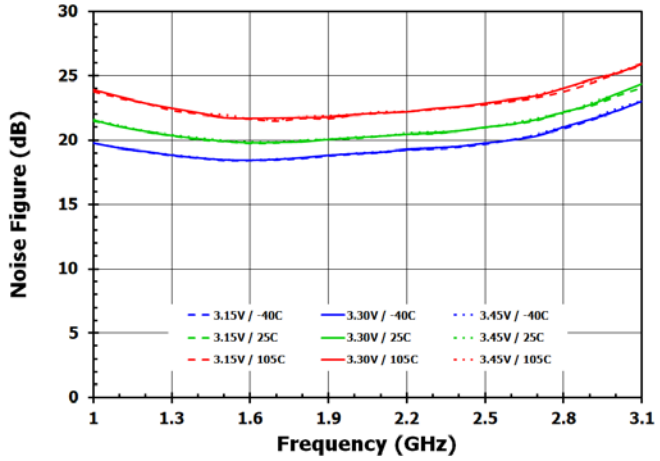


Figure 55. Noise Figure vs Channel (DSA = 0dB)

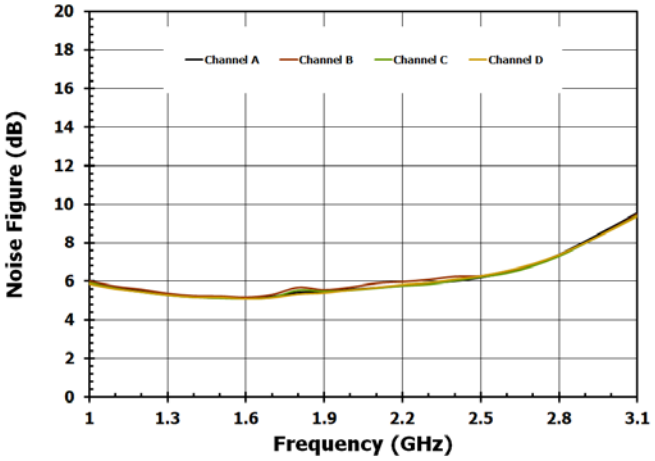


Figure 56. Band 1 OIP3 at DSA = 0dB

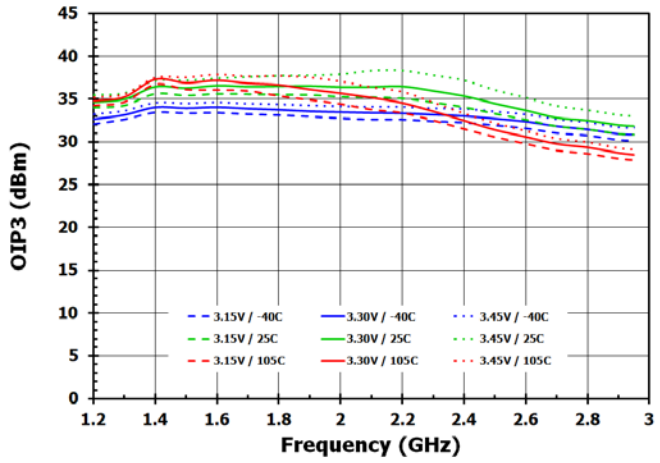


Figure 57. Band 1 OIP3 at DSA = 4dB

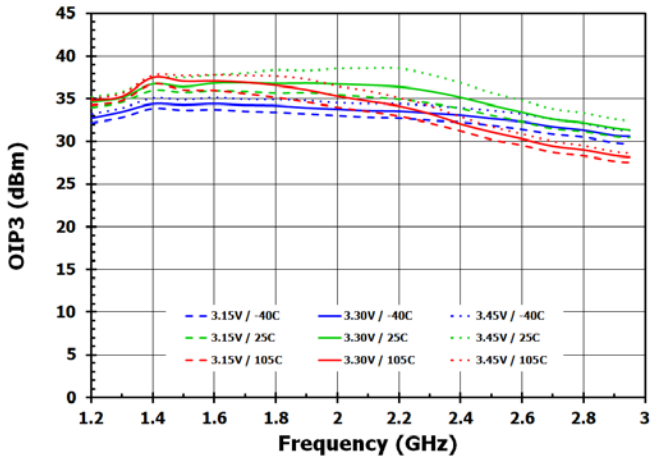


Figure 58. Band 1 OIP3 at DSA = 14dB

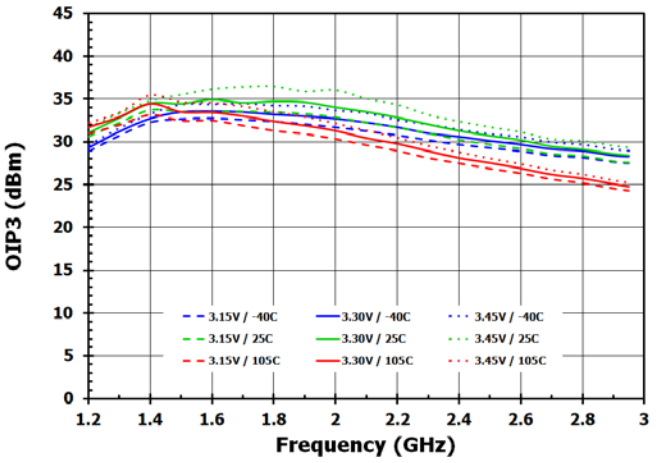


Figure 59. Band 1 OIP3 at DSA = 28dB

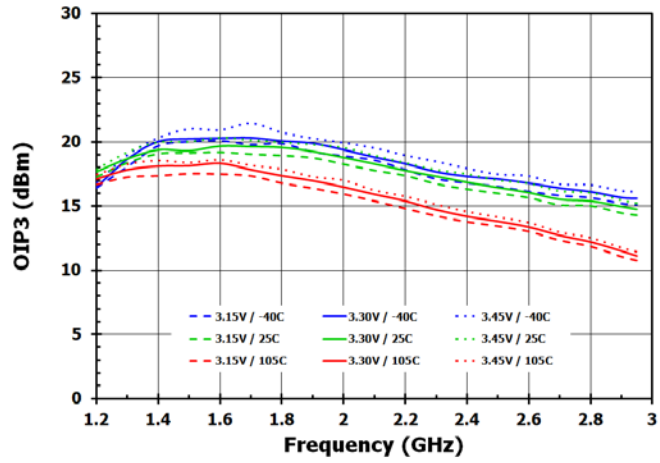


Figure 60. Band 2 OIP3 at DSA = 0dB

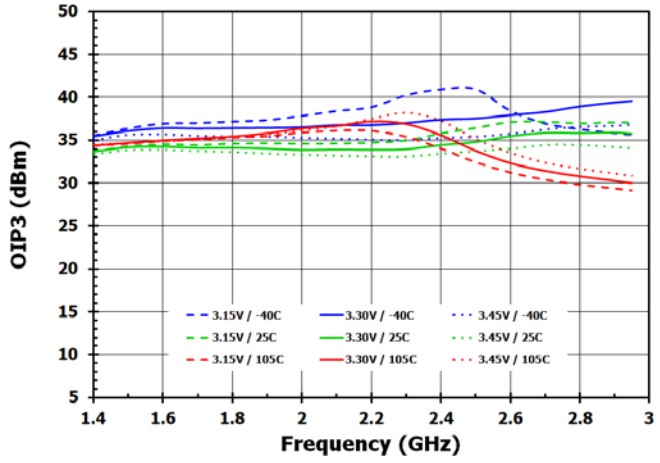


Figure 61. Band 2 OIP3 at DSA = 4dB

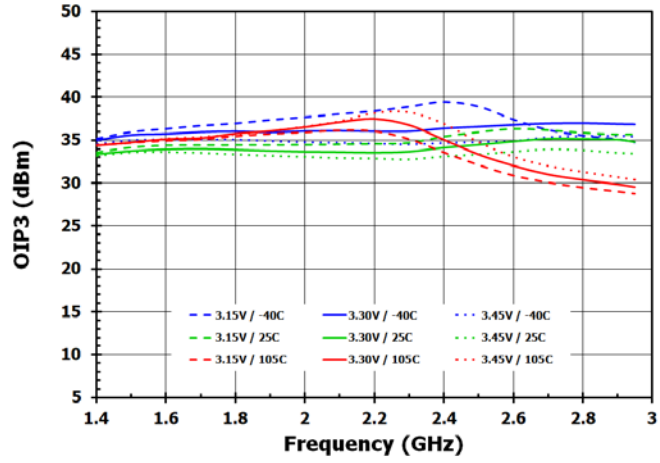


Figure 62. Band 2 OIP3 at DSA = 14dB

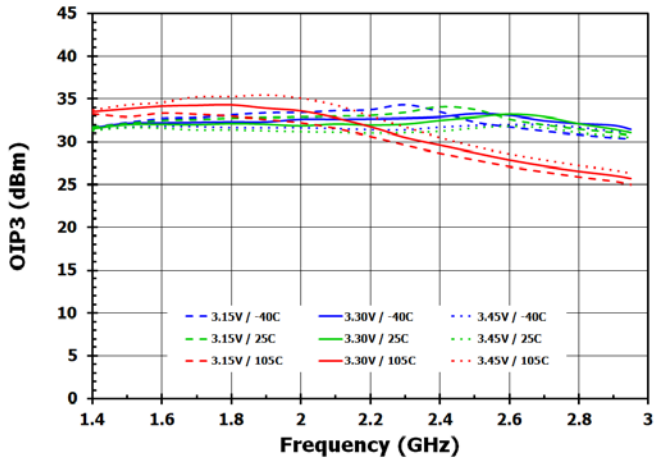


Figure 63. Band 2 OIP3 at DSA = 28dB

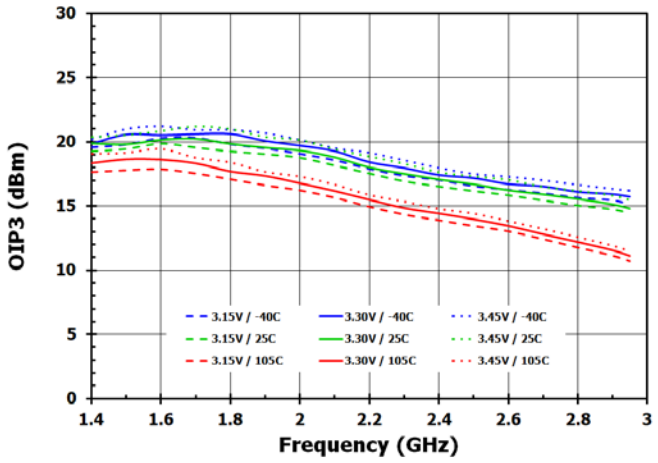


Figure 64. Band 1 OIP3 vs Channel (DSA = 0dB)

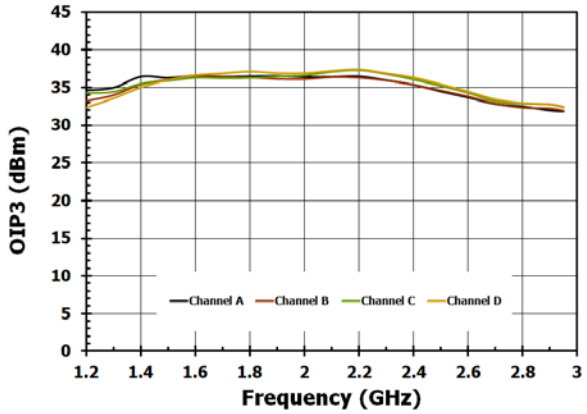


Figure 65. Band 2 OIP3 vs Channel (DSA = 0dB)

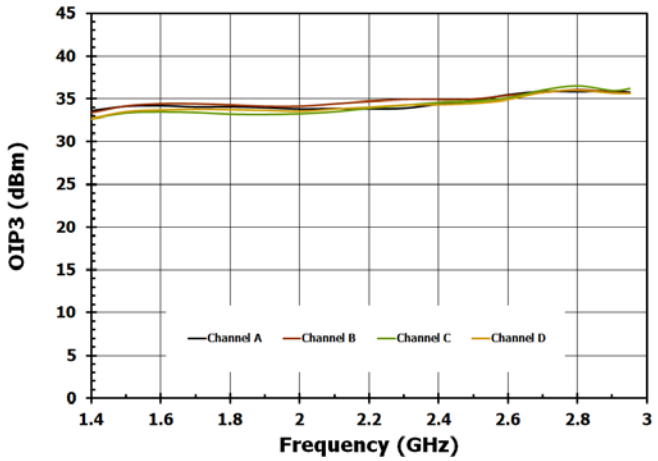


Figure 66. Band 1 OP1dB at DSA = 0dB

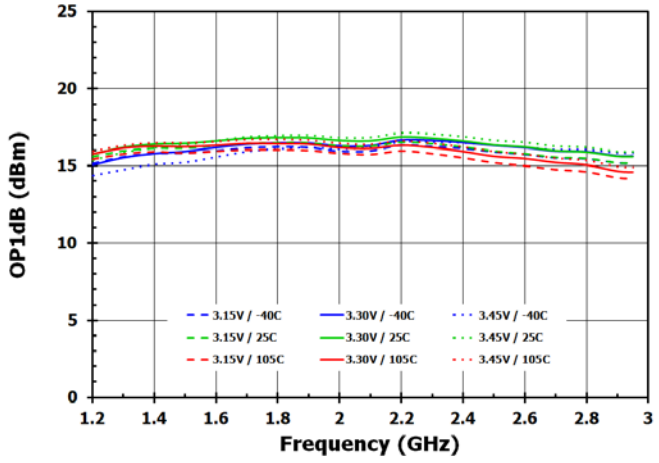
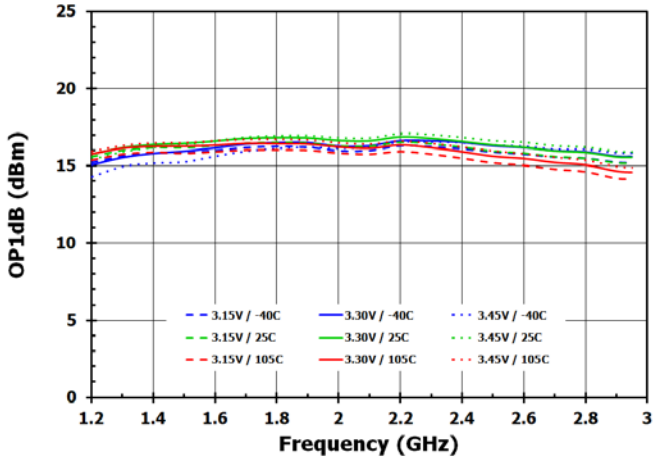


Figure 67. Band 1 OP1dB at DSA = 4dB



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Figure 68. Band 1 OP1dB at DSA = 14dB

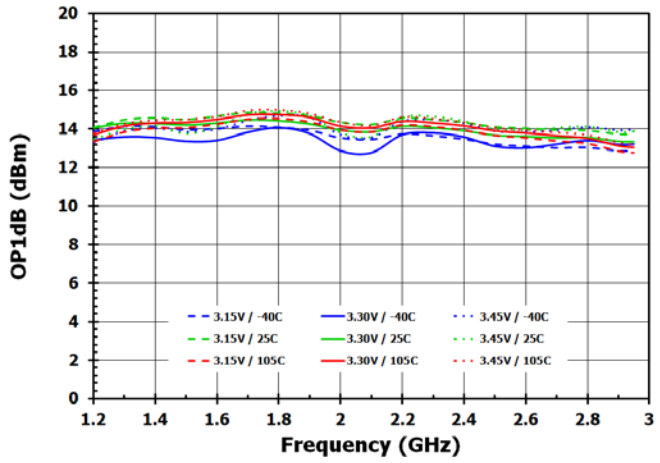


Figure 69. Band 1 OP1dB at DSA = 28dB

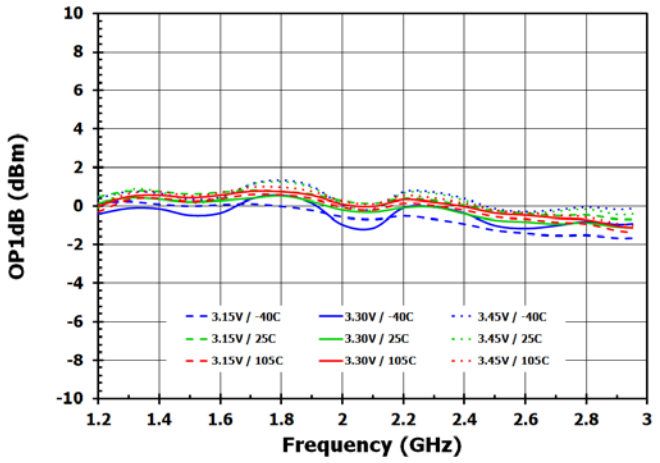


Figure 70. Band 2 OP1dB at DSA = 0dB

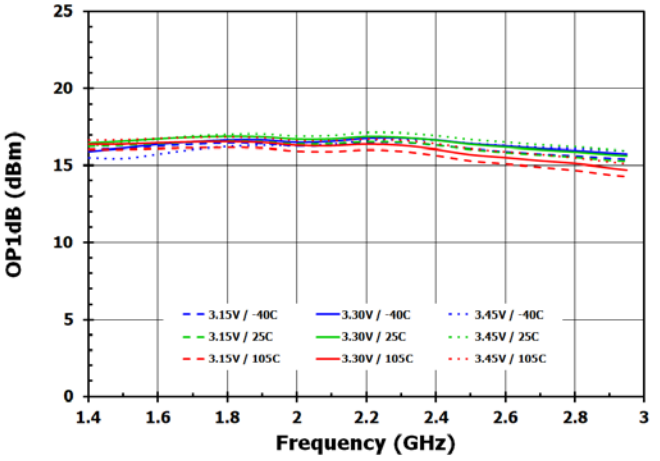


Figure 71. Band 2 OP1dB at DSA = 4dB

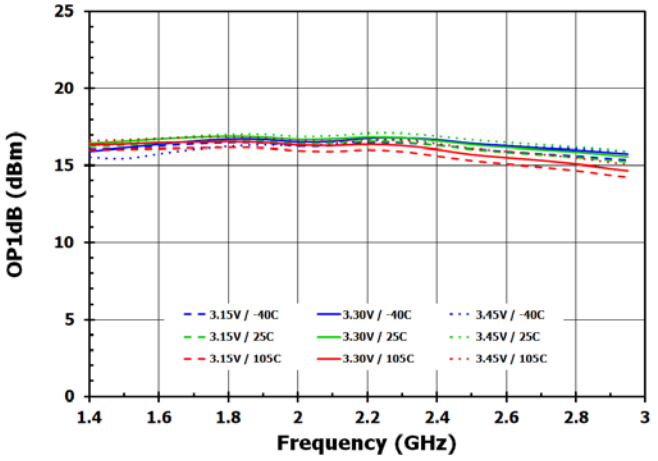


Figure 72. Band 2 OP1dB at DSA = 14dB

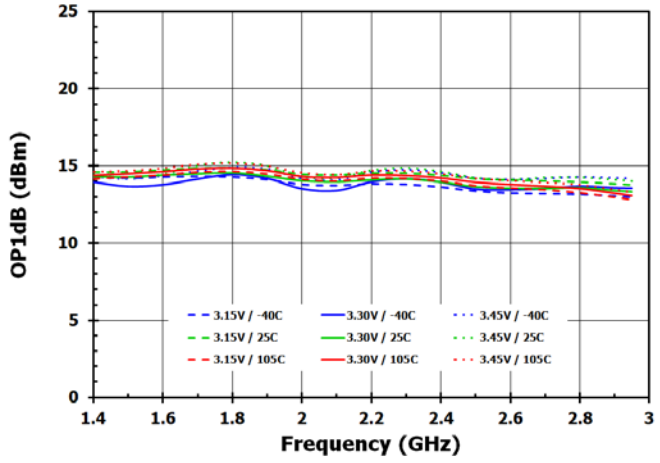


Figure 73. Band 2 OP1dB at DSA = 28dB

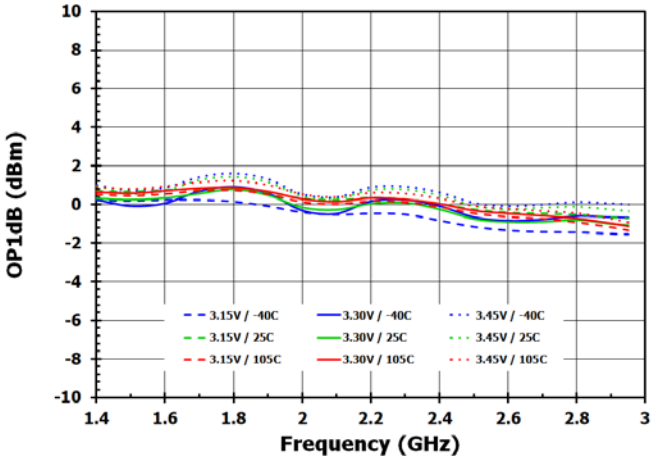


Figure 74. Band 1 OP1dB vs Channel (DSA = 0dB)

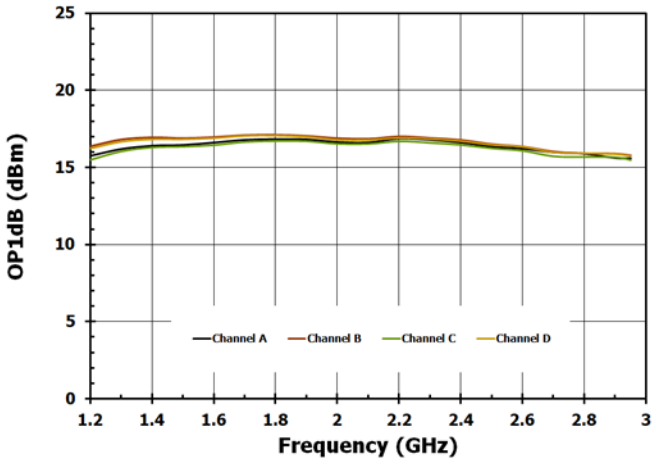
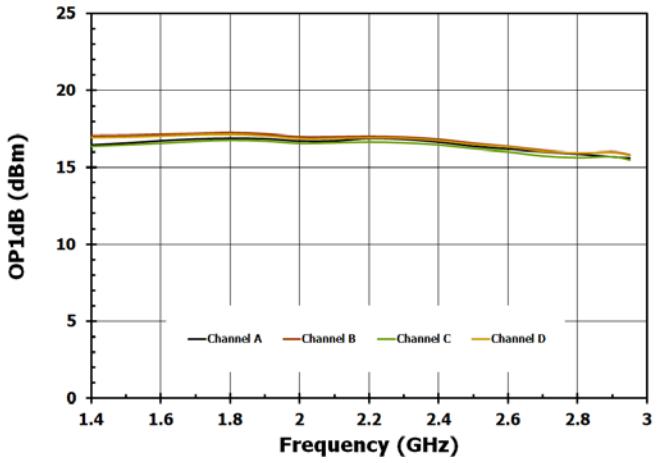


Figure 75. Band 2 OP1dB vs Channel (DSA = 0dB)



Programming

The F4482 uses a variety of programming options that can control the on-chip attenuators and band-select functions. The following sections provide specific details on each unique programming mode.

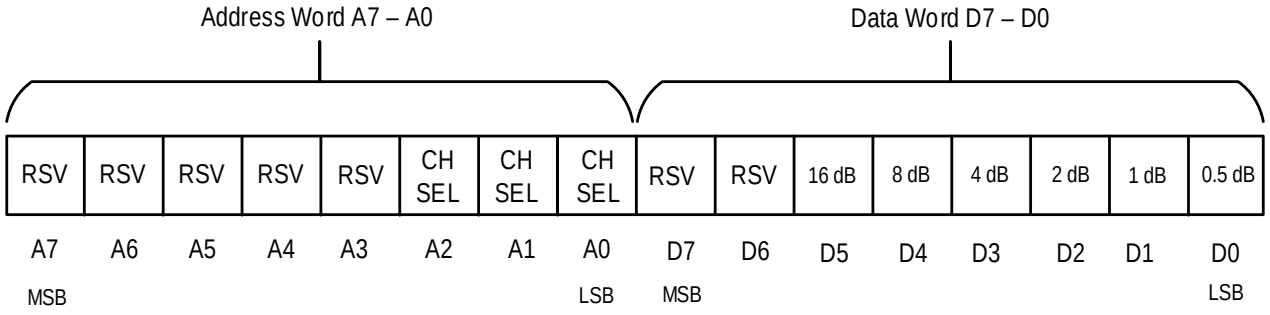
Serial Programming

The F4482 includes a SPI interface that is primarily used to program the device's on-chip attenuators.

Device Register Maps

Each channel of the VGA uses an 8-bit addressing word followed by an 8-bit data word to execute the attenuation level commands. Figure 76 shows the various bit assignments for each channel register.

Figure 76. Register Bit Map for Each Channel



The register address word (Bits A7-A0) includes five reserve bits (A7-A3) followed by three channel addressing bits (A2-A0). The "Channel Select" truth table is provided in Table 8.

Table 8. Channel Select Truth Table

Channel Select	Reserve					Address Bits		
	A7	A6	A5	A4	A3	A2	A1	A0
Channel A	X	X	X	X	X	0	0	0
Channel B	X	X	X	X	X	0	0	1
Channel C	X	X	X	X	X	0	1	0
Channel D	X	X	X	X	X	0	1	1
Channel A and B (Simultaneous Programming)	X	X	X	X	X	1	0	X
Channel C and D (Simultaneous Programming)	X	X	X	X	X	1	1	X

Note that address bit A2 is used to select either individual channel programming (logic LOW) or dual channel programming (logic HIGH). Simultaneous programming of channels A and B is achieved when setting bit A2 to a logic HIGH and A1 a logic LOW. Simultaneous programming of channels C and D occurs when bits A2 and A1 are both logic HIGHs.

Table 9 represents the truth table for the attenuator control bits. A full scale DSA setting of 000000 drives the channel DSA into its ***minimum*** attenuation state. Conversely, a setting of 111111 drives the channel DSA into its ***maximum*** attenuation state. Note that D5 is defined as the Most Significant Bit (MSB) for the attenuator control function within each respective channel.

Table 9. DVGA Attenuation Word Truth Table

Attenuation Setting (dB)	Reserve		Control Bits					
	D7	D6	D5	D4	D3	D2	D1	D0
0.0	X	X	0	0	0	0	0	0
0.5	X	X	0	0	0	0	0	1
1.0	X	X	0	0	0	0	1	0
2.0	X	X	0	0	0	1	0	0
4.0	X	X	0	0	1	0	0	0
8.0	X	X	0	1	0	0	0	0
16.0	X	X	1	0	0	0	0	0
31.5	X	X	1	1	1	1	1	1

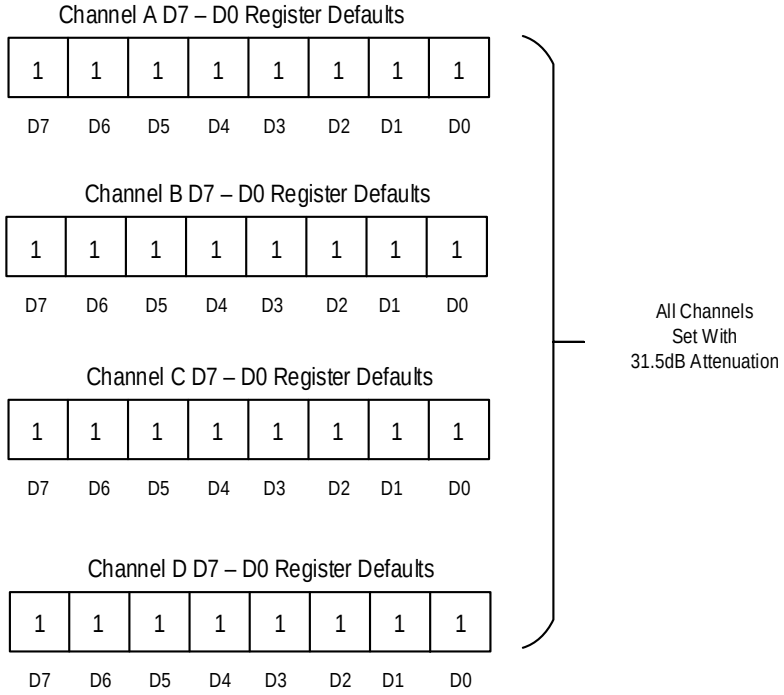
It should also be noted that the listing above represents an *abbreviated* version of the complete 6-bit attenuator control truth table. Any attenuator combination of 0.5dB, 1dB, 2dB, 4dB, 8dB, and 16dB can be achieved by simply assigning a logic HIGH in the respective control bit. For instance, to achieve an attenuation setting of 21.5dB within a given channel, assign a logic HIGH to bits D0, D1, D3, and D5 while assigning a logic LOW to bits D2 and D4. Doing so selects a combination of 0.5dB (D0) + 1dB (D1) + 4dB (D3) + 16dB (D5) = 21.5dB. Setting all of the control bits to logic HIGH will step in *all* of the attenuator stages.

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Serial Mode Default Condition

When the device is ***first powered on,*** each channel's DSA will default to its ***Maximum Attenuation*** setting as shown in Figure 77. These settings apply to a hard reset when first applying V_{CC}.

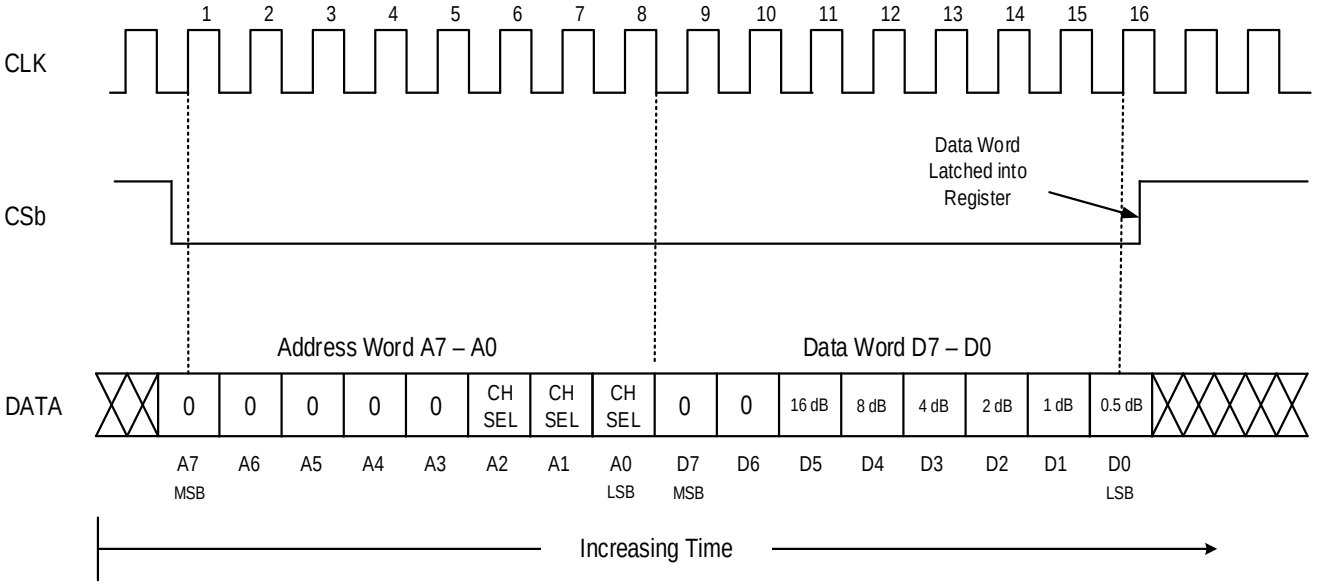
Figure 77. Serial Mode Default Condition Upon Initial Power-Up



Timing Associated with Programming the Serial Registers

To program each channel, the Address Word and Data Word must be clocked in sequentially with the Most Significant Bit (MSB) first (see Figure 78).

Figure 78. Timing Diagram Associated with Programming the Serial Register



SPI Timing Intervals

Figure 79 shows the relevant SPI timing intervals which are specified in Table 10.

Note: The F4482 includes a CLK inhibit feature designed to minimize sensitivity to CLK bus noise when the device is not being programmed. When CSb is high (> V_{IH}), the CLK input is disabled and serial data (DATA) is not clocked into the shift register. It is recommended that CSb be pulled high (> V_{IH}) when the device is not being programmed.

Figure 79. Serial Register Timing Diagram (Timing Spec Intervals are denoted in Blue)

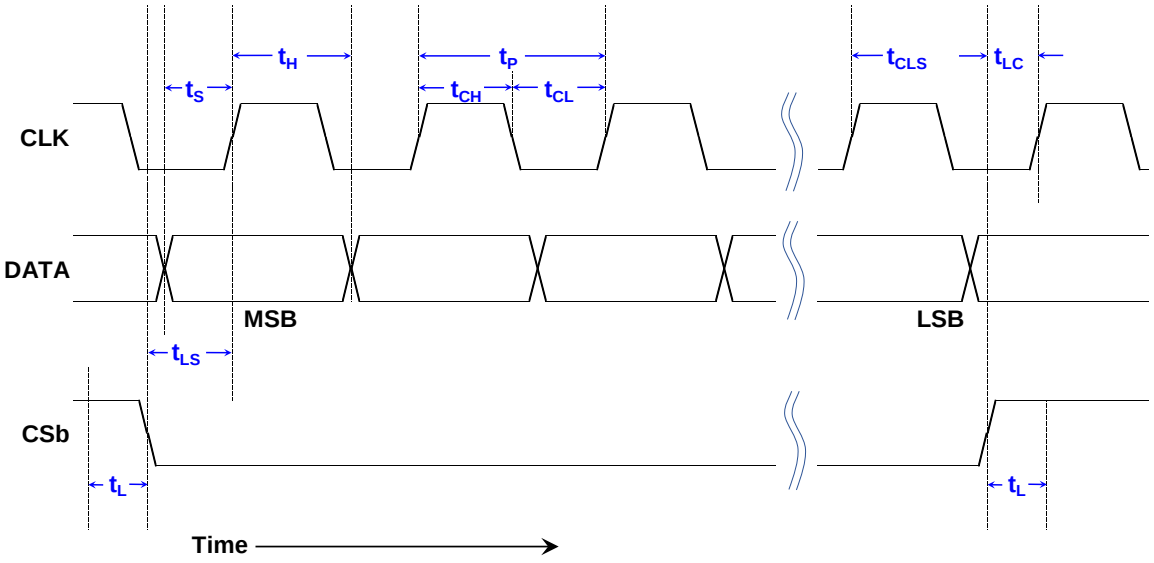


Table 10. SPI Timing Diagram Values for the Serial Mode

Parameter	Symbol	Test Condition	Minimum	Typical	Maximum	Units
CLK Frequency	f_C				20	MHz
CLK High Duration Time	t_{CH}		20			ns
CLK Low Duration Time	t_{CL}		20			ns
DATA to CLK Setup Time	t_S		10			ns
CLK Period [a]	t_P		40			ns
CLK to DATA Hold Time	t_H		10			ns
Final CLK Rising Edge to CSb Rising Edge	t_{CLS}		10			ns
CSb to CLK Setup Time	t_{LS}		10			ns
CSb Trigger Pulse Width	t_L		10			ns
CSb Trigger to CLK Setup Time [b]	t_{LC}		10			ns

[a] $(T_{CH} + T_{CL}) \geq 1/F_C$

[b] Once all desired DATA is clocked in, t_{LC} represents the time a CSb high needs to occur before any subsequent CLK signals.

Standby Mode Programming

Each F4482 channel can be placed into a standby mode via the dedicated Channel STBY pins (STBY_A, STBY_B, STBY_C, and STBY_D); for information, see truth table shown in Table 11). Note that when a channel is disabled, the serial register for that channel will hold the last enabled DSA state.

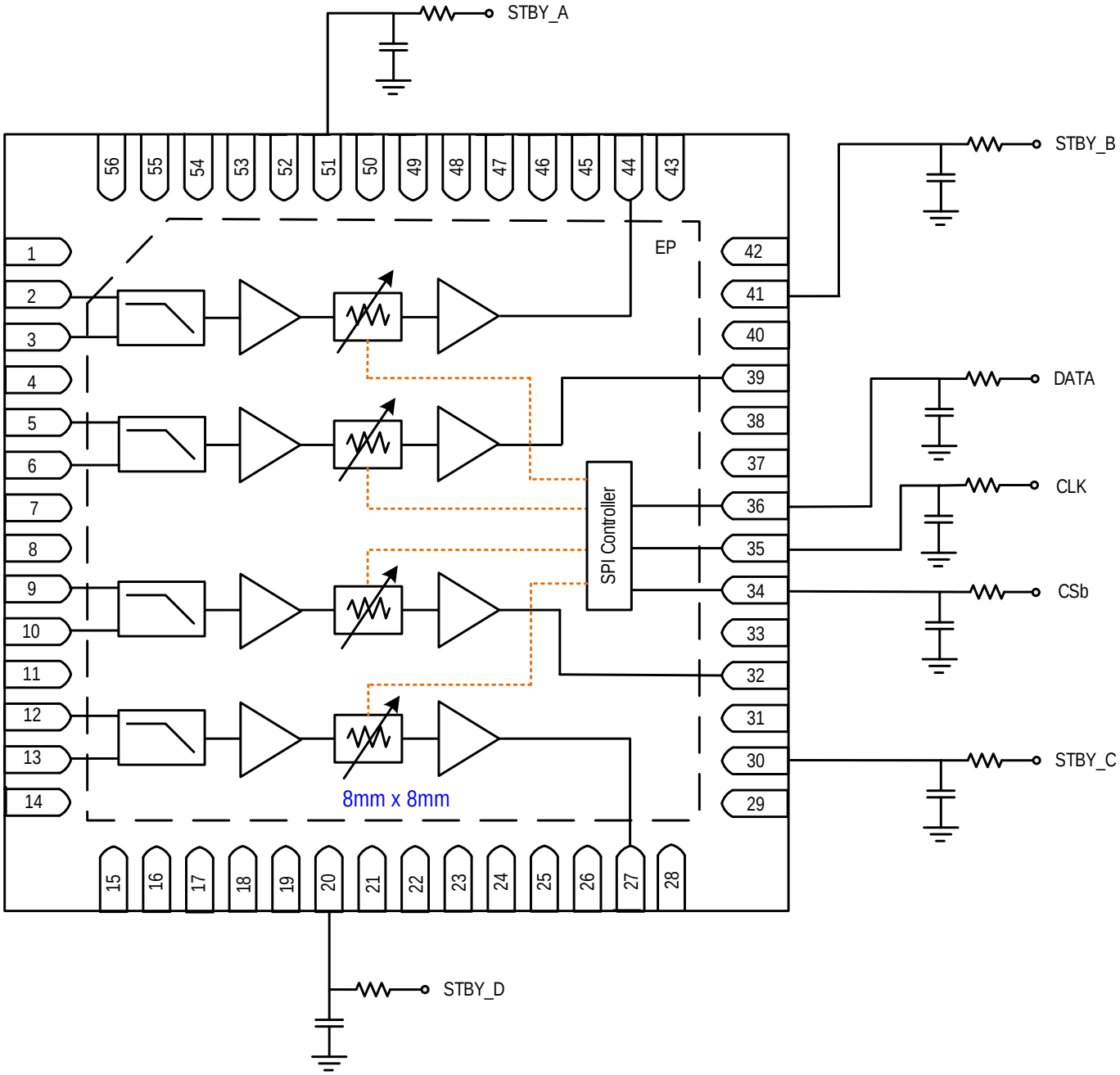
Table 11. STBY Logic Truth Table

Channel	STBY_X Pin Logic	Channel Power State
A	0	Channel A Standby (SPI still active)
	1	Channel A Power On
B	0	Channel B Standby (SPI still active)
	1	Channel B Power On
C	0	Channel C Standby (SPI still active)
	1	Channel C Power On
D	0	Channel D Standby (SPI still active)
	1	Channel D Power On

Control Pin Interface

If control signal integrity is a concern and clean signals cannot be guaranteed due to overshoot, undershoot, ringing, etc., the following circuit at the input of each control pin is recommended. This applies to all control pins. Note: The recommended resistor and capacitor values do not necessarily match the EV kit BOM for the case of poor control signal integrity.

Figure 80. Control Pin Interface for Signal Integrity



Evaluation Kit Picture

Figure 81. Top View

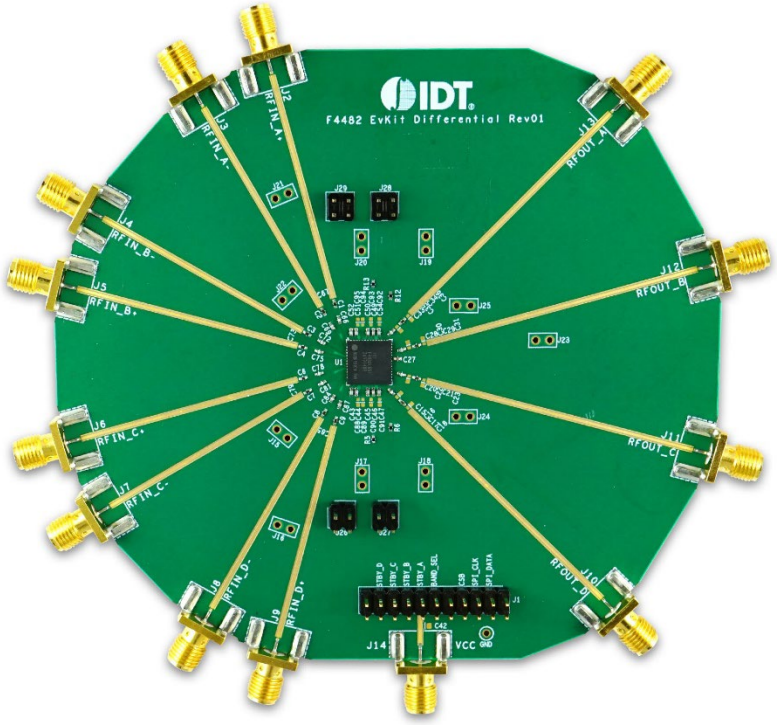
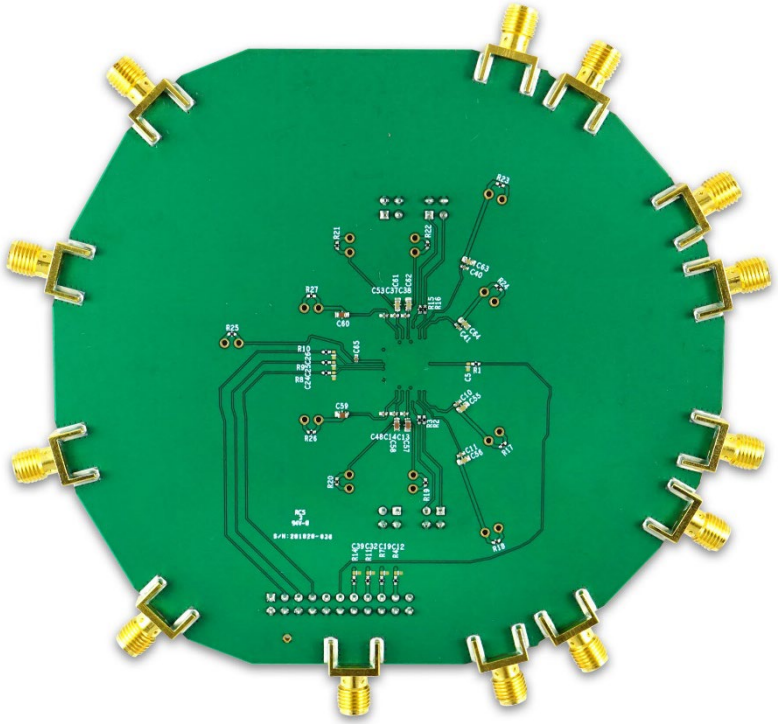


Figure 82. Bottom View



Evaluation Kit / Applications Circuit

Figure 83. Electrical Schematic

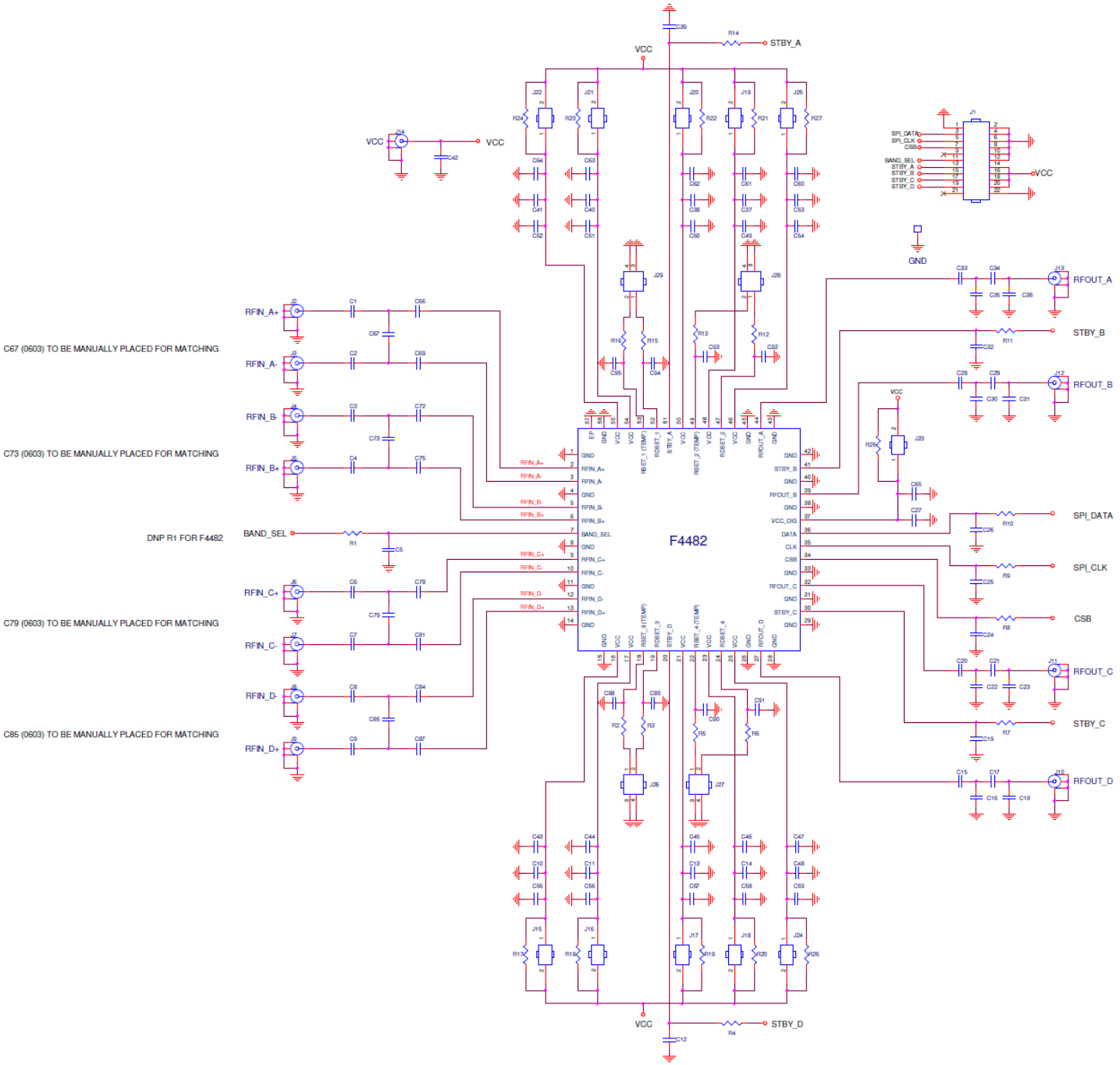


Table 12. Bill of Material (BOM)

Part Reference	QTY	Description	Manufacturer Part #	Manufacturer
C10, C11, C13, C14, C27, C37, C38, C40, C41, C48, C53	11	10nF ±5%, 50V, X7R Ceramic Capacitor (0402)	GRM155R71H103J	Murata
C15, C20, C28, C33, C66, C69, C72, C75, C78, C81, C84, C87	12	100pF ±5%, 50V, C0G Ceramic Capacitor (0402)	GRM1555C1H101J	Murata
C43-C47, C49-C52, C54	10	1000pF ±5%, 50V, C0G Ceramic Capacitor (0402)	GRM1555C1H102J	Murata
C65	1	100nF ±10%, 50V, X7R Ceramic Capacitor (0402)	GRM155R71H104K	MURATA
C55-C59, C60-C64	10	10uF ±20%, 16V, X6S Ceramic Capacitor (0603)	GRM188C81C106M	MURATA
R1, R4, R7-11, R14	8	100Ω ±1%, 1/10W, Resistor (0402)	ERJ-2RKF1000X	PANASONIC
R2, R16	2	1.96kΩ ±1%, 1/10W, Resistor (0402)	ERJ-2RKF1961X	PANASONIC
R3, R15	2	1.3GHz – 1.7GHz: 3.92kΩ ±1%, 1/10W, Resistor (0402)	ERJ-2RKF3921X	PANASONIC
		1.7GHz – 2.8GHz: 3.74kΩ ±1%, 1/10W, Resistor (0402)	ERJ-2RKF3741X	PANASONIC
R5, R13	2	1.3GHz – 1.7GHz: 2.26kΩ ±1%, 1/10W, Resistor (0402)	ERJ-2RKF2261X	PANASONIC
		1.7GHz – 2.8GHz: 2.26kΩ ±1%, 1/10W, Resistor (0402)	ERJ-2RKF2261X	PANASONIC
R6, R12	2	1.3GHz – 1.7GHz: 3.32kΩ ±1%, 1/10W, Resistor (0402)	ERJ-2RKF3321X	PANASONIC
		1.7GHz – 2.8GHz: 2.80kΩ ±1%, 1/10W, Resistor (0402)	ERJ-2RKF2801X	PANASONIC
R17-R27, C1-C4, C6-C9, C17, C21, C29, C34	23	0Ω Resistors (0402)	ERJ-2GE0R00X	PANASONIC
J1	1	CONN HEADER VERT DBL 11 X 2 POS GOLD	67997-122HLF	AMPHENOL FCI
J2-J14	13	Edge Launch SMA (0.375 inch pitch ground, tab)	142-0701-851	Emerson Johnson
J26, J27, J28, J29	4	CONN HEADER VERT DBL 2 X 2 POS GOLD	90131-0762	Molex
U1	1	Quad Path TX DVGA 1300MHz - 2800MHz	F4482	Renesas
		Printed Circuit Board	F4482 EVKIT DF REV01	Renesas
		Bill Of Material (Rev 01)		Renesas

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Evaluation Kit Operation

Power Supplies

A common V_{CC} power supply should be used for all pins requiring DC power. All supply pins should be bypassed with external capacitors to minimize noise and fast transients. Supply noise can degrade noise figure and fast transients can trigger ESD clamps and cause them to fail. Supply voltage change or transients should have a slew rate smaller than 1V/20µs. In addition, all control pins should remain at 0V (±0.3V) or floating while the supply voltage ramps or while it returns to zero.

Power Supply Setup

1. Connect pin 2 to pin 4, and pin 1 to pin 3 of J26-29. This ensures operation of the Distortion and Bias resistors.
2. Set up a power supply in the voltage range of 3.15V to 3.45V with the power supply output disabled. The voltage can be applied directly to the J14 SMA.

Power-On Procedure

Set up the voltage supplies and Evaluation Board as described in the “Power Supply Setup” and enable the V_{CC} supply.

Power-Off Procedure

1. Disable the RF input signal on all channels.
2. Disable the V_{CC} supply.

Application Information

The F4482 is optimized for use in high-performance RF applications ranging from 1.3GHz to 2.8GHz.

Startup Condition

Upon device power-up, all channels will default to the standby mode ON. For logic levels, see Table 11.

Default Channel Power On

The default attenuation state will be 31.5dB attenuation upon powering ON each channel (i.e., standby mode OFF). For default levels, see Figure 77.

Chip Select (CSb)

When CSb is set to logic high, the CLK input is disabled. When CSb is set to logic low, the CLK input is enabled and the DATA word can be programmed into the shift registers. The programmed word is then latched into the F4482 on the CSb rising edge (see Figure 79).

Standby Mode (STBY)

The F4482 has a power-down feature for power savings. The SPI bus is used to operate each channel in Standby On/Off mode (see Table 11).

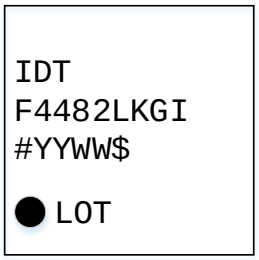
Package Outline Drawings

The package outline drawings are appended at the end of this document.

Ordering Information

Orderable Part Number	Package	MSL Rating	Shipping Packaging	Temperature
F4482LKGI	8 × 8 × 0.65 mm 56-LGA	3	Tray	-40° to +105°C
F4482LKGI8	8 × 8 × 0.65 mm 56-LGA	3	Reel	-40° to +105°C
F4482EVS-1P5	Evaluation Board (Band 1)			
F4482EVS-2P1	Evaluation Board (Band 2)			

Marking Diagram



- Line 1 is the manufacturer (IDT/Renesas).
- Line 2 is the part number.
- Line 3 indicates the following:
  - # denotes device stepping
  - "YY" is the last two digits of the year; "WW" is the work week that the part was assembled.
  - "$" denotes the mark code
- Line 4 is the lot number.

Revision History

Revision Date	Description of Change
December 15, 2020	Removed references to F4483.
October 15, 2020	Updated Ordering Information.
October 5, 2020	Updated Electrical Characteristics tables and Typical Performance Characteristics.
August 28, 2020	Updated Electrical Characteristics table.
August 14, 2020	Initial release.