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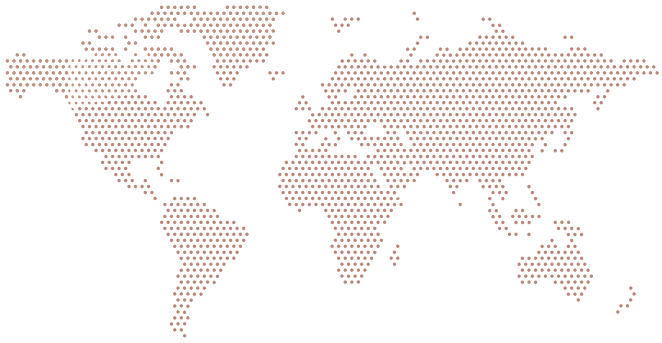
DATA SHEET

HKE21000/S

Ultra-Accurate, Low-Power 3-Axis Gyroscope



Revision 1.0, Oct 2019



World Leader in
MEMS Technology

HKE21000/S

Ultra-Accurate, 3-Axis Digital Output Gyroscope

General Description

The HKE 21000 /S is a low-power , low-noise 3-axis angular rate sensor that delivers unprecedented accuracy and sen- sitivity over temperature and time. It operates with a supply voltage as low as 1.71V for minimum power consumption. It includes a sensing element and an IC interface that provides the measured angular rate to the external world through a digital interface (I2C/SPI).

The IC has a full scale of ±31.25/±62.50/±125/±250/ ±500/±1k/±2k degrees per second (dps) and measures rates with a finely tunable user-selectable bandwidth. The low short time bias instability , the high stability over temperature , and the operational flexibility make the IC ideal for in-dash navigation systems.

The IC is a highly integrated solution available in a compact 3mm x 3mm x 0.9mm plastic land grid array (LGA) package and does not require any external components other than supply bypass capacitors. It can operate over the -40ºC to +85ºC temperature range.

Applications

- In-Dash Car Navigation Systems
- Motion Control with MMI (Man-Machine Interface)
- Appliances and Robotics

Benefits and Features

- Minimum Overall Footprint
  - Industry's Smallest and Thinnest Package (3mm x3mm x 0.9mm LGA)
  - No External Components
- High Accuracy and Stability
  - Ultra-Stable Over Temperature and Time
  - Factory Calibrated Automatic Temperature Compensation
  - Low Bias Instability
  - Embedded Digital-Output Temperature Sensor
- High Flexibility
  - Wide Supply Voltage Range (1.71V to 3.6V)
  - 7 Selectable Full Scales (31.25/62.5/125/250/500/ 1000/2000 dps)
  - Integrated Digitally Programmable Low- and Highpass Filters
  - Independently Selectable Data ODR and Interrupt ODR
  - 256 Selectable ODR
- Flexible Embedded FIFO
  - Size: 512 bytes (256 x 16 Bits)
  - Single-Byte Reading Available
  - Four Different FIFO Modes Available
- Flexible Interrupt Generator
  - Two Digital Output Lines
  - 2 Independent Interrupt Generators
  - 8 Maskable Interrupt Sources Each
  - Configurable as Latched/Unlatched/Timed
  - Embedded Independent Angular Rate Comparators
  - Independent Threshold and Duration
  - Level/Pulse and OD/PP Options Available
- Flexible Data Synchronization Pin
  - External Wakeup
  - Interrupt Generation
  - Single Data Capture Trigger
  - Multiple Data Capture Trigger
  - LSB Data Mapping
- High-Speed Interface
  - I2C Standard (100kHz), Fast (400kHz), and High-Speed (3.4MHz) Serial Interface
  - 10MHz SPI Interface
- Low Operating Current Consumption (6.1mA typ)
- High-Shock Survivability (10,000 G-Shock)

***Ordering Information* appears at end of data sheet.**

For related parts and recommended products to use with this part, refer to www.hankingmems.com/21001S.related.

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19-6837; Rev 1.0; 10/19

Absolute Maximum Ratings

V_{DD} ..... -0.3V to +6.0V
V_{DDIO} ..... -0.3V to Min (V_{DD} + 0.3V, +6.0V)
INT1, INT2, SDA_SDI_O, SA0_SDO,
SCL_CLK, CS, DSYNC ..... -0.3V to (V_{DDIO} + 0.3V)
I_{VDD} Continuous Current 100mA
I_{VDDIO} Continuous Current 100mA
Junction Temperature ..... +150ºC
Operating Temperature Range ..... -40ºC to +85ºC
Storage Temperature Range ..... -40ºC to +150ºC
Lead Temperature (soldering, 10s) ..... +260ºC

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Drops onto hard surfaces can cause shocks of greater than 10,000 g and can exceed the absolute maximum rating of the device. Exercise care in handling to avoid damage.

Package Thermal Characteristics(Note 1)

LGA
Junction-to-Ambient Thermal Resistance (θ_{JA}) ..... 160°C/W
Junction-to-Case Thermal Resistance (θ_{JC}) ..... 31.8°C/W

Note 1: Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to **www.hankingmems.com/thermal-tutorial**.

Electrical Characteristics

(V_{DD} = V_{DDIO} = 2.5V, T_A = -40°C to +85°C, INT1, INT2, **SDA and SCL are unconnected**, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SUPPLY AND CONSUMPTION						
V_{DD} Supply Voltage	V_{DD}		1.71	2.5	3.6	V
V_{DDIO} (Note 3)	V_{DDIO}		1.71	2.5	V_{DD} + 0.3V	V
IDD Current Consumption Normal Mode	I_{VDDN}			5.4	6.1	mA
IDD Current Consumption Standby Mode (Note 4)	I_{VDDS}			2.7	3.3	mA
IDD Current Consumption Power Down Mode	I_{VDDP}			8.5	70	µA
TEMPERATURE SENSOR						
Temperature Sensor Output Change vs. Temperature (Note 5)	T_{SDR}	8 bit	0.92	1	1.08	digit/°C
		16 bit	236	256	276	digit/°C
Temperature BW	T_{BW}			1		Hz
Temperature Sensor Bias	T_{BIAS}	At T_A = +25°C, 8 bit	20	25	30	digit
		At T_A = +25°C, 16 bit	5120	6400	7680	
GYROSCOPE						
Gyro Full-Scale Range	G_{FSR}	User selectable		±31.25		dps
				±62.5		
				±125		
				±250		

Electrical Characteristics (continued)

(V_{DD} = V_{DDIO} = 2.5V, T_A = -40°C to +85°C, INT1, INT2, **SDA and SCL are unconnected**, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Gyro Full-Scale Range	G_{FSR}	User selectable		±500		dps
				±1000		
				±2000		
Gyro Rate Noise Density (Note 5)	G_{RND}	For all the f_S and over the whole V_{DD} including 1.8V		0.009	0.045	dps/√Hz
Gyro Bandwidth (Lowpass) (Note 6)	G_{BWL}		2		400	Hz
Gyro Bandwidth (Highpass) (Note 6)	G_{BWH}		0.1		100	Hz
Phase Delay	G_{PDL}	At 10Hz, 400Hz bandwidth, 10kHz ODR		2.9		deg
Output Data Rate (Note 7)	G_{ODR}		4		10k	Hz
Sensitivity Error	G_{SE}		-6		+6	%
Nominal Sensitivity	G_{SO}	G_{FSR} = 31.25		960		digit/ dps
		G_{FSR} = 62.5		480		
		G_{FSR} = 125		240		
		G_{FSR} = 250		120		
		G_{FSR} = 500		60		
		G_{FSR} = 1000		30		
		G_{FSR} = 2000		15		
Sensitivity Drift Over Temperature (Note 5)	G_{SD}	Maximum delta from T_A = +25°C	-3		+3	%
Zero Rate Level Error	G_{ZRLE}		-10	±0.5	+10	dps
Zero Rate Level Drift Over Temperature (Note 5)	G_{ZRLD}	Maximum delta from T_A = +25°C	-10		+10	dps
			-0.15		+0.15	dps/°C
Startup Time from Power Down	G_{TUPL}			45	120	ms
Nonlinearity (Note 5)	G_{NLN}		-0.5		+0.5	$\%f_S$
Angular Random Walk (ARW)	G_{ARW}			0.45		°/√hr
In-Run Bias Stability	G_{IBS}	At 1000s		4		°/hr
Cross Axis	G_{XX}			1		%
Self-Test Output	STOR	All GFS, axes X, Z	+10	+25	+50	$\%f_S$
		All GFS, axis Y	-50	-25	-10	

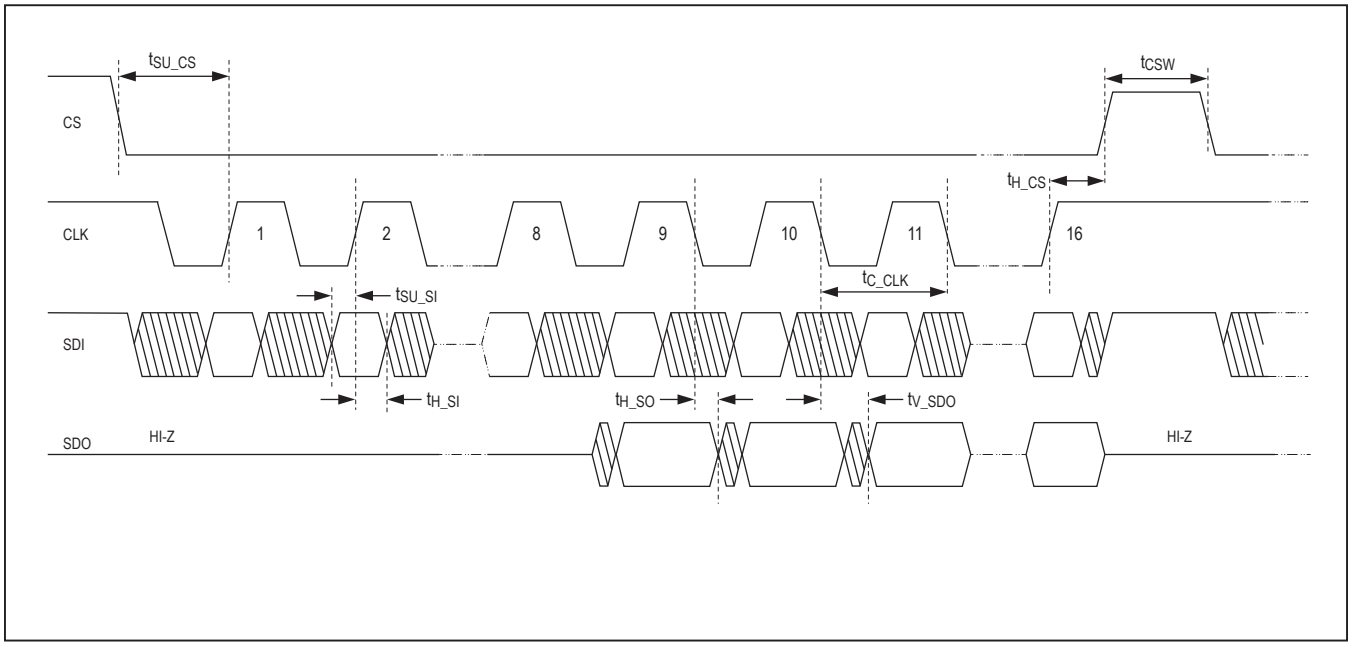
Electrical Characteristics (continued)

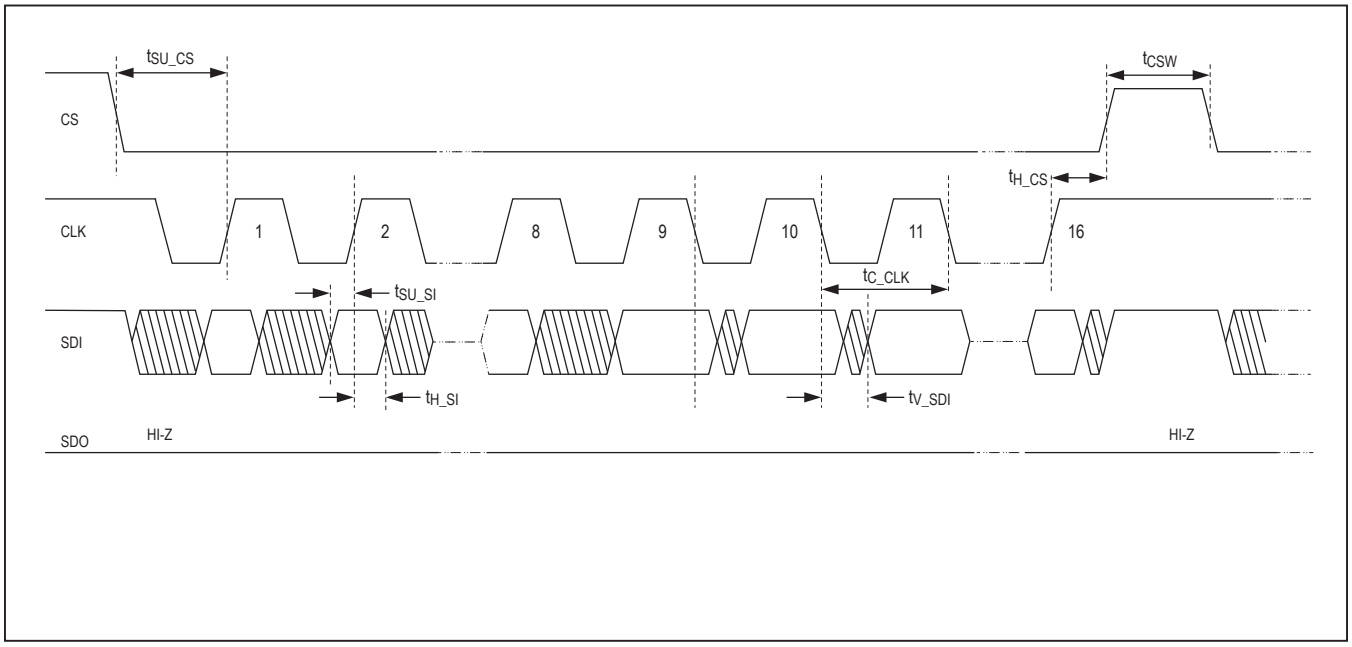
(V_{DD} = V_{DDIO} = 2.5V, T_A = -40°C to +85°C, INT1, INT2, **SDA and SCL are unconnected**, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
IO DC SPECIFICATIONS (Note 5)						
Input Threshold Low	V_{IL}	T_A = +25°C			+0.3 x V_{DDIO}	V
Input Threshold High	V_{IH}	T_A = +25°C	0.7 x V_{DDIO}			V
Hysteresis of Schmitt Trigger input	V_{HYS}	T_A = +25°C	0.05 x V_{DDIO}			V
Output Current (Note 8)	I_{OH}/I_{OL}	I2C_CFG[3:2] = 00		3		mA
		I2C_CFG[3:2] = 01		6		mA
		I2C_CFG[3:2] = 11		12		mA
SPI SLAVE TIMING VALUES (Note 9)						
CLK Frequency	f_{C_CLK}				10	MHz
CS Setup Time	t_{SU_CS}		6			ns
CS Hold Time	t_{H_CS}		12			ns
SDI Input Setup Time	t_{SU_SI}		6			ns
SDI Input Hold Time	t_{H_SI}		12			ns
CLK Fall to SDO Valid Output Time	t_{V_SDO}				50	ns
SDO Output Hold Time	t_{H_SO}		10			ns
ESD PROTECTION						
Human Body Model	HBM			±2.5		kV
Charged Device Model	CDM			500		V

Note 2: Limits are 100% tested at T_A = +25°C, +85°C, and -40°C, unless otherwise noted.
Note 3: V_{DDIO} must be lower or equal than V_{DD} analog.
Note 4: In standby mode, only the drive circuit is powered on. In this condition, the outputs are not available. In this condition, the startup time depends only on the filters responses.
Note 5: Based on characterization results, not production tested.
Note 6: Enable/disable with user selectable bandwidth. Gyro bandwidth accuracy is ±10%. Guaranteed by design.
Note 7: User selectable with 256 possible values from 10kHz down to 5Hz. ODR accuracy is ±10%.
Note 8: User can choose the best output current based on his PCB, interface speed, load, and consumption.
Note 9: 10pF load on SPI lines. Min max based on characterization results.

SPI Timing Diagrams

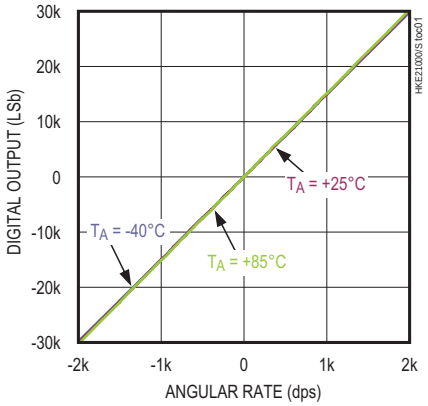




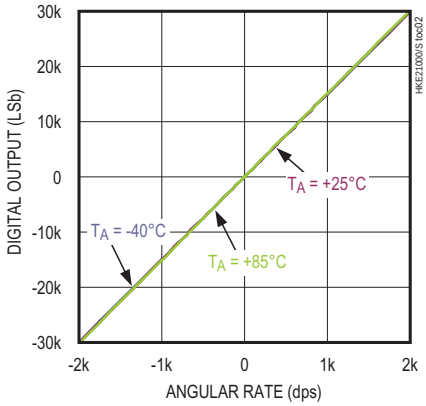
Typical Operating Characteristics

(V_{DD} = V_{DDIO} = 2.5V, T_A = +25ºC, unless otherwise noted.)

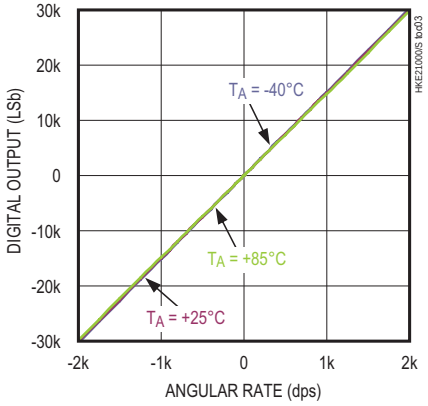
X-AXIS DIGITAL OUTPUT vs. ANGULAR RATE



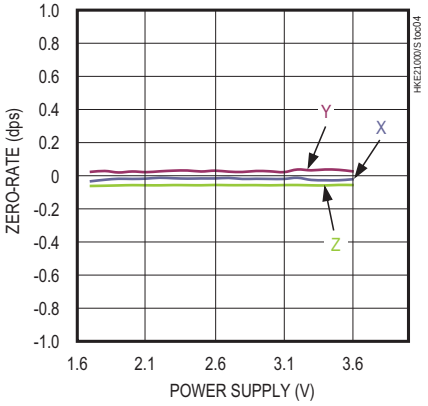
Y-AXIS DIGITAL OUTPUT vs. ANGULAR RATE



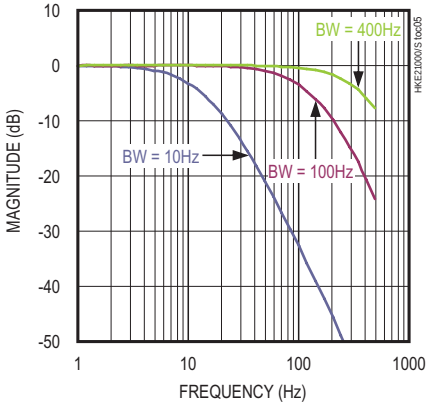
Z-AXIS DIGITAL OUTPUT vs. ANGULAR RATE



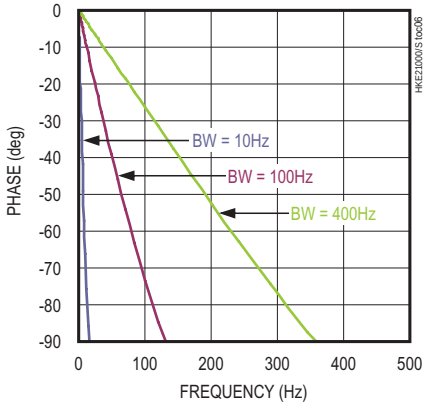
ZERO-RATE LEVEL vs. POWER SUPPLY



MAGNITUDE RESPONSE

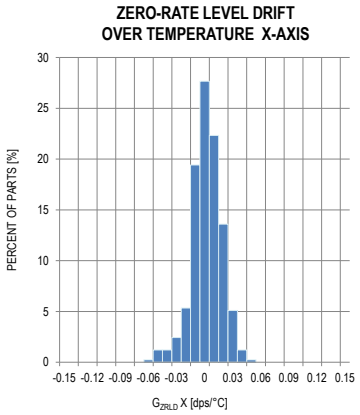


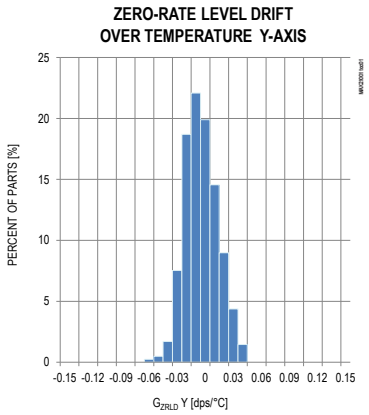
PHASE RESPONSE

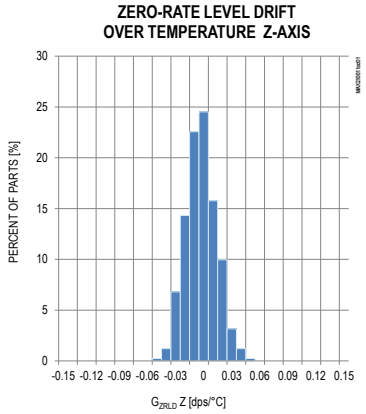


Typical Operating Characteristics

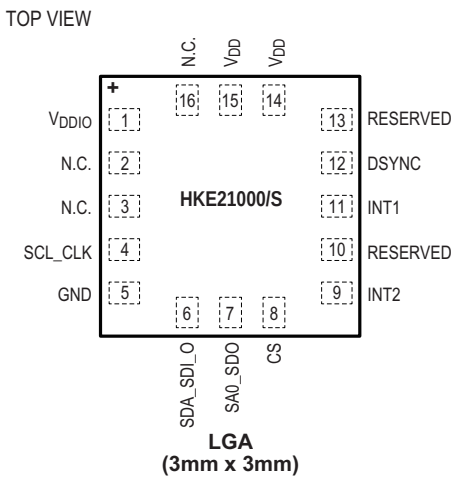
(V_{DD} = V_{DDIO} = 2.5V, T_A = +25ºC, unless otherwise noted.)







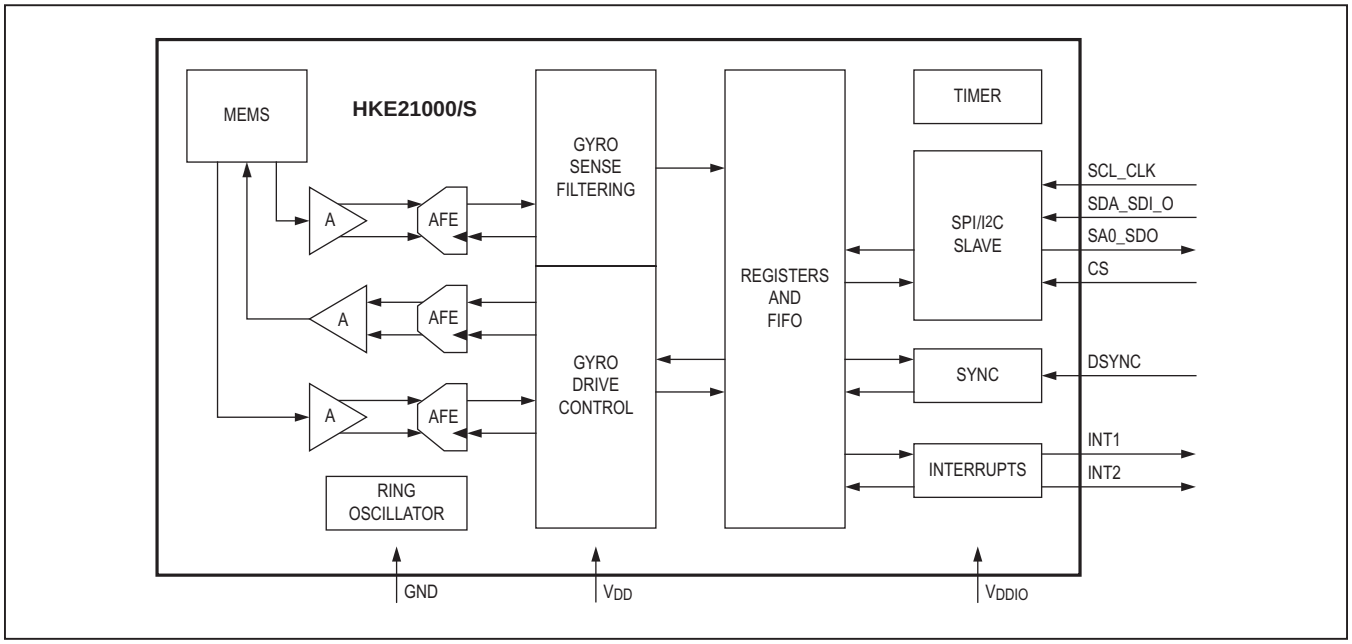
Pin Configuration



Pin Description

PIN	NAME	FUNCTION
1	V_{DDIO}	Interface and Interrupt Pad Supply Voltage
2, 3, 16	N.C.	Not Internally Connected
4	SCL_CLK	SPI and I2C Clock. When in I2C mode, the IO has selectable antispike filter and delay to ensure correct hold time.
5	GND	Power-Supply Ground
6	SDA_SDI_O	SPI In/Out Pin and I2C Serial Data. When in I2C mode, the IO has selectable antispike filter and delay to ensure correct hold time.
7	SA0_SDO	SPI Serial Data Out or I2C Slave Address LSB
8	CS	SPI Chip Select/Serial Interface Selection
9	INT2	Second Interrupt Line
10	RESERVED	Must Be Connected to GND
11	INT1	First Interrupt Line
12	DSYNC	Data Synchronization Pin. Used to wake up the HKE21000/S from power down/standby and synchronize data with GPS/camera.
13	RESERVED	Leave Unconnected
14	V_{DD}	Analog Power Supply. Bypass to GND with a 0.1µF capacitor and one 1µF.
15	V_{DD}	Must be tied to V_{DD} in the application.

Functional Diagram



Detailed Description

The HKE 21000 /S is a low-power, low-voltage, small package 3-axis angular rate sensor able to provide unprecedented accuracy and sensitivity over temperature and time.

The IC is also the industry's first gyroscope available in a 3 mm x 3mm package and capable of working with a supply voltage as low as 1.71V.

It includes a sensing element and an IC interface that provides the measured angular rate to the external world through a digital interface (I2C/SPI).

The IC has a selectable full scale of ±31.25/±62.5/ ±125/±250/±500/±1k/±2k dps. It measures rates with user-selectable bandwidth and ODR.

The IC is available in a 3mm x 3mm x 0.9 mm plastic land grid array (LGA) package and operates over the -40 ºC to +85ºC temperature range.

See the *Definitions* section for more information.

Definitions

Power supply (V): This parameter defines the operating DC power-supply voltage range of the MEMS gyroscope. Although it is always a good practice to keep VDD clean with minimum ripple, unlike most of the competitors, who require an ultra-low noise, low-dropout regulator to power the MEMS gyroscope, the HKE21000/S can not only operate at 1.71V but that supply can also be provided by a switching regular, to minimize the system power consumption.

Power-supply current (mA): This parameter defines the typical current consumption when the MEMS gyroscope is operating in normal mode.

Power-supply current in standby mode (mA): This parameter defines the current consumption when the MEMS gyroscope is in Standby mode. To reduce power consumption and have a faster turn-on time, in Standby mode only an appropriate subset of the sensor is turned off.

Power-supply current in power-down mode (µA): This parameter defines the current consumption when the MEMS gyroscope is powered down. In this mode, both the mechanical sensing structure and reading chain are turned off. Users can configure the control register through the I2C/SPI interface for this mode. Full access to the control registers through the I2C/SPI interface is guaranteed also in power-down mode.

Full-scale range (dps): This parameter defines the measurement range of the gyroscope in degrees per second (dps). When the applied angular velocity is beyond the full-scale range, the gyroscope output signal is saturated.

Zero-rate level (dps): This parameter defines the zero-rate level when there is no angular velocity applied to the gyroscope.

Sensitivity (digit/dps): Sensitivity (digit/dps) is the relationship between 1 LSB and dps. It can be used to convert a digital gyroscope 's measurement in LSBs to angular velocity.

Sensitivity change vs. temperature (%): This parameter defines the sensitivity change in percentage (%) over the operating temperature range specified in the data sheet. **Zero-rate level change vs. temperature (dps):** This parameter defines the zero-rate level change in dps over the operating temperature range.

Non-linearity (% FS): This parameter defines the maximum error between the gyroscope's outputs and the best-fit straight line in percentage with respect to the full-scale (FS) range.

System bandwidth (Hz): This parameter defines the frequency of the angular velocity signal from DC to the built-in bandwidth (BW) that the gyroscopes can measure. A dedicated register can be modified to adjust the gyroscope's bandwidth.

Rate noise density (dps/√Hz): This parameter defines the standard resolution that users can get from the gyroscopes outputs together with the BW parameter.

HKE21000/S Architecture

The HKE21000/S comprises the following key blocks and functions:

- 3-axis MEMS rate gyroscope sensor with 16-bit ADCs and signal conditioning
- Primary I2C and SPI serial communications interfaces
- Sensor data registers
- FIFO
- Synchronization
- Interrupt generators
- Digital output temperature sensor
- Self-test

3-Axis MEMS Gyroscope with 16-Bit ADCs and Signal Conditioning

The IC consists of a single-drive vibratory MEMS gyroscope that detects rotations around the X, Y, and Z axes. When the gyroscope rotates around any of the sensing axes, the Coriolis Force determines a displacement, which can be detected as a capacitive variation. The resulting signal is then processed to produce a digital stream proportional to the angular rate. The analog-to-digital conversion uses 16-bit ADC converters. The gyro full-scale range can be digitally programmed to ±31.25/±62.5/±125/±250/±500/±1000/±2000 dps.

Interrupt Generators

The IC offers two completely independent interrupt generators to ease the SW management of the interrupt generated. For instance, one line could be used to signal a DATA_READY event whilst the other line might be used, for instance, to notify the completion of the internal startup sequence.

Interrupt functionality can be configured through the Interrupt Configuration registers. Configurable items include the INT pin level and duration, the clearing method, as well as the required triggers for the interrupts.

The interrupt status can be read from the Interrupt Status registers. The event that has generated an interrupt is available in two forms: latched and unlatched.

Interrupt sources can be enabled/disabled and cleared individually. The list of possible interrupt sources includes the following conditions: DATA_READY, FIFO_READY, FIFO_THRESHOLD, FIFO_OVERRUN, RESTART, DSYNC.

The interrupt generation can also be configured as latched, unlatched, or timed with programmable length. When configured as latched, the interrupt can be cleared by reading the corresponding status register (clear-on-read) or by writing an appropriate mask to the status register (clear-on-write).

Digital-Output Temperature Sensor

A digital output temperature sensor is used to measure the IC die temperature. The readings from the ADC can be accessed from the Sensor Data registers.

The temperature data is split over 2 bytes. For faster and less accurate reading, accessing the MSB allows to read the temperature data as an absolute value expressed in Celsius degrees (°C). By reading the LSB, the accuracy is greatly increased, up to 256 digit/°C.

Power Modes

The IC features four power modes, allowing selecting the appropriate tradeoff between power consumption, accuracy, and turn-on time.

The transition between power modes can be controlled by software, by explicitly setting a power mode in the Configuration register, or by enabling the automatic power mode transition based on the DSYNC pin.

Normal Mode

In normal mode, the IC is operational with minimum noise level.

Standby Mode

To reduce power consumption and have a shorter turn-on time, the IC features a standby mode. In standby mode, the IC does not generate data, as a significant portion of the signal processing resources is turned off to save power. Still, this mode enables a much quicker turn-on time.

Power-Down Mode

In power-down mode, the IC is configured to minimize the power consumption. In power-down mode, registers can still be read and written, but the gyroscope cannot generate new data. Compared to the standby mode, it takes longer to activate the IC and to start collecting data from the gyroscope.

Digital Interfaces

The registers embedded inside the IC can be accessed through both the I2C and SPI serial interfaces. The latter can be SW-configured to operate either in 3-wire or 4-wire interface mode.

The serial interfaces are mapped onto the same pins. To select/exploit the I2C interface, CS line must be tied high (i.e., connected to V_{DDIO}).

I2C Interface

I2C is a two-wire interface comprised of the signals serial data (SDA) and serial clock (SCL). In general, the lines are open-drain and bidirectional. In a generalized I2C interface implementation, attached devices can be a master or a slave. The master device puts the slave address on the bus, and the slave device with the matching address acknowledges the master.

The IC always operates as a slave device when communicating to the system processor, which thus acts as the master. SDA and SCL lines typically need pullup resistors to V_{DDIO}. The maximum bus speed is 3.4MHz (I2C HS); this reduces the amount of time the system processor is kept busy in supporting the exchange of data.

The slave address of the IC is b101100X, which is 7 bits long. The LSb of the 7-bit address is determined by the logic level on pin SA0. This allows two HKE21000/Ss to be connected on the same I2C bus. When used in this configuration, the address of one of the two devices should be b1011000 (pin SA0_SD0 is set to logic-low) and the address of the other should be b1011001 (pin SA0_SD0 is set to logic-high).

SPI Interface

The IC's SPI can operate up to 10MHz, in both 3-wires (half duplex) and 4-wires mode (full duplex).

Table 1. Power Modes

NAME	DESCRIPTION
Normal	Device is operational with maximum performances.
Standby	In standby mode, the current consumption is reduced by 50%, with a shorter turn-on time of 5ms.
Power-Down	This is the minimum power consumption mode, at the price of a longer turn-on time.

Table 2. Digital Interface Pin Description

NAME	DESCRIPTION
CS	SPI enable and I2C/SPI mode selection (1: I2C mode, 0: SPI enabled)
SCL/CLK	SPI and I2C clock. When in I2C mode, the IO has selectable anti-spike filter and delay to ensure correct hold time.
SDA/SDI/ SDO	SPI in/out pin and I2C serial data. When in I2C mode, the IO has selectable anti-spike filter and delay to ensure correct hold time.
SDO/SA0	SPI serial data out or I2C slave address LSB

Table 3. I2C Address

I2C BASE ADDRESS	SA0/SDO PIN	R/$\overline{W}$ BIT	RESULTING ADDRESS
0x2C (6 bit)	0	0	0xB0
0x2C	0	1	0xB1
0x2C	1	0	0xB2
0x2C	1	1	0xB3

It is recommended to set the I2C_DISABLE bit at address 0x15 if the IC is used together with other SPI devices to avoid the possibility to switch inadvertently into I^2C mode when traffic is detected with the CS unasserted.

The IC operates as an SPI slave device. Both the read register and write register commands are completed in 16 clock pulses, or in multiples of 8 in case of multiple read/write bytes. Bit duration is the time between two falling edges of CLK.

The first bit (bit 0) starts at the first falling edge of CLK after the falling edge of CS while the last bit (bit 15, bit 23, etc.) starts at the last falling edge of CLK just before the rising edge of CS.

Bit 0: RW bit. When 0, the data DI[7:0] is written to the IC. When 1, the data DO[7:0] from the device is read. In the latter case, the chip drives SDO at the start of bit 8.

Bit 1: MS bit. Depending on the configuration of IF_PARITY, this bit can either be used to operate in multi-addressing standard mode or to check the parity with the register address.

If used as MS bit, when 1, the address remains unchanged in multiple read/write commands. When 0, the address is autoincremented in multiple read/write commands.

Bits 2–7: Address AD[5:0]. This is the address field of the indexed register.

Bits 8–15: Data DI[7:0] (write mode). This is the data that is written to the device (MSb first).

Bits 8–15: Data DO[7:0] (read mode). This is the data that is read from the device (MSb first).

SPI Half- and Full-Duplex Operation

The IC can be programmed to operate in half-duplex (a bidirectional data pin) or full-duplex (one data-in and one data-out pin) mode. The SPI master sets a register bit called SPI_3_WIRE into ITF_OTP to 0 for full-duplex, and 1 for half-duplex operation. Full duplex is the power-on default.

Full-Duplex Operation

The IC is put into full-duplex mode at power-up, or when the SPI master clears the SPI_3_WIRE bit, the SPI interface uses separate data pins, SDI and SDO to transfer data. Because of the separate data pins, bits can be simultaneously clocked into and out of the IC. The IC makes use of this feature by clocking out 8 output data bits as the command byte is clocked in.

Reading from the SPI Slave Interface (SDO)

The SPI master reads data from the IC slave interface using the following steps:

1) When CS is high, the IC is unselected and three-states the SDO output.
2) After driving SCL_CLK to its inactive state, the SPI master selects the IC by driving CS low.
3) The SPI master simultaneously clocks the command byte into the HKE21000/S. The SPI Read command is performed with 16 clock pulses. Multiple byte read command is performed adding blocks of 8 clock pulses at the previous one.

   Bit 0: READ bit. The value is 1.

   Bit 1: MS bit. When 1, do not increment address. When 0, increment address in multiple reading.

   Bits 2–7: address AD[5:0]. This is the address field of the indexed register.

   Bits 8–15: data DO[7:0] (read mode). This is the data that is read from the device (MSb first).

   Bits 16–... : data DO[...–8]. Further data in multiple byte reading.
4) After 16 clock cycles, the master can drive CS high to deselect the IC, causing it to three-state its SDO output. The falling edge of the clock puts the MSB of the next data byte in the sequence on the SDO output.
5) By keeping CS low, the master clocks register data bytes out of the IC by continuing to supply SCL_CLK pulses (burst mode). The master terminates the transfer by driving CS high. The master must ensure that SCL_CLK is in its inactive state at the beginning of the next access (when it drives CS low).

Writing to the SPI Slave Interface (SDI)

The SPI master writes data to the IC slave interface through the following steps:

1) The SPI master sets the clock to its inactive state . When CS is high, the master can drive the SDI input.
2) The SPI master selects the HKE21000/S by driving CS low.
3) The SPI master simultaneously clocks the command byte into the IC. The SPI write command is performed with 16 clock pulses . Multiple byte write command is performed adding blocks of 8 clock pulses at the previ- ous one.

   Bit 0: WRITE bit. The value is 0.

   Bit 1: MS bit. When 1, do not increment address, when 0, increment address in multiple writing.

   Bits 2–7: address AD[5:0]. This is the address field of the indexed register.

   Bits 8–15: data DI[7:0] (write mode). This is the data that is written inside the device (MSb first).

   Bits 16–... : data DI[...–8]. Further data in multiple byte writing.
4) By keeping CS low, the master clocks data bytes into the IC by continuing to supply SCL_CLK pulses (burst mode). The master terminates the transfer by driving CS high . The master must ensure that SCL_CLK is inactive at the beginning of the next access (when it drives CS low). In full-duplex mode, the IC outputs data bits on SDO during the first 8 bits (the command byte), and subsequently outputs zeros on SDO as the SPI master clocks bytes into SDI.

Half-Duplex Operation

When the SPI master sets SPI_3_WIRE = 1, the IC is put into half-duplex mode . In half-duplex mode , the IC three-states its SDO pin and makes the SDI pin bidirectional , saving a pin in the SPI interface . The SDO pin can be left unconnected in half-duplex operation . The SPI master must operate the SDI pin as bidirectional . It accesses a IC register as follows : the SPI master sets the clock to its inactive state . While CS is high , the master can drive the SDI pin to any value.

1) The SPI master selects the IC by driving CS low and placing the first data bit (MSB) to write on the SDI input.
2) The SPI master turns on its output driver and clocks the command byte into the IC . The SPI read command is performed with 16 clock pulses:

   Bit 0: READ bit. The value is 1.

   Bit 1: MS bit. When 1, do not increment address. When 0, increment address in multiple readings.

   Bit 2–7: Address AD[5:0]. This is the address field of the indexed register.

   Bit 8–15: data DO[7:0] (read mode). This is the data that is read from the device (MSb first). Multiple read command is also available in 3-wire mode.

Sensor Data Registers

The sensor data registers contain the latest gyroscope and temperature measurement data.

They are read-only registers and are accessed through the serial interface. Data from these registers can be read anytime. However, the interrupt function can be used to determine when new data is available.

FIFO

The IC embeds a 256-slot of a 16-bit data FIFO for each of the three output channels: yaw, pitch, and roll. This allows a consistent power saving for the system since the host processor does not need to continuously poll data from the sensor, but it can wake up only when needed and burst the significant data out from the FIFO. When configured in Snapshot mode, it offers the ideal mechanism to capture the data following a Rate Interrupt event.

This buffer can work according to four main modes: off, normal, interrupt, and snapshot.

Both Normal and Interrupt modes can be optionally configured to operate in overrun mode, depending on whether, in case of buffer under-run, newer or older data are lost.

Various FIFO status flags can be enabled to generate interrupt events on INT1/INT2 pin.

FIFO Off Mode

In this mode, the FIFO is turned off; data are stored only in the data registers and no data are available from the FIFO if read.

When the FIFO is turned off, there are essentially two options to use the device: synchronous and asynchronous reading.

Synchronous Reading

In this mode, the processor reads the data set (e.g., 6 bytes for a 3 axes configuration) generated by the IC every time that DATA_READY is set. The processor must read once and only once the data set in order to avoid data inconsistencies.

Benefits of using this approach include the perfect reconstruction of the signal coming the gyroscope and minimum data traffic.

Asynchronous Reading

In this mode, the processor reads the data generated by the IC regardless the status of the DATA_READY flag. To minimize the error caused by different samples being read a different number of times, the access frequency to be used must be much higher than the selected ODR (e.g., 10x). This approach normally requires a much higher BW.

FIFO Normal Mode

Overrun = false

- FIFO is turned on.
- FIFO is filled with the data at the selected output data rate (ODR).
- When FIFO is full, an interrupt can be generated.
- When FIFO is full, all the new incoming data is discharged. Reading only a subset of the data already stored into the FIFO keeps locked the possibility for new data to be written.
- Only if all the data are read, the FIFO restarts saving data.
- If communication speed is high, data loss can be prevented.
- To prevent a FIFO-FULL condition, the required condition is to complete the reading of the data set before the next DATA_READY occurs.
- If this condition is not guaranteed, data can be lost.

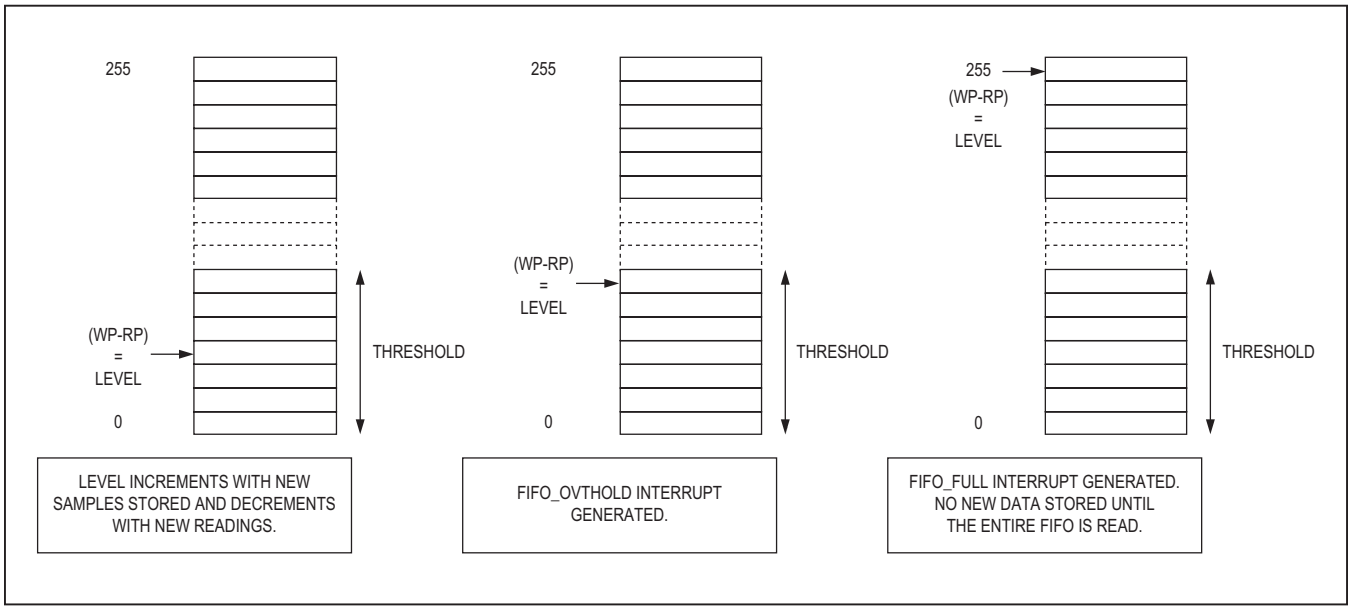


Figure 1. FIFO Normal Mode, Overrun = False

Overrun = true

- FIFO is turned on.
- FIFO is filled with the data at the selected ODR.
- When FIFO is full, an interrupt can be generated.
- When FIFO is full, the oldest data is overwritten-with the new ones.
- If communication speed is high, data integrity can be preserved.
- To prevent a DATA_LOST condition, the required condition is to complete the reading of the data set before the next DATA_READY occurs.
- If this condition is not guaranteed, data can be overwritten.
- When an overrun condition occurs the reading pointer is forced to writing pointer -1 to ensure only older data are discarded and newer data have a chance to be read.

Interrupt Mode

Overrun = false

- FIFO is initially disabled. Data are stored only in the data registers.
- When a rate interrupt (either OR or AND) is generated, the FIFO is turned on automatically. It stores the data at the selected ODR.
- When FIFO is full, all the new incoming data is discharged. Reading only a subset of the data already stored into the FIFO keeps locked the possibility for new data to be written.
- Only if all the data are read, the FIFO restarts saving data.
- If communication speed is high, data loss can be prevented.
- To prevent a FIFO-FULL condition, the required condition is to complete the reading of the data set before the next DATA_READY occurs.
- If this condition is not guaranteed, data can be lost.

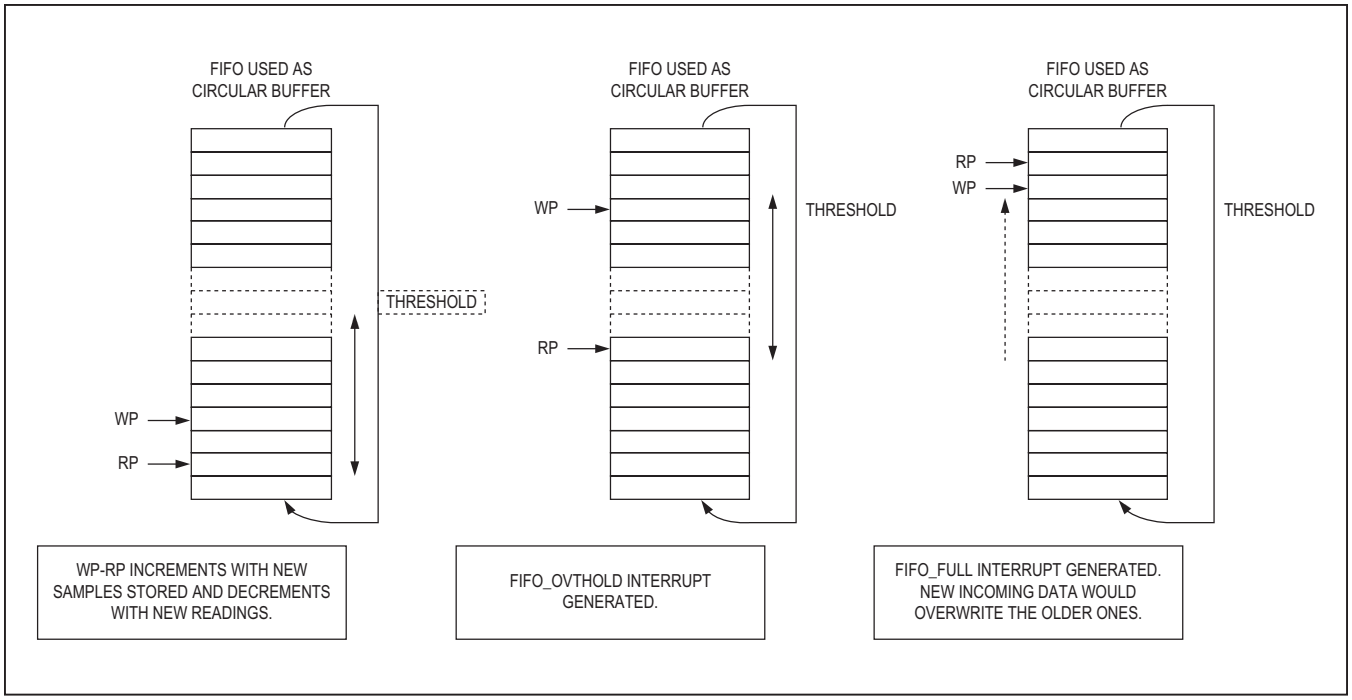


Figure 2. FIFO Normal Mode, Overrun = True

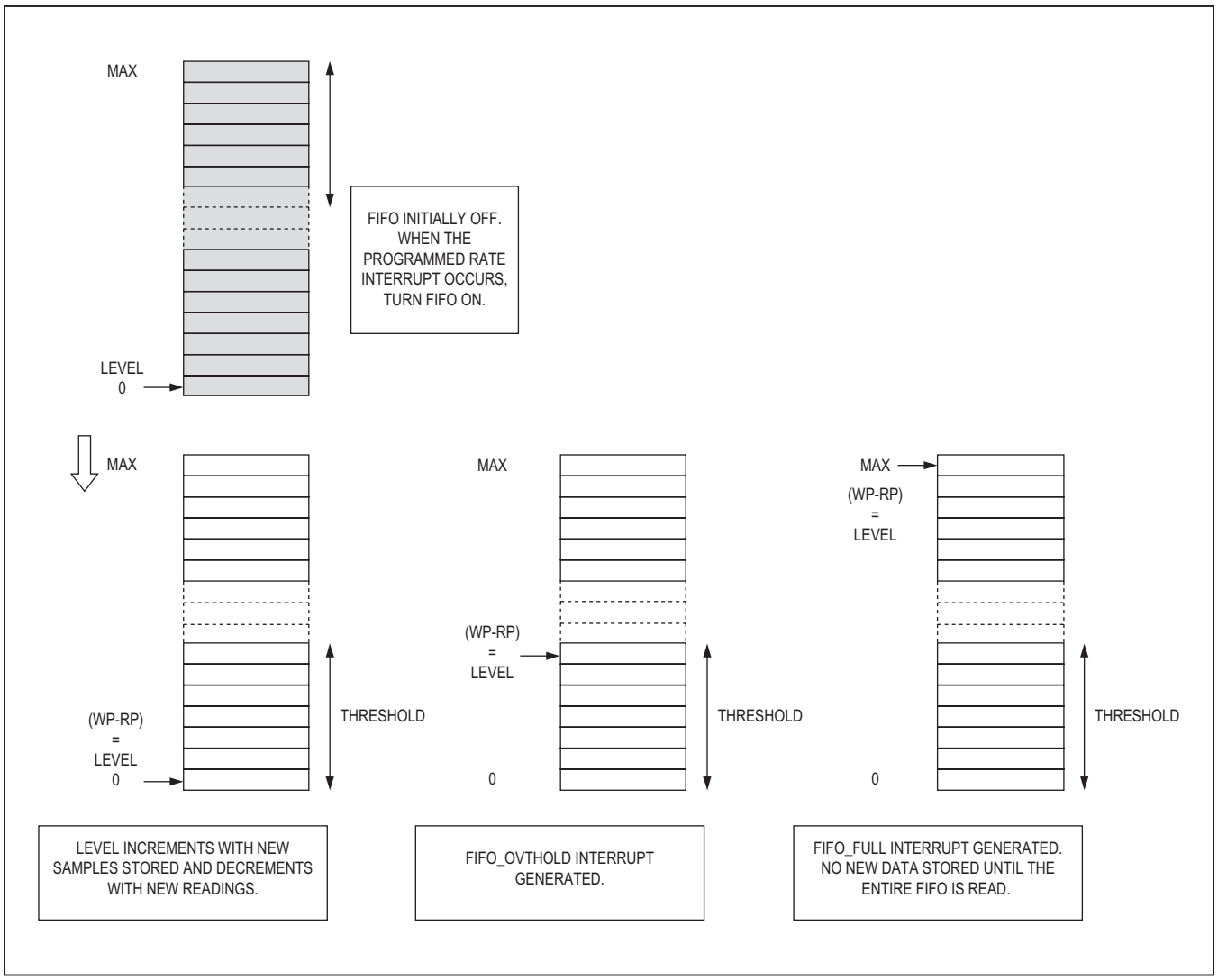


Figure 3. FIFO Interrupt Mode, Overrun = False

Overrun = true

- FIFO is initially disabled. Data are stored only in the data registers.
- When a Rate Interrupt (either OR or AND) is generated, the FIFO is turned on automatically. It stores the data at the selected ODR.
- When FIFO is full, an interrupt can be generated.
- When FIFO is full, the oldest data is overwritten with the new ones.
- If communication speed is high, data integrity can be preserved.
- In order to prevent a DATA_LOST condition, the required condition is to complete the reading of the data set before the next DATA_READY occurs.
- If this condition is not guaranteed, data can be overwritten.
- When an overrun condition occurs, the reading pointer is forced to writing pointer -1 to ensure only older data are discarded and newer data have a chance to be read.

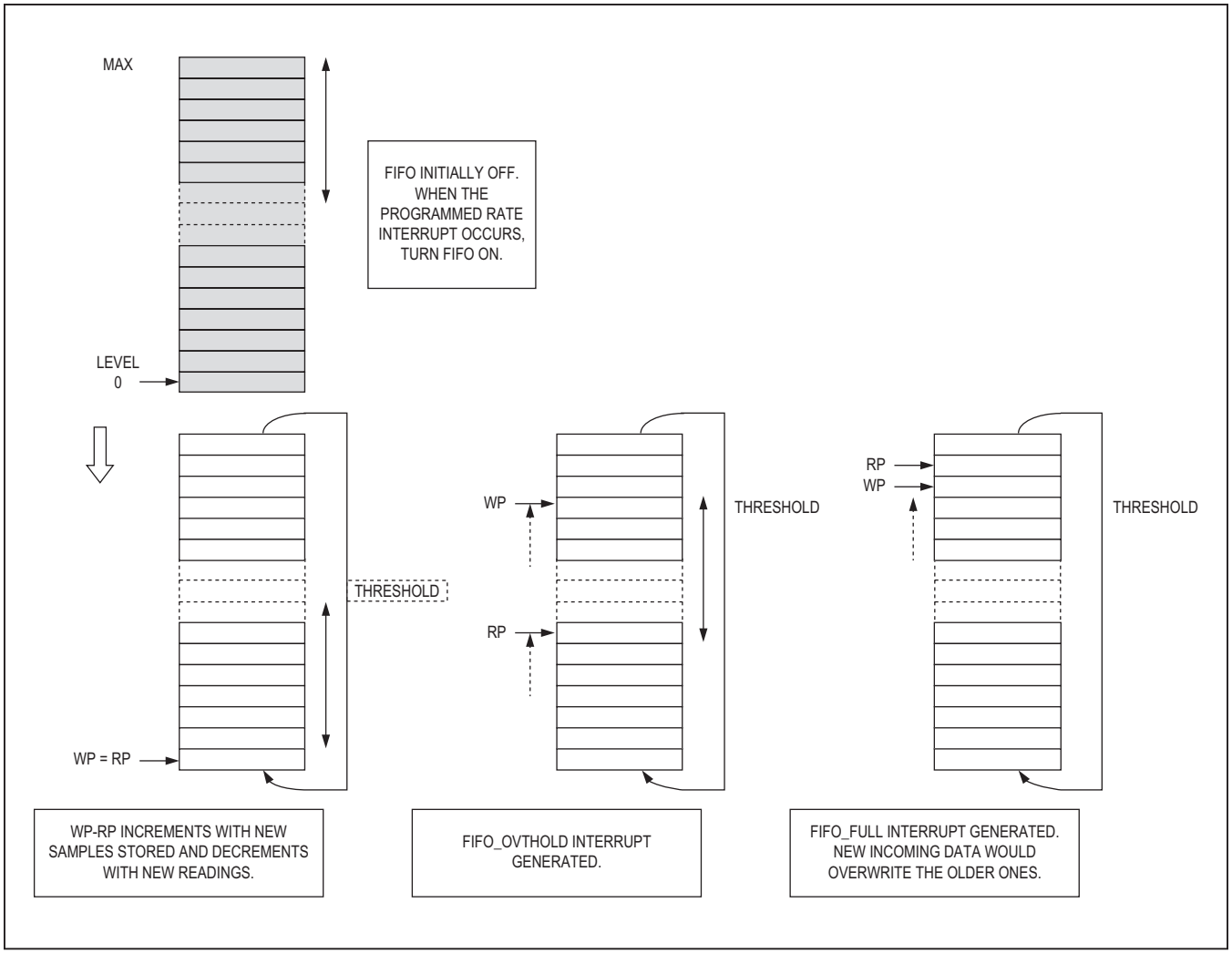


Figure 4. FIFO Interrupt Mode, Overrun = True

Snapshot Mode

- FIFO is initially in normal mode with overrun enabled.
- When a Rate Interrupt (either OR or AND) is generated, the FIFO switches automatically to not-overrun mode. It stores the data at the selected ODR until the FIFO becomes full.
- When FIFO is full, an interrupt can be generated.
- When FIFO is full, all the new incoming data is discharged. Reading only a subset of the data already stored into the FIFO keeps locked the possibility for new data to be written.
- Only if all the data are read the FIFO restarts saving data.
- If communication speed is high, data loss can be prevented.
- To prevent a FIFO_FULL condition, the required condition is to complete the reading of the data set before the next DATA_READY occurs.
- If this condition is not guaranteed, data can be lost.

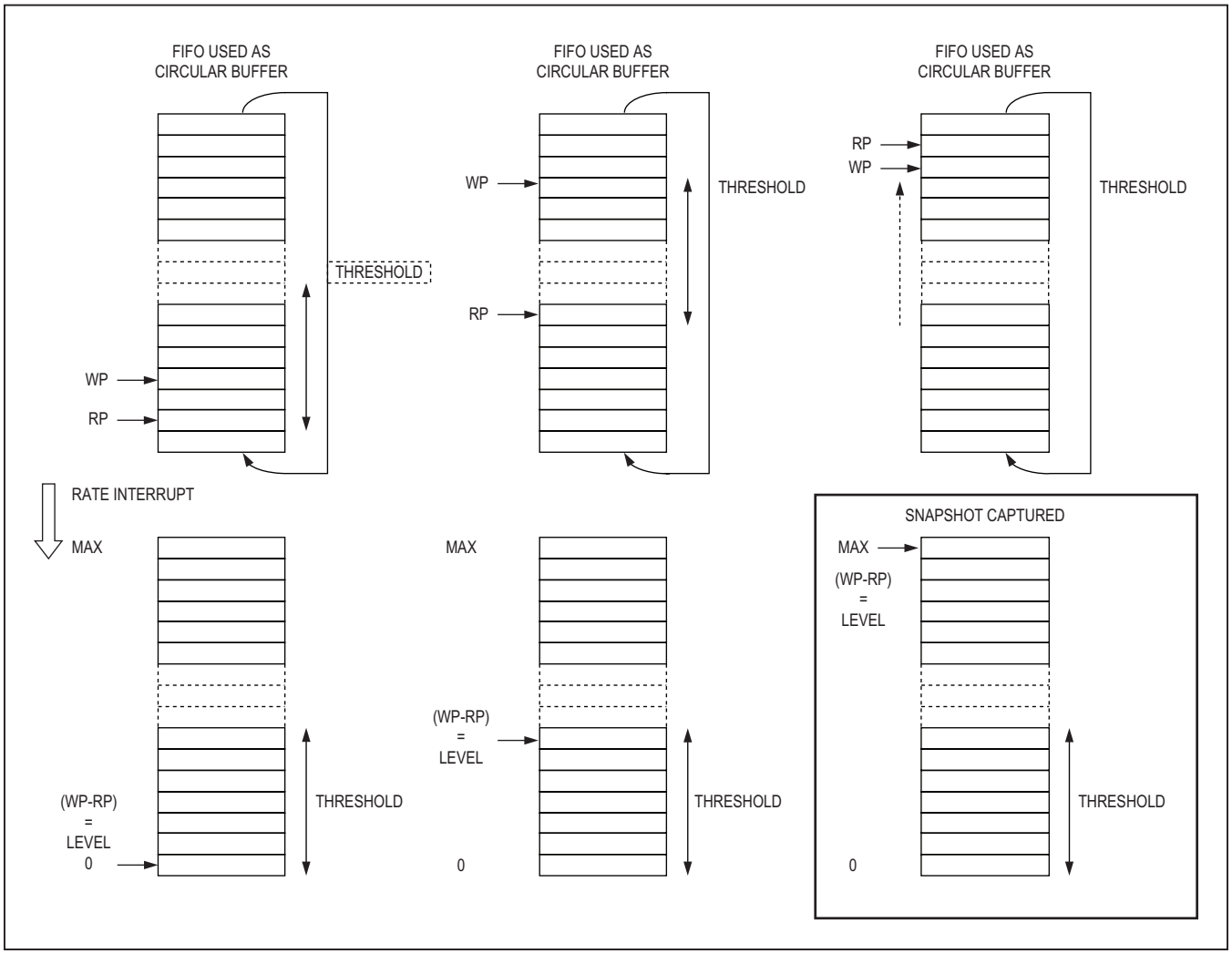


Figure 5. FIFO Snapshot Mode

Bias Instability and Angular Random Walk

Bias instability is a critical performance parameter for gyroscopes. The IC provides a typical bias instability of 4°/hour on each axis and an ARW of 0.45°/√hour, measured using the Allan Variance method.

Data Synchronization

The DSYNC pin enables a number of synchronization options.

Wake-Up Feature

The DSYNC pin can be used to wake-up the IC from the power-down or suspend mode. Repeatedly changing DSYNC from active to not active and vice-versa can be used to control the power mode of the IC using an external controlling device, be it a microprocessor, another sensor or a different kind of device.

DSYNC can be configured to active either high or low and on either edge or level. This feature is controlled by a specific bit in the DSYNC_CFG register.

Data Capture Feature

Another way to use the DSYNC pin is as data capture trigger. The IC can be configured to stop generating data until a given edge occur on DSYNC. Once the programmed active edge occurs, the IC collects as many data as specified in the DSYNC_CNT register.

DSYNC Mapping on Data

DSYNC can also be optionally mapped onto the LSB of the sensor data to perform synchronization afterwards. The mapping occurs on every enabled axis of the gyroscope. This feature is controlled by a specific bit in the DSYNC_CFG register.

DSYNC Interrupt Generation

The DSYNC pin can also be used as an interrupt source to determine a different kind of data synchronization based on the software management performed by an external processor.

The DSYNC-based wake-up, data capture, data mapping, and interrupt generation features can be combined together.

Unique Serial Number

Each IC is uniquely identified by 48 bits that can be used to track the history of the sample, including manufacturing, assembly, and testing information. Note that this serial number is simply a set of 48 out of the 512 total trimming bits. Therefore, its univocity is not guaranteed by design.

Self-Test

For digital gyroscopes, there are two dedicated bits in a control register to enable the self-test. This feature can be used to verify if the gyroscope is working properly without physically rotating the gyroscope. That may be used either before or after it is assembled on a PCB. If the gyroscope's outputs are within the specified self-test values in the data sheet, then the gyroscope is working properly. Therefore, the self-test feature is an important consideration in a user's end-product mass production line.

The embedded self-test in Hanking's 3-axis digital gyroscope is an additional key feature that allows the gyroscope to be tested during final product assembly without requiring physical device movement.

Register File

The register file is organized per banks. On the common bank are mapped addresses from 0x20 to 0x3F and these registers are always available. It is possible to map on addresses 0x00 to 0x1F two different user banks by properly programming address 0x21. The purpose of this structure is to limit the management of the register map addresses in the 0x00 to 0x3F range even though the number of physical registers is in excess of 64.

Common Bank

The common is the bank whose locations are always available regardless the register bank selection.

This bank contains all the registers most commonly used, including data registers and the FIFO data.

Table 4. Common Bank

NAME	REGISTER ADDRESS	TYPE	DEFAULT VALUE	COMMENT
WHO_AM_I	0x20	R	1011 0001	Device ID
BANK_SELECT	0x21	RW	0000 0000	Register bank selection
SYSTEM_STATUS	0x22	R	0000 0000	System Status register
GYRO_X_H	0x23	R	Data	Bits [15:8] of X measurement
GYRO_X_L	0x24	R	Data	Bits [07:0] of X measurement
GYRO_Y_H	0x25	R	Data	Bits [15:8] of Y measurement
GYRO_Y_L	0x26	R	Data	Bits [07:0] of Y measurement
GYRO_Z_H	0x27	R	Data	Bits [15:8] of Z measurement
GYRO_Z_L	0x28	R	Data	Bits [07:0] of Z measurement
TEMP_H	0x29	R	Data	Bits [15:8] of T measurement
TEMP_L	0x2A	R	Data	Bits [07:0] of T measurement
RFU	0x2B	R	0000 0000	
RFU	0x2C	R	0000 0000	
RFU	0x2D	R	0000 0000	
RFU	0x2E	R	0000 0000	
RFU	0x2F	R	0000 0000	
RFU	0x30	R	0000 0000	
RFU	0x31	R	0000 0000	
RFU	0x32	R	0000 0000	
RFU	0x33	R	0000 0000	
RFU	0x34	R	0000 0000	
RFU	0x35	R	0000 0000	
RFU	0x36	R	0000 0000	
RFU	0x37	R	0000 0000	
RFU	0x38	R	0000 0000	
RFU	0x39	R	0000 0000	
RFU	0x3A	R	0000 0000	
HP_RST	0x3B	RW	0000 0000	Highpass filter reset
FIFO_COUNT	0x3C	R	0000 0000	Available FIFO samples for data set
FIFO_STATUS	0x3D	R	0000 0000	FIFO status flags
FIFO_DATA	0x3E	R	Data	FIFO data to be read in burst mode
PAR_RST	0x3F	W and reset	0000 0000	Parity reset (reset on write)

User Bank 0

User bank 0 is the register used to configure most of the features of the IC, with the exception of the interrupts, which are part of the user bank 1.

Table 5. User Bank 0

NAME	REGISTER ADDRESS	TYPE	DEFAULT VALUE	COMMENT
POWER_CFG	0x00	RW	0000 0111	Power mode configuration
SENSE_CFG1	0x01	RW	0010 1000	Sense configuration: LP and OIS
SENSE_CFG2	0x02	RW	0010 0011	Sense configuration: ODR
SENSE_CFG3	0x03	RW	0000 0000	Sense configuration: HP
RFU	0x04	R	0000 0000	
RFU	0x05	R	0000 0000	
RFU	0x06	R	0000 0000	
RFU	0x07	R	0000 0000	
RFU	0x08	R	0000 0000	
RFU	0x09	R	0000 0000	
RFU	0x0A	R	0000 0000	
RFU	0x0B	R	0000 0000	
RFU	0x0C	R	0000 0000	
RFU	0x0D	R	0000 0000	
RFU	0x0E	R	0000 0000	
RFU	0x0F	R	0000 0000	
RFU	0x10	R	0000 0000	
RFU	0x11	R	0000 0000	
RFU	0x12	R	0000 0000	
DR_CFG	0x13	RW	0000 0001	Data ready configuration
IO_CFG	0x14	RW	0000 0000	Input/output configuration
I2C_CFG	0x15	RW	0000 0100	I^2C configuration
ITF_OTP	0x16	RW	0000 0000	Interface and OTP configuration
FIFO_TH	0x17	RW	0000 0000	FIFO threshold configuration
FIFO_CFG	0x18	RW	0000 0000	FIFO mode configuration
RFU	0x19	R	0000 0000	
DSYNC_CFG	0x1A	R	0000 0000	DATA_SYNC configuration
DSYNC_CNT	0x1B	R	0000 0000	DATA_SYNC counter
RFU	0x1C	R	0000 0000	
RFU	0x1D	R	0000 0000	
RFU	0x1E	R	0000 0000	
RFU	0x1F	R	0000 0000	

User Bank 1

User Bank 1 is primarily devoted to the configuration of the interrupts. It also contains the unique serial number.

Table 6. User Bank 1

NAME	REGISTER ADDRESS	TYPE	DEFAULT VALUE	COMMENT
INT_REF_X	0x00	RW	0000 0000	Interrupt reference for X axis
INT_REF_Y	0x01	RW	0000 0000	Interrupt reference for Y axis
INT_REF_Z	0x02	RW	0000 0000	Interrupt reference for Z axis
INT_DEB_X	0x03	RW	0000 0000	Interrupt debounce, X
INT_DEB_Y	0x04	RW	0000 0000	Interrupt debounce, Y
INT_DEB_Z	0x05	RW	0000 0000	Interrupt debounce, Z
INT_MSK_X	0x06	RW	0000 0000	Interrupt mask, X axis zones
INT_MSK_Y	0x07	RW	0000 0000	Interrupt mask, Y axis zones
INT_MSK_Z	0x08	RW	0000 0000	Interrupt mask, Z axis zones
INT_MASK_AO	0x09	RW	0000 0000	Interrupt masks, AND/OR
INT_CFG1	0x0A	RW	0000 0000	Interrupt configuration 1
INT_CFG2	0x0B	RW	0010 0100	Interrupt configuration 2
INT_TMO	0x0C	RW	0000 0000	Interrupt timeout
INT_STS_UL	0x0D	R	0000 0000	Interrupt sources, unlatched
INT1_STS	0x0E	R	0000 0000	Interrupt 1 status, latched
INT2_STS	0x0F	R	0000 0000	Interrupt 2 status, latched
INT1_MSK	0x10	RW	1000 0000	Interrupt 1 mask
INT2_MSK	0x11	RW	0000 0010	Interrupt 2 mask
RFU	0x12	R	0000 0000	
RFU	0x13	R	0000 0000	
RFU	0x14	R	0000 0000	
RFU	0x15	R	0000 0000	
RFU	0x16	R	0000 0000	
RFU	0x17	R	0000 0000	
RFU	0x18	R	0000 0000	
RFU	0x19	R	0000 0000	
SERIAL_0	0x1A	R	Variable	Unique serial number, byte 0
SERIAL_1	0x1B	R	Variable	Unique serial number, byte 1
SERIAL_2	0x1C	R	Variable	Unique serial number, byte 2
SERIAL_3	0x1D	R	Variable	Unique serial number, byte 3
SERIAL_4	0x1E	R	Variable	Unique serial number, byte 4
SERIAL_5	0x1F	R	Variable	Unique serial number, byte 5

Orientation of Axes

The diagram below shows the orientation of the axes of sensitivity and the polarity of rotation. Note the pin 1 identifier (•) in Figure 6.

Soldering Information

Visit **www.hankingmems.com/HKE21001S.related** for soldering recommendations.

Application Notes

Bypass V_{DD} and V_{DDIO} to the ground plane with 0.1µF ceramic chip capacitors on each pin as close as possible to the IC to minimize parasitic inductance.

Depending on the specific application, add at least one bulk 1µF decoupling capacitor to V_{DD} and V_{DDIO} per PCB. For best performance, keep separate V_{DD} and V_{DDIO} power supplies.

Table 7. Bill of Materials for External Components

COMPONENT	LABEL	SPECIFICATION	QUANTITY
V_{DD}/V_{DDIO} bypass capacitor	C1	Ceramic, X7R, 0.1µF ±10%, 4V	1
V_{DD}/V_{DDIO} bypass capacitor	C2	Ceramic, X7R, 1µF ±10%, 4V	1

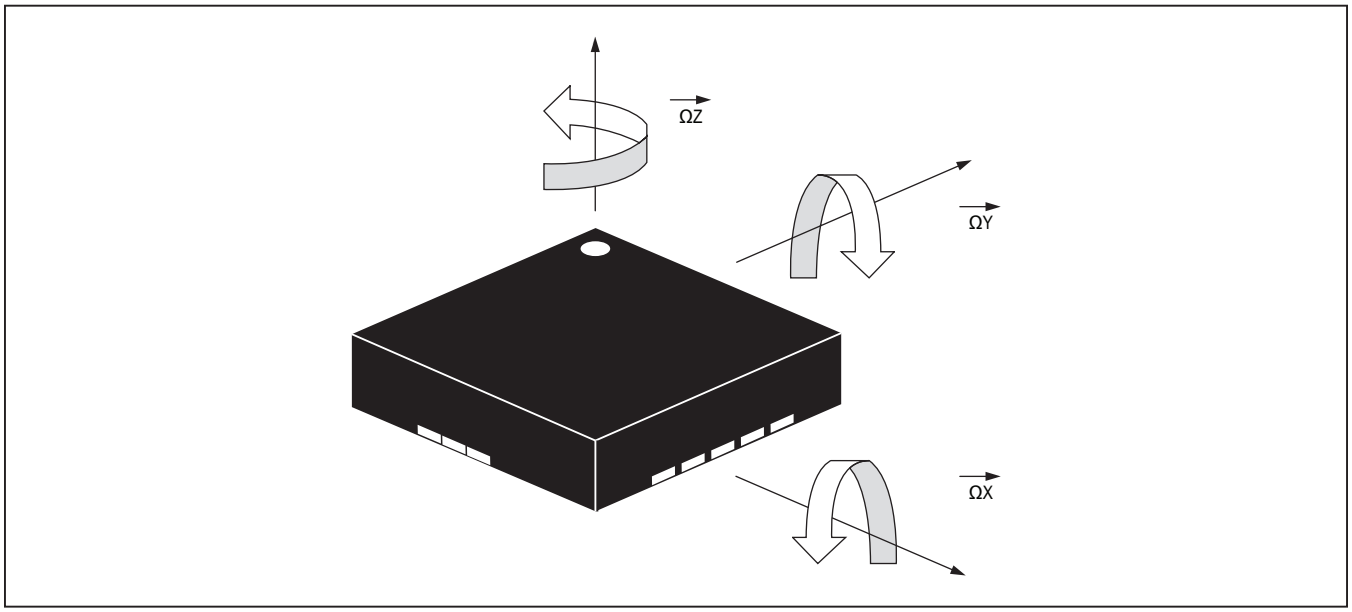
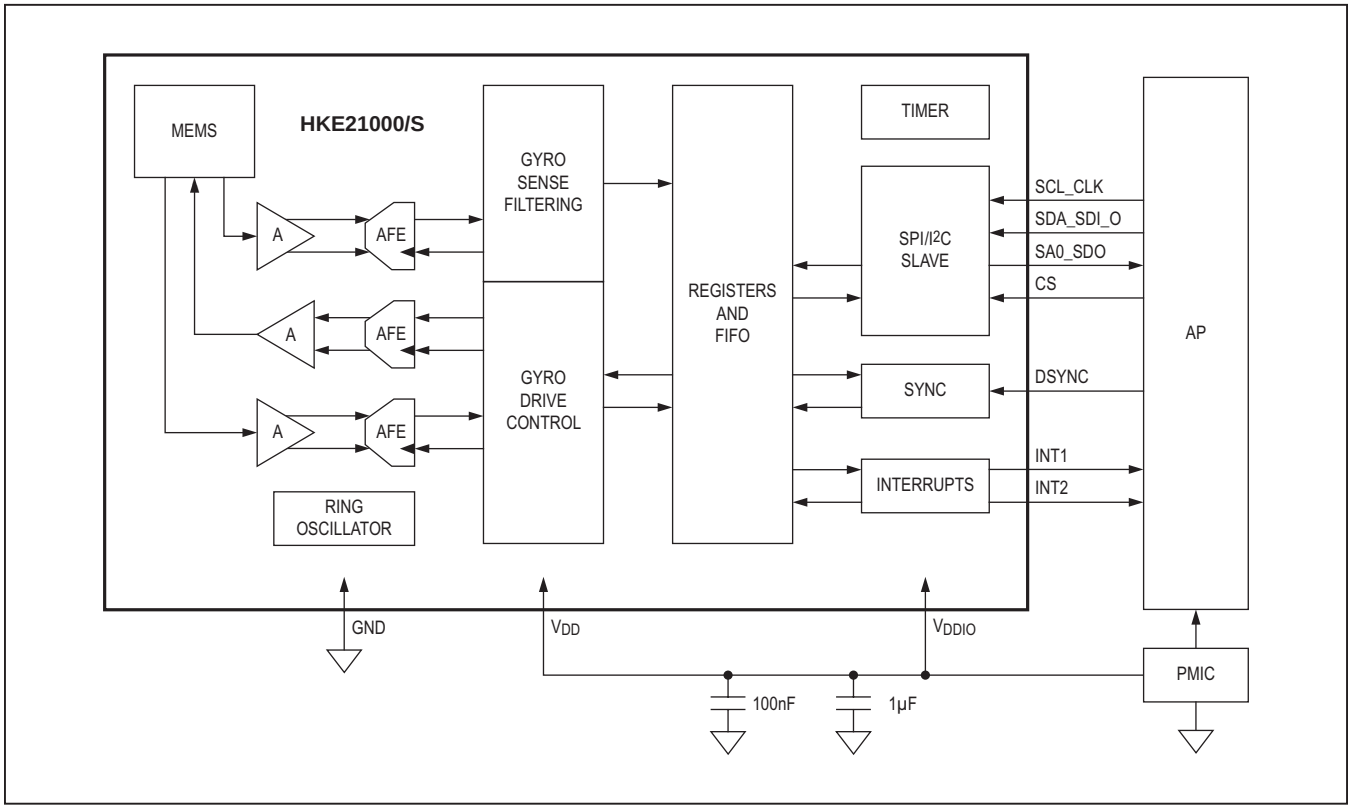


Figure 6. Orientation of Axes

Typical Application Circuit



Ordering Information

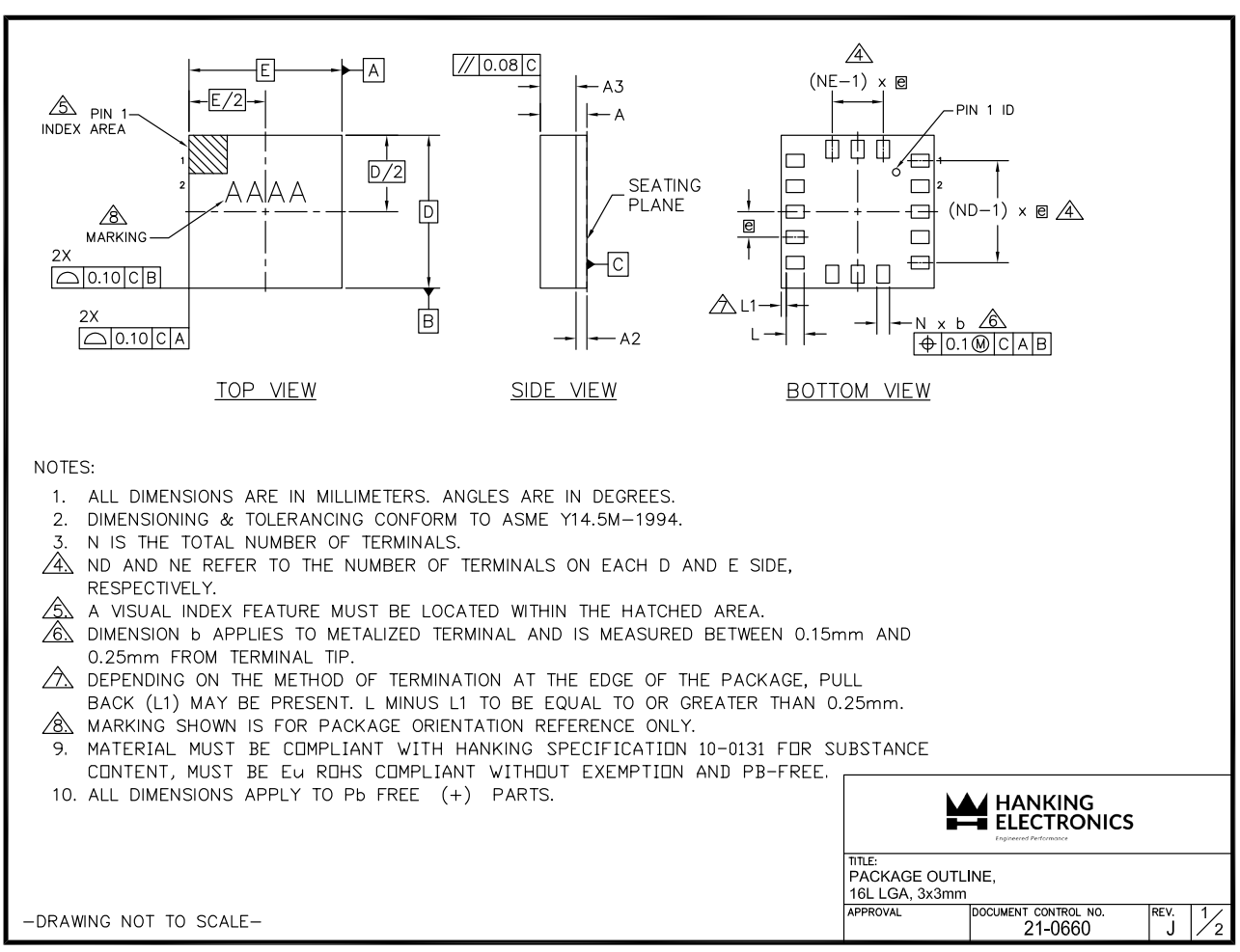
PART	TEMP RANGE	PIN-PACKAGE
HKE21000/S+	-40°C to +85°C	16 LGA
HKE21000/S+T	-40°C to +85°C	16 LGA

+Denotes lead(Pb)-free/RoHS-compliant package.

T = Tape and reel.

Package Information

For the latest package outline information and land patterns (footprints), go to **www.hankingmems.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.



NOTES:

1. ALL DIMENSIONS ARE IN MILLIMETERS. ANGLES ARE IN DEGREES.
2. DIMENSIONING & TOLERANCING CONFORM TO ASME Y14.5M–1994.
3. N IS THE TOTAL NUMBER OF TERMINALS.
4. ND AND NE REFER TO THE NUMBER OF TERMINALS ON EACH D AND E SIDE, RESPECTIVELY.
5. A VISUAL INDEX FEATURE MUST BE LOCATED WITHIN THE HATCHED AREA.
6. DIMENSION b APPLIES TO METALIZED TERMINAL AND IS MEASURED BETWEEN 0.15mm AND 0.25mm FROM TERMINAL TIP.
7. DEPENDING ON THE METHOD OF TERMINATION AT THE EDGE OF THE PACKAGE, PULL BACK (L1) MAY BE PRESENT. L MINUS L1 TO BE EQUAL TO OR GREATER THAN 0.25mm.
8. MARKING SHOWN IS FOR PACKAGE ORIENTATION REFERENCE ONLY.
9. MATERIAL MUST BE COMPLIANT WITH HANKING SPECIFICATION 10-0131 FOR SUBSTANCE CONTENT, MUST BE Eu ROHS COMPLIANT WITHOUT EXEMPTION AND PB-FREE.
10. ALL DIMENSIONS APPLY TO Pb FREE (+) PARTS.

–DRAWING NOT TO SCALE–

HANKING ELECTRONICS
Engineered Performance

TITLE: PACKAGE OUTLINE, 16L LGA, 3x3mm			
APPROVAL	DOCUMENT CONTROL NO. 21-0660	REV. J	1/2

Package Information (continued)

For the latest package outline information and land patterns (footprints), go to **www.hankingmems.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

REF.	MIN.	NOM.	MAX.
A	0.80	0.90	1.00
A2		0.21 REF	
A3	0.65	0.70	0.75
b	0.20	0.25	0.30
D		3.00 BSC	
E		3.00 BSC	
e		0.50 BSC	
L	0.30	0.35	0.40
L1	--		0.10
N		16	
ND		5	
NE		3	

HANKING ELECTRONICS
Engineered Performance

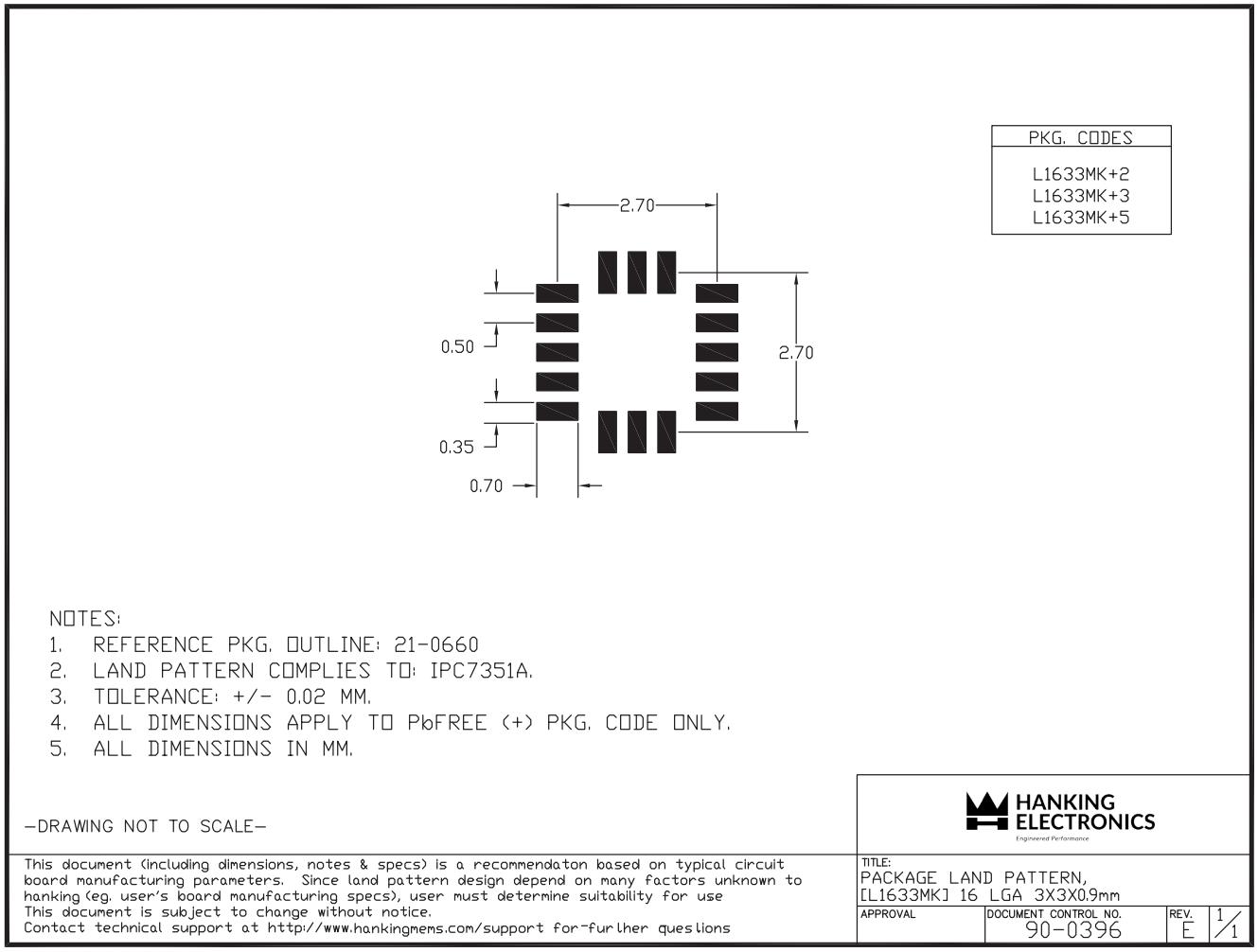
TITLE:
PACKAGE OUTLINE,
16L LGA, 3x3mm

APPROVAL	DOCUMENT CONTROL NO.	REV.	
	21-0660	J	2/2

-DRAWING NOT TO SCALE-

Package Information (continued)

For the latest package outline information and land patterns (footprints), go to **www.hankingmems.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.



Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
1.0	10/19	Initial release	—

For pricing, delivery, and ordering information, please contact Hanking Electronics Direct at (+86)24-5810-4375, or website at www.hankingmems.com

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