HR2000

Fluorescent Lamp HB Driver with PFC

The Future of Analog IC Technology

DESCRIPTION

The HR2000 is a fluorescent lamp ballast controller with PFC function and high voltage half-bridge driver. Only 16pin is used to offer cost effective solutions with minimized external components.

The HR2000 can properly drive the two MOSFETs of half-bridge to control fluorescent lamp, ensuring all the features at the same time. The operating frequency is programmable and the sweeping frequency is controlled to limit the preheat current. The preheat time and ignition time can be smartly set up for types of lamps and applications. Sufficient protection functions are provided for different fault modes such as over voltage, over current, over temperature, capacitive mode, end of life (EOL). Preheat driving signal is offered in preheat state to meet low power loss application which usually needs a MOSFET to cut off filament transformer.

The PFC part only uses 4 pins to realize PFC function with On-time (Ton) control at boundary conduction mode (BCM). It is suitable for wide input range. Over voltage protection and over current protection are integrated for the PFC part.

The HR2000 is available in the 16-pin SOIC16 package.

FEATURES

PFC PART

- Only four pins realize PFC function.
- Ton control.
- Boundary Conduction Mode operation.
- Less peripheral components.
- Over voltage and over current protection.

HALF-BRIDGE PART

- 600V bootstrap half-bridge driver.
- Programmable preheat current.
- Programmable preheat time.
- Programmable ignition time.
- Single ignition attempt.
- Over voltage protection.
- Over current protection.
- End-Of-Life protection
- Capacitive mode protection.
- Minimized external components.
- Over temperature protection

APPLICATIONS

- Tube fluorescent lamp ballast
- Compact fluorescent lamp ballast

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TYPICAL APPLICATION

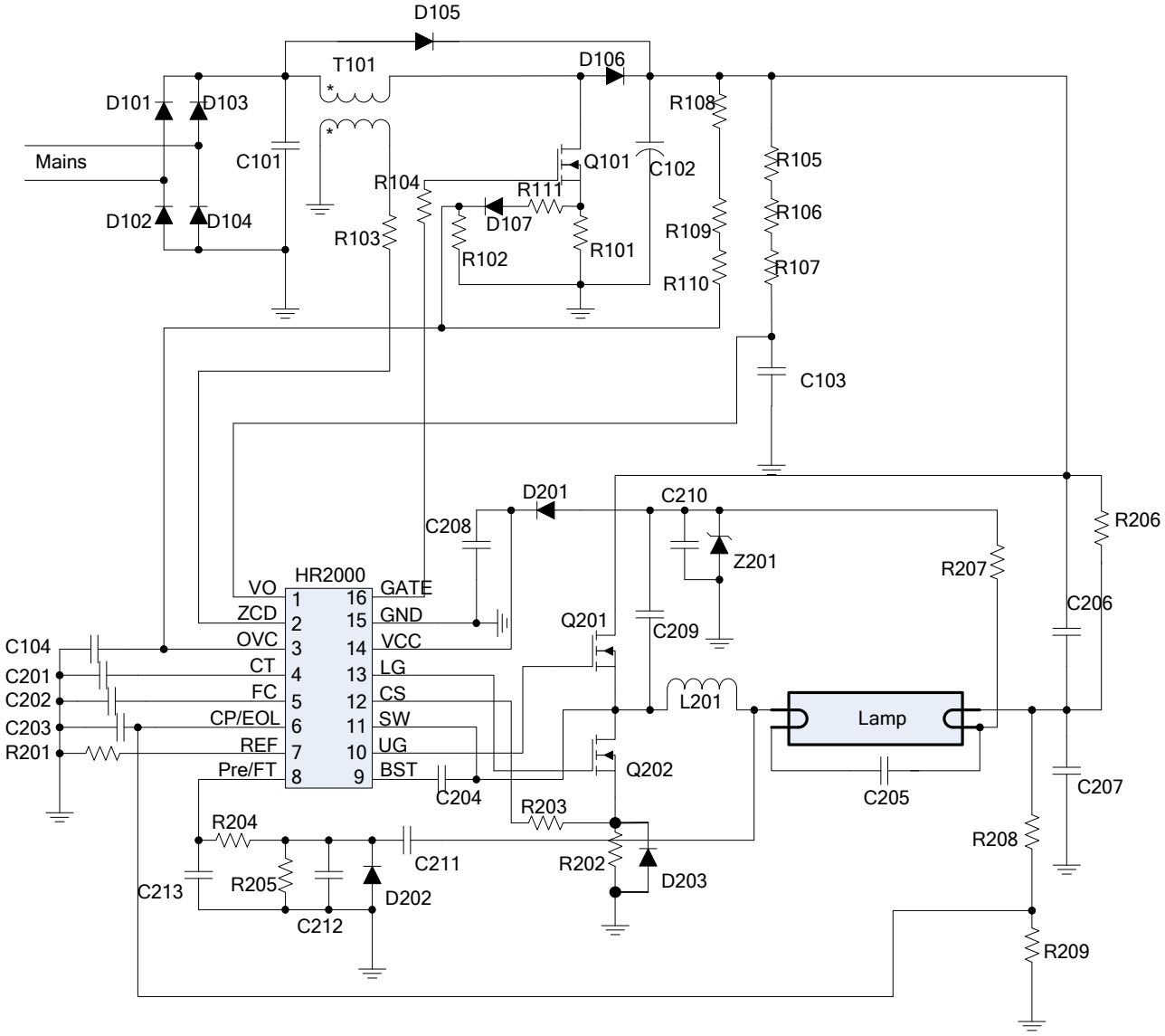


Figure 1

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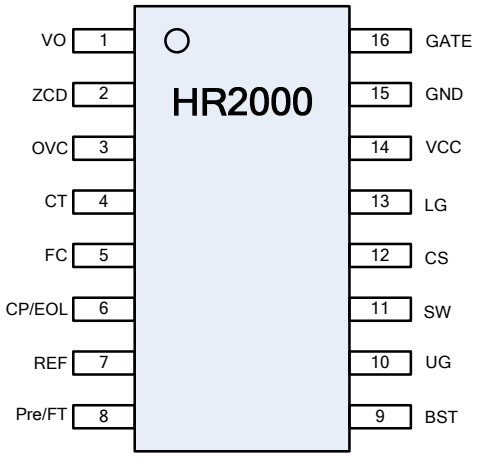
ORDERING INFORMATION

Part Number*	Package	Top Marking
HR2000GS	SOIC16	HR2000

* For Tape & Reel, add suffix –Z (e.g. HR2000GS–Z).

PACKAGE REFERENCE

HR2000 SOIC16 PACKAGE (TOP VIEW)



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LIMITING VALUE (1)

		Condition	Symbol	Min.	Max.	Unit
A	High side floating supply voltage	Operation	Vbst		630	V
B	Voltage at SW		Vsw	-3	630	V
C	Voltage at pin CS	Note7	Vcs	-0.5	V_{BE}	V
D	Current in pin CS	t<1.0μs, note4	Ics	-10	10	mA
E	Voltage at pin UG	Note7	V_{UG}	Vsw-V_{BE}	V_{BST}	V
F	Voltage at pin LG	Note7	V_{LG}	-V_{BE}	Vvcc	V
G	Low voltage supply	t<0.5s over lifetime	Vvcc	0	15	V
H	Low voltage supply		Vvcc	0	14	V
I	Clamp current in pin VCC	In fault state	Ivcc		5	mA
I	Voltage at pin ZCD		Vzcd	-7	7	V
J	Voltage at pin OVC		V_{OVC}	0	5	V
K	Current in pin VO	Vvcc=0 to Vvccmax	Ivo	0	200	μA
L	Current in pin CT	Vvcc=0 to Vvccmax	I_{CT}	0	200	μA
M	Current in pin CP/EOL	Vvcc=0 to Vvccmax Note9	I_{EOL}	-1	1	mA
N	Slew rate at pins SW,HG and BST	With respect to ground	SR	-4	4	V/ns
O	Junction temperature		Tj		150	°C
P	Ambient temperature		Tamb	-40	125	°C
Q	Storage temperature		Tstg	-55	150	°C
R	HBM electrostatic handling voltage SW,HG,BST,VCC and LG VO, OVC, CT, FC, CP/EOL, REF, Pre/FT, CS, ZCD, GATE	Note5	Vesd(HBM)		2000	V V
S	MM electrostatic handling voltage Pins Pre/FT	Note6	Vesd(MM)		150	V
	Pins VO, OVC, CT, FC, CP/EOL, REF, CS, ZCD, GATE, SW,HG,BST,VCC and LG				200	V
T	Charge coupling at pins REF and CT	Operating	Qcoupl	-8	8	pC
U	Reference resistor		R_{REF}	36	91	kΩ

Recommended Operating Conditions (3)

Supply Voltage VCC ..... 10V to 12V
Analog inputs and outputs ..... -0.3V to 6.5V
Operating Junction Temp (T_J) . -40°C to + 125°C

Thermal Resistance (4)

	θ_{JA}	θ_{JC}	
SOIC16	80	35	...°C/W

Notes:

1) Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature T_J(MAX), the junction-to-ambient thermal resistance θ_{JA}, and the ambient temperature T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by D(MAX)=(T_J(MAX)-T_A)/ θ_{JA}. Exceeding the maximum allowable power dissipation will cause excessive die temperature, and the regulator will go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
3) The device is not guaranteed to function outside of its operating conditions.
4) Measured on JESD51-7, 4-layer PCB
5) In accordance with the Human Mody Model (HBM), i.e. equivalent to discharging a 100pF capacitor through a 1.5kΩ series resistor
6) In accordance with the Mancine Model (MM), i.e. equivalent to discharging a 200pF capacitor through a 10Ω series resistor and a 0.75μH inductor.
7) At Tamb=25°C the typical V_{BE} IS 0.7V.
8) At negative CS currents (typ<-5mA) the capacitive mode protection can be triggered.
9) When EOL detection is enabled

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ELECTRICAL CHARACTERICS

Ta=25^{O}C; Vvcc=13.0V; C_{CT}=100pF; R_{REF}=51kohm; $C_{CP/EOL}$=100n, C_{FC}=100nF; all voltage referenced to ground; unless otherwise specified.

No		Condition	Symbol	MIN.	TYP.	MAX.	UNIT
High voltage supply							
1.0	Leakage current high voltage pins	SW,HG,BST=630V, Vvcc=0	I_{Leak}			15	µA
Start-up state							
2.0	Start of oscillation		VCC(start)	11.2	12	12.8	V
2.1	Stop of oscillation		VCC(low)	7.7	8.2	8.7	V
2.2	Non-oscillating current	Vvcc=11V;note2	Ivcc(nonosc)	230	285	340	µA
2.3	Clamp voltage VCC	At 5mA non-oscillating	VCC(clamp)	14.5	16	17	V
2.4	Reset voltage	Note8	VCC(reset)	4.5	5.5	6.5	V
Preheat State							
3.0	Starting frequency	VFC=0, note1	Fstart	96	102	108	kHz
3.1	Preheat time	CCP=100nF	Tph	540	620	700	ms
3.2	Charge current at CP/EOL pin	Vcpeol=1.0V, note10	I_{CP}(charge)		6.0		µA
3,3	Discharge current at CP/EOL pin	Vcpeol=3.5V, note10	I_{CP}(disch)		6.0		µA
3.4	Peak voltage difference at CP/EOL pin	When timing	ΔCc_{PEOL}(pk)		2.25		V
3.5	CP comparator level low		V_{CP}(min)	1.15	1.25		V
3.6	Control voltage at CS pin	Note3	Vcs(pre)	375	410	445	mV
3.7	Maximum voltage at Pre/FT pin		Vpre		VCC		V
Ignition state							
4.0	Ignition time	CCP=100n	Tig	500	600	700	ms
4.1	Saturation current detection level	At ICS(ig)=0.1mA	Vcs(clamp)		0.75		V
4.2	over current feedback gain	Note4	koc	0.9	1	1.1	A/A
4.3	Pre/FT pin reset level	After preheat, Pre/FT will be dropped to this level. Then detecting the voltage at Pre/FT is active.	Vfault(reset2)	150	200	250	mV
Burn State							
5.0	Bottom frequency	Note1	f_B	42	43.5	45	kHz
5.1	Non-overlap time		T_{NO}	0.85	1.20	1.55	µs
5.2	Symmetry half-bridge	Note1,7	SYM f_B	0.9	1.0	1.1	
5.3	Symmetry non-overlap time	Note 9	SYM T_{NO}		1.0		
5.4	Total supply current	Notes 1,5	Itot		1.7	2.5	mA
5.5	Charge current at FC pin	VFC=1.5V	I_{FC}(ch)	43	50	57	µA
5.6	Discharge current at FC pin	VFC=1.5V	I_{FC}(disch)	84	100	116	µA
5.7	FC transconductance	VFC=1.5V	$\Delta I_{CT}/\Delta V_{FC}$		10		µA/V
5.8	Capacitive mode control voltage	Note6	Vcs(cap)	-32	-14	0	mV
5.9	Reference voltage		Vref	2.425	2.500	2.575	V
5.10	On voltage at pin UG	|IUG|=1mA	VUG(on)		12.96		V
5.11	Off voltage at pin UG	|IUG|=1mA	VUG(off)		16		mV
5.12	On voltage at pin LG	|ILG|=1mA	VLG(on)		12.96		V

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ELECTRICAL CHARACTERICS *(continued)*

Ta=25°C; Vvcc=13.0V; C_{CT}=100pF; R_{REF}=51kohm; $C_{CP/EOL}$=100n, C_{FC}=100nF; all voltage referenced to ground; unless otherwise specified.

No		Condition	Symbol	MIN.	TYP.	MAX.	UNIT
5.13	Off voltage at pin LG	|ILG|=1mA	VLG(off)		16		mV
5.14	Up side driver on resistance		RUG(on)		33		Ω
5.15	Up side driver off resistance		RUG(off)		16		Ω
5.16	Low side driver on resistance		RLG(on)		33		Ω
5.17	Low side driver off resistance		RLG(off)		16		Ω
5.18	Voltage drop at bootstrap switch	10mA source current	Vdrop		1.7		V
5.19	On resistance of the discharge switch at CP/EOL pin		Rcp(disch)		14		kΩ
5.20	On resistance connected Pre/FT pin and VCC pin		Rpre		16		kΩ
Fault and End of Life							
6.0	Fault reference level		Vfault(ref)		1.22		V
6.1	Fault reset level	Note8	Vfault(reset1)		0.9		V
6.2	Fault charge current source	V_{PreFT}=0.75V	Ifault(ch)		3.2		µA
6.3	Fault discharge current	V_{PreFT}=0.75V	Ifault(disch)		0.62		µA
6.4	On resistance discharge switch	V_{PreFT}=0.5V	Rfault(disch)		16		kΩ
6.5	High level EOL comparator		Veol(high)	2.9	3.0	3.1	V
6.6	Low level EOL comparator		Veol(low)	1.9	2.0	2.1	V
Power Factor Control							
7.0	Output voltage reference current	Vvo=3.0V	Ivo(ref)	97	102	107	µA
7.1	OVC reference level		Vovc(ref)	1.22	1.27	1.32	V
7.2	Delay OVC comparator		Tovc		100		ns
7.3	VO offset voltage		Vvo(low)		0.72		V
7.4	VO dynamic range		ΔVvo		3.1		V
7.5	Maximum on time	Vvo=Vvo(low)	Ton(max)	20			µs
7.6	ZCD reference		Vzcdref		2		V
7.7	Duration off pulse		Toff		1.4		µs
7.8	OVC low voltage		Vovc(low)		94		mV
7.9	VO low reference		Ivo(low)	80	90	100	µA
7.10	Off-voltage PFC		Vvo(off)		3.8		V
7.11	Active VO clamp voltage	Ivo=200µA	Vvo(clamp)		6.2		V
7.12	Passive VO clamp voltage	Ivo=200µA, Vvcc=0V	Vvo(pas)		3.5		V
7.13	Gate pull down resistance		$R_{gate\ pull\ down}$		14		Ω

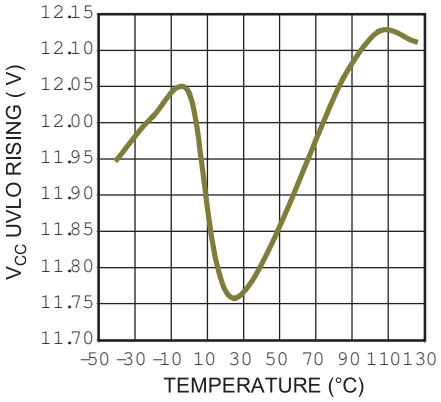
NOTES

1) Excluding situations where the over current protection is active.
2) The non oscillation current is specified in a temperature range of 0 to 100 0C. For Tj < 0 0C and Tj > 100 0C the maximum start-up current is 350 mA.
3) Data sampling of VCS(ph) is performed at the end of conduction of T2.
4) Gain is defined as ICT/ICS with VCS>VCS(clamp).
5) Total supply current is specified in a Tj temperature range of -20 0C to 125 0C at fB, excluding gate drive charge.
6) Data sampling of VCS(cap) is performed at the start of conduction of T2.
7)
8) The symmetry SYM fB is calculated from the quotient SYM fB = T1tot/T2tot, with T1tot the time between turn-off of G2 and the turn-off of G1, and T2tot the time between turn-off of G1 and the turn-off of G2.
9) Not measured, guaranteed by design.
10) The symmetry SYM TNO is defined as the ratio between deadtime1 and deadtime2. Deadtime1 is the time between turning off G1 and turning on G2. Deadtime2 is the time between turning off G2 and turning on G1.
11) Preheat & ignition states.

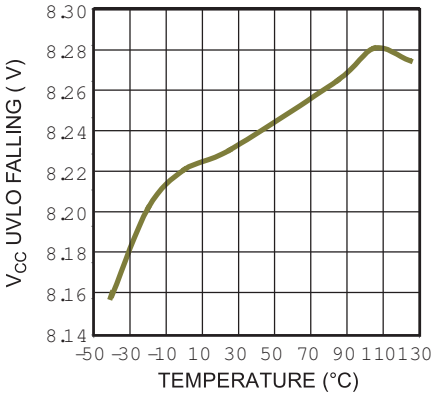
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TYPICAL CHARACTERISTICS

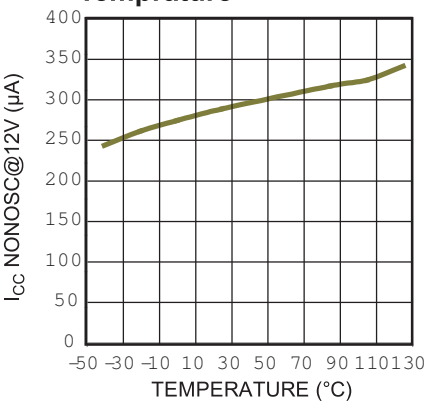
V_{CC} UVLO Rising Threshold vs. Temprature



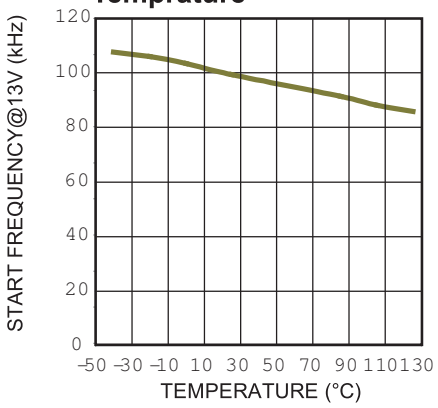
V_{CC} UVLO Falling Threshold vs. Temprature



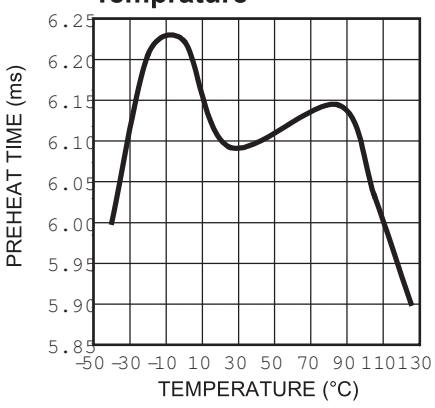
Supply Current @ Non-oscillation vs. Temprature



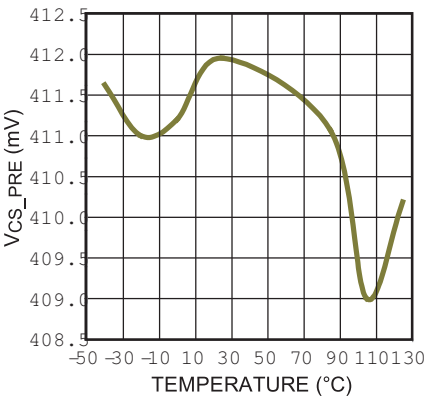
Start Frequency vs. Temprature



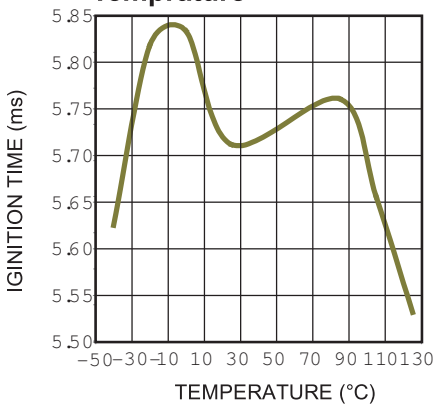
Preheat Time vs. Temprature



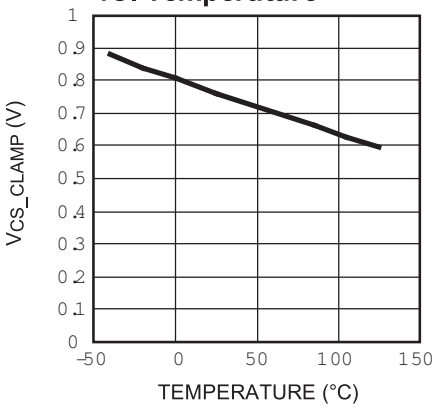
V_{CS_PRE} vs. Temprature



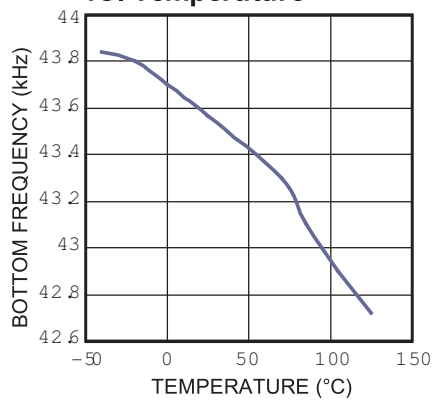
Ignition Time vs. Temprature



CS Clamp Voltage @100µA vs. Temperature



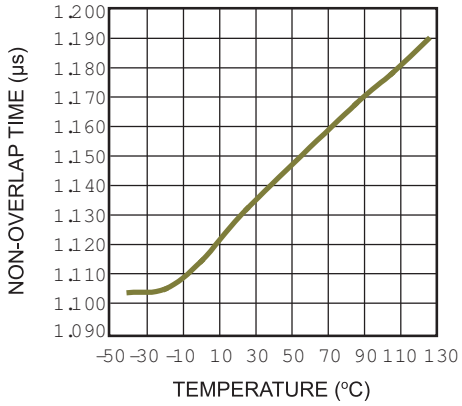
Bottom Frequency vs. Temperature



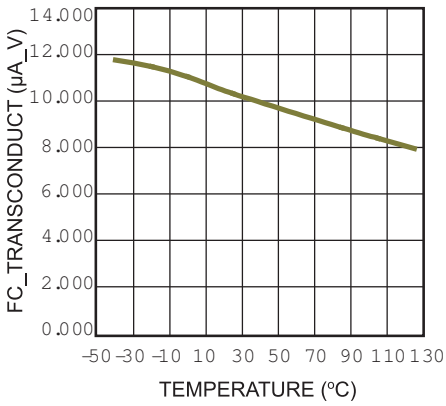
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TYPICAL CHARACTERISTICS *(continued)*

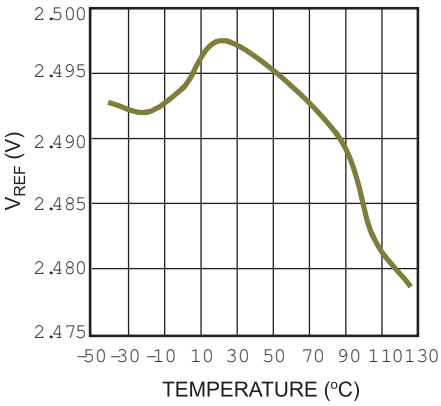
Non-overlap Time vs. Temperature



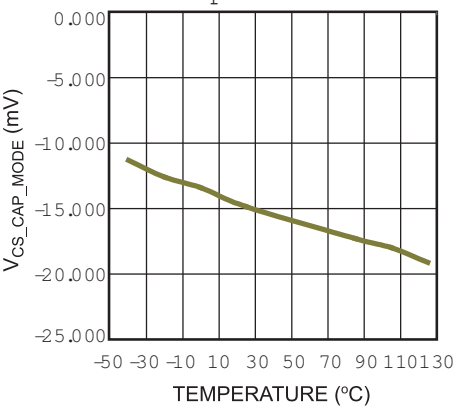
FC Transconductance vs.Temperature



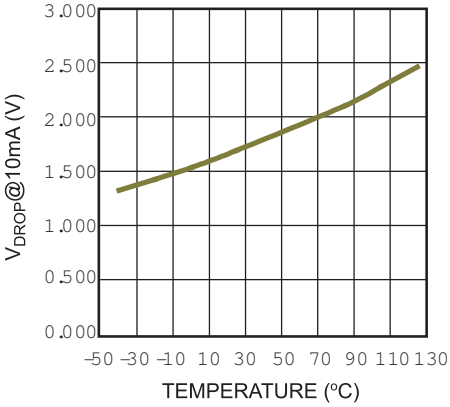
V_{REF} vsTemperature



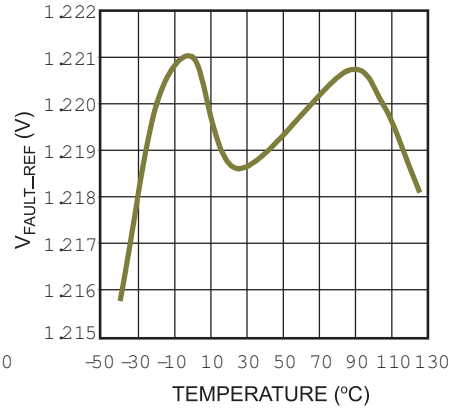
CS Capacitive Mode Detection Threshold vs.Temperature



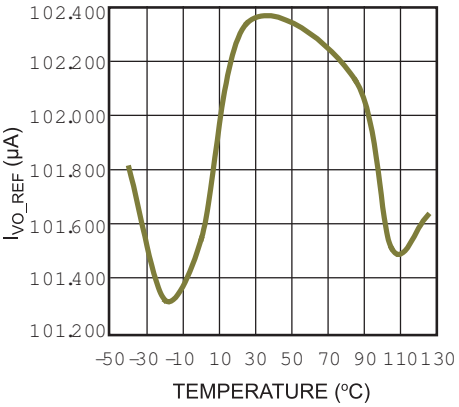
Voltage Drop at Bootstrap Switch vsTemperature



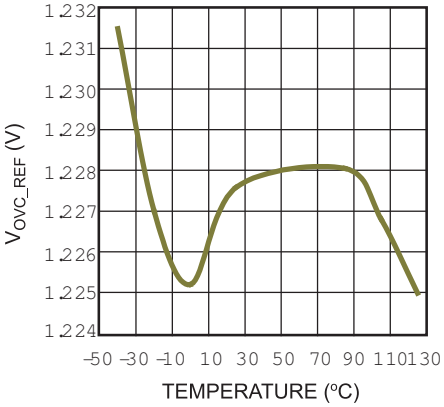
Fault Reference Level vs.Temperature



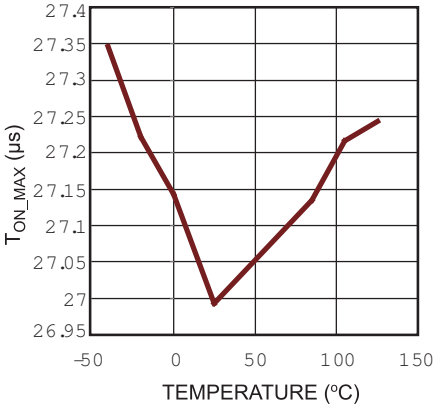
OutputVoltage Reference Current vsTemperature



OVC ReferenceVoltage vs.Temperature



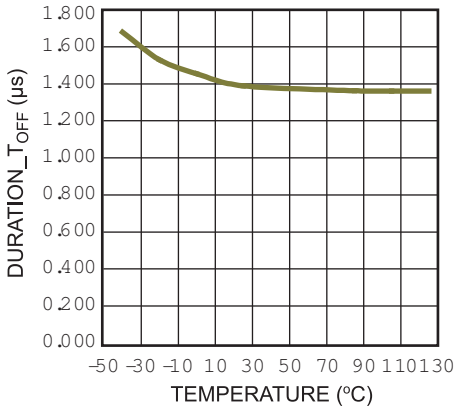
Gate Maximum onTime vs.Temperature



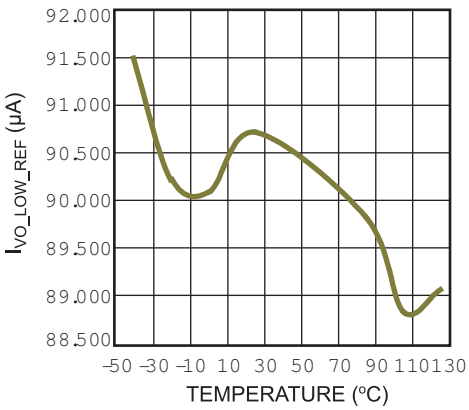
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TYPICAL CHARACTERISTICS *(continued)*

Duration Offtime vs.Temperature



V_{OUT} Low Reference Current vs.Temperature

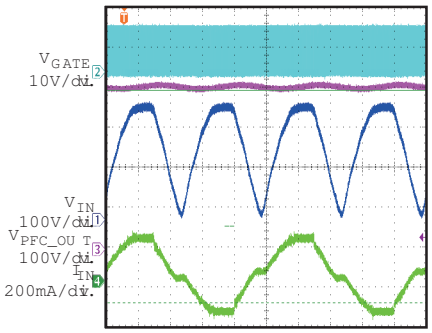


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TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

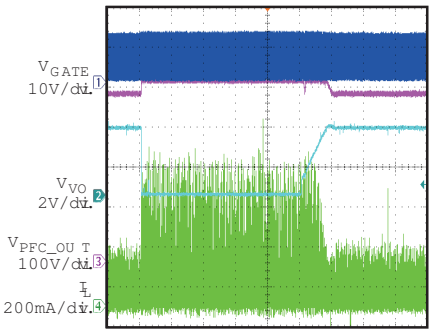
Performance waveforms are tested on the evaluation board of the Application Example. V_{IN} = 220VAC, 18W FL load, C_{CT}=100pF, R_{REF}=51kohm, $C_{CP/EOL}$=100n, C_{FC}=33nF, T_A = 25°C, unless otherwise noted.

PFC



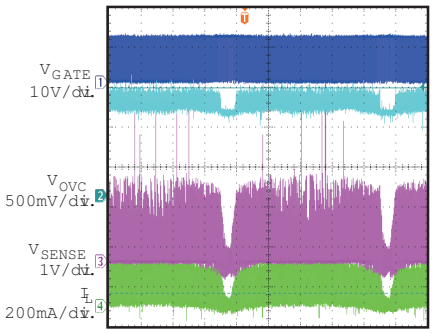
OVP and Recover

Pull VO Pin Low and Release

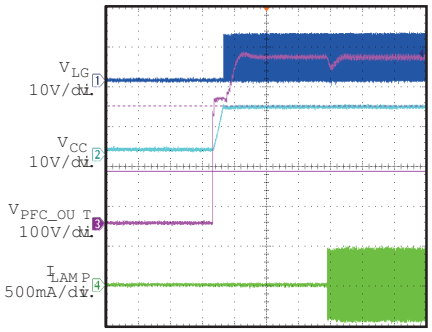


Over Current Protection

Increase R_{SENSE_PFC}

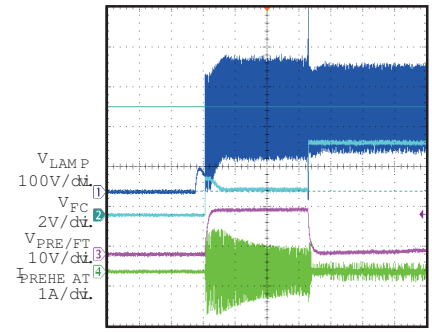


Start Up

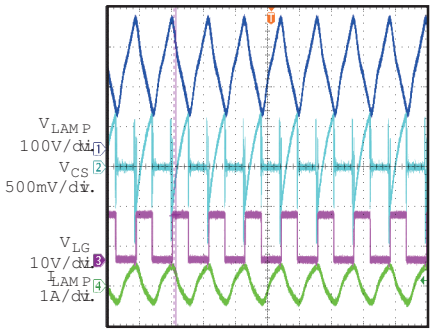


Preheat & Ignition

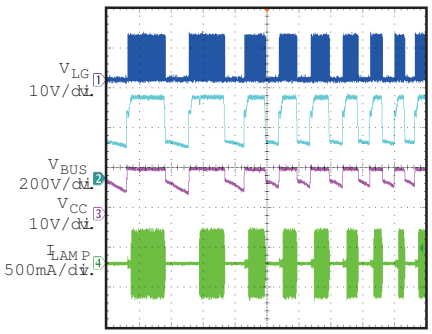
Controlled Preheat Time, Frequency, Current/Lamp Voltage



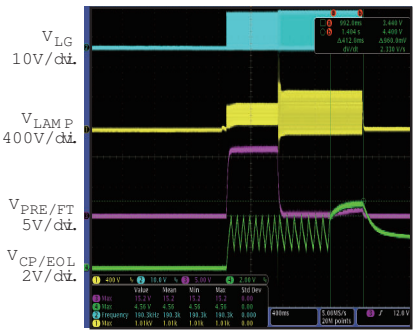
Burn State



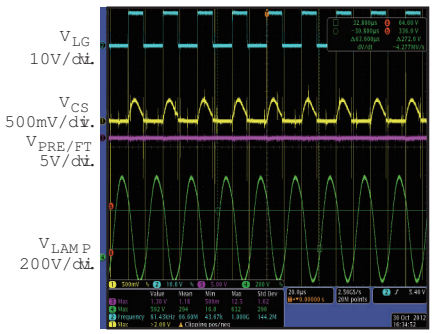
Quick Power On/Off



EOL Protection



Capacitive Mode Protection (Always Soft Switching)

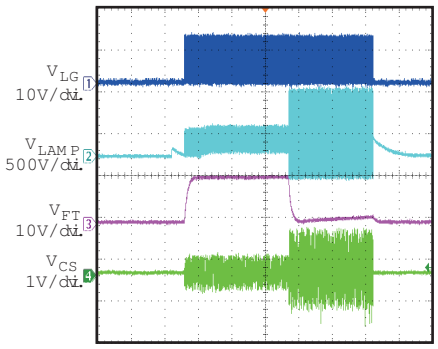


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TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

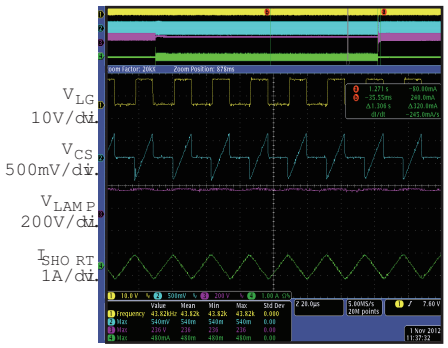
Performance waveforms are tested on the evaluation board of the Application Example.
V_{IN} = 220VAC, 18W FL load, C_{CT}=100pF, R_{REF}=51kohm, $C_{CP/EOL}$=100n, C_{FC}=33nF, T_A = 25°C, unless otherwise noted.

Open Lamp Protection



200ms/div.

Short Lamp and Recover



20µs/div.

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PIN FUNCTIONS

Pin #	Name	Description
1	VO	PFC output control pin. Connect a resistor from this pin to the PFC output to set the PFC output voltage. Connect a capacitor (or a R-C-C network) from this pin to GND for the compensation of the PFC regulation loop.
2	ZCD	PFC inductor zero current detection pin.
3	OVC	PFC over voltage/current protection pin.
4	CT	Frequency setting capacitor pin. Connect a capacitor from this pin to GND to set the frequency.
5	FC	Frequency control pin. It is voltage controlled oscillator (VCO) pin for controlling half bridge frequency.
6	CP/EOL	Preheat/ignition timing pin and EOL detector. A capacitor from this pin to GND sets the preheat time and ignition time. Before half-bridge works, it is discharged internally to GND. In the preheat state and ignition state, a triangle waveform is generated on this pin and used as a timer. The voltage of the blocking capacitor is sensed to this pin to indicate the EOL condition. After preheat and ignition state, the voltage at this pin is internally discharged to the middle of the EOL window comparator's reference, and then the lamp's EOL information is under monitoring. If EOL condition is confirmed, an internal current source charges the Pre/FT pin's capacitor.
7	REF	Internal reference current setting resistor pin. Connect a resistor from this pin to GND to set the frequency.
8	Pre/FT	In the preheat state, this pin outputs a high level voltage to drive the external preheating MOSFET. After this period, it is discharged to Vfault (reset2). Then it is used as a fault timer to stop IC at fault condition. At fault condition, an internal current source charges up this pin, and when its voltage hits the fault reference threshold, IC latches up. Connect a capacitor on this pin to set the fault timer.
9	BST	Bootstrap voltage supply for half bridge level shifter. Connect a capacitor (usually 10nF to 100nF) between this pin and SW pin.
10	UG	Half bridge up side MOSFET driver.
11	SW	Half bridge floating middle point.
12	CS	Half bridge current sensor.
13	LG	Half bridge low side MOSFET driver.
14	VCC	Supply voltage of the IC.
15	GND	Ground
16	GATE	PFC GATE driver pin.

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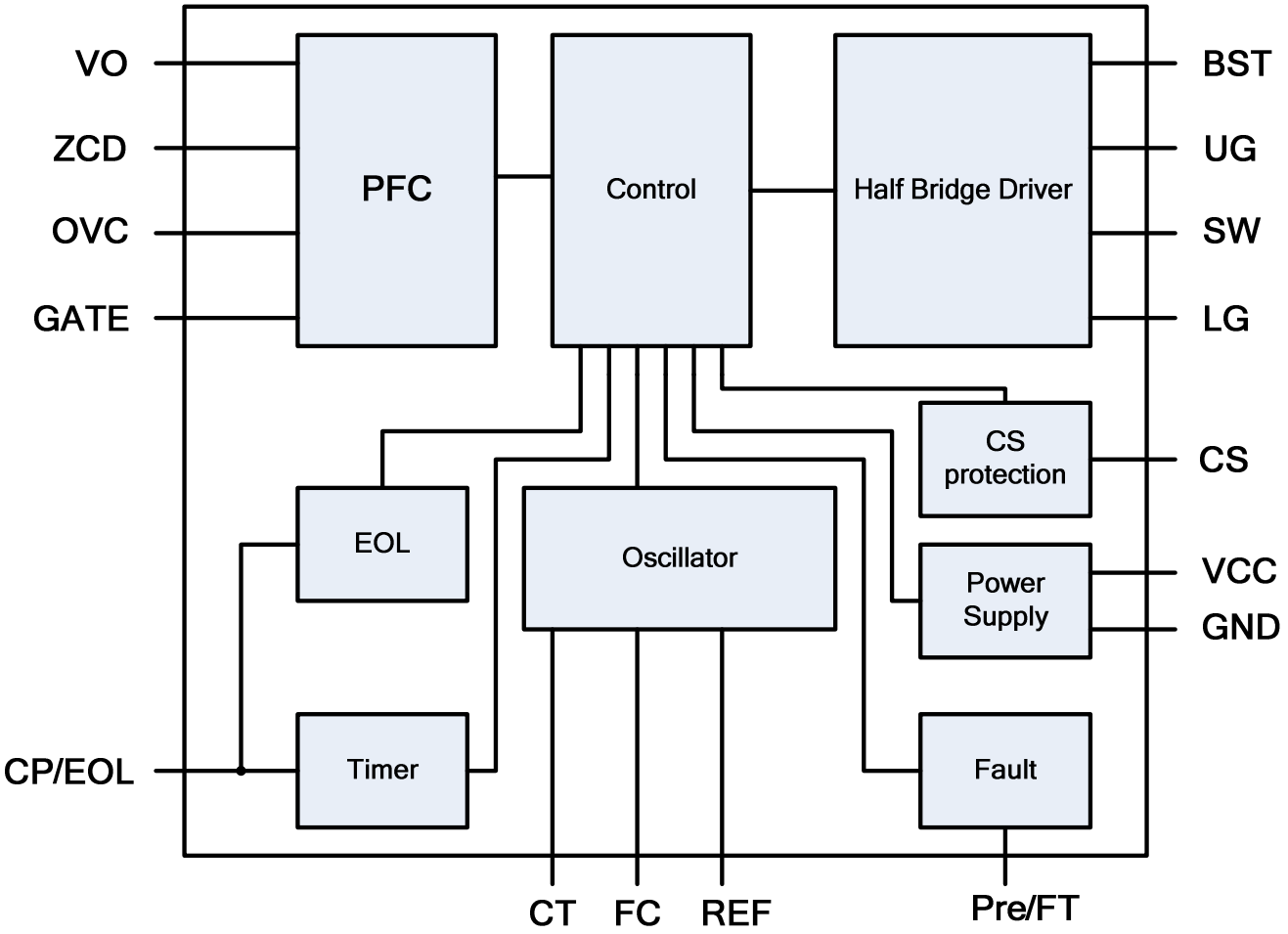


Figure 2— Block Diagram

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FUNCTIONAL DESCRIPTION

HR2000 includes Half-bridge part and PFC part.

Half-bridge part

In the typical application, the half-bridge can be defined to two basic states: Oscillating state and None-oscillating state.

Non oscillating state:

In non-oscillating state, IC stops to work. There are 4 sub-states:

- Start up state;
- Fault state;
- VCC under voltage state;
- Over temperature protection (OTP) state

Start-up state

When Vcc<Vcc(reset), HR2000 will get into Start-up state.

Initially, the IC can be supplied from the outside resistor such as R207 in Figure1.

All internal circuit is reset in this state.

In this state, CP/EOL, Pre/FT, FC pin are discharged by the internal switches.

Fault state

There are two conditions resulting in Fault state.

The first one is before Vvcc>Vvcc(reset), if VPreFT>Vfault(reset), then IC will not start up.

The second one is after Pre/FT pin's detection function is active in all oscillating sub-states, HR2000 will get into Fault state if Pre/FT pin voltage VPreFT>Vfault(ref) & low side drive is high.

The following items will affect Pre/FT pin in oscillation state.

The voltage detected by the sample circuit such as C211, C212, C213, D202, R204, R205 in Fig1.

In EOL protection and Capacitive Mode protection, a current source Ifault(ch) will charge the capacitor at this pin such as C213 in Fig1.

In PFC VO-low state a current source Ifault(disch) will discharge C213.

Before Vvcc>Vvcc(reset), this pin will be detected. If VPreFT>Vfault(reset), IC will not start up.

VCC under voltage state

There is a hysteresis for Vcc detection. When power on, HR2000 begin's to work after Vvcc>Vvcc(start). If Vvcc<Vvcc(low) & low side drive is high in oscillation state, the device will get into VCC under voltage state.

OTP state

The temperature is monitor by IC internal circuit. If detected temperature is higher than Thigh, then IC will get into non-oscillation state. When temperature is lower than Tlow, the oscillation is enabled again.

Oscillating State

After start-up state, once the VCC pin gets to the level VCC(start), IC begins to work.

In oscillating state, there are 3 sub-states:

- Preheat state;
- Ignition state;
- Burn state;

Half-bridge oscillator

The oscillating frequency is programmed by the capacitor on CT pin. The capacitor on CT pin is charged by internal current source which is related to REF pin resistor and FC pin voltage which is voltage controlled current source for CT pin. The waveform of CT pin is saw-tooth and its frequency is twice of the half-bridge operating frequency. There is a dead time between UG and LG for ensuring their non-overlap operating. The dead time is defined by REF resistor.

FC pin controls the operating frequency directly. Higher Vfc results in a lower frequency.

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Preheat State

When Vvcc>Vvcc(start) & VPreFT<Vfault(reset), HR2000 gets into Preheat state from the start up state. During this state, Pre/FT pin's detection function will be disabled. High voltage will be sent out in this state.

During this state, CP/EOL pin will disable EOL detection function and only take the timing function.

In this state, only CS pin has a current limit function. If Vcs>Vcs(pre) in a switching period, the FC pin will be discharged by an internal current source IFC(disch) cycle-by-cycle. This controls the working frequency.

Ignition State

Ignition state follows preheat state closely. In this state, EOL protection and CS(pre) limit are disabled. FC voltage increases which results in frequency decreasing. Then the voltage on lamp gets higher and higher to ignite the lamp.

CP/EOL pin also only takes timing function in this state. Once preheat state is over, Pre/FT pin is dropped to Vfault(reset2), and then the detection function is active. If Pre/FT pin VPreFT>Vfault(ref) & low side drive is high, then HR2000 will consider it is fault state.

After preheat state, CS pin over current protection is active and limits CS voltage (power stage current).

When Vcs>Vcs(clamp) @ low side drive=high, the impedance of CS pin will become very small and a current flows into this pin. The koc of this current will charge the CT pin to increase frequency. The low side MOSFET will be turned off quickly while high side MOSFET will not be affected. This results in a narrow turn on time of low side MOSFET and a relatively larger turn on time of high side MOSFET. This asymmetric operation of half bridge limits the output power.

Burn state

After ignition state, Burn state is entered. At the beginning of burn state, CP/EOL pin will be dropped to the middle level of the EOL detection window Veol(middle). Then the EOL detection function is active instead of the timing function.

Voltage on FC pin will continue to increase until it reaches a clamping level. CS pin over current protection mentioned in ignition state is still used to limit CS voltage (power stage current).

Protection

In oscillation state, the half-bridge protection includes:

- EOL protection
- Capacitive mode protection
- Current limit
- VCC low protection
- Over temperature protection

EOL protection

'End of Life'(EOL) protection is enabled after CP/EOL is dropped to Veol(middle). There is a window comparator for this protection. If the voltage on CP/EOL pin get out of Veol(low)~Veol(high), then the current source Ifault(ch) will charge the capacitor at Pre/FT pin. If VPreFT>Vfault(ref), then HR2000 will get into fault state.

This protection is disabled in PFC Vo-low state.

Capacitive mode protection

The capacitive mode protection is active during all oscillating states. It is detected by the voltage on CS at the moment of turning on of low side MOSFET. If at this moment, Vcs>Vcs(cap), then capacitive mode is confirmed and FC pin is discharged at this switching cycle. VFC will decrease towards zero which means the maximum frequency if the capacitive mode always exists. If capacitive mode @ fmax is detected, then Ifault(ch) is actived to charge the capacitor at Pre/FT pin.

Current limit

The current limit is realized on CS pin. There are three kinds of limitation on CS pin.

Vcs(pre) in preheat state;

Vcs(clamp) of over current protection function in oscillating states;

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Capacitive protection in oscillating states.

They have been described in the related states above.

VCC low protection
It is mentioned in VCC under voltage state.

Over temperature protection (OTP)

It is described in OTP state.

PFC part

In the typical application, PFC can be defined to 3 states:

- Normal state;
- VO-low state;
- OVC state;

Normal state

PFC works at boundary conduction mode (BCM) with Ton control. Fig3 shows the internal block.

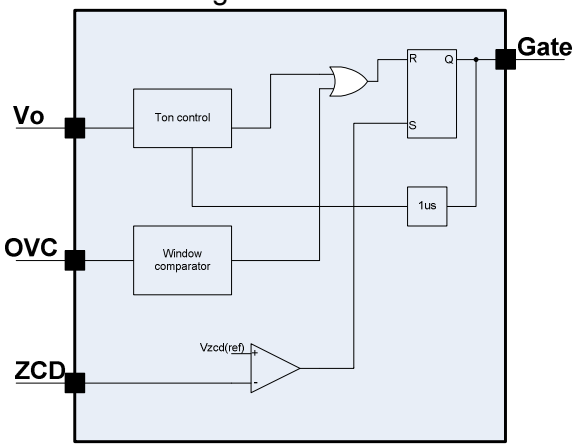


Figure 3— PFC part block

The Ton is set by the voltage at Vo pin. Higher Vvo, shorter Ton. The circuit in Fig1 shows the example. ZCD pin detects the inductor current zero-crossing point. When The Vzcd<Vzcdref, Gate will be high and the external MOSFET will be turned on.
In the range of Vvo(low)~Vvo(off), Ton varies linearly from Ton(max) to zero. When Vvo> Vvo(off), Ton is zero, and GATE pin is low.
The minimum turn off time is set internally to 1.4μs.

Vo-low state

In case of main voltage too low, PFC may not maintain its intended output voltage. In order to keep on working, the current sunk into Vo pin is monitored. If it is lower than Ivo(low) the IC will get into Vo-low state.

In Vo-low state:

There is a current Ifault(disch) to discharge Pre/FT pin. This can increase the protection level. EOL protection is disabled.

Vovc<Vovc(low) will overrule Vo-low condition.

OVC state

OVC pin monitors PFC output voltage and Boost PFC MOSFET current. Fig1 shows the example. If Vovc>Vovcref or Vovc<Vovclow, then PFC will stop immediately.

Vovclow is set to prevent the absence of PFC output detection.

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APPLICATION INFORMATION

PFC Part

Setting the PFC Output Voltage

The Vo pin is used to set the PFC output voltage. Connect a resistor (R105, R106, R107 in figure 1) between the PFC output and Vo pin, its value is set by:

$$R_{PFC_OUT} = \frac{V_{O_PFC} - 2V}{I_{VO(REF)}}$$

Where $I_{vo(ref)}$=102μA is the reference sink current through Vo pin.
Connect a capacitor in range of 0.47μF to 10μF (C103 in figure 1) or a R-C-C network from Vo pin to GND to compensate the PFC regulation loop.

Setting the Over Voltage and Over Current Protection

The OVC pin is used for the over voltage and over current protection for the PFC stage. Connect this pin to the voltage divider (R108, R109, R110 and R102 in figure 1) of the PFC output to set the over voltage protection point.

$$\frac{R_{OV_H}}{R_{OV_L}} = \frac{V_{o_PFC_pro}}{V_{OVC(ref)}}$$

Where $V_{OVC(ref)}$=1.26V is the OVC protection threshold voltage, and $V_{o_PFC_pro}$ is protection point of the PFC output voltage. R_{OV_H} is the upper side resistor of the divider and R_{OV_L} is the low side resistor of the voltage divider.
The over current protection senses the peak current through the PFC MOSFET. the sensing resistor (R101 in figure 1) is set by:

$$R_{oc} = \frac{V_{OVC(ref)} + V_{f_diode}}{I_{oc}}$$

Where V_{f_diode}≈0.7V is the forward voltage of the diode (D107 in figure 1), and I_{oc} is the over current protection point.

Setting the ZCD Detection

An auxiliary winding of the PFC inductor is used to sense the voltage across the inductor to indicate the zero inductor current condition. Set the turn ratio of the auxiliary winding large enough to make sure the reflected voltage across the auxiliary winding is higher than the ZCD reference voltage Vzcdref. Usually, setting the reflected ZCD voltage at around 5V at maximum input voltage is recommended.
A zener diode is integrated on ZCD pin. Add a resistor in 10kΩ to 100kΩ range between the auxiliary winding and the ZCD pin to limit the current sunk into ZCD pin, according to the input voltage range.

Half Bridge Part

Setting the Oscillator of Half Bridge

The capacitor on CT pin (C201 in figure 1) and the resistor on REF pin (R201 in figure 1) determine the bottom operating frequency. The resistor on REF pin also determines the non-overlap time of the half bridge.
Estimate the frequency set resistor on REF pin with the desired non-overlap time:

$$T_{no} = 0.15 + 1.127 \times \frac{R_{REF}}{51k\Omega}(\mu s)$$

Note that the R_{REF} resistor should not exceed the range in the limiting values.
Choose a proper capacitor on CT pin to set the bottom operating frequency.

$$f_B = \frac{0.5}{2(R_{REF} + R_{int}) * (C_T + C_{par}) + 300ns}$$

Where C_T is the capacitor on CT pin, R_{int}=0.3kΩ is the internal parasitic resistance on REF pin and C_{par}=5pF is the internal parasitic capacitance on CT pin. Choose a proper capacitor on CT pin and then redesign the resistor on REF pin to make sure the bottom operating frequency is accurate.
The start up frequency is:

$$f_{ST} = \frac{0.5}{\frac{2.5V \times (C_T + C_{par})}{\frac{2.5V}{2(R_{REF} + R_{int})} + 35\mu A} + 300ns}$$

Setting the Preheat time and Ignition Time

The capacitor on CP/EOL pin (C203) and the resistor on REF pin determine the preheat time and ignition time.

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$$T_{preheat} = 600 \times \frac{C_{CP}}{100nF} \times \frac{R_{REF}}{51k\Omega}(ms)$$

$$T_{ignition} = 562 \times \frac{C_{CP}}{100nF} \times \frac{R_{REF}}{51k\Omega}(ms)$$

Setting the Preheat Current Limitation

In the preheat stage, the CS pin limits the preheat current through the filament of the FL. The preheat current is limited by setting the sense resistor on CS pin (R202 in figure 1) through:

$$I_{preheat_pk} = \frac{V_{CS(pre)}}{R_{CS}}$$

Where the $V_{CS(pre)}$=410mV is the threshold voltage of CS pin to limit the preheat current.
If using the filament transformer for preheating, this CS pin function will limit the resonant current in the preheat stage.
The over current limitation function on CS pin limits the ignition voltage or ignition current in the ignition state and any exceeded output current/power condition. Add a diode (D203 in figure 1) like 1N4148 in parallel with the sense resistor and a 1k resistor (R203 in figure 1) between the CS pin and the current sense resistor to limit the negative voltage on CS pin.

Design the PFC Inductor

The HR2000 operates the PFC in boundary conduction mode (BCM) with on-time (Ton) control. The frequency of the PFC stage is variable. The design of the PFC inductor relates to the output power, the range of the input AC voltage and the desired minimum operating frequency. It is also limited by the maximum turn on time of HR2000. The maximum peak current through this inductor is:

$$I_{L_pk_max} = \frac{2\sqrt{2}P_{o_max}}{\eta \times V_{in_min_RMS}}$$

Where ηis the efficiency of the PFC stage, usually in range of 0.95 to 0.98.

The maximum turn on time of the PFC MOSFET occurs at the minimum AC input voltage:

$$T_{on_max} = \frac{L \times I_{L_pk_max}}{\sqrt{2}V_{in_min_RMS}} = \frac{L \times 2P_{o_max}}{\eta \times V_{in_min_RMS}^{2}}$$

Then the inductor is restricted by the maximum on time limit of IC:

$$L \le \frac{\eta \times V_{in_min_RMS}^{2} \times T_{on_limit}}{2P_{o_max}}$$

Where T_{on_limit} is the IC's limit for maximum on time, design its value with 20μs.

The minimum operating frequency occurs at the minimum AC input voltage or the maximum AC input voltage.

$$f_{min} = \min\left(\frac{\sqrt{2}V_{in_min_RMS} \times (V_o - \sqrt{2}V_{in_min_RMS})}{L \times V_o \times I_{L_pk_max}}, \frac{\sqrt{2}V_{in_max_RMS} \times (V_o - \sqrt{2}V_{in_max_RMS})}{L \times V_o \times I_{L_pk_max}}\right)$$

For most of the specifications, such as the universal input (85VAC to 265VAC) and 400V PFC output, the minimum frequency occurs at the maximum AC input voltage.
Design the inductor value with the desired minimum operating frequency, and it should be in the restricted range by the IC's limit of the maximum on time.

Application Example

This application example introduces the design of a 16W FL based on HR2000. It requires the PF (power factor) over 0.9. The boost PFC stage and resonant half bridge power structure is used for this FL driver. The integrated PFC control and half bridge driver of HR2000 fits for this type of application well.

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Specification:

Parameter	Symbol	Condition	Min	Typ	Max	Units
Input Supply Voltage	Vin	2 Wire	198		264	VAC
AC Line Frequency	f_{LINE}		47	50	63	Hz
Lamp Voltage	V_{lamp}			55		Vrms
Lamp Current	I_{lamp}			0.29		A
Output Lamp Power	P_{lamp}			16		W
Preheat Current	I_{pre}		0.18		0.3	A
Preheat time	t_{Pre}	Rref=51k, CCP=100nF		674		ms
Ignition time	t_{ign}	Rref=51k, CCP=100nF		611		ms
Open circuit voltage	Voc	t<te		270		Vrms
	Voc	t>te		300		Vrms
Burning mode frequency	f_{run}			44.6		kHz
Efficiency (Full Load)	η		80			%
Line regulation						%
Startup time	t_{ST}			1		s
Conducted EMI			Meets EN55015B			
Power Factor			90			%
Harmonics			Meets IEC61000-3-2 Class C			
Ambient Temperature	TAMB	Free convection, sea level			40	□

Schematic:

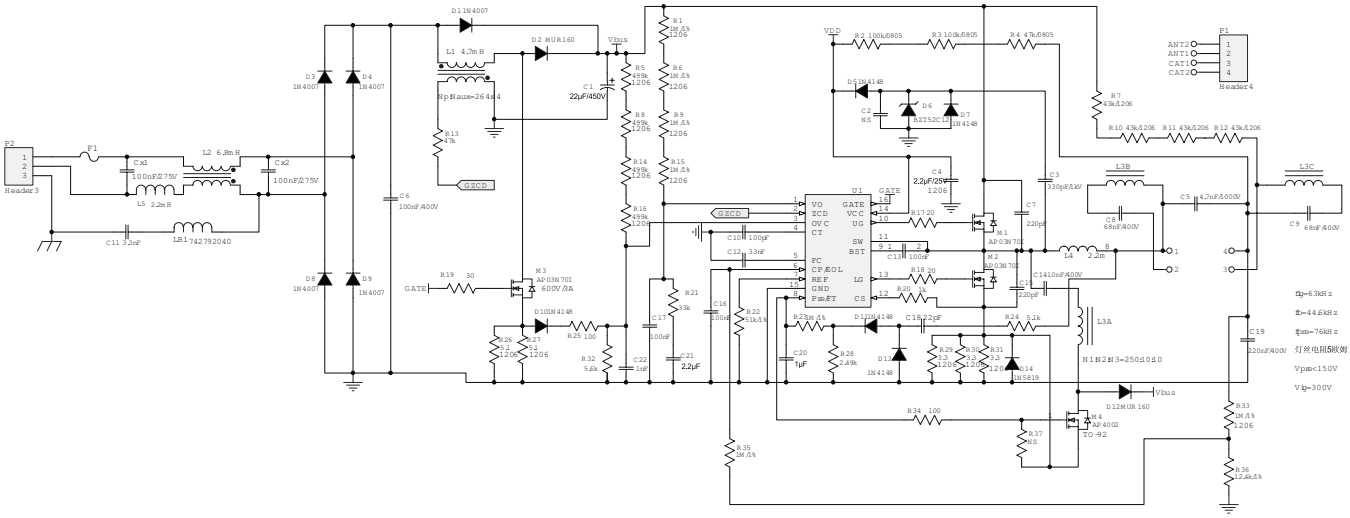


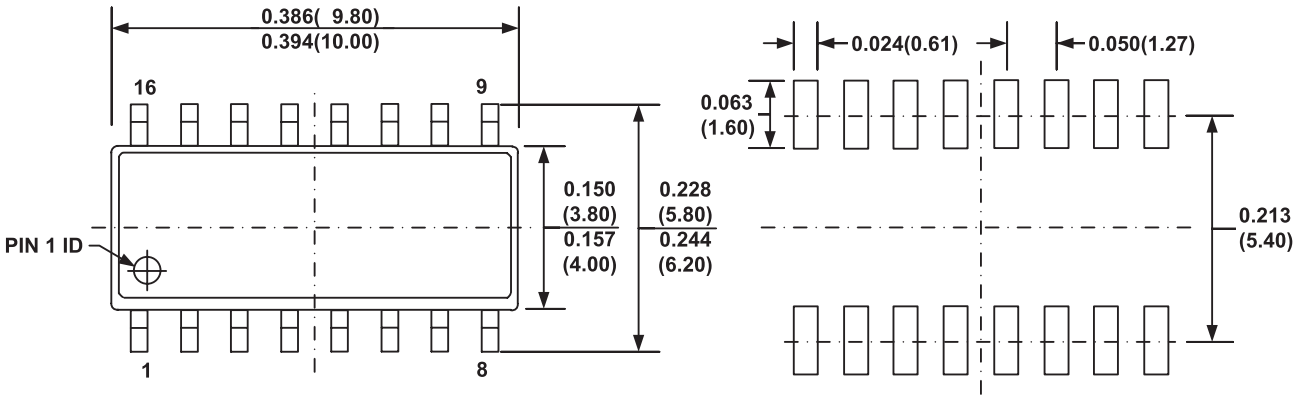
Figure 4—HR2000 FL Driver for 16W Lamp

Design Procedure:

Please refer to the application note of HR2000 for the design procedure.

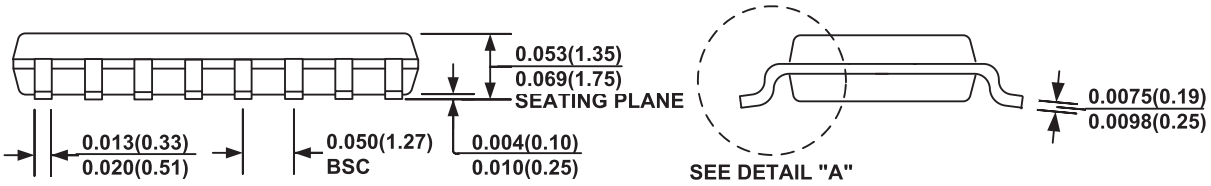
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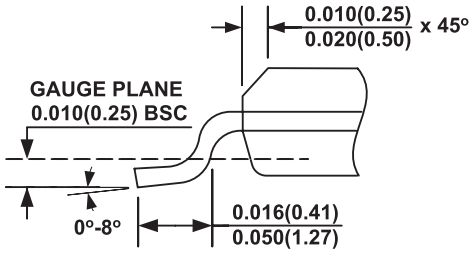
TOP VIEW

RECOMMENDED LAND PATTERN



FRONT VIEW

SIDE VIEW



DETAIL "A"

NOTE:

1) CONTROL DIMENSION IS IN INCHES. DIMENSION IN BRACKET IS IN MILLIMETERS.
2) PACKAGE LENGTH DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
3) PACKAGE WIDTH DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS.
4) LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.004" INCHES MAX.
5) DRAWING CONFORMS TO JEDEC MS-012, VARIATION AC.
6) DRAWING IS NOT TO SCALE.

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