

Description

The ICS513 LOCO™ is the most cost effective way to generate a high quality, high frequency clock output from a 14.31818 MHz crystal or clock input. The name LOCO stands for Low Cost Oscillator, as it is designed to replace crystal oscillators in most electronic systems. Using Phase-Locked-Loop (PLL) techniques, the device uses a standard, inexpensive crystal to produce output clocks up to 100 MHz.

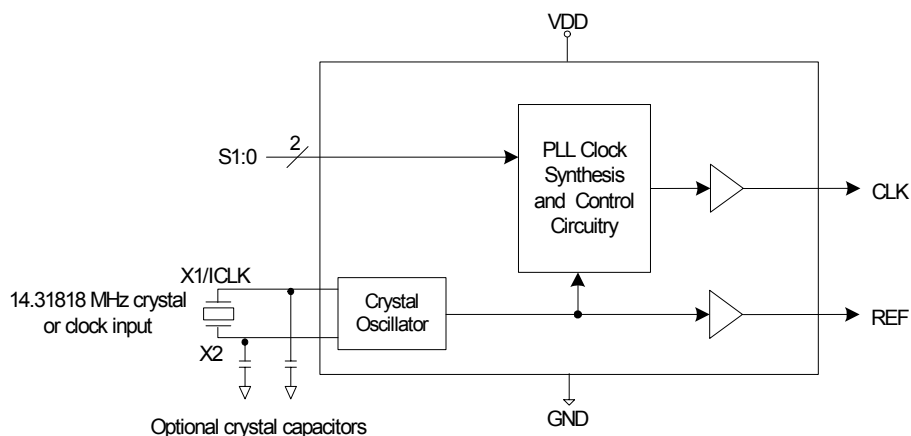
Stored in the chip's ROM is the ability to generate five different output frequencies, allowing one chip to work in different speed processor systems.

The device also has a power-down mode that turns off the clock outputs when both select pins are low. In this mode, the internal PLL is not running.

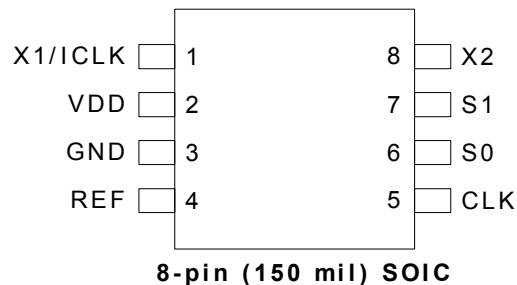
Features

- Packaged as 8-pin SOIC or die
- Pb (lead) free package
- IDT's lowest cost PLL clock plus reference
- Produces common computer frequencies
- Input crystal frequency typically 14.3182 MHz
- Output clock frequencies up to 100 MHz from a 14.3182 MHz crystal or input clock
- Low jitter of 40 ps (one sigma)
- Compatible with all popular CPUs
- Duty cycle of 45/55 up to 200 MHz
- Custom frequencies available
- Operating voltage of 3.3 V to 5.5 V
- Power-down mode turns off chip
- 25 mA drive capability at TTL levels
- Advanced, low-power CMOS process

Block Diagram



Pin Assignment



Clock Decoding Table (MHz) with 14.31818 MHz Crystal or Clock Input

S1	S0	CLK	Multiplier	Accuracy
0	0	Power-down CLK	—	—
0	1	100	6.984	1 ppm
M	0	24	1.676	1 ppm
M	1	14.31818	1	0 ppm
1	0	48	3.353	0.017%
1	1	3.6864	0.2576	0.044%

0 = connect directly to ground

1 = connect directly to VDD

M = leave unconnected (floating)

CLK and REF stop low in power-down state

Pin Descriptions

Pin Number	Pin Name	Pin Type	Pin Description
1	XI/ICLK	Input	Crystal connection to a 14.31818 MHz crystal or clock input.
2	VDD	Power	Connect to +3.3 V or +5 V.
3	GND	Power	Connect to ground.
4	REF	Output	Reference 14.31818 MHz crystal oscillator buffered clock output.
5	CLK	Output	Clock output per table above.
6	S0	Tri-level Input	Select 0 for output clock. Connect to GND or VDD or float. See table above.
7	S1	Tri-level Input	Select 1 for output clock. Connect to GND or VDD or float. See table above.
8	X2	Output	Crystal connection to a 14.31818 MHz crystal. Leave unconnected for clock input.

External Components

Decoupling Capacitor

As with any high-performance mixed-signal IC, the ICS513 must be isolated from system power supply noise to perform optimally.

A decoupling capacitor of 0.01μF must be connected between VDD and the GND. It must be connected close to the ICS513 to minimize lead inductance. No external power supply filtering is required for the ICS513.

Series Termination Resistor

A 33Ω terminating resistor can be used next to the CLK and REF pins for trace lengths over one inch.

Crystal Load Capacitors

The total on-chip capacitance is approximately 12 pF. A parallel resonant, fundamental mode crystal should be used. The device crystal connections should include pads for small capacitors from X1 to ground and from

X2 to ground. These capacitors are used to adjust the stray capacitance of the board to match the nominally required crystal load capacitance. Because load capacitance can only be increased in this trimming process, it is important to keep stray capacitance to a minimum by using very short PCB traces (and no vias) between the crystal and device. Crystal capacitors, if needed, must be connected from each of the pins X1 and X2 to ground.

The value (in pF) of these crystal caps should equal $(C_L - 12 \text{ pF}) \times 2$. In this equation, C_L = crystal load capacitance in pF. Example: For a crystal with a 16 pF load capacitance, each crystal capacitor would be 8 pF $[(16 - 12) \times 2] = 8$.

Absolute Maximum Ratings

Stresses above the ratings listed below can cause permanent damage to the ICS513. These ratings, which are standard values for IDT commercially rated parts, are stress ratings only. Functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods can affect product reliability. Electrical parameters are guaranteed only over the recommended operating temperature range.

Item	Rating
Supply Voltage, VDD	7 V
All Inputs and Outputs (referenced to GND)	-0.5 V to VDD+0.5 V
Ambient Operating Temperature	0 to +70° C
Storage Temperature	-65 to +150° C
Soldering Temperature	260° C

Recommended Operation Conditions

Parameter	Min.	Typ.	Max.	Units
Ambient Operating Temperature	0		+70	°C
Power Supply Voltage (measured in respect to GND)	+3.0		+5.5	V

DC Electrical Characteristics

VDD=5.0 V ±5% , Ambient temperature 0 to +70° C, unless stated otherwise

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Operating Voltage	VDD		3.0		5.5	V
Input High Voltage, ICLK only	V _{IH}	ICLK (pin 1)	(VDD/2)+1	VDD/2		V
Input Low Voltage, ICLK only	V _{IL}	ICLK (pin 1)		VDD/2	(VDD/2)-1	V
Input High Voltage	V _{IH}	S0	2.0			V
Input Low Voltage	V _{IL}	S0			0.8	V
Input High Voltage	V _{IH}	S1	VDD-0.5			V
Input Mid Voltage	V _{IM}	S1		VDD/2		V
Input Low Voltage	V _{IL}	S1			0.5	V
Output High Voltage	V _{OH}	I _{OH} = -25 mA	2.4			V
Output Low Voltage	V _{OL}	I _{OL} = 25 mA			0.4	V
IDD Operating Supply Current		No load, 100MHz		20		mA
IDD Power-down Supply Current, 3.3 V		S1=S0=0		1.5		mA
Short Circuit Current		CLK output		±70		mA
On-Chip Pull-up Resistor		Pin 6		270		kΩ
Input Capacitance, S1, S0		Pins 6, 7		4		pF

AC Electrical Characteristics

VDD = 5.0 V ±5%, Ambient Temperature 0 to +70° C, unless stated otherwise

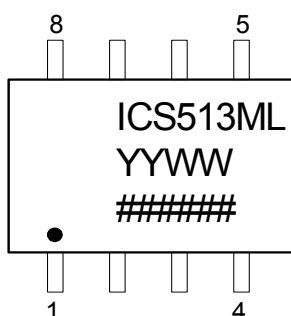
Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Input Frequency, crystal input	F _{IN}		5	14.31818	27	MHz
Input Frequency, clock input	F _{IN}		2	14.31818	50	MHz
Output Frequency, VDD = 4.5 to 5.5 V	F _{OUT}		14	100	140	MHz
Output Frequency, VDD = 3.0 to 3.6 V	F _{OUT}		14	100	100	MHz
Output Clock Rise Time	t _{OR}	0.8 to 2.0 V		1		ns
Output Clock Fall Time	t _{OF}	2.0 to 8.0 V		1		ns
Output Clock Duty Cycle	t _{OD}	1.5 V, up to 140 MHz	45	49-51	55	%

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Power-up time, from PD to outputs stable				5	10	ms
Power-down time, from running to PD state					50	ns
Absolute Clock Period Jitter	t_{ja}	Deviation from mean		± 140		ps
One Sigma Clock Period Jitter	t_{js}			50		ps

Thermal Characteristics

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Thermal Resistance Junction to Ambient	θ_{JA}	Still air		150		°C/W
	θ_{JA}	1 m/s air flow		140		°C/W
	θ_{JA}	3 m/s air flow		120		°C/W
Thermal Resistance Junction to Case	θ_{JC}			40		°C/W

Marking Diagram

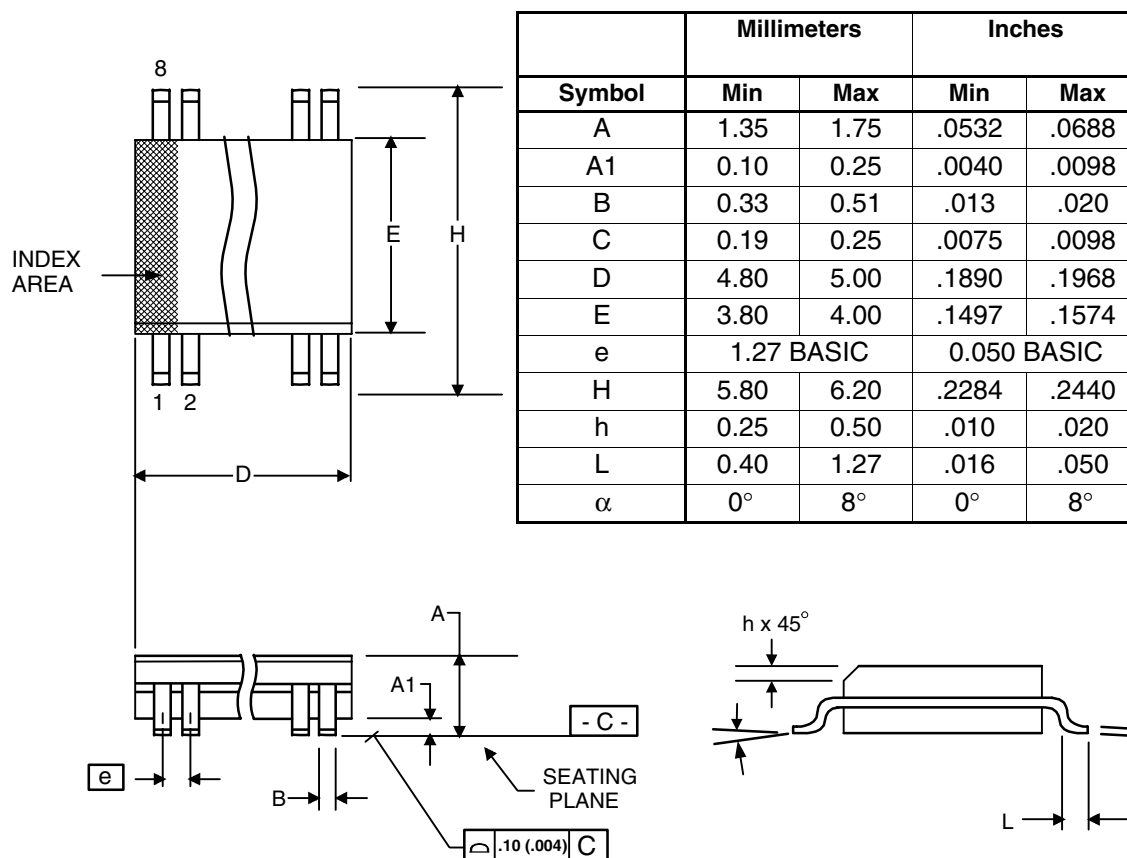


Notes:

1. ##### is the lot code.
2. YYWW is the last two digits of the year and the week.
3. "L" designates Pb (lead) free package.

Package Outline and Package Dimensions (8-pin SOIC, 150 Mil. Narrow Body)

Package dimensions are kept current with JEDEC Publication No. 95



Ordering Information

Part / Order Number	Marking	Shipping Packaging	Package	Temperature
513MLF	ICS513ML	Tubes	8-pin SOIC	0 to +70° C
513MLFT	ICS513ML	Tape and Reel	8-pin SOIC	0 to +70° C

“LF” denotes Pb (lead) free package.

While the information presented herein has been checked for both accuracy and reliability, Integrated Devic Technology (IDT) assumes no responsibility for either its use or for the infringement of any patents or other rights of third parties, which would result from its use. No other circuits, patents, or licenses are implied. This product is intended for use in normal commercial applications. Any other applications such as those requiring extended temperature range, high reliability, or other extraordinary environmental requirements are not recommended without additional processing by IDT. IDT reserves the right to change any circuitry or specifications without notice. IDT does not authorize or warrant any IDT product for use in life support devices or critical medical instruments.

ICS513

LOCO™ PLL CLOCK GENERATOR

CLOCK MULTIPLIER

IMPORTANT NOTICE AND DISCLAIMER

RENESAS ELECTRONICS CORPORATION AND ITS SUBSIDIARIES ("RENESAS") PROVIDES TECHNICAL SPECIFICATIONS AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS OR IMPLIED, INCLUDING, WITHOUT LIMITATION, ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for developers skilled in the art designing with Renesas products. You are solely responsible for (1) selecting the appropriate products for your application, (2) designing, validating, and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. Renesas grants you permission to use these resources only for development of an application that uses Renesas products. Other reproduction or use of these resources is strictly prohibited. No license is granted to any other Renesas intellectual property or to any third party intellectual property. Renesas disclaims responsibility for, and you will fully indemnify Renesas and its representatives against, any claims, damages, costs, losses, or liabilities arising out of your use of these resources. Renesas' products are provided only subject to Renesas' Terms and Conditions of Sale or other applicable terms agreed to in writing. No use of any Renesas resources expands or otherwise alters any applicable warranties or warranty disclaimers for these products.

(Rev.1.0 Mar 2020)

Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,
Koto-ku, Tokyo 135-0061, Japan
www.renesas.com

Contact Information

For further information on a product, technology, the most up-to-date version of a document, or your nearest sales office, please visit:
www.renesas.com/contact/

Trademarks

Renesas and the Renesas logo are trademarks of Renesas Electronics Corporation. All trademarks and registered trademarks are the property of their respective owners.