LOW SKEW 1 TO 4 CLOCK BUFFER PECL IN, PECL OUT ICS554-01A

Description

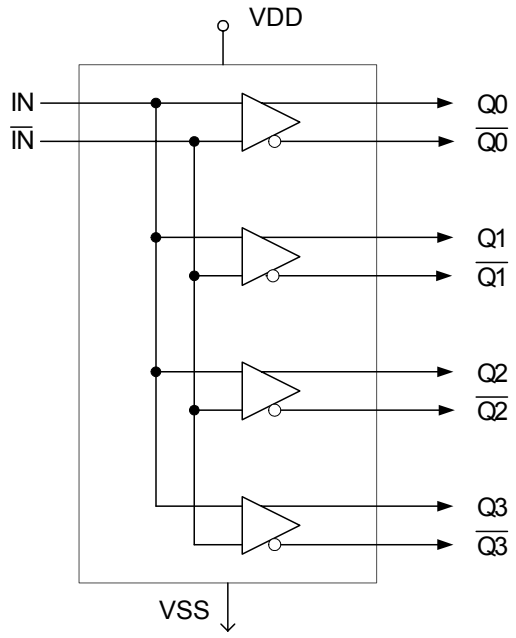
The ICS554-01A is a low skew clock buffer with a single complimentary PECL input to four PECL outputs. Part of IDT's Clock Blocks™ family, this is our lowest skew PECL clock buffer. The ICS554-01A is footprint compatible with the ICS554-01, but requires fewer passive components for termination thus providing a cost-saving alternative. For parts which do not require PECL inputs or outputs, see the ICS553 for a 1 to 4 low skew buffer, or the ICS552-02 for a 1 to 8 low skew buffer. For more than 8 outputs see the MK74CBxxx Buffalo™ series of clock drivers.

IDT makes many non-PLL and PLL based low skew output devices as well as Zero Delay Buffers to synchronize clocks. Contact us for all of your clocking needs.

Features

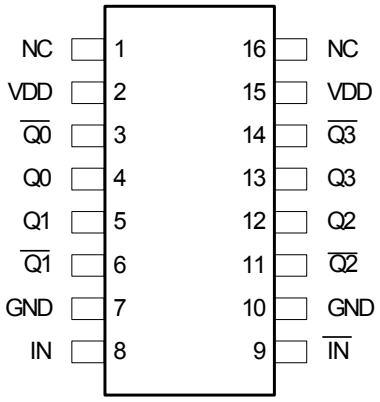
- Input frequency up to 200 MHz
- Advanced CMOS process
- Outputs are skew matched to within 50 ps
- Packaged in 16-pin TSSOP, Pb-free
- One PECL input to 4 PECL output clock drivers
- Operating Voltages of 3.3 V or 5 V
- Industrial temperature range
- Functional equivalent to ICS554-01
- Simplified passive termination network compared to ICS554-01

Block Diagram



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Pin Assignment



16-pin 173 mil (0.65mm) TSSOP

Pin Descriptions

Number	Name	Type	Pin Description
1	NC	—	No Connect.
2	VDD	Power	Connect to +3.3 V or 5 V. Must be same as pin 15.
3	$\overline{Q0}$	Output	Clock Output $\overline{Q0}$.
4	Q0	Output	Clock Output Q0.
5	Q1	Output	Clock Output Q1.
6	$\overline{Q1}$	Output	Clock Output $\overline{Q1}$.
7	GND	Power	Connect to Ground.
8	IN	Input	PECL Clock Input.
9	$\overline{IN}$	Input	Complementary PECL Clock Input.
10	GND	Power	Connect to Ground
11	$\overline{Q2}$	Output	Clock Output $\overline{Q2}$.
12	Q2	Output	Clock Output Q2.
13	Q3	Output	Clock Output Q3.
14	$\overline{Q3}$	Output	Clock Output $\overline{Q3}$.
15	VDD	Power	Connect to +3.3 V or 5 V. Must be same as pin 2.
16	NC	—	No Connect.

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External Components

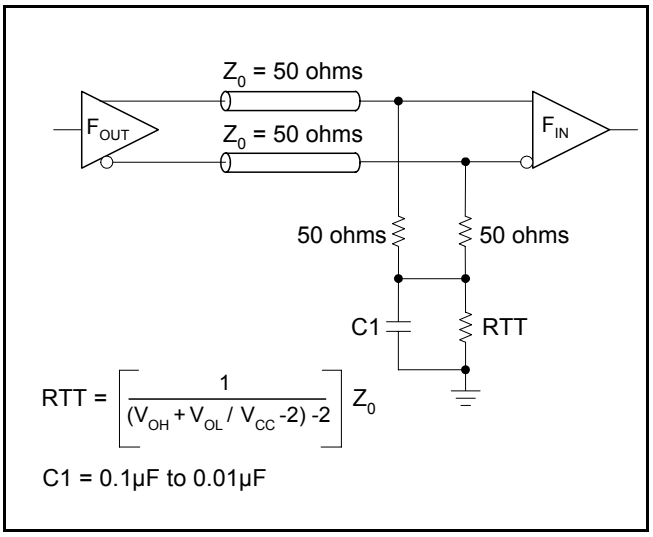
The ICS554-01A requires a decoupling capacitor of 0.01µF to be connected between VDD on pin 2 and GND on pin 7, as well as between VDD on pin 15 and GND on pin 10. These decoupling capacitors should be placed as close to the device as possible.

To achieve the low output skews that the ICS554-01A is capable of, careful attention must be paid to board layout. Essentially, all 8 outputs must have identical terminations, loads, and trace geometries. If they do not, the output skew will be degraded. For example, using a 30Ω series termination on one output (with 33Ω on the others) will cause at least 15ps of skew.

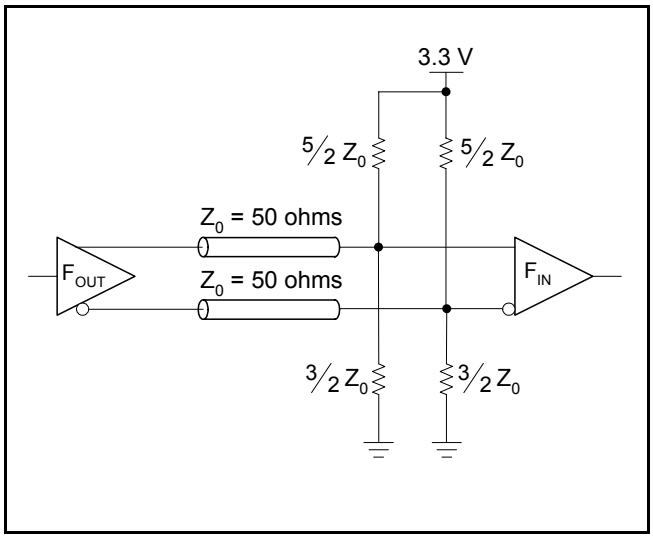
Termination for PECL or LVPECL Outputs

The clock layout topology shown below is a typical termination for PECL or LVPECL outputs. The two different layouts mentioned are recommended only as guidelines.

FOUT and nFOUT are low impedance follower outputs that generate PECL/LVPECL compatible outputs. Therefore, termination resistors (DC current path to ground) or current sources must be used for functionality. These outputs are designed to drive 50 ohm transmission lines. Matched impedance techniques should be used to maximize operating frequency and minimize signal distortion. There are a few simple termination schemes. The figures below show two different layouts which are recommended only as guidelines. Other suitable clock layouts may exist, but it is recommended that board designers simulate to guarantee compatibility across all printed circuit and clock component process variations.



PECL or LVPECL Output Termination



LVPECL Output Termination

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Absolute Maximum Ratings

Stresses above the ratings listed below can cause permanent damage to the ICS554-01A. These ratings, which are standard values for IDT commercially rated parts, are stress ratings only. Functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods can affect product reliability. Electrical parameters are guaranteed only over the recommended operating temperature range.

Item	Rating
Supply Voltage, VDD	7 V
All Inputs and Outputs	-0.5 V to VDD+0.5 V
Ambient Operating Temperature	-40 to +85 ° C
Storage Temperature	-65 to +150° C
Junction Temperature	125° C
Soldering Temperature	260° C

Recommended Operation Conditions

Parameter	Min.	Typ.	Max.	Units
Ambient Operating Temperature	-40	–	+85	° C
Power Supply Voltage (measured in respect to GND)	+3.15		+5.25	V

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DC Electrical Characteristics

VDD=3.3 V ±5% Ambient temperature -40 to +85 ° C

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Operating Voltage	VDD		3.15		5.25	V
Peak to Peak Input Voltage	IN		0.3		1.0	V
Input Common Mode Range	IN	VDD=3.3 V	VDD-2		VDD-0.6	
Input Common Mode Range	IN	VDD=5 V	VDD-3.7		VDD-0.6	
Output High Voltage	V_{OH}	Note 1	VDD-1.2			V
Output Low Voltage	V_{OL}	Note 1			VDD - 2.0	V
Operating Supply Current	IDD	No Load, 135 MHz		80		mA
Short Circuit Current, 3.3 V	I_{OS}			±50		mA
Short Circuit Current, 5 V	I_{OS}			±60		mA

Note 1: V_{OH} and V_{OL} can be set by the external resistor values on the PECL outputs.
note 2: IDD includes the current through the external resistors which can be modified.

AC Electrical Characteristics

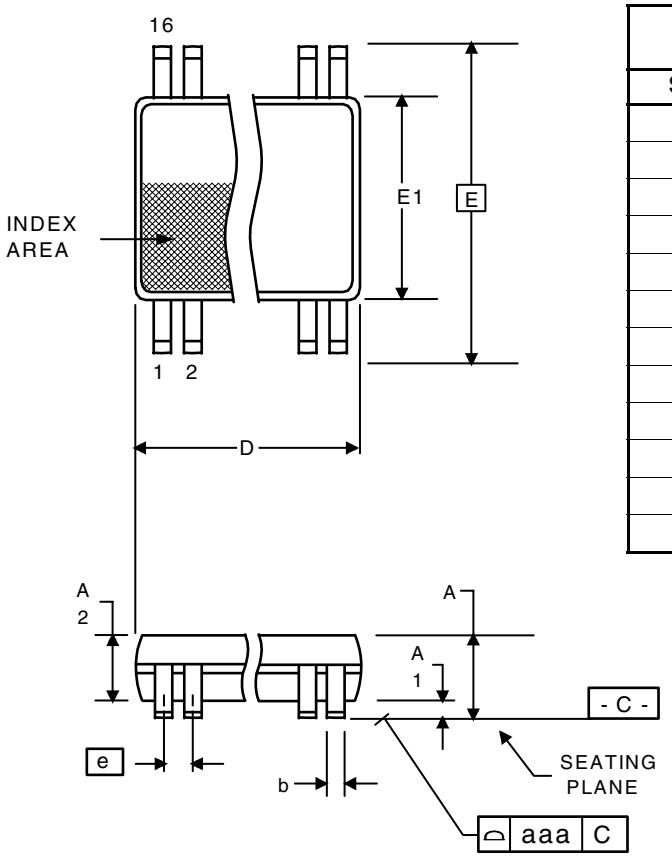
VDD = 3.3 V ±5, Ambient Temperature -40 to +85 ° C

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Input Frequency			0		200	MHz
Propagation Delay		VDD = 3.3 V		2		ns
		VDD = 5 V		2		ns
Output to Output Skew		Crosspoint of pair		0	50	ps
Duty Cycle		Crosspoint of pair	45	50	55	%

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Package Outline and Package Dimensions (16-pin TSSOP, 4.40 mm Body, 0.65 mm Pitch)

Package dimensions are kept current with JEDEC Publication No. 95



	Millimeters		Inches	
Symbol	Min	Max	Min	Max
A	--	1.20	--	0.047
A1	0.05	0.15	0.002	0.006
A2	0.80	1.05	0.032	0.041
b	0.19	0.30	0.007	0.012
C	0.09	0.20	0.0035	0.008
D	4.90	5.1	0.193	0.201
E	6.40 BASIC		0.252 BASIC	
E1	4.30	4.50	0.169	0.177
e	0.65 Basic		0.0256 Basic	
L	0.45	0.75	0.018	0.030
α	0°	8°	0°	8°
aaa	--	0.10	--	0.004

Ordering Information

Part / Order Number	Marking	Shipping Packaging	Package	Temperature
554G-01AILF	554G1AIL	Tubes	16-pin TSSOP	-40 to +85 °C
554G-01AILFT		Tape and Reel	16-pin TSSOP	-40 to +85 °C

"LF" denotes Pb free packaging, RoHS compliant

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